Ans to the Q.no: 1

2 bit bidirectional shift register with parallel load.

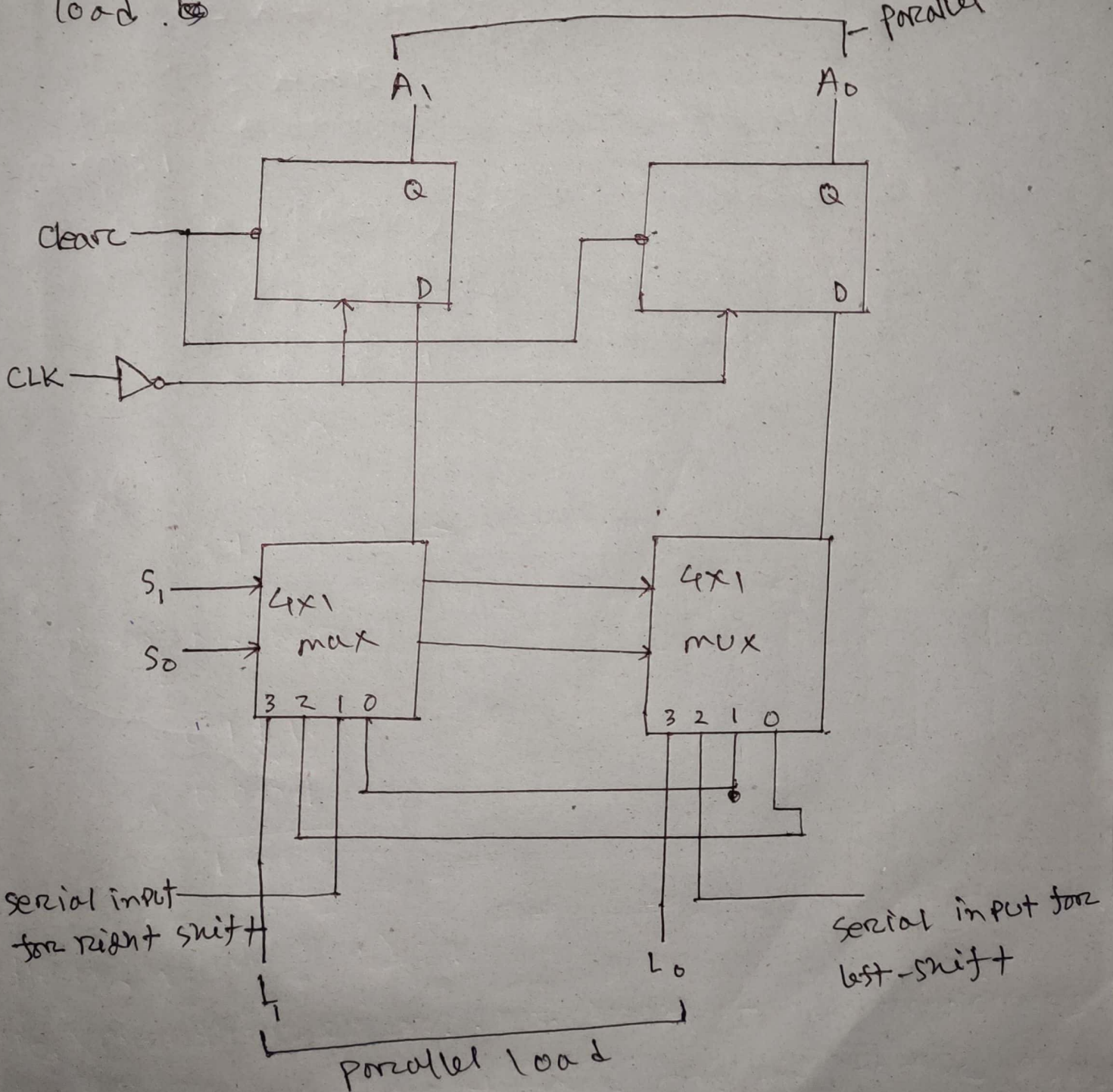


Table:

S_1	S_0	operation
0	0	no change
0	1	shift right
1	0	shift left
1	1	parallel load.

Given that,

Serial input is 10

CLK	A_0	A_1
0	0	0
1	1	0
2	0	1

10 is contented to 01 by Right shift register operation of 2 bits bidirectional shift register with parallel load circuit.

Ans to the Q.no:2

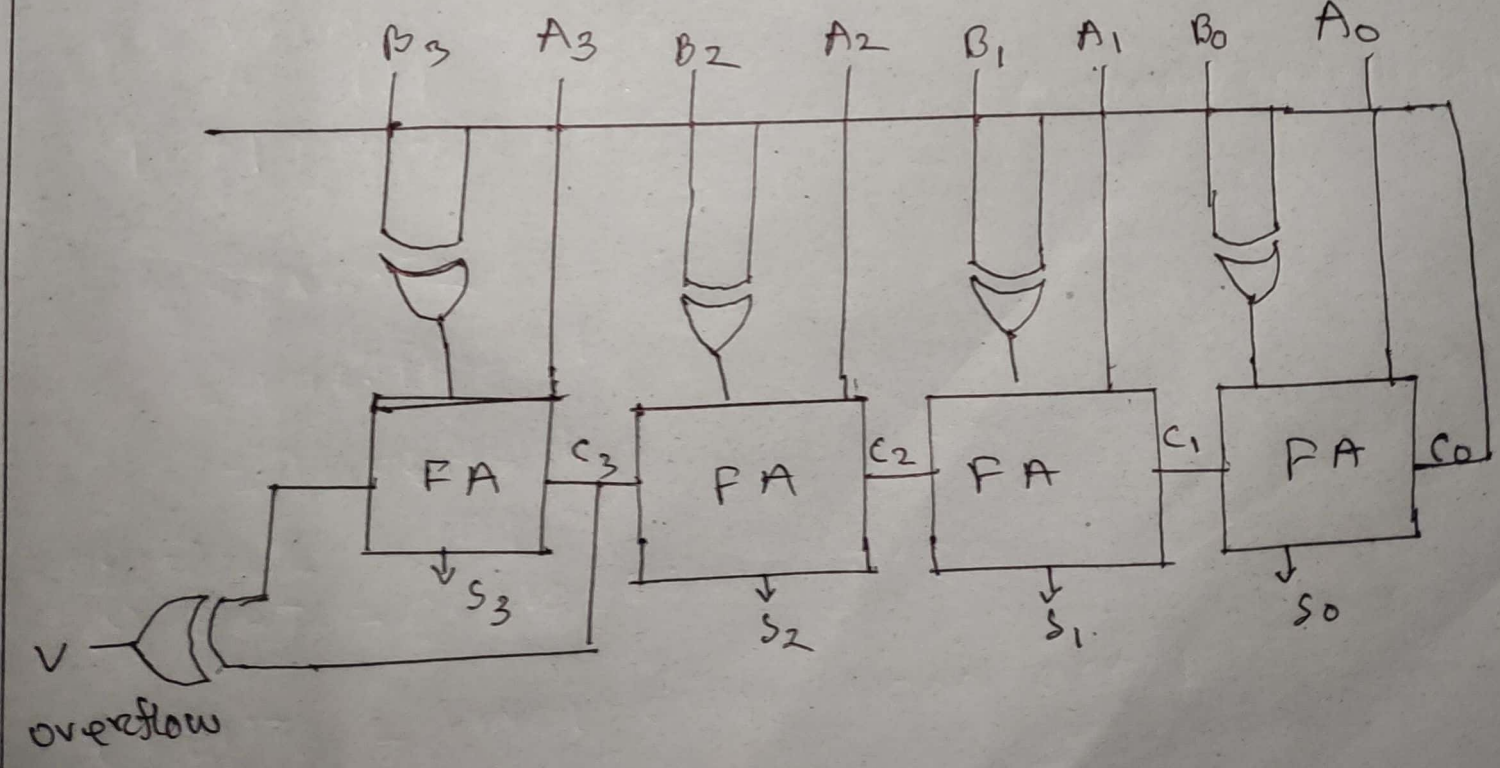
Given that two 4-bit binary numbers. numbers are 0111 and 0001. we know MSD is the signed digit.

bit is zero then the number is positive.

bit is one then the number is negative.

Here, Given two number 4-bit digit is positive, so both are positive.

Circuit diagram: 4bit binary addere-subtractore.



when, $m = 0$

$$S = A + (B \oplus m) + m$$
$$= A + (B \oplus 0) + 0$$
$$= A + B$$

$m = 1$

$$S = A + (B \oplus m) + m$$
$$= A + (B \oplus 1) + 1$$
$$= A + \bar{B} + 1$$
$$= A - B$$

$$C_3 + C_4 = 1 \Rightarrow \text{overflow}$$

Given numbers

$$\begin{array}{r} 0111 \\ (+)\ 0001 \\ \hline 1000 \end{array}$$

Here, $V(\text{overflow}) = 1$

So, overflow occurs. we know it overflow occurs now we have to add one bit to the MSB.

∴ result is $= 01000$
$= +8$

Ans to the Q.NO:03

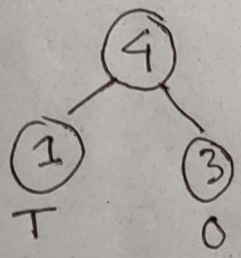
Characters	A	E	I	O	U	S	T
frequency	10	15	12	3	4	13	1

Huffman

Step: 1

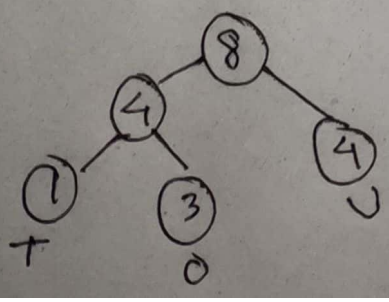
1	3	4	10	12	13	15
T	O	U	A	I	S	E

Step: 2



4	10	12	13	15
U	A	I	S	E

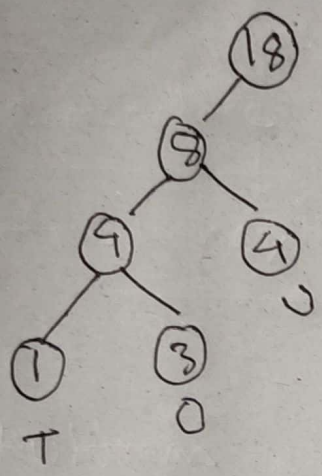
Step: 3



10 12 13 15

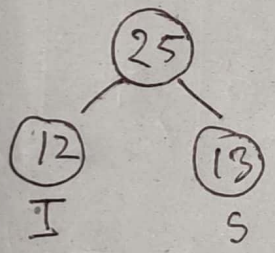
A I S E

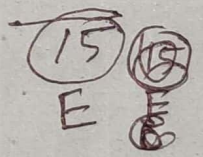
Step : 4

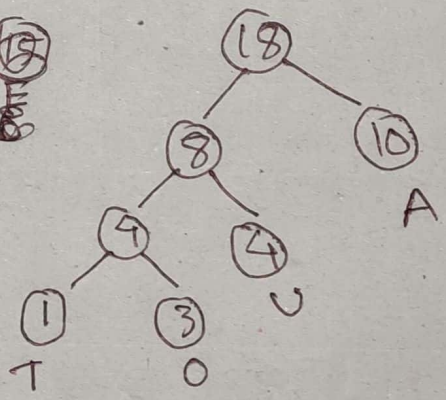


12	13	15
I	S	E

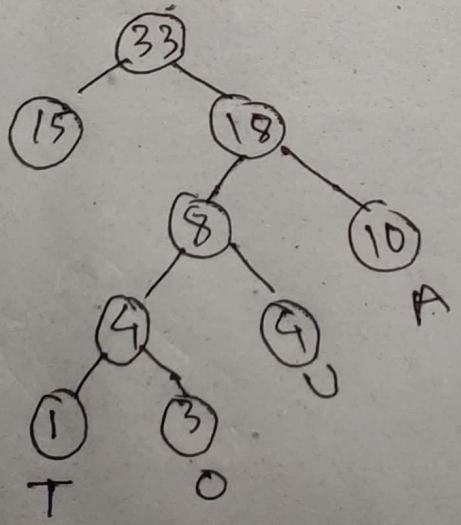
Step: 5

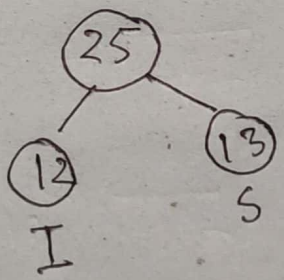




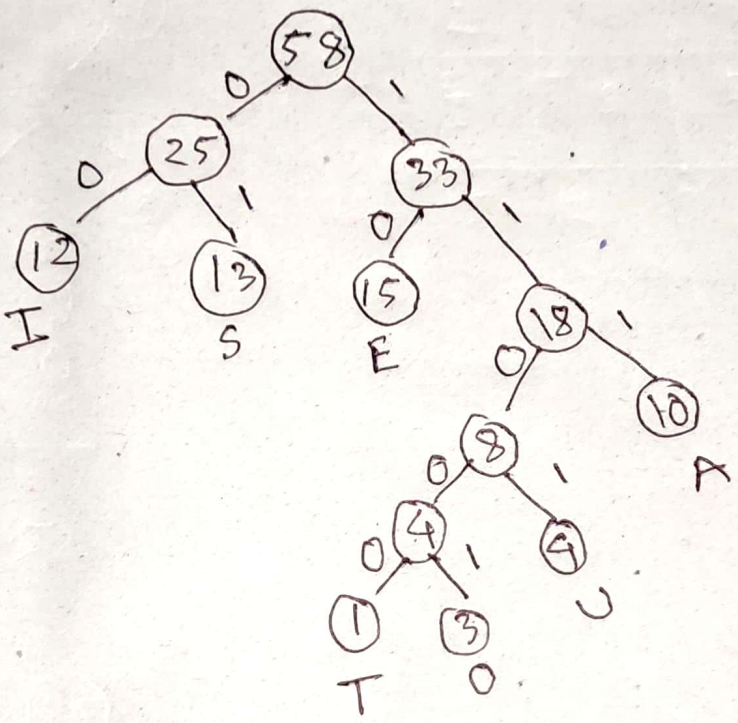


Step: 6





Step: 7



Huffman codes fore each characters:

A = 111

E = 10

I = 00

O = 11001

U = 1101

S = 01

T = 11000

Average code size:

we know,

$$\text{Average code size} = \frac{\Sigma(\text{frequency} \times \text{length})}{\text{frequency}}$$

$$= \frac{10\times3 + 15\times2 + 12\times2 + 4\times4 + 13\times2 + 1\times5}{10+15+12+3+4+13+1}$$

$$= \frac{131}{59}$$

$$= 2.220$$

$$= 2.52$$

Huffman Encoding length:

we know,

Total numbere of charactere x Avercage code length

$$= 58 \times 2.52$$

$$= 146.16$$

$$= 147 \text{ bits}$$

Opcodes:

(a) EAT = 00010 00111 11000

(b) OUTS = 11001 01101 11000 00001