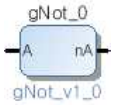
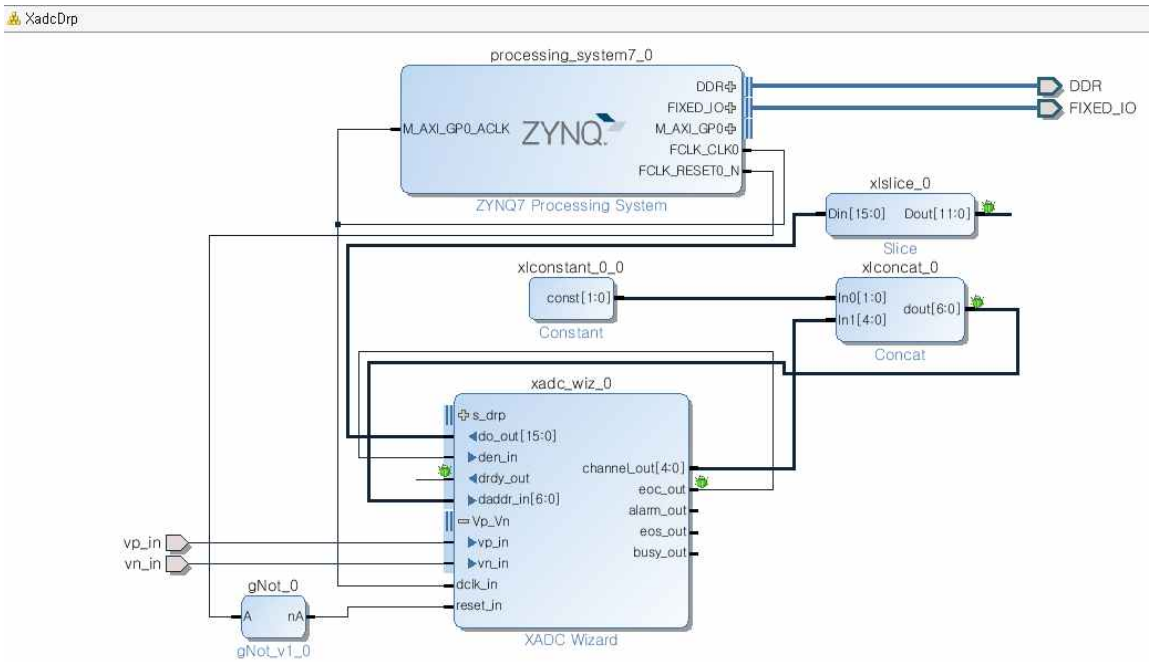
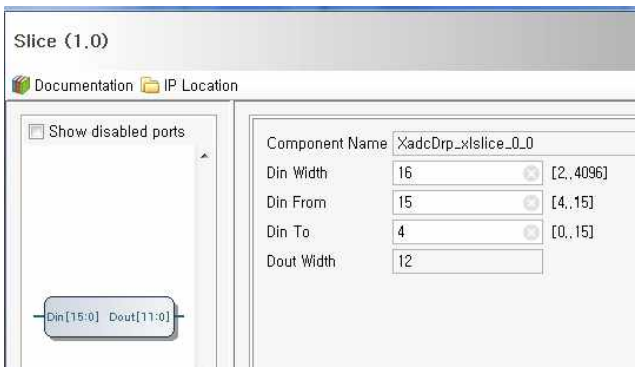
1. Make Project (XAdcDrp.xpr)

2. Create Block Design

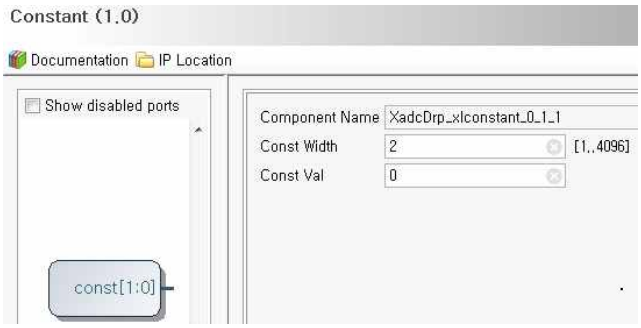
Make IP for not-Gate --- > 

(because the reset_in of xadc_wiz_0 is active-high, but FCLK_RESET0_N of ps-7 is active-low.)



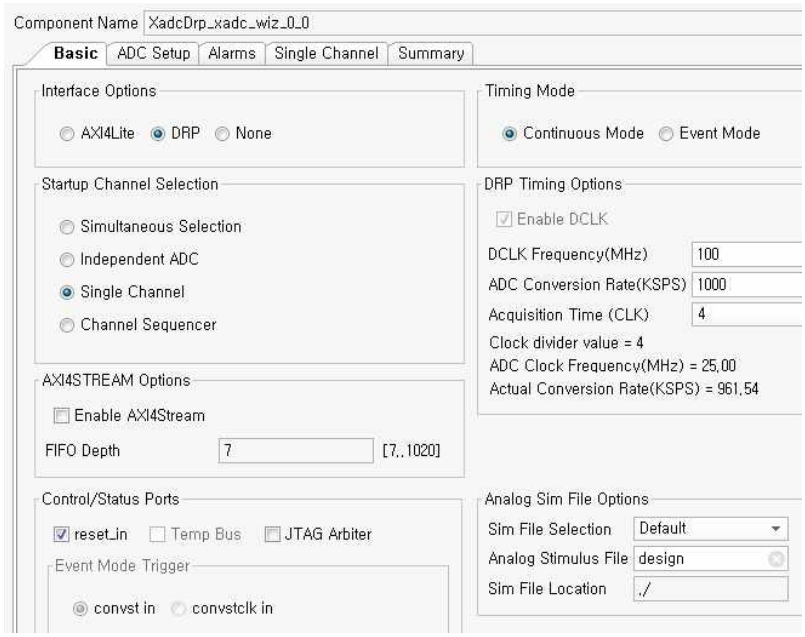
--> 

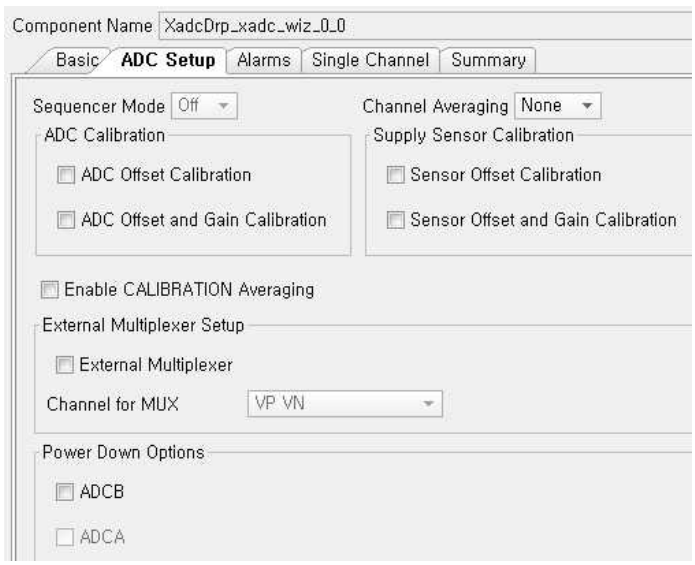
extract high 12bits

--> 

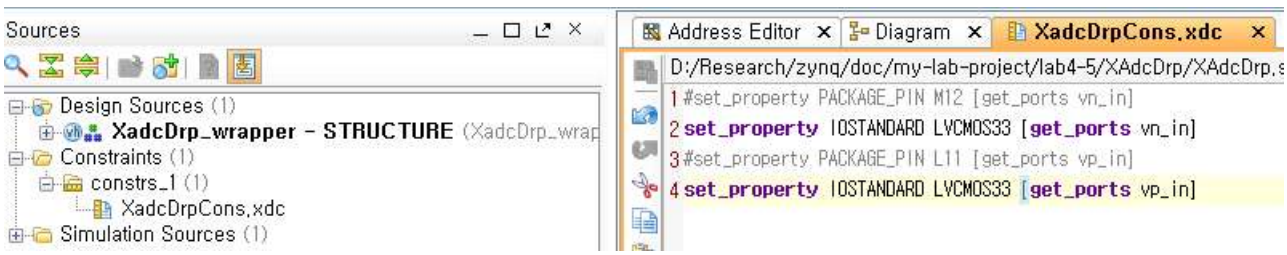
make constant (00)

Set XADC Wizard (3.0) :



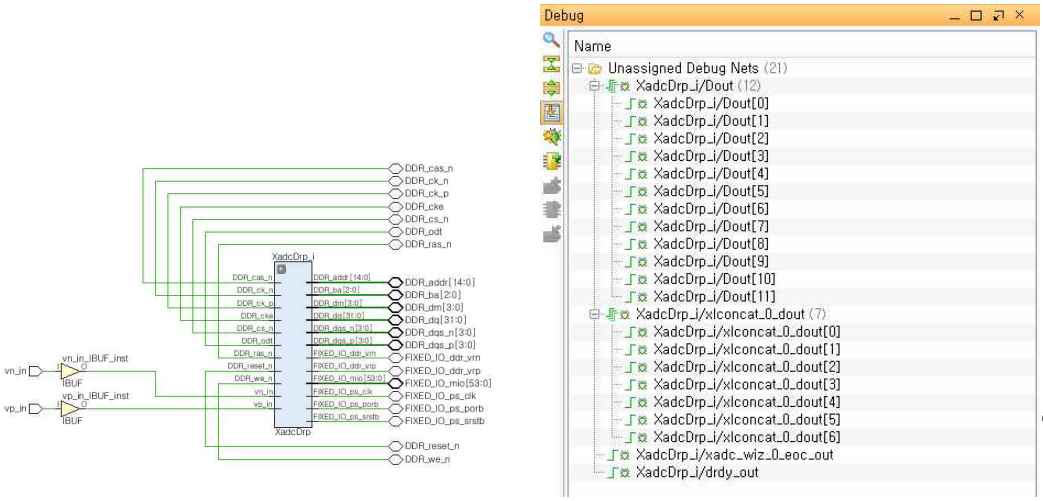


Click Summary, *OK*
Validate, OK
Generate Block Design
Create HDL Wrapper
Make constraint file

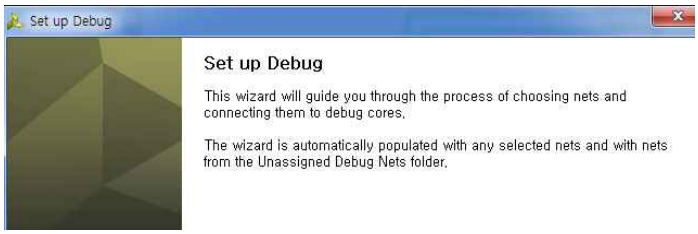


3. Run Synthesis and Setup Debug

open synthesised design

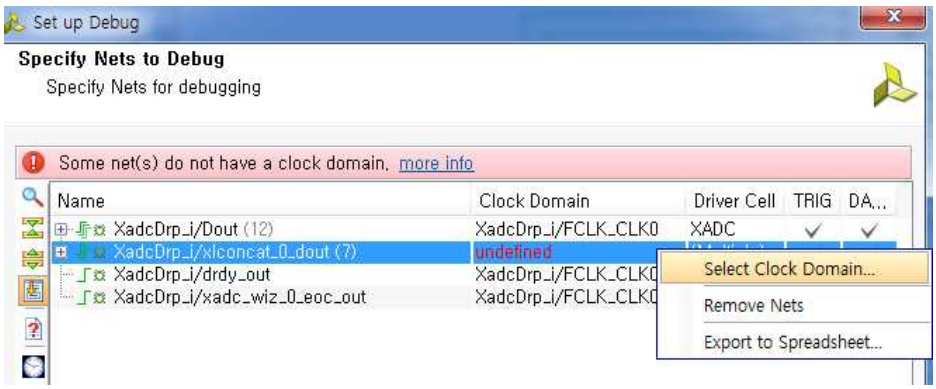


click (set up debug)

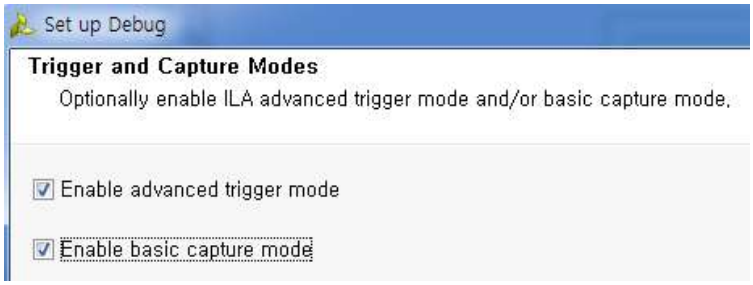


click next

select undefined , ***select*** Select Clock Domain...

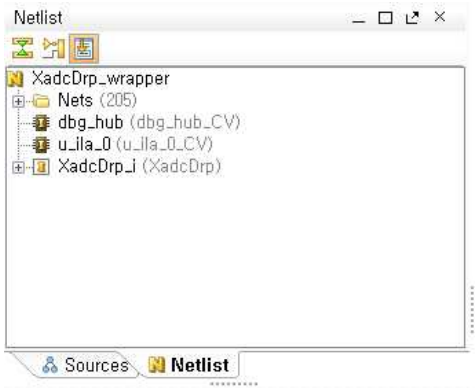


select XadcDrp_i/FCLK_CLK0 , ***Next***

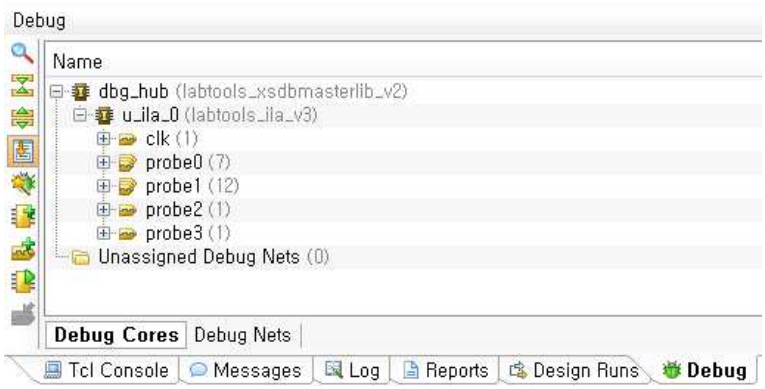


Check all, ***next, finish***

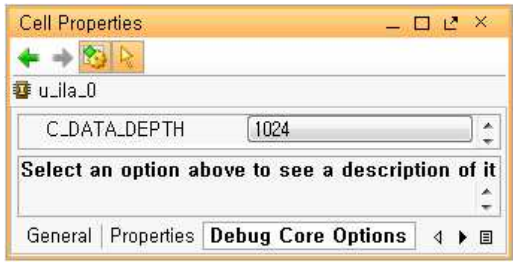
Check if nets for debug hub(dbg_hub) and integrated logic analyzer(ila) are produced.



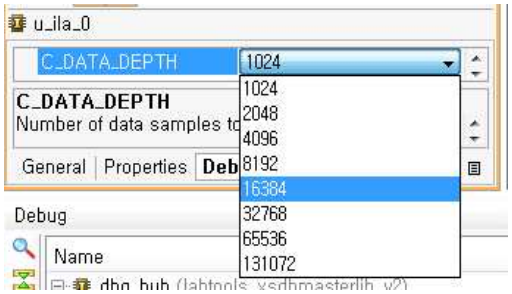
Check if there is no unassigned nets.



click 

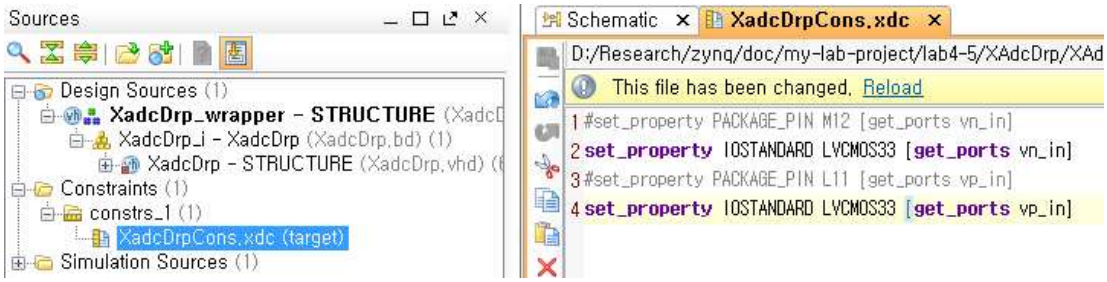


click **Debug Core Options**



change C_DATA_DEPTH, *Save* ( )

check constraint file, *click* Reload

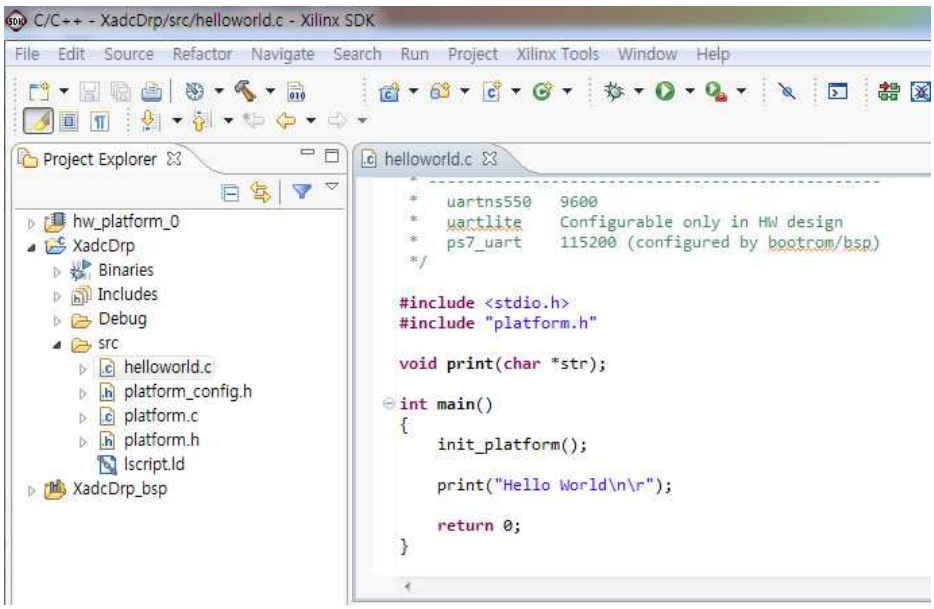


check if debug port properties are included in the constraint file

4. Generate Bitstream

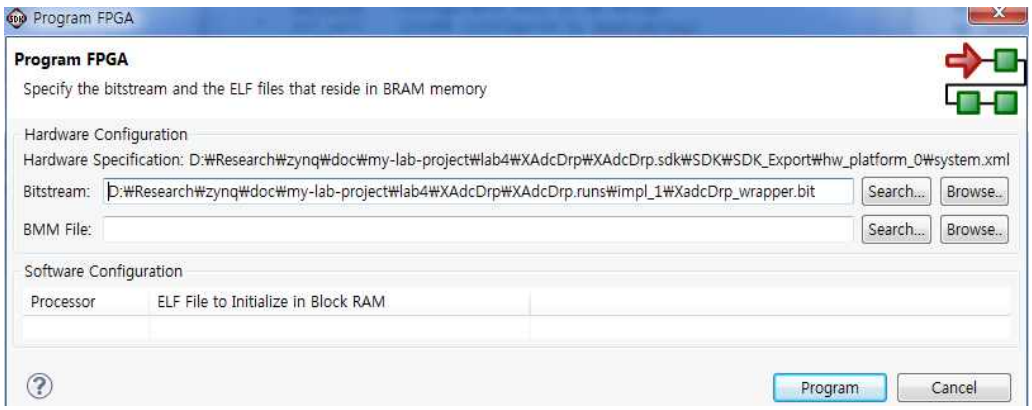
5. Export to SDK

6. Make an application project (XadcDrp)



7. Run application program

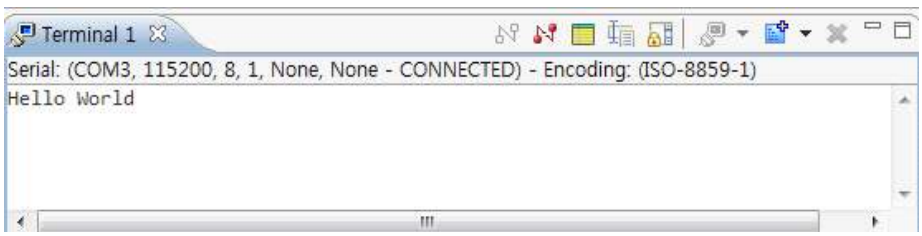
Turn-on and ***Program*** ( ) the ZED board



click Program

Connect Terminal

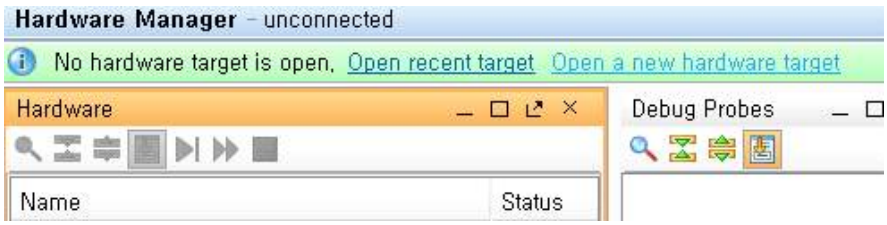
Run program ( )



8. Program Debugging

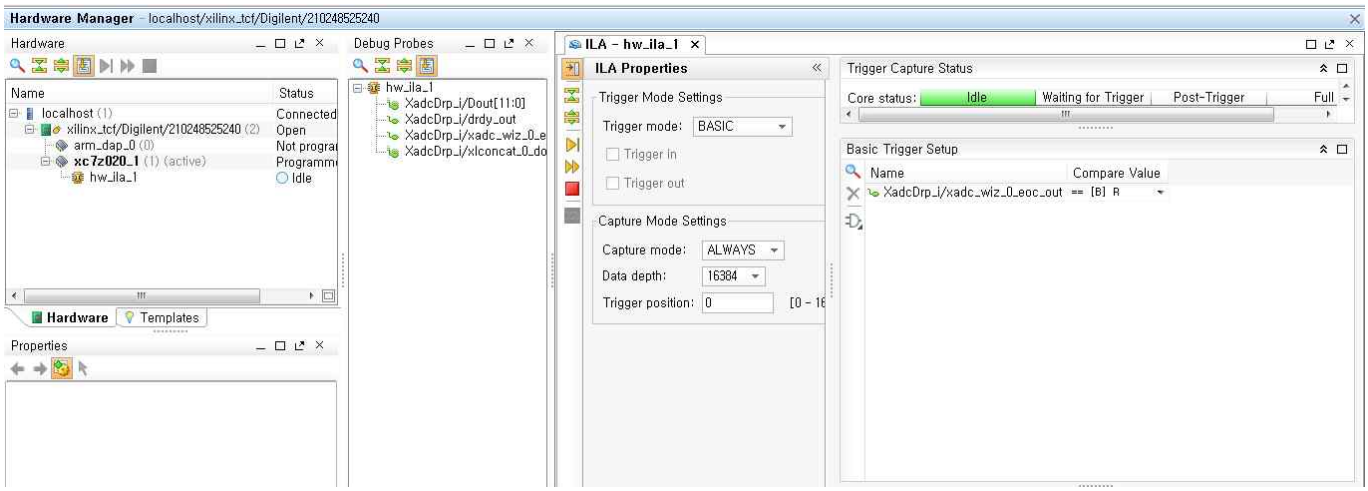
click Open Hardware Manager

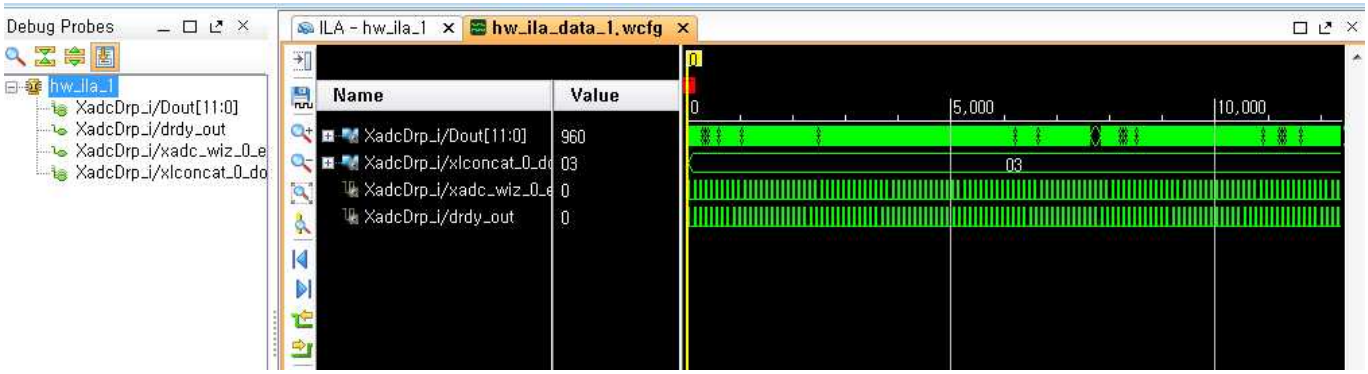
click Open a new hardware target , *Next, Next, Next, Next*



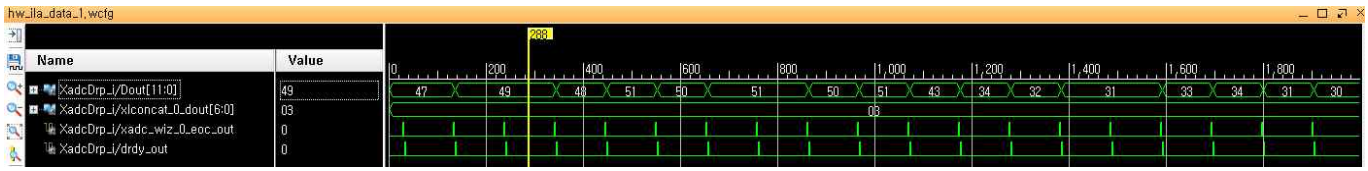
Finish

click (trig immediate)

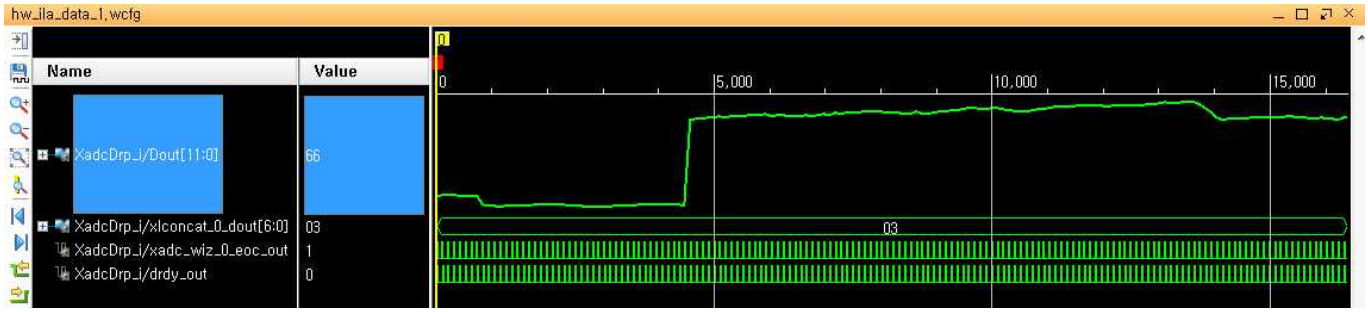




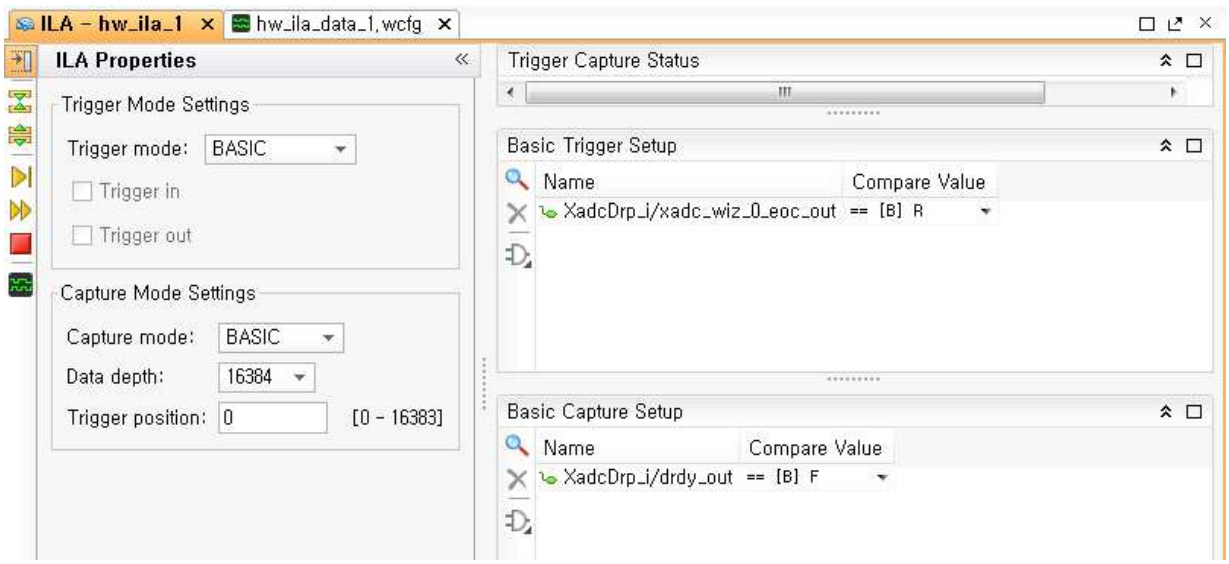
click

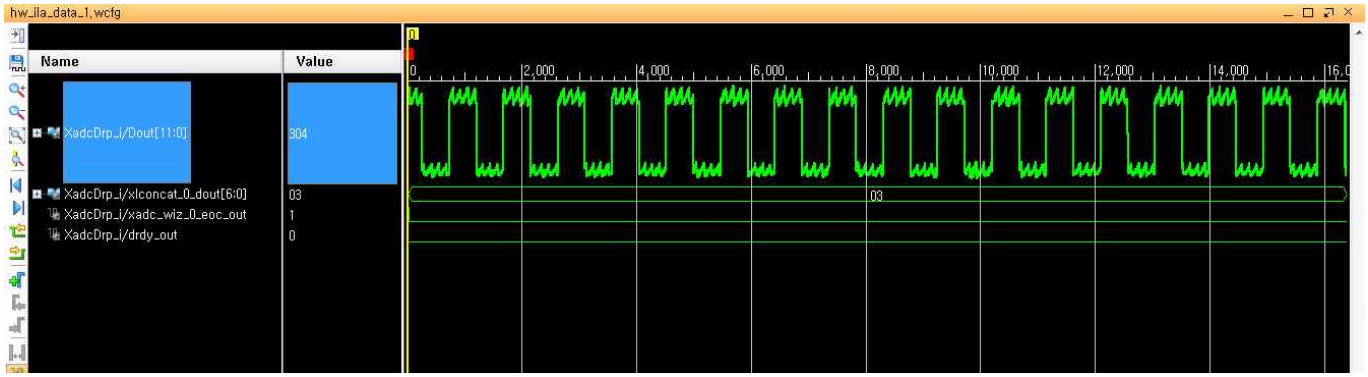


Sample 1KHz Pulse train

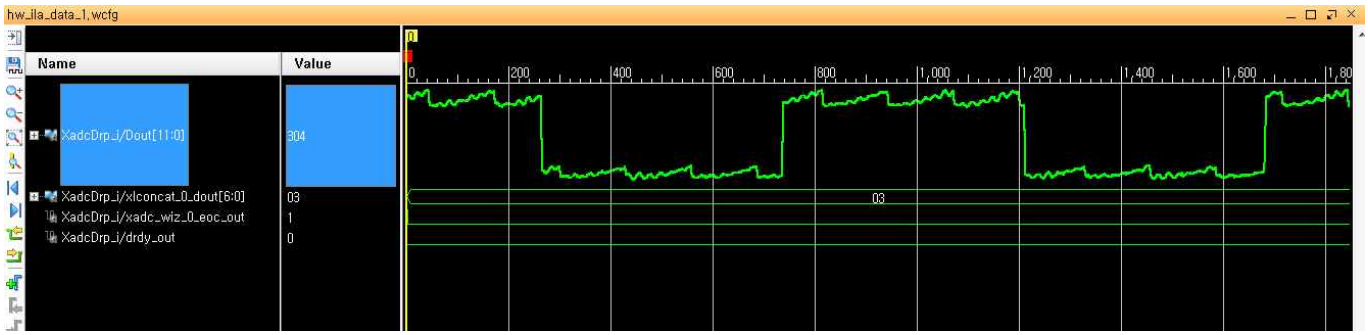


Change capture mode to basic, ***click*** (run trigger)





click 



- about 940 samples per a cycle --> 961.54 ksps/940 samples = about 1.02k/s = 1.02KHz
- pulse amplitude ---> 304/4096*1 V = about 74 mV

See you next Lab5.