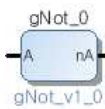
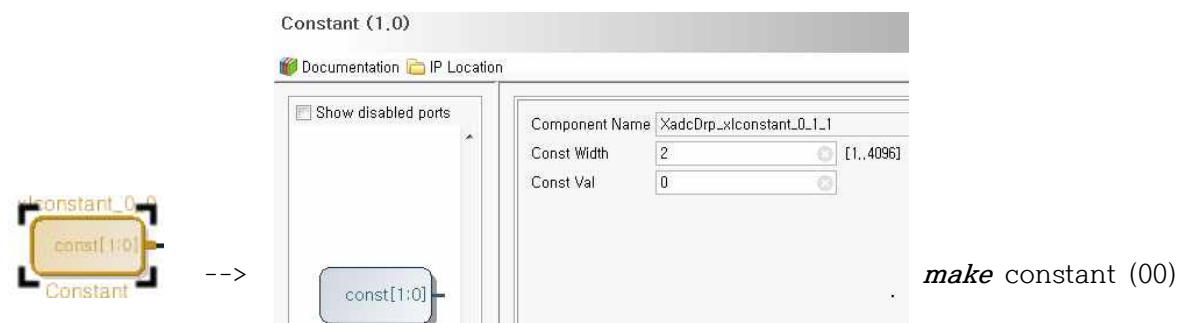
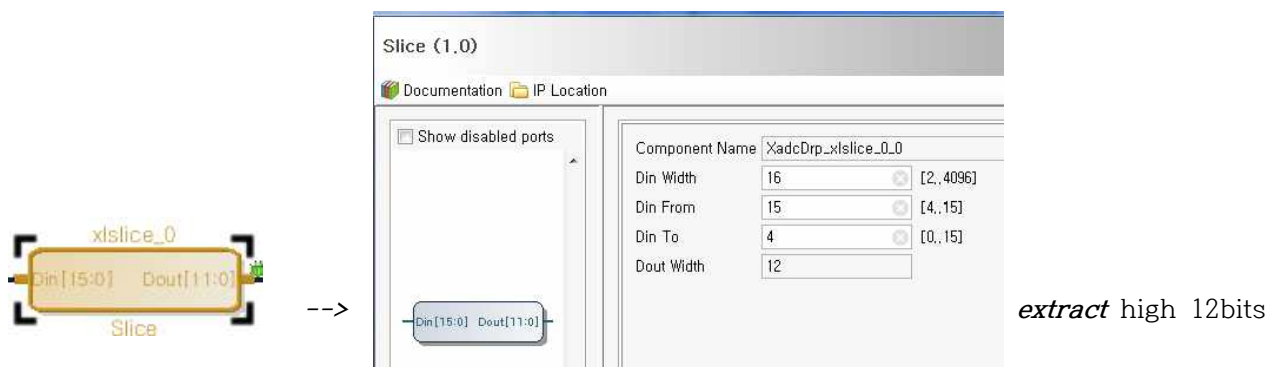
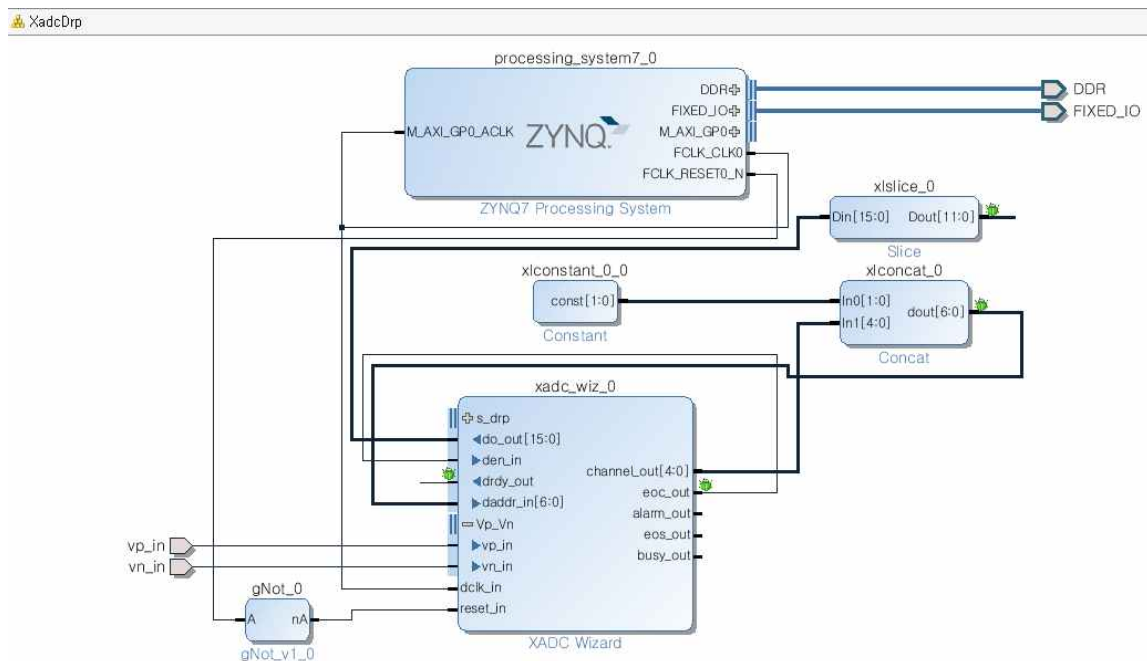


1. Make Project (XAdcDrp.xpr)

2. Create Block Design

Make IP for not-Gate --->  (because the reset_in of xadc_wiz_0 is active-high, but FCLK_RESET0_N of ps-7 is active-low.)



Set XADC Wizard (3,0) :

Component Name: XadcDrp_xadc_wiz_0_0

Basic | ADC Setup | Alarms | Single Channel | Summary

Interface Options

☐ AXI4Lite ☒ DRP ☐ None

Startup Channel Selection

☐ Simultaneous Selection
☐ Independent ADC
☒ Single Channel
☐ Channel Sequencer

AXI4STREAM Options

☐ Enable AXI4Stream

FIFO Depth: 7 [7..1020]

Control/Status Ports

☒ reset_in ☐ Temp Bus ☐ JTAG Arbiter

Event Mode Trigger

☒ convst_in ☐ convstclk_in

Timing Mode

☒ Continuous Mode ☐ Event Mode

DRP Timing Options

☒ Enable DCLK

DCLK Frequency(MHz): 100

ADC Conversion Rate(KSPS): 1000

Acquisition Time (CLK): 4

Clock divider value = 4

ADC Clock Frequency(MHz) = 25,00

Actual Conversion Rate(KSPS) = 961,54

Analog Sim File Options

Sim File Selection: Default

Analog Stimulus File: design

Sim File Location: ./

Component Name: XadcDrp_xadc_wiz_0_0

Basic | **ADC Setup** | Alarms | Single Channel | Summary

Sequencer Mode: Off

Channel Averaging: None

ADC Calibration

☐ ADC Offset Calibration
☐ ADC Offset and Gain Calibration

Supply Sensor Calibration

☐ Sensor Offset Calibration
☐ Sensor Offset and Gain Calibration

☐ Enable CALIBRATION Averaging

External Multiplexer Setup

☐ External Multiplexer

Channel for MUX: VP_VN

Power Down Options

☐ ADCB
☐ ADCA

Basic | **ADC Setup** | **Alarms** | **Single Channel**

Select Channel	Channel Enable
VP_VN	<input checked="" type="checkbox"/>

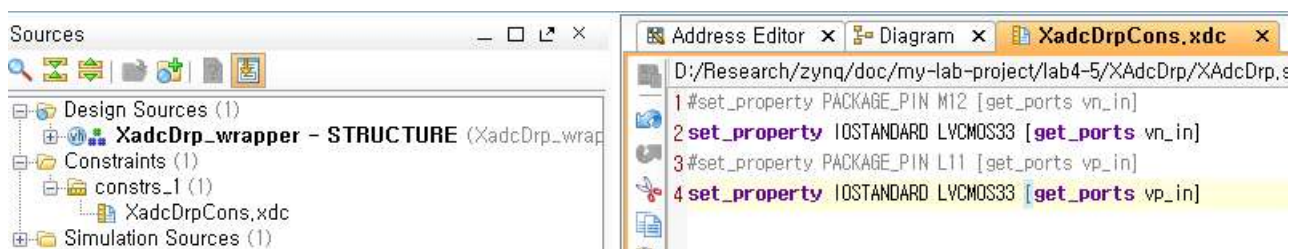
Click Summary, OK

Validate, OK

Generate Block Design

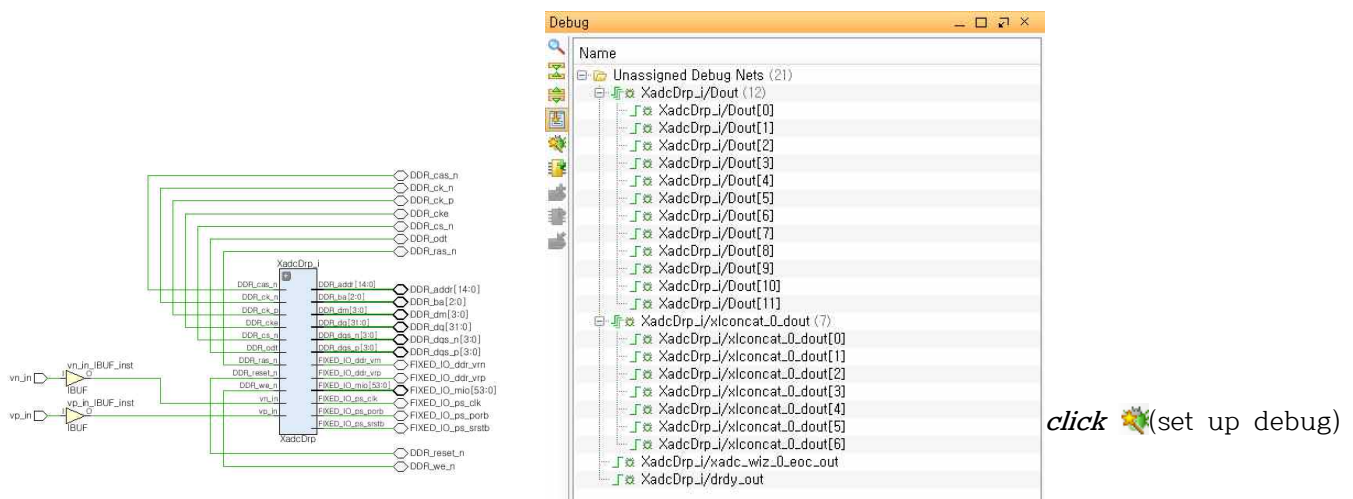
Create HDL Wrapper


Make constraint file

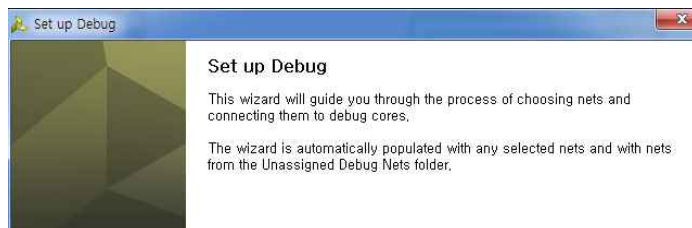


3. Run Synthesis and Setup Debug

open synthesised design

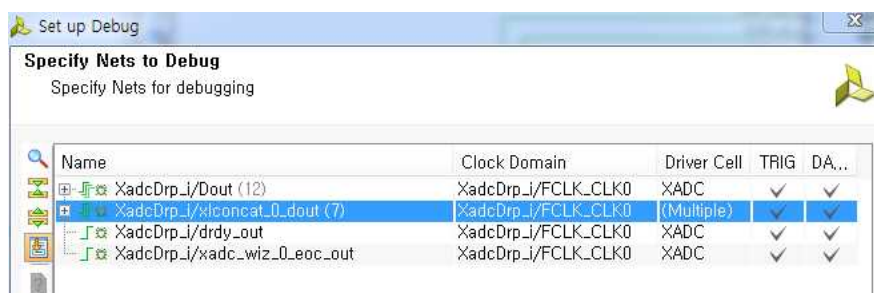
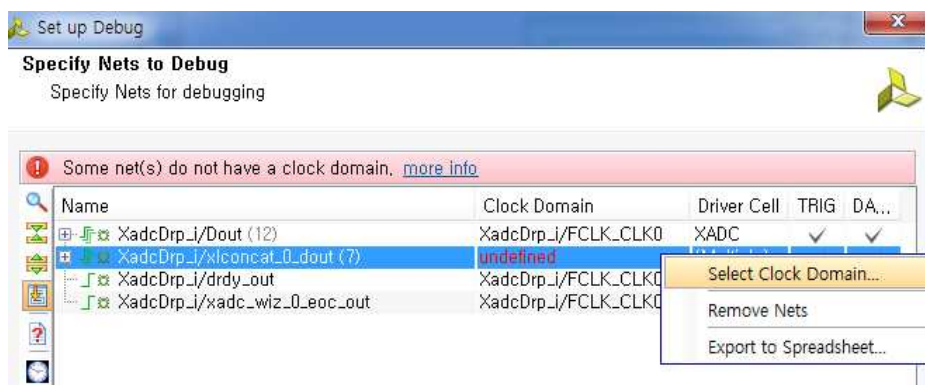


click  (set up debug)

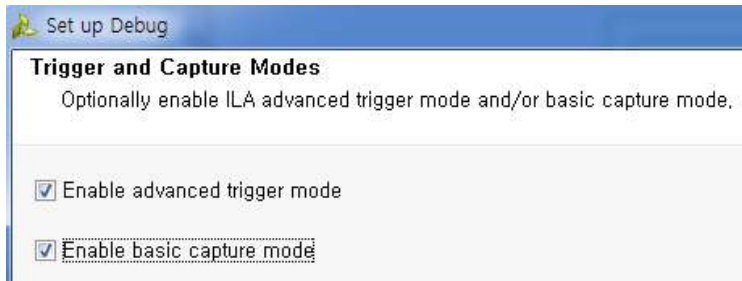


click next

select **undefined** , *select* **Select Clock Domain...**

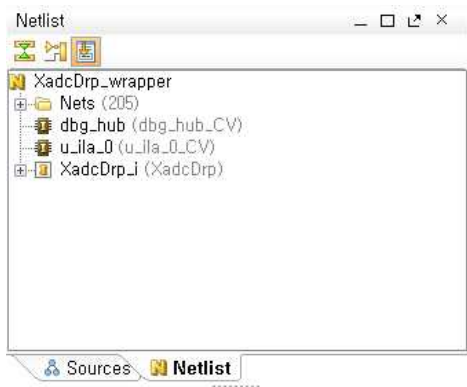


select XadcDrp_i/FCLK_CLK0 , *Next*

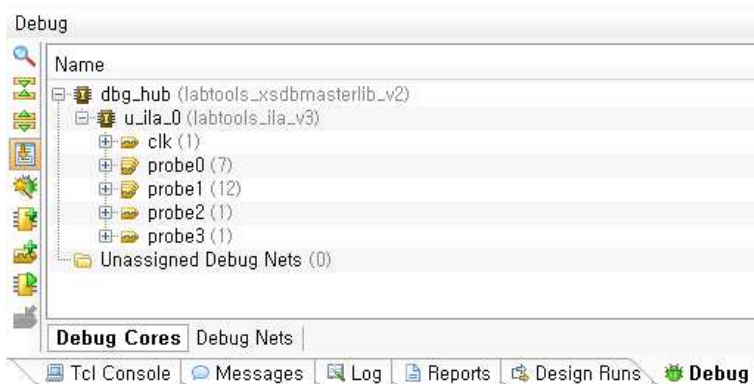


Check all, next, finish

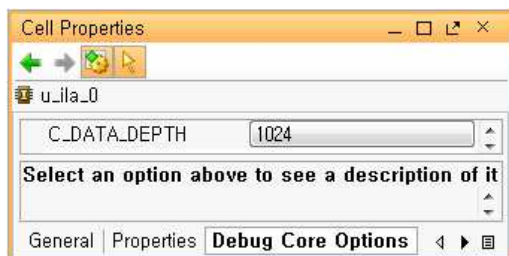
Check if nets for debug hub(dbg_hub) and integrated logic analyzer(ila) are produced.



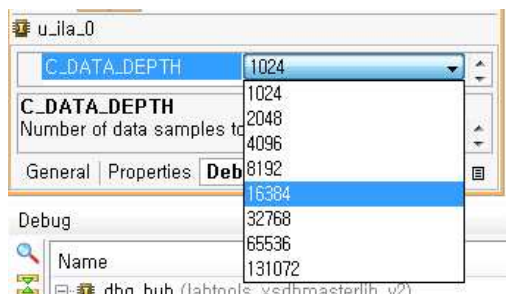
Check if there is no unassigned nets.



click  **u_ila_0 (u_ila_0_CV)**

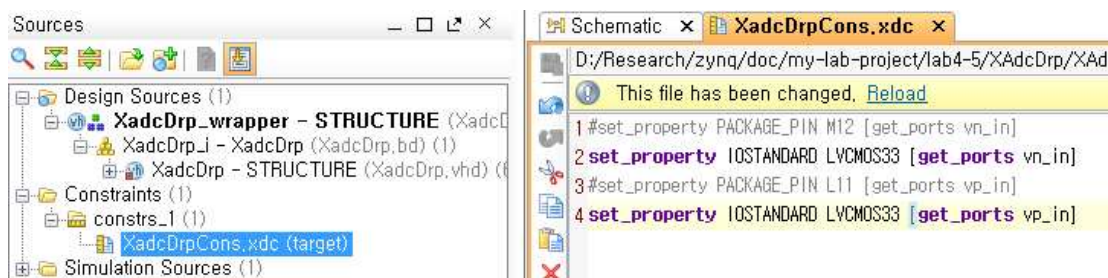


click **Debug Core Options**



change **C_DATA_DEPTH**, Save ()

check constraint file, click **Reload**



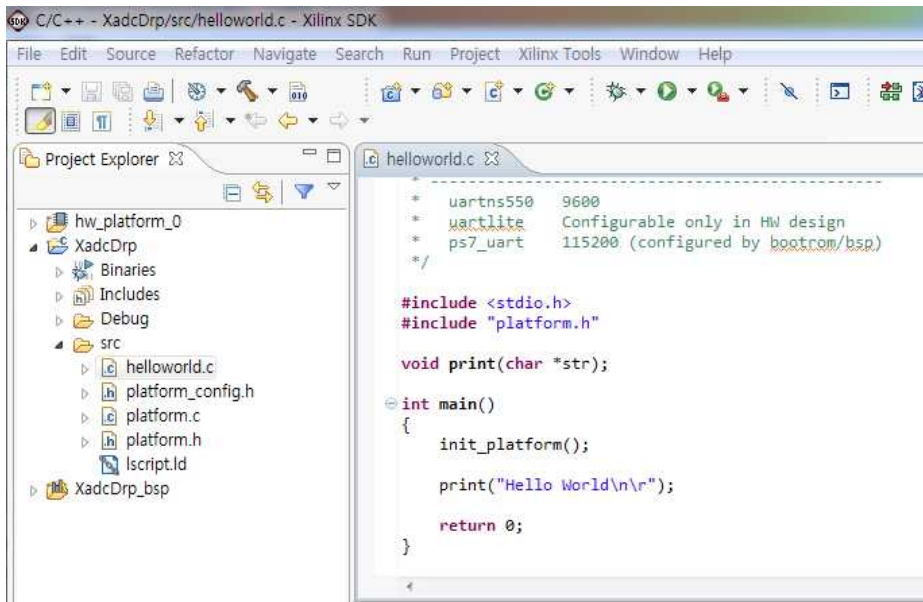
check if debug port properties are included in the constraint file




4. Generate Bitstream

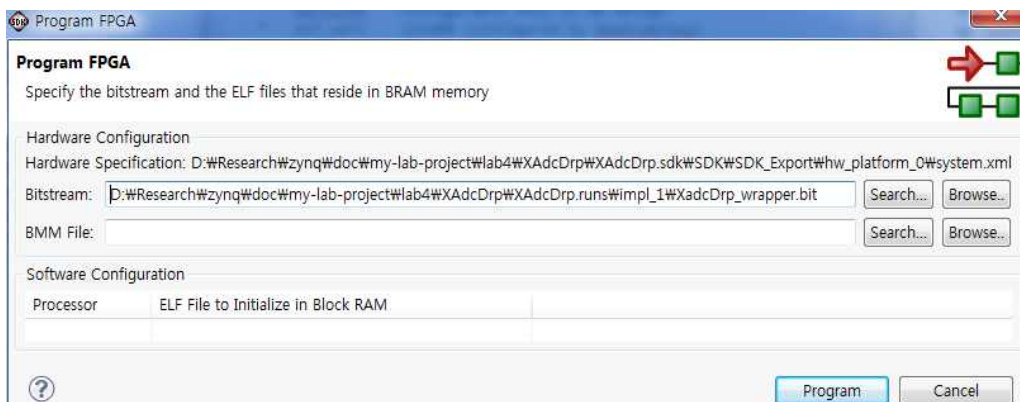
5. Export to SDK

6. Make an application project (XadcDrp)




7. Run application program

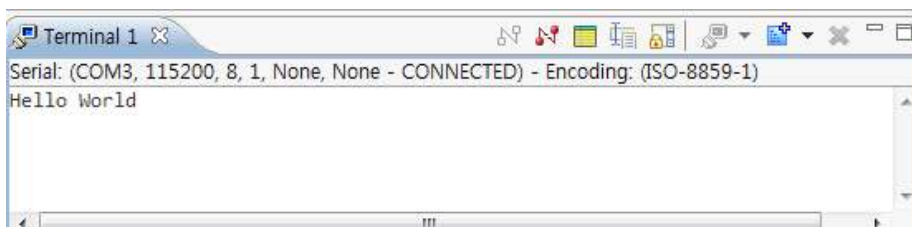
Turn-on and *Program* () the ZED board



click Program

Connect Terminal

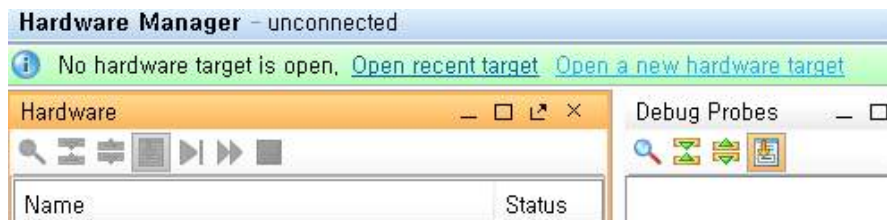
Run program ()



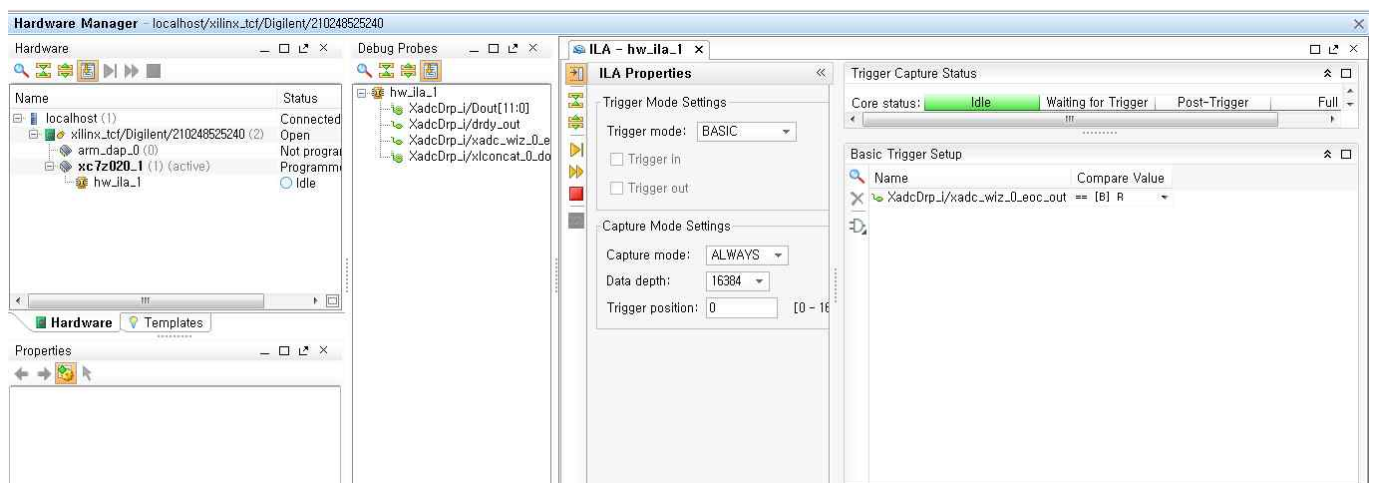
8. Program Debugging

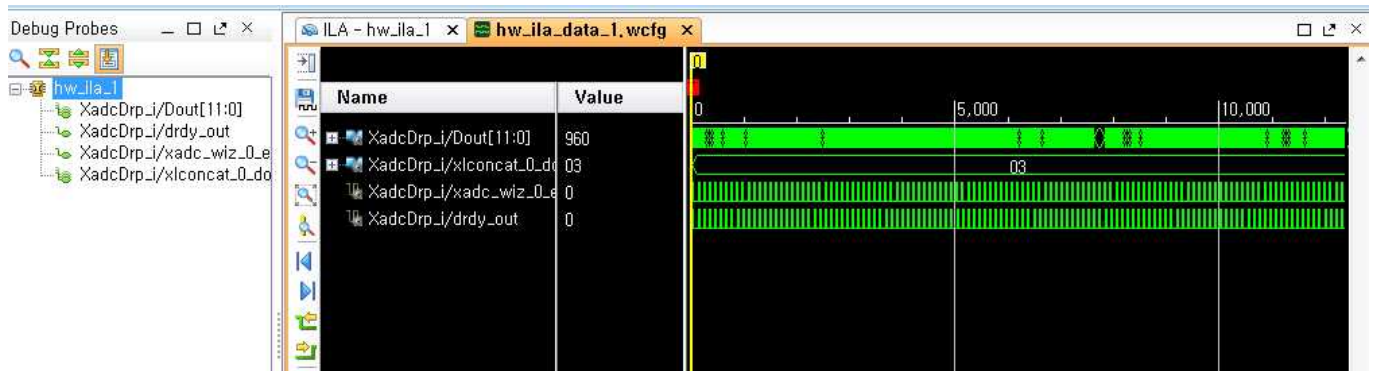


click **Open a new hardware target**, Next, Next, Next, Next

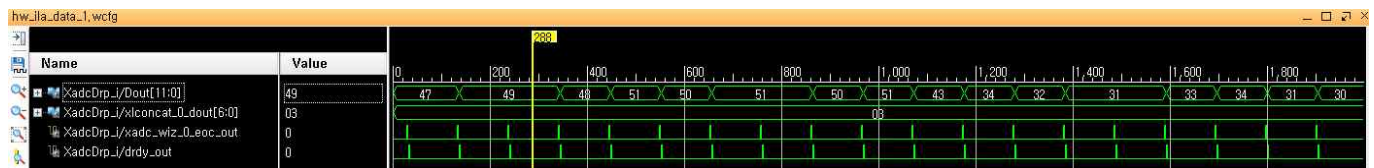


click **▶▶** (trig immediate)

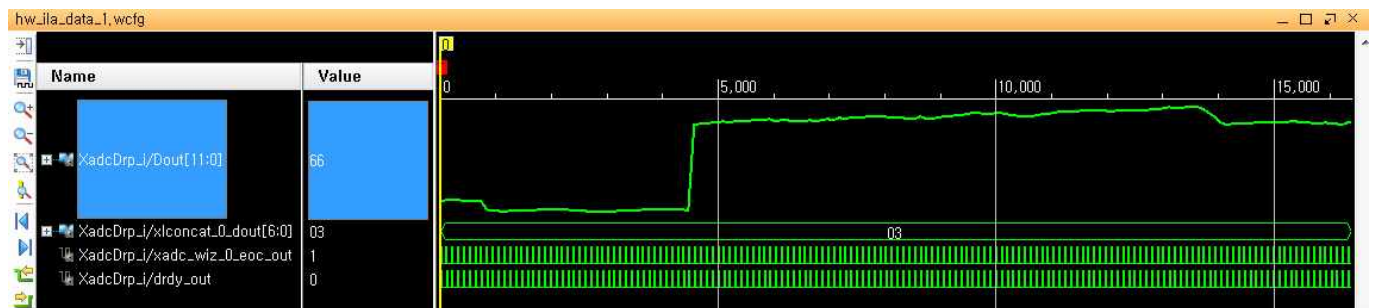




click



Sample 1KHz Pulse train



Change capture mode to basic, click (run trigger)

ILA Properties

Trigger Mode Settings

Trigger mode: BASIC

☐ Trigger in

☐ Trigger out

Capture Mode Settings

Capture mode: BASIC

Data depth: 16384

Trigger position: 0 [0 - 16383]

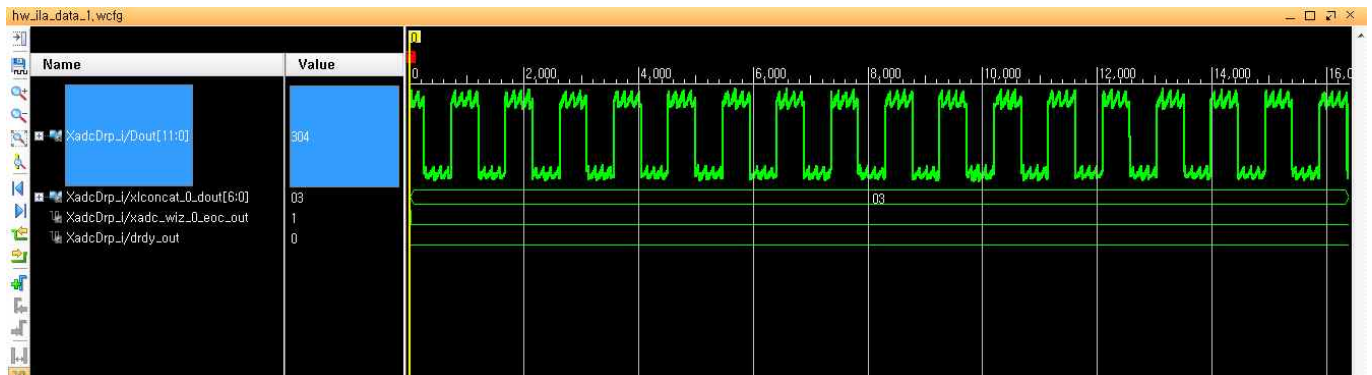
Trigger Capture Status

Basic Trigger Setup

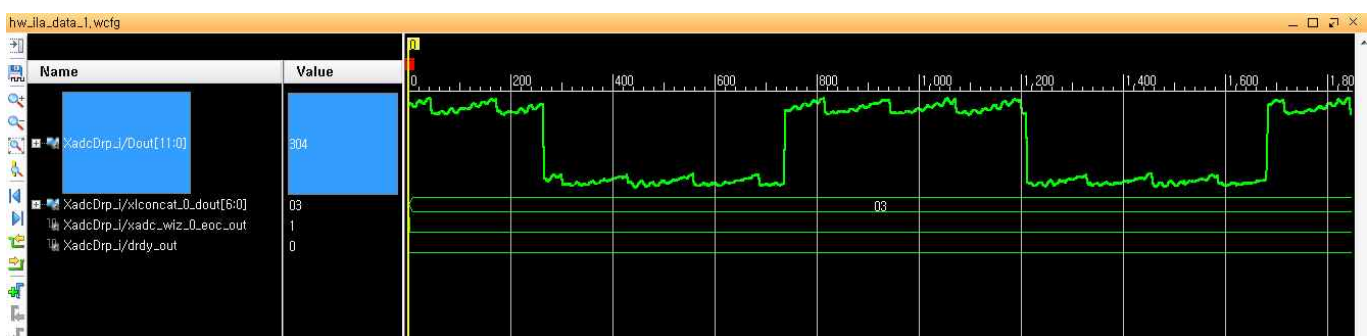
Name	Compare Value
XadcDrp_i/xadc_wiz_0_eoc_out	== [B] R

Basic Capture Setup

Name	Compare Value
XadcDrp_i/drdy_out	== [B] F



click



- about 940 samples per a cycle --> $961.54 \text{ ksp/s} / 940 \text{ samples} = \text{about } 1.02 \text{ k/s} = 1.02 \text{ KHz}$
- pulse amplitude ----> $304 / 4096 * 1 \text{ V} = \text{about } 74 \text{ mV}$

See you next Lab5.