	ESP32-S2				
	Memory Map				
I-bus		D-bus			
0x4000_0000					
	ROM0				
0 4000 ====	(64 kB)				
0x4000_FFFF					
04001 0000					
0x4001_0000		0x3FFA_0000 			
	DOM				
	ROM1 (64 kB)				
0x4001_FFFF	(04 KB)	0x3FFA FFFF			
		L			
0x4002_0000		0x3FFB_0000			
	SRAM0				
2 1222 5	(32 kB)				
0x4002_7FFF		0x3FFB_7FFF			
0x4002 8000		0x3FFB 8000			
		1			
	SRAM1				
	(288 kB)	(*) the boundary addresses depends on the boot stage.			
	, ,	The buffers area used during bootstrapping ends at address 0x3FFF_C410			
0x4005_AB00		0x3FFE_AB00 *			
	(DOM and a recomined)				
0x4006_FFFF	(ROM-code reserved)	0x3FFF_FFFF			
0*5000 0000		Peripheral bus 1: Peripheral bus 2	<u>2:</u>		
0×5000_0000		<u>Peripheral bus 1: Peripheral bus 3:</u> 0x5000_0000 0x3F42_1000 0x6002_1000	<u>?:</u>		
-	RTCSLOW		<u>?:</u>		
0x5000_0000 0x5000_1FFF	RTCSLOW (8 kB)		<u>?:</u> 		
-		0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF	<u>2:</u> 		
-	(8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF	<u>2:</u> 		
-	(8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000	<u>2:</u>		
-	(8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF	<u>2:</u>		
-	(8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF	<u>:</u>		
-	(8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF	<u>2:</u>		
-	(8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF 0x3F00_0000	<u>2:</u>		
-	(8 kB) RTCFAST (8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF 0x3F00_0000 (Read Only) (Ext. Flash or RAM)	<u>2:</u>		
-	(8 kB) RTCFAST (8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF 0x3F00_0000 (Read Only)	<u>2:</u>		
-	(8 kB) RTCFAST (8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF 0x3F00_0000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks)	<u>2:</u>		
-	(8 kB) RTCFAST (8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF 0x3F00_0000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F3F FFFFF	-		
-	(8 kB) RTCFAST (8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF 0x3F00_0000 (Read Only) (Ext. Flash or RAM) (64kB 1-cache blocks) (8,16,32 bit alig. RD) 0x3F3F_FFFF 0x3F50_0000	<u>2:</u>		
-	(8 kB) RTCFAST (8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF 0x3F00_0000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F3F_FFFF	<u>2:</u>		
-	(8 kB) RTCFAST (8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF 0x3F00_0000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F3F_FFFF 0x3F50_0000 (PSRAM RDWR, or	<u>2:</u>		
-	(8 kB) RTCFAST (8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF 0x3F00_0000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F3F_FFFF 0x3F50_0000 (PSRAM RD/WR, or ext. Flash RD only) (64kB D-Cache blocks)	-		
-	RTCFAST (8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F3F_FFFF 0x3F50_0000 (PSRAM RD/WR, or ext. Flash RD only) (64kB D-Cache blocks) (8,16,32 bit align. RD/WR) (DMA access)	-		
-	(8 kB) RTCFAST (8 kB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_EFFF 0x3F00_0000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F3F_FFFF 0x3F50_0000 (PSRAM RD/WR, or ext. Flash RD only) (64kB 0-Cache blocks) (8,16,32 bit align. RD/WR)	<u>::</u>		
-	(8 kB) RTCFAST (8 kB) I-Cache (4 MB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF 0x3F00_0000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F3F_FFFF 0x3F50_0000 (PSRAM RD/WR, or ext. Flash RD only) (64kB D-Cache blocks) (8,16,32 bit align. RD/WR) (DMA access) (if DMA+D-Cache access	<u>::</u>		
-	(8 kB) RTCFAST (8 kB) I-Cache (4 MB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF 0x3F00_0000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F3F_FFFF 0x3F50_0000 (PSRAM RD/WR, or ext. Flash RD only) (64kB D-Cache blocks) (8,16,32 bit align. RD/WR) (DMA access) (if DMA+D-Cache access	<u>::</u>		
-	(8 kB) RTCFAST (8 kB) I-Cache (4 MB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 0x3FF9_FFFF 0x3F00_0000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F3F_FFFF 0x3F50_0000 (PSRAM RD/WR, or ext. Flash RD only) (64kB D-Cache blocks) (8,16,32 bit align. RD/WR) (DMA access) (if DMA+D-Cache access	<u>::</u>		
-	(8 kB) RTCFAST (8 kB) I-Cache (4 MB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F50_0000 (PSRAM RD/WR, or ext. Flash RD only) (64kB D-Cache blocks) (8,16,32 bit align. RD/WR) (DMA access) (if DMA+D-Cache access data must be consistent)	<u>::</u>		
0x5000_1FFF	(8 kB) RTCFAST (8 kB) I-Cache (4 MB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F50_0000 (PSRAM RD/WR, or ext. Flash RD only) (64kB D-Cache blocks) (8,16,32 bit align. RD/WR) (DMA access) (if DMA+D-Cache access data must be consistent)	<u>::</u>		
0x5000_1FFF 0x4008_0000 (Ext. Flash or RAM)	RTCFAST (8 kB) I-Cache (4 MB) D-Cache (10.5 MB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F50_0000 (PSRAM RD/WR, or ext. Flash RD only) (64kB D-Cache blocks) (8,16,32 bit align. RD/WR) (DMA access) (if DMA+D-Cache access data must be consistent)	<u>::</u>		
0x5000_1FFF	RTCFAST (8 kB) I-Cache (4 MB) D-Cache (10.5 MB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F50_0000 (PSRAM RD/WR, or ext. Flash RD only) (64kB D-Cache blocks) (8,16,32 bit align. RD/WR) (DMA access) (if DMA+D-Cache access data must be consistent)	<u>::</u>		
0x5000_1FFF 0x4008_0000 (Ext. Flash or RAM) (64kB I-Cache blocks)	RTCFAST (8 kB) I-Cache (4 MB) D-Cache (10.5 MB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F50_0000 (PSRAM RD/WR, or ext. Flash RD only) (64kB D-Cache blocks) (8,16,32 bit align. RD/WR) (DMA access) (if DMA+D-Cache access data must be consistent)	<u>:</u>		
0x5000_1FFF 0x4008_0000 (Ext. Flash or RAM) (64kB I-Cache blocks)	RTCFAST (8 kB) I-Cache (4 MB) D-Cache (10.5 MB)	0x5000_0000 0x3F42_1000 0x6002_1000 0x5000_1FFF 0x3F42_2FFF 0x6002_2FFF 0x3FF9_E000 (Read Only) (Ext. Flash or RAM) (64kB l-cache blocks) (8,16,32 bit alig. RD) 0x3F50_0000 (PSRAM RD/WR, or ext. Flash RD only) (64kB D-Cache blocks) (8,16,32 bit align. RD/WR) (DMA access) (if DMA+D-Cache access data must be consistent)	-		

PeriBus1 addr:

(speculative rd/wr add volatile

0x3F40_0000 OR use peribus2) 0x3F40_0000 UART (restricted*) 0x3F40 2000 SPI1 (SPI flash) SPI0 0x3F40_3000

0x3F40_4000 **GPIO** 0x3F40 4F00 GPIO_SD 0x3F40_5000 FE2 0x3F40_6000 FΕ

0x3F40_7000 FRC_TIMER 0x3F40_8000 RTCCNTL 0x3F40_8400 RTCIO SENS

0x3F40_8800 0x3F40_8C00 RTC_I2C IO MUX 0x3F40 9000 0x3F40_B000 HINF

0x3F40_F000 I2S 0x3F41_0000 UART1 (restricted*)

0x3F41_3000 I2C_EXT 0x3F41_4000 UHCI0 0x3F41_5000 SLCHOST

0x3F41_6000 RMT (restricted*) 0x3F41_7000 **PCNT**

0x3F41_8000 SI C 0x3F41_9000 LEDC0x3F41 A000 **EFUSE** 0x3F41_C000 NRX 0x3F41_D000 ВВ

0x3F41 F000 TIMERGROUP0 TIMERGROUP1 0x3F42_0000 0x3F42_1000 RTC_SLOWMEM 0x3F42_3000 SYSTIMER

0x3F42_4000 SPT2 0x3F42_5000 SPI3 0x3F42_6000

SYSCON (APB_CTRL*) 0x3F42_7000 I2C1_EXT

0x3F43_7000 SPI4 0x3F43 9000 USB WRAP APB_SARADC 0x3F44_0000

0x3F4C 0000 SYSTEM 0x3F4C_1000 **SENSITIVE** 0x3F4C_2000 0x3F4C_3000 INTERRUPT DMA_COPY 0x3F4D_0000 INTRUSION

0x6180_0000

Peripherals (16 kB)

ESP32-S2

Peripherals

(1 MB)

0x6180_0000 EXMEM_BASE 0x6180_1000 MMU_TABLE 0x6180_2000 ITAG_TABLE 0x6180_3000 DTAG_TABLE

PeriBus2 addr:

(FIFO registers; No-instr. fetch)

ANA_CONFIG_REG 0x6000_E044 0x6002_1000 RTCSLOW1 0x6003_5110 WDEV_RND_REG 0x6003 A000 AES

0x6003_B000 SHA 0x6003_C000 RSA

0x6003 D000 DIGITAL_SIGNATURE 0x6003_E000 **HMAC**

0x6003_F000 CRYPTO_DMA

0x6008_0000 USB

	Blk#	Bits	Purpose		
(3)	0	640	SYSTEM		
SP32-S2	1	288	MAC,SPI_PAD,SYS_DATA0		
	2	352	SYS_DATA_PART1		
	3	352	USR_DATA*		
	4	352	KEY0_DATA*		
e-Fuses	5	352	KEY1_DATA*		
C-1 U3C3	6	352	KEY2_DATA*		
	7	352	KEY3_DATA*		
	8	352	KEY4_DATA*		
	9	352	KEY5_DATA*		
	10	352	SYS_DATA_PART2		
	(*) RD/WR can be disabled				