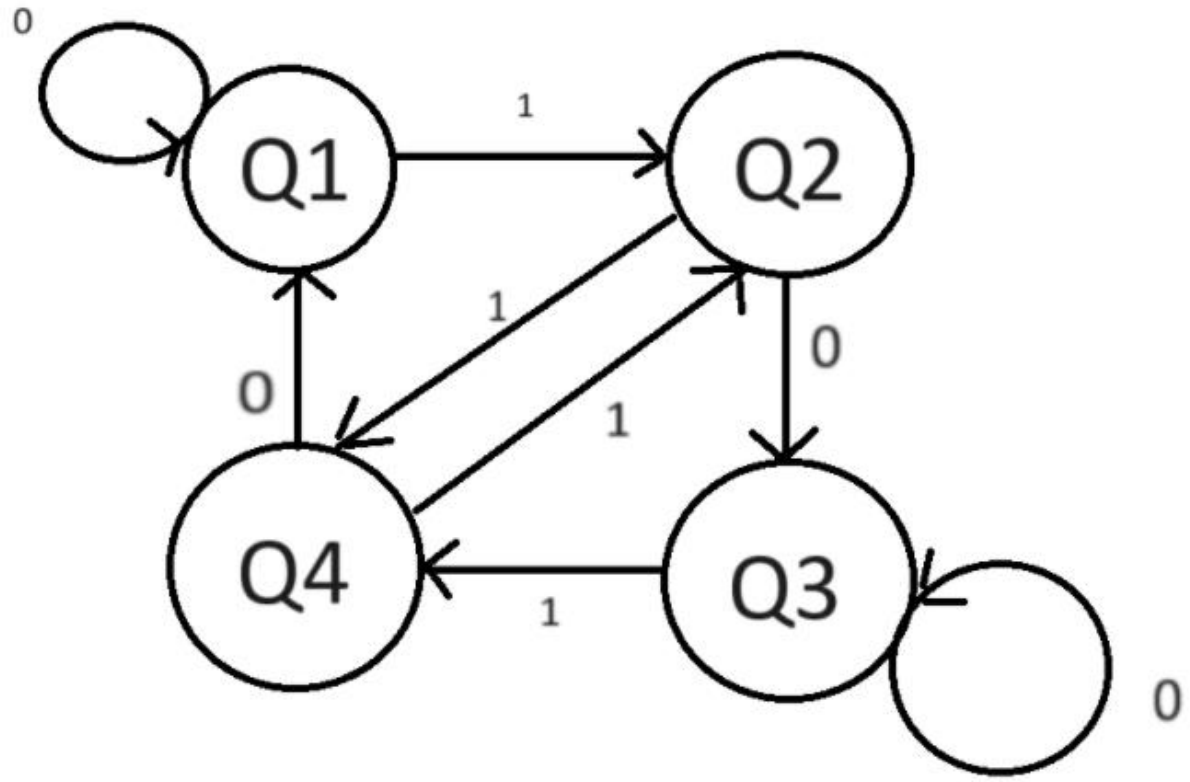
Digital circuits laboratory class	**Year 2024, exercise 5**
Author: Jakub Turkowski	Title of the exercise: Synthesis of synchronous circuit
Laboratory group number: 2	Week day: Tuesday Realization date: 16.04.2024 Hours of the lab: 15:15-16:55

Moore machine



where:

	Q1	Q2	Q3	Q4
Y1 Y2	0 0	0 1	1 1	1 0

X	Y1	Y2	Y1 NEXT	Y2 NEXT	D1	D2
0	0	0	0	0	0	0
0	1	1	1	1	1	1
0	0	1	1	1	1	1
0	1	0	0	0	0	0
1	0	0	0	1	0	1
1	1	1	1	0	1	0
1	0	1	1	0	1	0
1	1	0	0	1	0	1

And from the table:

D1 = X'Y2+XY2=Y2

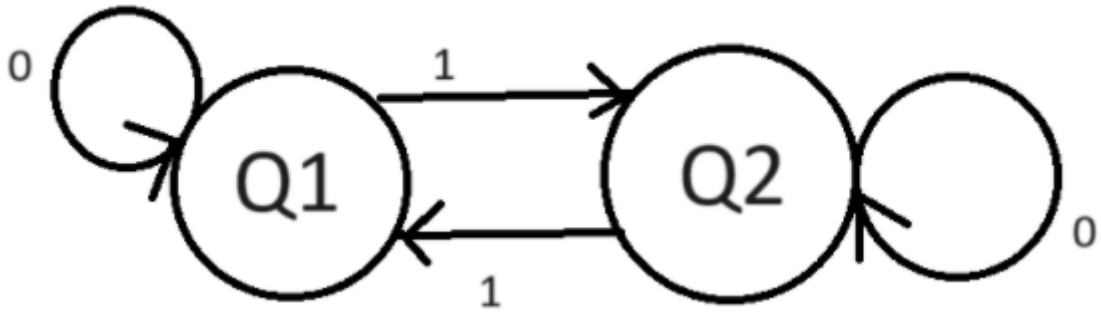
D2 = X'Y2+XY2'

And for the outputs (as one will be odd and two even):

Z1=Y2Y1'

Z2=Y2'Y1

Mealy's machine



where:

	Q1	Q2
Y	0	1

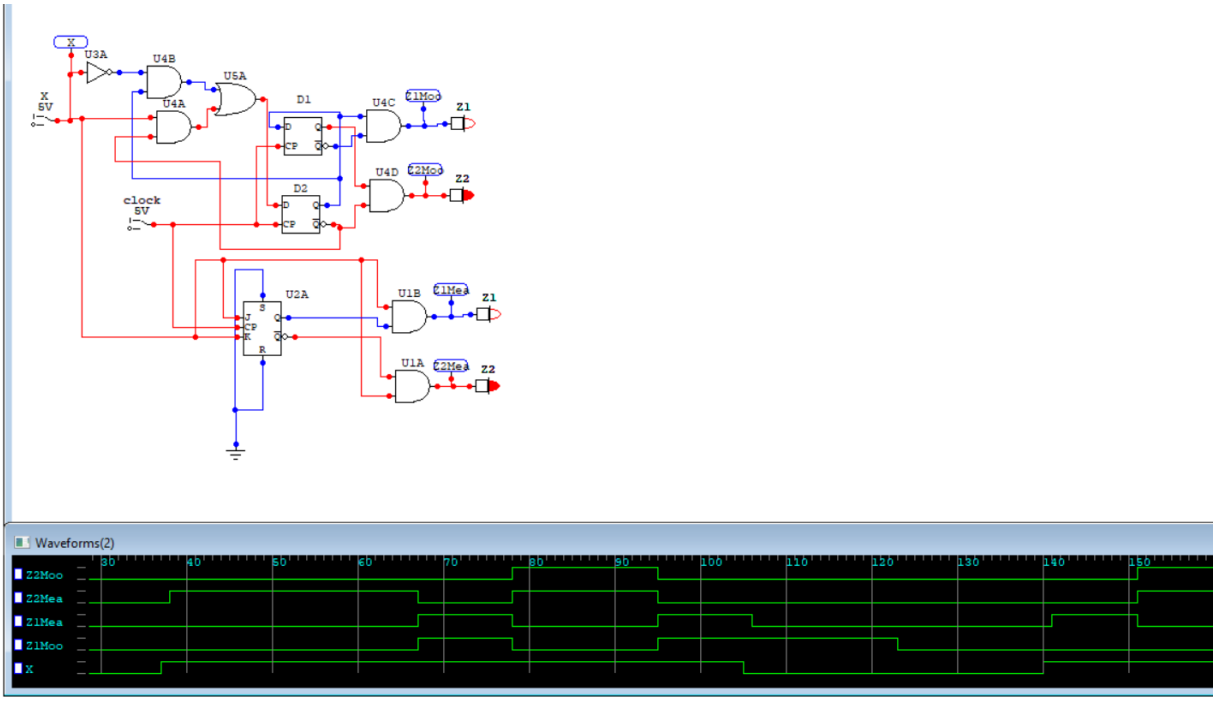
X	Y	Y NEXT	J	K
0	0	0	0	-
1	0	1	1	-
0	1	1	-	0
1	1	0	-	1

And from the table:

J=X

K=X

As this implementation only uses one JK flip flop, we only take into account the J and K (X) and the outputs – the negated one for even ones and regular for odd ones.


X
U3A
U4B
U5A
U4A
X
5V
D1
U4C
Z1Moo
Z1
U4D
Z2Moo
Z2
D2
clock
5V
U2A
U1B
Z1Mea
Z1
U1A
Z2Mea
Z2
Waveforms(2)
Z2Moo
Z2Mea
Z1Mea
Z1Moo
X
30
40
50
60
70
80
90
100
110
120
130
140
150