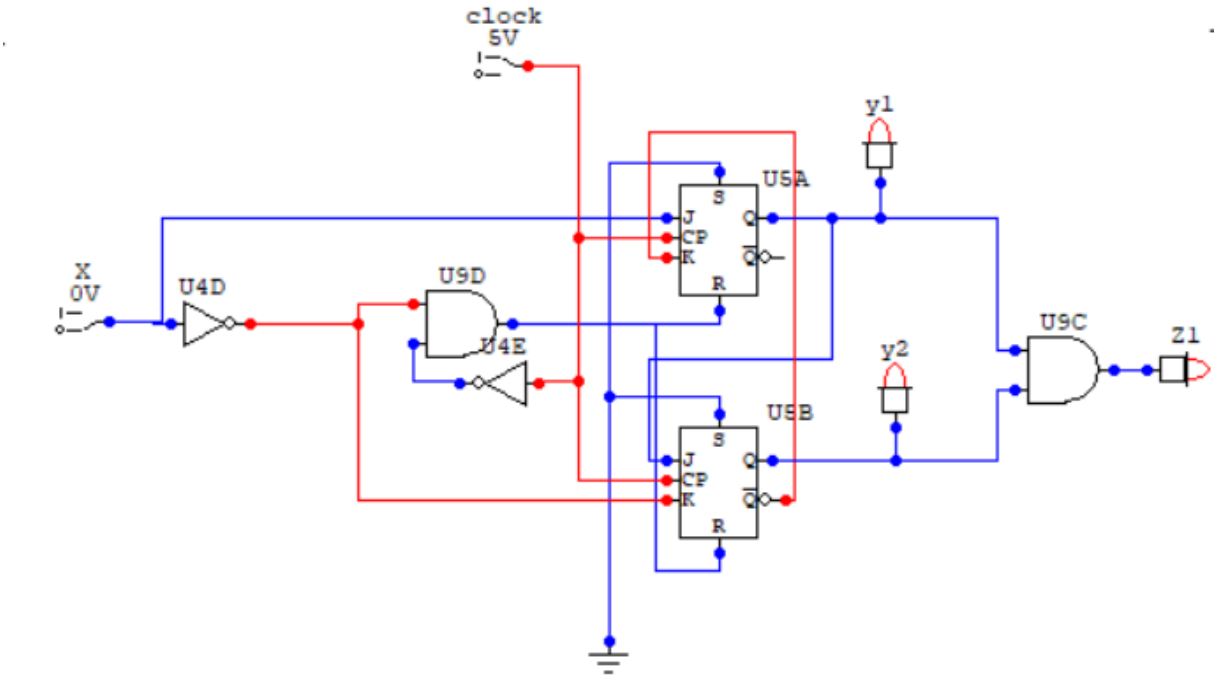
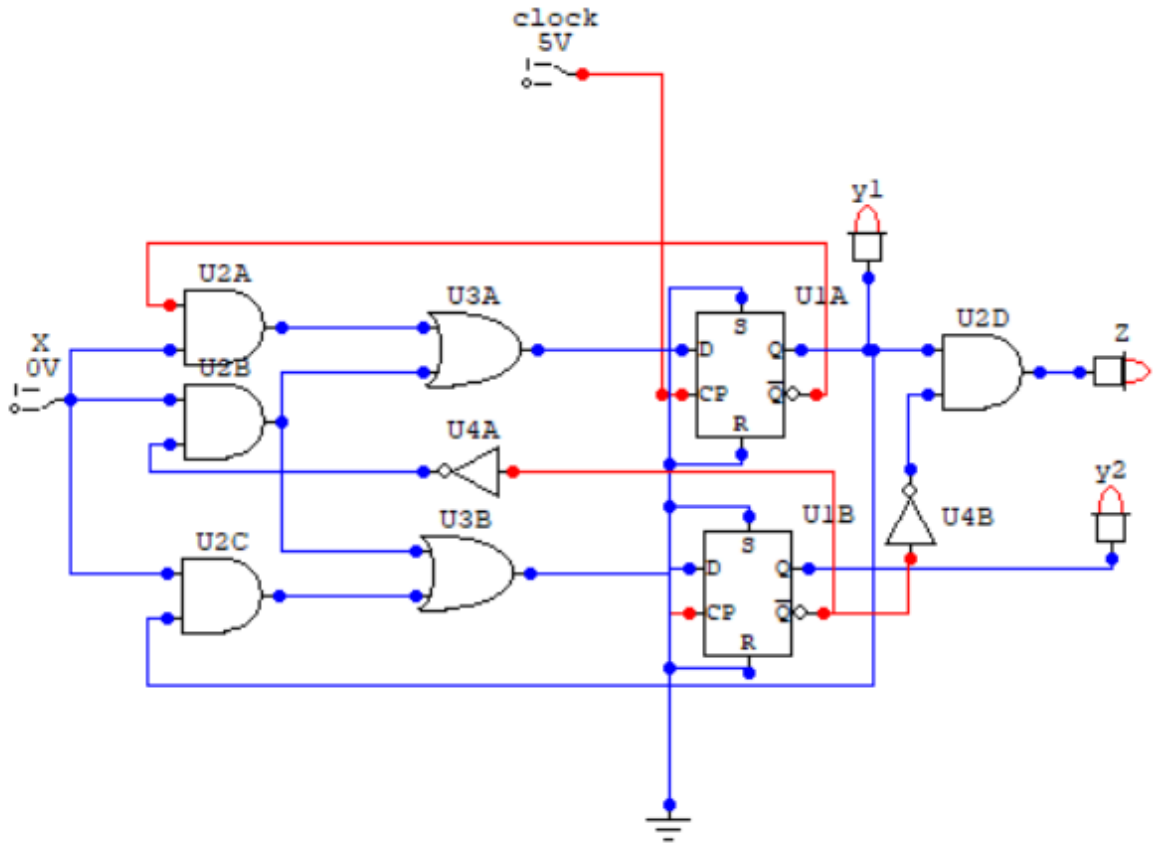
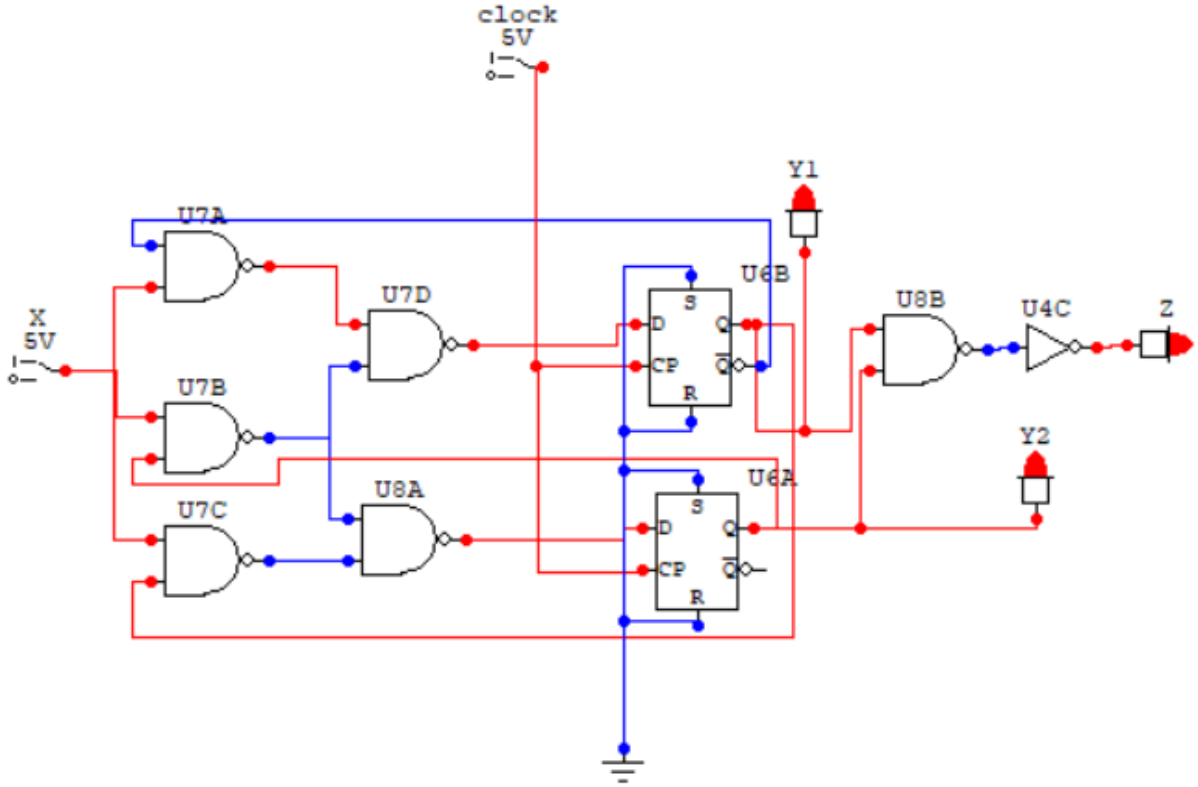
Digital circuits laboratory class	**Year 2024, exercise 4**
Author: Jakub Turkowski	Title of the exercise: Analysis of synchronous circuit
Laboratory group number: 2	Week day: Tuesday Realization date: 09.04.2024 Hours of the lab: 15:15-16:55

X	D1	D1 NEXT	D2	D2 NEXT	Y
0	0	0	0	0	0
0	0	0	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
1	0	1	0	0	0
1	0	1	1	1	1
1	1	0	0	1	0
1	1	1	1	1	1



As the first row of NAND gate of a JK flipflop additionally takes in the output (regular and negated) it kind makes the gates of the circuit with D flipflop obsolete. For it to reset however we need to take into account the change of clock and value of X, which will be inserted using the and gate.


clock
5V
y1
U2A
U3A
U1A
U2D
Z
X
0V
U2B
U4A
y2
U3B
U1B
U4B
U2C
S
D
Q
CP
R


clock
5V
Y1
U7A
U6B
U8B
U4C
Z
X
5V
U7D
U7B
Y2
U8A
U6A
U7C
S
D
Q
CP
R

time	t1	t2	t3	t4	t5	t6
x	1	1	1	1	0	0
y1y2	1 0	0 1	1 1	1 1	0 0	0 0
Z	0	0	1	1	0	0

For the NAND version:

D1: (y1'x)+(y2x) = ((y1'x)'(y2x)')'

D2: (y1x)+(y2x) = ((y1x)'(y2x)')'

O: (y2y1) = ((y2y1)')'