1. (10 Points) Explain in your own words how two-four bit integer values would be multiplied. (HINT It might be easiest to show an example of 2 numbers and then explain what was done.)

   1000 <= **Multiplicand = 8**
   0110 <= **Multiplier = 6**
   0000
   1000
   1000
   0000 =
   0110000 **= 48**

2. (10 Points) Using the IEEE 754 Single Precision Format, express 36.125 * 10 ^ 0 in binary

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
s	exponent								fraction																						
1 bit	8 bits								23 bits																						

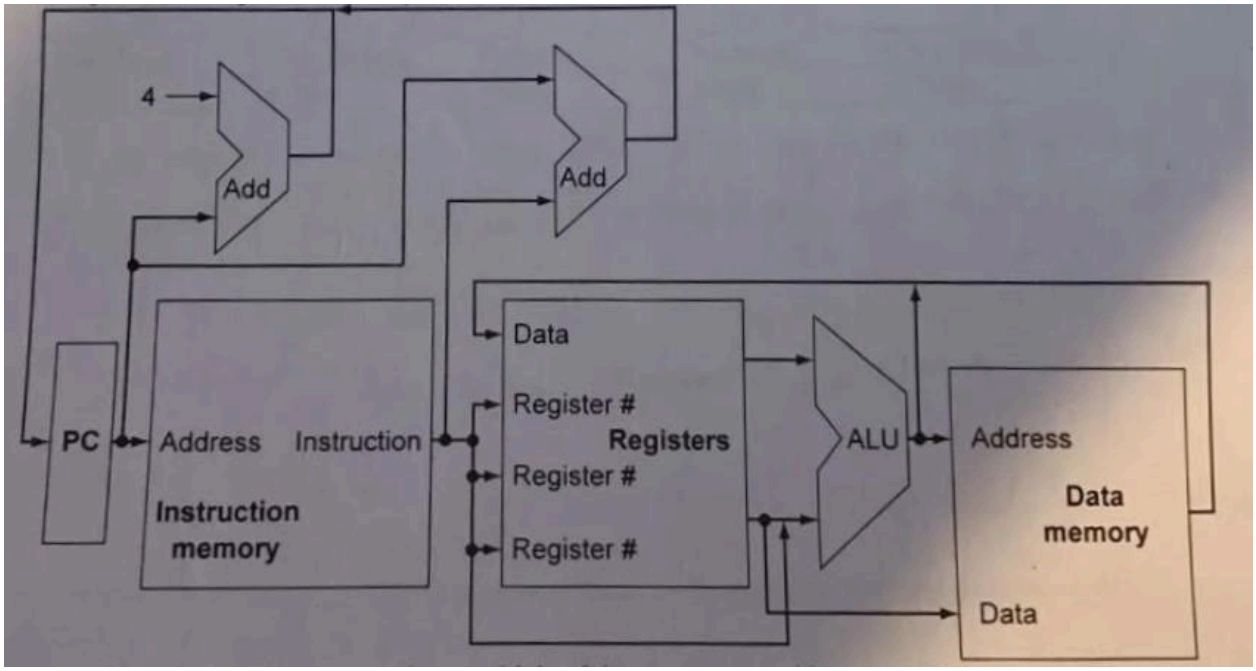
   36.125
   36 = 100100 Normalize 100100.001 = 1.00100001 * 2^5
   36.125 = 100100.001 Exponent = 127 + 5 = 132
   Sign is positive, so s bit = 0 So Exponent = 10000100
   Therefore the final answer is 0 1000100 00100001000

3. (10 Points) Convert the value C0A00000 (base 16) to a base 10 floating point value
   C0A0 = 1100 0000 1010 0000 …. 0000
   Sign = 1, negative
   Exponent = 1000 0001 = 129, so 129 - 127 = 2
   Fraction is 1.01 = 1.25
   So it is -1.25 * 2^2

4. (10 Points) Section 3.6 in the text introduces the idea of a *subword parallelism*. What does the author mean by this term and explain how it is supported on the LEGv8 processor

   Subword parallelism is explained as a large data element being broken apart into smaller parts. Which makes it faster to process them. A good example would be a 128-bit adder being broken into 8 16-bit adders. It is supported by breaking large data inputs and separating into different parts.

5. (10 Points) Using the following figue, please answer the questions listed below.



   a. How is the decision made on which of the two upper adders to use?
      Top-Left: Adds 4 to the program counter to go to the next instruction

   b. Why does the bottom input to the ALU have two possible sources?
      Top-Right: This is dealt with by a branch condition and may add branch address to PC

6. (10 Points) What is meant by the term *edge-triggered* clocking methodology?

   Edge-triggered clocking methodology is the way to detect a change of an action. So when either a rising edge or falling edge is encountered the inputs can change, it is used for data reads/writes

7. (10 Points) Explain in your own words the basic idea behind pipelined execution. You may assume the following 5 stages and times exist in the data path. Finally answer what your clock cycle time must be for this pipeline.

Inst. Fetch	Inst. Decode	Execute	Memory	Writeback
300ps	400ps	200ps	400ps	200ps

Pipeline execution is the idea that perform instructions in **overlapped** fashion as different instructions are being executed. This increases the amount of instructions that can be done.

Clock Cycle Time = longest instruction * #number of instructions 400 * 5 = 2000 pico seconds

8. (15 Points) There are three hazards that may occur in the pipeline. List and describe each of them

   Structural: The same action is incapable of occurring at the same clock cycle. Two instructions cant both be using the same component

   Data: The data needed isnt fully ready yet and system needs to stall

   Control: Control authorization depends on previous instruction

9. (15 Points) Using the following information and the figure on page 1 of the exam answer the following two questions (Clearly label your work)

I-D Mem	Reg File	Mux	ALU	Adder	Gate	Register Read	Register Setup	Sign Extend	Control
275 ps	175 ps	30 ps	250 ps	150 ps	5 ps	30 ps	20 ps	50 ps	75 ps

   a. What is the latency of the R-type instruction?

      R-type: PC + IM + MUX + RF + MUx + ALU + MUX + RS = 840 PS

   b. What is the latency of the LDUR instruction?

      LDUR: PC + IM + RF + ALU + I-D Mem + MUZ + RS = 1055 PS