**MUX0**

0

31

**INV**

rd(32)

rsc(5)

rtc(5)

rdc(5)

rs(32)

rti(32)

rto(32)

**npc**

(ADD)

**pc**

Address

**IMem**

0

31

4

**ALU**

a(32)

**RegFile**

b(32)

ALUC(4)

overflow

op(6)

rsc(5)

rtc(5)

rdc(5)

sa(5)

func(6)

**MUX1**

M1\_1 & ~exc

[imm(26)]

r(32)

zero

**MUX2**

M2

**EXT5**

sa

32b

rtin

RT\_IN & ~exc

s

00

1x

1

0

000

010

**S\_EXT16**

imm16

32b

**MUX3**

11

00

M3\_1

Address

**DMem**

Data

DM\_WEA & ~exc

**MUX4**

00

01

M4\_1

**S\_EXT18**

imm16

32b

**ADD**

A

**||**

00

B

**MUXJ**

1

0

001

M0\_0

**MUX5**

01

00

M5\_1

**EXT16**

10

imm16

M3\_0

011

[imm(16)]

**||**

00

31 ~ 28

imm26

32b

**ADD**

A

B

8

**MUX6**

M6\_0

00

01

01

M1\_0 & ~exc

CLK\_WB

CLK\_PC

CLK\_MA

**hi**

**MUL**

**DIV**

**CP0**

**ENC**

A

B

R

Q

A

B

HI

LO

DSIGN

MSIGN

**lo**

**MUX7**

M7\_0 & ~dbz

00

M7\_1 & ~dbz

01

10

11

**MUX8**

M8\_0 & ~dbz

00

M8\_1 & ~dbz

01

10

11

negative

M5\_0

1x

width

WIDTH(2)

SIGN

sign

pc

exc\_type

EXC\_T(8)

10x

11x

M0\_1

exception

handler

address

wea

C0\_WEA

addr

din

dout

M6\_1

10

11

M4\_0

1x

exc

**MUX9**

M9\_0

01

00

**MUXE**

1

0

M\_E

**MUXO**

1

overflow

0

0x0c

**MUXT**

1

TRAP & zero

0

0x0d

01

0

**INV**

M9\_1

1x

**AND**

dbz

DIV

dbz

**MUXA**

1

0

0xff

err

**MUXW**

1

0

0x04

DM\_WEA

0x05