**pc**

**DMEM**

d\_in

d\_out

addr

w\_ena

width

ext

**IMEM**

d\_in

d\_out

addr

w\_ena

**GPReg**

rs1\_addr

rd\_addr

rs2\_addr

rs1

rd

rs2

**ALU**

a

b

r

aluc

flags

**Extractor**

ir

rs1

rs2

rd

One stage

opcode

funct3

funct7

**Decoder**

opcode

funct7

funct3

ctrl\_bits

**Adder**

4

Multiplexer with control bits after decoding

output

inputs

extra selection except control bits

In origin get pc.

Stage1: after IF pc, control bits, imm, rs1, rs2, rd\_addr

Stage2: after EX pc, control bits, imm, rs1, rs2, rd\_addr, r, flags

Stage3: after MA pc, control bits, imm, rs1, rs2, rd\_addr, r, flags, dout

Stage4: after WB pc, control bits, imm, rs1, rs2, rd\_addr, r, flags, dout, new pc

clk

registers

MUX control bits:

Before PC: m1(1)

Before rd: m2(2)

Before a & b: m3(1), m4(1)

Which are

m1, m2(2), m3, m4, func3(3), func7(7), w\_ena, rd\_w

imm

Async