**pc**

**DMEM**

d\_in

d\_out

addr

w\_ena

width

ext

**IMEM**

d\_in

d\_out

addr

w\_ena

**GPReg**

rs1\_addr

rd\_addr

rs2\_addr

rs1

rd

rs2

**ALU**

a

b

r

aluc

flags

**Extractor**

ir

rs1

rs2

rd

opcode

funct3

funct7

**Decoder**

opcode

funct7

funct3

ctrl\_bits

**Adder**

4

imm

**IF stage**

**IMEM**

axi\_in

d\_out

addr

axi\_out

pc

**Extractor**

ir

rs1

rs2

rd

opcode

funct3

funct7

imm

**ID stage**

**Decoder**

opcode

funct7

funct3

op

**Reg**

rs1

rs2

rd

Use sv structures to store input and output signals for each stage to eliminate naming conflict

**WB stage**

**GPRs**

rs\_addr

rd\_addr

rs\_data

**Forward**

**control**

rs

rd\_data

rs\_addr

fwd\_addr

fwd\_data

**EX stage**

**ALU**

rs1

rs2

r

flags

funct3

funct7

funct3

funct7

op

valid

**MA stage**

**DMEM**

d\_in

d\_out

addr

w\_ena

width

ext

r

funct3

rs2

op

op

valid

valid

axi\_in

axi\_out