TODO:

1. The order of ALU input ports should be properly designed when combining all the data pathes.
2. Hardwired CU decoding and encoding may need to be simplified by good use of function code(group by option code), take notice.

Public Components

**pc**

clk\_pc

pc\_out(32)

pc\_in(32)

**IMEM**

d\_in(32)

d\_out(32)

addr(32)

clk\_mem

w\_ena

**GPReg**

rs1\_addr(5)

rd\_addr(5)

rs2\_addr(5)

rs1(32)

rd(32)

rs2(32)

w\_ena

clk\_gpr

**ALU**

a(32)

b(32)

r(32)

aluc(4)

flags(znco)

**Extractor**

ir(32)

immi(32)

rs1(5)

rs2(5)

rd(5)

imms(32)

immb(32)

immu(32)

immj(32)

opcode(6)

funct3(3)

funct7(7)

LUI

**pc**

**IMEM**

d\_out

addr

**Extractor**

ir

immu

rd

**GPReg**

rd\_addr

rd

**Adder**

4

AUIPC

**pc**

**IMEM**

d\_out

addr

**Extractor**

ir

immu

rd

**GPReg**

rd\_addr

rd

**Adder**

4

**ALU**

a

b

r

JAL

**pc**

**IMEM**

d\_out

addr

**Extractor**

ir

immj

rd

**ALU**

a

b

r

**Adder**

4

**GPReg**

rd\_addr

rd

**pc**

**IMEM**

d\_out

addr

**Extractor**

ir

immj

rd

**ALU**

a

b

r

**Adder**

4

**GPReg**

rd\_addr

rd

JALR

**pc**

**IMEM**

d\_out

addr

**Extractor**

ir

immi

rd

**ALU**

a

b

r

**Adder**

4

**GPReg**

rd\_addr

rd

rs1

rs1\_addr

rs1

BEQ/BNE/BLT/BGE/BLTU/BGEU

**pc**

**IMEM**

d\_out

addr

**Extractor**

ir

immb

**ALU**

a

b

z/n/c

**Adder**

**GPReg**

rs2\_addr

rs1

rs1\_addr

rs1

rs2

rs2

**MUX**

1

0

4

**INV**

LB/LH/LW/LBU/LHU

**pc**

**IMEM**

d\_out

addr

**Extractor**

ir

immi

rs1

rd

**GPReg**

rd\_addr

rs1\_addr

rs1

rd

**ALU**

a

b

r

**DMEM**

d\_out

addr

width

ext

SB/SH/SW

**pc**

**IMEM**

d\_out

addr

**Extractor**

ir

imms

rs1

**GPReg**

rs2\_addr

rs1\_addr

rs1

**ALU**

a

b

r

**DMEM**

d\_in

addr

width

ext

rs2

rs2

w\_ena

ADDI/SLTI/SLTIU/XORI/ORI/ANDI/SLLI/SRLI/SRAI

**pc**

**IMEM**

d\_out

addr

**Extractor**

ir

immi

rs1

**GPReg**

rd\_addr

rs1\_addr

rs1

**ALU**

a

b

r

rd

rd

ADD/SUB/SLL/SLT/SLTU/XOR/SRL/SRA/OR/AND

**pc**

**IMEM**

d\_out

addr

**Extractor**

ir

rs1

**GPReg**

rs2\_addr

rs1\_addr

rs1

**ALU**

a

b

r

rd

rd

rs2

rd\_addr

rs2

FENCE

Implemented in out-of-order process.

ECALL/EBREAK

Implemented in privileged instructions.