System Controller Firmware Release Notes

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Chapter 1

Introduction

This document contains release notes for the i.MX8 System Controller Firmware (SCFW). This includes:

- Highlights
- Changes from the previous release
- Known issues
- Additional info

The table below lists the release information:

Release Info	
Release name	imx_4.14.62_beta_p3
Previous release	imx_4.9.88_imx8qxp_beta2
Branch	imx_4.14.62_1.0.0_beta
Build number	2814
Commit ID	0x006ff1979
Build date	Nov 19 2018
Supported devices	i.MX8QM (A0), i.MX8QM (B0), i.MX8QXP (B0), and derivatives

1.1 Highlights

- Added support for i.MX8QM B0
- Dropped support for i.MX8QXP A0
- Supported SECO FW v0.1.0, dropped support for older SECO FW
- Added support for low power modes (KS1 and KS1.5)
- Added DDR retention support to NXP board ports

Note SCFW version 0.1.0 is **REQUIRED** for correct operation!

Chapter 2

Change List

Below is a list of changes between the previous release (imx_4.14.62_beta_p2) and this release (imx_4.14.62_beta_p3).

2.1 Bug

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-265	Ensure clocks are enabled before performing memory repair	Y	Y	Y

2.2 Improvement

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-253	Add ddr_stress_test_parser.cfg to all platform/board/<So↩ C>/dcd folders	Y	Y	Y

2.3 Prior 4.14.62 Beta Patch 2 Change List

Below is a list of changes between the previous release (imx_4.14.62_beta_p1) and this release (imx_4.14.62_beta_p2).

2.4 Improvement

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-256	Update 8QM GPU operating point based on design targets		Y	

2.5 Prior 4.14.62 Beta Patch 1 Change List

Below is a list of changes between the previous release (imx_4.14.62_beta) and this release (imx_4.14.62_beta_p1).

2.6 Bug

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-249	PCIE internal clk jitter improvement		Y	

2.7 Prior 4.14.62 Beta Change List

Below is a list of changes between previous release (imx_4.9.88_imx8qxp_beta2) and this release (imx_4.14.62_beta).

2.8 New Feature

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-70	Add support for KS1.5 during suspend	Y	Y	Y
SCF-78	Add individual PF100 register access	Y	Y	Y
SCF-112	Support MLB PLL	Y	Y	Y
SCF-113	Support customer merge of porting kits [detail]	Y	Y	Y
SCF-126	Add misc control for CAN IPG_STOP [detail]	Y	Y	Y
SCF-131	Add support for missing eLCDIF clocks and PLL in the Audio D↩ MA subsystem			Y
SCF-135	Add support for multiple bypass clock inputs	Y	Y	Y
SCF-136	Add DDR retention test for 8QM/QXP LPDDR4/DDR4/DDR3	Y	Y	Y
SCF-143	Support SECO FW v0.0.7		Y	Y
SCF-144	Use OP trim from fuses for i.MX8QM	Y	Y	
SCF-146	Support SECO FW v0.1.0 [detail]		Y	Y
SCF-151	Add combined sync control for DC	Y	Y	Y
SCF-152	Support C code in DCD config files	Y	Y	Y
SCF-154	Changes for i.MX8QM B0 bring-up		Y	
SCF-155	Add support for KS1 during suspend	Y	Y	Y
SCF-157	Support boot from OCRAM alias on B0		Y	Y
SCF-161	Allow DC pixel clock to source from bypass clock inputs from H↩ DMI and VPU SS for i.MX8QM	Y	Y	
SCF-163	Add pmic_get_mode() for PF8100	Y	Y	Y
SCF-164	Add i.MX8QM support for HW limited GPU frequency for derivative parts	Y	Y	
SCF-169	Add support for new CLKOUT_ALT output in AVPLL required by HDMI in QM B0		Y	
SCF-176	Add new trim values programmed into fuses for iMX8QM B0		Y	

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-177	Ensure the regulator in AVPLL_0 added for DC in VPU is enabled all the time		Y	
SCF-178	Add support for DDR retention mode [detail]	Y	Y	Y
SCF-181	Add capability to track if a partition has booted	Y		
SCF-189	Add function to configure the SNVS button time parameters [detail]	Y	Y	Y
SCF-192	Show SCU ROM patch version in monitor [detail]		Y	Y
SCF-208	Add i.MX8QXP support for HW limited GPU frequency for derivative parts			Y
SCF-222	Add function to return boot type [detail]	Y	Y	Y

2.9 Improvement

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-61	Implement new DPLL sequence for i.MX8QM B0		Y	
SCF-67	Update M4 warm reset support to align with M4 LPM support		Y	Y
SCF-111	Increase PMIC baud rate for MEK boards	Y	Y	Y
SCF-118	Implement command history buffer in debug monitor	Y	Y	Y
SCF-119	Return system reset reason	Y	Y	Y
SCF-120	Remove root clk handling from powerup/down xtal_osc	Y	Y	Y
SCF-122	Change MU assignments in ALT_CONFIG boot mode [detail]	Y	Y	Y
SCF-123	Update temp sensor conversion equation [detail]		Y	Y
SCF-125	Allow character insert in debug monitor	Y	Y	Y
SCF-128	Improve debug output for MSI timeout errors	Y	Y	Y
SCF-130	Enable debug monitor temp command to run concurrent with S↩ CFW clients	Y	Y	Y
SCF-132	Clean up SoC code to eliminate code duplication	Y	Y	Y
SCF-137	Update i.MX8QXP DDR config to aligned with RPA v10			Y
SCF-139	Fix incorrect copyright information	Y	Y	Y
SCF-140	Display SECO error in monitor		Y	Y
SCF-142	Dump actual temp panic values in monitor debug temp command	Y	Y	Y
SCF-156	Display warning if build options M=1 and D=0 are used together	Y	Y	Y
SCF-160	Sync operating frequencies with datasheet	Y	Y	
SCF-166	Re-enable i.MX8QXP DB PG1 auto clock gating for B0			Y
SCF-170	Optimize early boot time by avoiding SECO calls		Y	Y
SCF-182	Update i.MX8QXP/DX DDR3L configs to aligned with RPA v15			Y
SCF-183	Improve DC test		Y	Y
SCF-185	Leave all refgens enabled when system is active - SW workaround for HW bug			Y
SCF-188	Implement Digital PLL DCO PC selection based on frequency	Y	Y	Y
SCF-190	Increase QM DB PLL to 750MHz from 744MHz	Y	Y	
SCF-191	Allow Ctrl-C to terminate the debug monitor temp loop	Y	Y	Y
SCF-195	Improve error reporting/handling for I2C transfers	Y	Y	Y
SCF-196	Update i.MX8QXP LPDDR4 configs to aligned with RPA_v11			Y

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-197	Update i.MX8QM LPDDR4 configs to aligned with RPA_v16		Y	
SCF-198	Remove R=A0 assumption from Makefile [detail]	Y	Y	Y
SCF-203	Change board_parameter return type to uint32_t and add KS1 board parameters	Y	Y	Y
SCF-205	Align QXP/QM GPU operating points with datasheet		Y	Y
SCF-207	Fix refgen autocal to reduce noise during measurements	Y	Y	Y
SCF-210	Disable all 24MHz clocks when SS is powered down		Y	Y
SCF-211	Relock SCU PLL for QXP B0			Y
SCF-212	Restore DRC LPCG when resuming from KS1 state		Y	Y
SCF-213	Align QXP A35 operating points with datasheet			Y
SCF-229	Disable internal voltage regulator when an AP core is powered down	Y	Y	
SCF-236	Improve debug pll command in monitor	Y	Y	Y
SCF-237	Display warning if old SECO FW used		Y	Y

2.10 Bug

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-51	Partition reboot request hangs	Y	Y	Y
SCF-121	Fix diffclk disable order in SCU subsystem	Y	Y	Y
SCF-124	Fix SCU root clock buffer for i.MX8QM B0		Y	
SCF-127	Fix HSIO phymix disable	Y	Y	Y
SCF-129	Some boards crash if DDR config by ROM but no DDR image	Y	Y	Y
SCF-133	Fix issue building SCFW with debug monitor from porting kit	Y	Y	Y
SCF-138	Fix SCFW test build break due to DDR retention test	Y	Y	Y
SCF-141	Block access to eCSR controls if power state is STBY or OFF	Y	Y	Y
SCF-149	Add clock repeater work around to 8QXP DDR setup			Y
SCF-150	Workaround temp sensor crosstalk HW issue for i.MX8QM [detail]	Y	Y	
SCF-153	FTM0 clock incorrectly mapped to CAN0 clock			Y
SCF-158	Fix i.MX8QM 800MHz DDR script for B0		Y	
SCF-159	Fix i.MX8QM B0 DPLL v18 lock sequence		Y	
SCF-162	PF8100 temp alarm interrupt triggers at incorrect temp	Y	Y	Y
SCF-165	Fix i.MX8QM B0 VPU GPR bit definition		Y	
SCF-174	Fix incorrect AHB/AXI clock frequencies during GPU DVFS operations	Y	Y	
SCF-175	Fix bug in clock(pll) enable/disable code, add valid clock index check	Y	Y	Y
SCF-179	Add workaround for hangs after exit from LPM on closed devices		Y	Y
SCF-180	Simulation compile with monitor broken	Y	Y	Y
SCF-194	Remove dynamic clock management of SCU UART/I2C to avoid LPCG hazards		Y	Y
SCF-200	PCIe detect issue on reset due to too short power off time	Y	Y	Y
SCF-201	Don't enable HW/SW auto clock gate for MSLICE clocks	Y	Y	Y
SCF-202	Can't access CSI_1 without powering up DC_0	Y	Y	Y

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-204	QXP DDR3L clock gating failure due to IO retn			Y
SCF-206	Fix HDMI and HDMI_RX phymix powerdown function	Y	Y	
SCF-214	Reset HDMI RX HPD when HDMI powered on	Y	Y	
SCF-215	Configuration of ADMA UART for test in wrong place			Y
SCF-223	Add partition/virtualization support for DC DPR [detail]	Y	Y	Y

2.11 Task

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-134	Add a Bamboo job to test building from the porting kit	Y	Y	Y
SCF-167	Remove i.MX8QXP A0 build option			
SCF-184	Rework Bamboo nightly builds and test	Y	Y	Y

2.12 Details

This section provides details for select changes.

2.12.1 SCF-113: Support customer merge of porting kits

This change results in all object files being in a unique build directory for each SoC and SoC version. This allows users to combine multiple porting kits into a common kit by just merging the directory structures. The only conflicting file is build_info.h but this is common except for the build time.

The porting kit contains separate tar files for each SoC/version combination. These can be combined using the following command:

find scfw_export_mx8∗.gz -exec tar –strip-components 1 –one-top-level=scfw_export_mx8 -xzvf {} \;

2.12.2 SCF-122: Change MU assignments in ALT_CONFIG boot mode

ALT_CONFIG is only used for internal NXP test cases. No impact to customers except this code is used as an example.

2.12.3 SCF-123: Update temp sensor conversion equation

Temp sensor conversion functions updated to new formula with a fuse-based per-sensor offset. No API changes.

2.12.4 SCF-126: Add misc control for CAN IPG_STOP

New controls added (IPG_STOP and IPG_STOP_ACK) for all three CAN controllers.

2.12.5 SCF-146: Support SECO FW v0.1.0

Added the following new APIs:

- Added sc_misc_seco_attest_mode()
- Added sc_misc_seco_attest()
- Added sc_misc_seco_get_attest_pkey()
- Added sc_misc_seco_get_attest_sign()
- Added sc_misc_seco_attest_verify()
- Added sc_misc_seco_commit()
- Changed sc_misc_seco_forward_lifecycle() parameters and docs to make usage more clear
- Added new SECO authentication commands for SECO FW

2.12.6 SCF-150: Workaround temp sensor crosstalk HW issue for i.MX8QM

To avoid a temp sensor crosstalk issue, sensors are now sequentially driven by SCFW. This adds some delay in getting first reading after power up so read calls might return SC_ERR_BUSY if no reading is available yet. Clients should treat this error as a try again indicator.

2.12.7 SCF-178: Add support for DDR retention mode

Requires customers update board.c to:

- Define retention data structures
- Call soc_ddr_config_retention() from board_init_ddr()
- Call soc_self_refresh_power_down_clk_disable_entry() from board_ddr_config()
- Call soc_refresh_power_down_clk_disable_exit() from board_ddr_config()

DDR retention parameters come from defines generated by the DDR RPA tool.

See reference board.c implementations for NXP boards.

2.12.8 SCF-189: Add function to configure the SNVS button time parameters

New internal SNVS_ButtonTime() function added. This can be called from the board_init() function in board.c. Allows the button debounce time, on time, and press time to be configured. See the SNVS section of the SRM for more details.

2.12.9 SCF-192: Show SCU ROM patch version in monitor

SCFW performs an XOR CRC or the ROM patch fuses. The value can be returned via the sc_misc_rompatch_↩ checksum() function. It is also displayed in the SCFW debug monitor using the 'info' command.

For i.MX8QXP B0:

- V0.0.3 0x24180B1E
- V0.0.6 0x753A8E47
- V0.0.8 0x8B33D88F

2.12.10 SCF-198: Remove R=A0 assumption from Makefile

Make no longer defaults to a silicon rev of A0. It now requires an R=<srev> argument, otherwise an error is displayed.

2.12.11 SCF-222: Add function to return boot type

Added sc_misc_get_boot_type() function to return boot type:

- SC_MISC_BT_PRIMARY
- SC_MISC_BT_SECONDARY
- SC_MISC_BT_RECOVERY
- SC_MISC_BT_MANUFACTURE
- SC_MISC_BT_SERIAL

2.12.12 SCF-223: Add partition/virtualization support for DC DPR

Modified XRDC MDAC mask configuration to also catch DPR transactions. No API change.

Chapter 3

Known Issues

Below is a list of known outstanding issues in this release (imx_4.14.62_beta_p2).

3.1 New Feature

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-147	Support SECO FW v0.2.0		Y	Y
SCF-148	Support SECO FW v1.1.0		Y	Y
SCF-225	Support SECO FW v1.2.0		Y	Y
SCF-230	Limit the ethernet frequency for DX based on fuses			Y
SCF-234	Eliminate need for srec for non-emulation builds	Y	Y	Y

3.2 Improvement

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-187	Code clean-up to eliminate duplicate code between devices	Y	Y	Y
SCF-218	Support setting the rate of bypass clock in DC SS on QM B0		Y	
SCF-219	Disallow transition from OFF to STBY power modes	Y	Y	Y
SCF-220	Disable DB clock gating when R/W from debug monitor	Y	Y	Y
SCF-226	Reduce SCFW stack usage	Y	Y	Y
SCF-228	Call to board code for DDR actions and align actions to system PM	Y	Y	Y

3.3 Bug

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-173	CM4 reset on boot when accessing RGPIO	Y	Y	Y

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-209	Sync LPM state and partition reboot	Y	Y	Y
SCF-217	For emulation builds, startup uses some uninitialized data	Y	Y	Y
SCF-224	Remove i.MX8QM A0 build option	Y		
SCF-238	i.MX8QM validation board with DDR4 has incorrect PCIe clock configuration	Y	Y	

3.4 Documentation

Key	Summary	QM (A0)	QM (B0)	QXP (B0)
SCF-75	Add documentation for porting the client API	Y	Y	Y
SCF-89	Add documentation of definition of power modes	Y	Y	Y

Chapter 4

Additional Notes

This section details any additional notes about this release.

4.1 General

When the SCFW is compiled for release into production devices, it is critical that this is done without debug (default is debug enabled, D=1) and without the debug monitor (default is no monitor, M=0). For example:

```
make qm R=B0 D=0 M=0
```

Turning off debug will eliminate the linking of the standard C library. See the porting guide for more information.

4.2 SCFW API Changes

Power Management (PM) Service

- Unified sc_pm_reset_cause_t and sc_pm_reset_reason_t

Miscellaneous (MISC) Service

Changes are associated with new SECO FW integration.

- Added sc_misc_seco_attest_mode()
- Added sc_misc_seco_attest()
- Added sc_misc_seco_get_attest_pkey()
- Added sc_misc_seco_get_attest_sign()
- Added sc_misc_seco_attest_verify()
- Added sc_misc_seco_commit()
- Changed sc_misc_seco_forward_lifecycle() parameters and docs to make usage more clear
- Added new SECO authentication commands for SECO FW

In addition:

- Added sc_misc_rompatch_checksum()

4.3 Resource Changes

- Added SC_R_ELCDIF_PLL - for i.MX8QXP
- Added SC_R_DMA5_CHx - for future device(s)
- Added SC_R_ATTESTATION - virtual resource; only owner can call misc_seco_attest∗() functions

4.4 Clock Changes

- Added eLCDIF PLL
- Added MLB PLL
- Changed i.MX8QM DB from 744MHz to 750MHz
- Remove default HDMI TX user PLL 2 frequency

4.5 Control Changes

- Added SC_C_SYNC_CTRL - provides control for setting both DC sync controls in one call

4.6 Board Interface Changes

- Added new board_parm_t values for KS1 retention and wake
- Changed board_parm_rtn_t to a uint32_t; moved returns to defines; added new return values
- Added new board_init() phase (3) used only for SCFW unit test board configuration

Chapter 5

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