Integrated Synthesizer/Mixer/Modulator Family Register Map Description

RFMD's second-generation integrated synthesizer/mixer products.

RFMD Multi-Market Products Group

REVISION HISTORY

Version	Date	Description of change(s)	Author(s)
1.5	12-Jul-12	Section 4.2 Default register settings updated. Details of chip revision mrev_id added. IQ modulator references added.	Eric Schonthal
1.4	01-Mar-12	Update to Register Map on Page 10 and to Register Content Description on Pages 11 to 19. Addition of section 4.2.	Eric Schonthal
1.3	06-June-11	Correction to Register Content Description on Page 17	Eric Schonthal
1.2	05-May-11	Addition of new sections and drawings	Eric Schonthal
1.1	07-Dec-10	Correction to p2presc Path2 VCO PLL feedback path divider setting on Page 15	Barbara Cox
1.0	25-Oct-10	First publication	Robert Pipkin
0.4	22-Oct-10	Publication prep	Robert Pipkin
0.3	29-Sep-10	Slight changes before submitting to MarCom	Chris Shepherd
0.2	06-Aug-10	Correct the number of address bits given in section 2 (should be seven, not six) and update timing diagram.	Chris Shepherd
0.1	01-Jul-10	Second draft.	Chris Shepherd
0.0	24-Jun-10	Initial Draft for second version of chips	Chris Shepherd

CONTENTS

1. INTRODUCTION

This guide contains instructions on how to program RFMD's second-generation integrated synthesizer/mixer/modulator devices. It includes a description of the proprietary serial interface as well as detailed information on the register map.

For more information, see "References" or visit http://www.rfmd.com.

2. TIMING

2.1 WRITE OPERATION

To perform a write operation the ENX line should be pulled low. The SCLK line is then used to clock the data into the chip. The first bit is undefined; this is followed by the R/W bit set low, then the seven address bits and the 16 data bits. The address and data bits are read on the rising edge of the clock signal. When the register write is complete the ENX line should be pulled high.

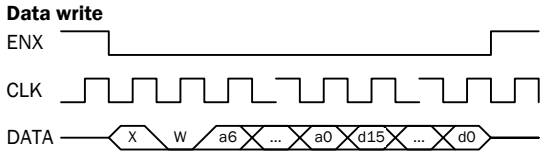

Figure 1. Timing Diagram for Write Operation

2.2 READ OPERATIONS

2.2.1 Three-Wire Bus Read Operation

To perform a read operation the ENX line should be pulled low. The SCLK line is then used to clock the data into the chip. The first bit is undefined; this is followed by the R/W bit set high, then the seven address bits. The address bits are read on the rising edge of the clock signal. After 1.5 clock cycles delay the 16 data bits are clocked out of the chip on the falling edge of the clock. When the register read is complete the ENX line should be pulled high.

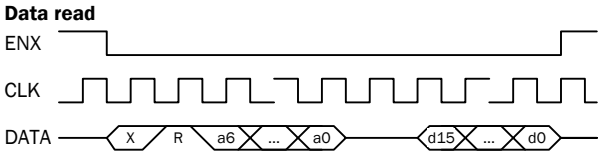

Figure 2. Timing Diagram for Three-Wire Bus Read Operation

2.2.2 Four-Wire Bus Read Operation

If the 4wire bit in the SDI_CTRL register has been set the data output stream is diverted to GPO4[1]. To perform a read operation the ENX line should be pulled low. The SCLK line is then used to clock the data into the chip. The first bit is undefined; this is followed by the R/W bit set high, then the seven address bits. The address bits are read on the rising edge of the clock signal. After 1.5 clock cycles delay the 16 data bits are clocked out of the chip on the falling edge of the clock and are available on the DOUT line. When the register read is complete the ENX line should be pulled high.

Note: [1] If GPO4 is also configured as a LOCK output the data output signal is only available from this pin when the ENBL line is low.

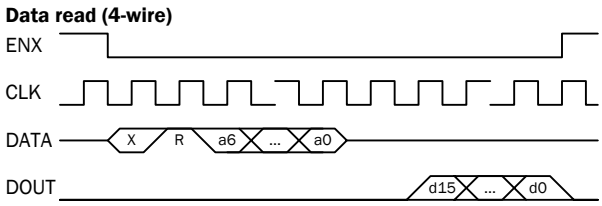

Figure 3. Timing Diagram for Four-Wire Bus Read Operation

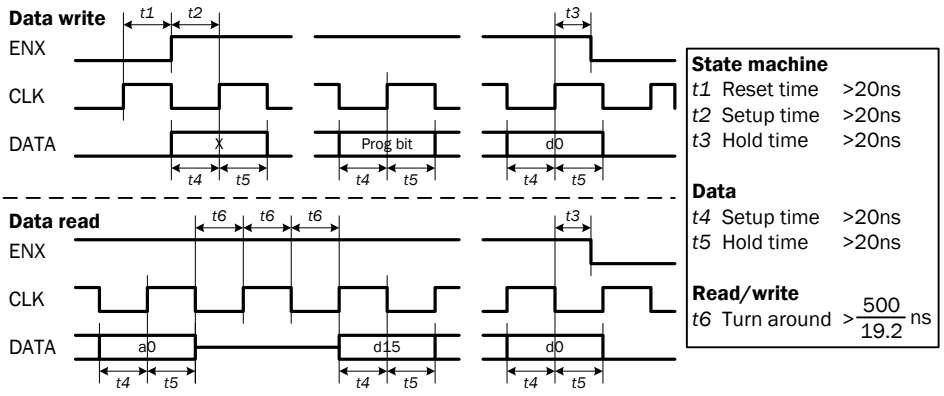

Figure 4. Critical Timing Diagram

3. DEVICE SETUP

3.1 STANDBY STATES

It is possible to configure the device so that the frequency synthesizer and VCO remain operating when the device is disabled. The ***pllst*** bit in the ***PLL_CTRL*** register should be set.

3.2 FREQUENCY MODULATION

The modulation frequency is F_{ref} * ***modulation*** / $2^{(24 - modstep)}$
where ***modulation*** is in 2's complement format and is found in the ***FMOD*** register and ***modstep*** is found in the ***EXT_MOD*** register. The maximum allowable value for ***modstep*** is 8.

3.2.1 Continuous Modulation

If the ***modsetup*** bits in the ***EXT_MOD*** register are set to 01 it is possible to change the frequency of the VCO by writing to the ***modulation*** bits in the ***FMOD*** register. By continuously writing these bits it is possible to continuously vary the deviation frequency of the VCO thus implementing a simple form of analogue modulation.

3.2.2 Binary FSK

If the ***modsetup*** bits in the ***EXT_MOD*** register are set to 11 the frequency of the VCO can be switched in a binary fashion either side of the carrier by the frequency programmed into the ***modulation*** bits of the ***FMOD*** register.

3.3 GENERAL PURPOSE OUTPUTS

Up to six General Purpose Outputs are available on the device, depending on configuration. The output state is configured using the ***GPO*** register. The output is dependent on the state of the **MODE** and **ENBL** signals. The ***p1gpo*** bits determine the output when **MODE** is low and ***p2gpo*** when **MODE** is high. The device can be configured so that the output remains active when the device is enabled only or always according to the state of the ***gate*** bit; if the ***gate*** bit is not set the outputs will go high impedance when the device is disabled.

All of the GPOs have multiple functions depending on the configuration of the device, this is discussed further below.

3.3.1 Serial Bus Control

Setting the ***sipin*** bit in the ***SDI_CTRL*** register to one allows the device to be controlled by the ***enbl***, ***mode*** and ***reset*** bits in the ***SDI_CTRL*** register. When the ***sipin*** bit is set the **MODE** and **ENBL** pins become available as **GPO5** and **GPO6**.

3.3.2 MultiSlice Operation

It is possible to control up to four chips from a single three-wire bus. If the ***addr*** bit in the ***SDI_CTRL*** register is set **GPO1** and **GPO2** are configured as inputs and their state is read by the chip and used to determine the value of address bits A5 and A6. From the point at which the ***addr*** bit is set, until the chip is reset or the bit cleared, the chip must be written or read using its extended six bit address.

3.3.3 Frequency Modulation Input

If the ***modsetup*** bits in the ***EXT_MOD*** register are set to 11 then **GPO3** is configured as an input and controls the modulation of the carrier. When high the frequency set in the ***FMOD*** and ***EXT_MOD*** registers is added to the synthesizer frequency, if it is low the frequency is subtracted.

3.3.4 Lock Detect Output

If the ***lock*** bit in the ***GPO*** register is set the lock flag is sent to **GPO4** where it is available to control an LED or similar. If the ***lock*** bit and the ***4wire*** bit are both set the lock signal is sent to **GPO4** when the device is enabled and the data when the device is disabled.

3.3.5 Four-Wire Bus Operation

If the ***4wire*** bit in the ***SDI_CTRL*** register is set the device is configured as a four-wire bus with the data output from as read operation being diverted to **GPO4** instead of the **SDATA** pin. If the ***lock*** bit and the ***4wire*** bit are both set the lock signal is sent to **GPO4** when the device is enabled and the data when the device is disabled.

4. REGISTER MAP

#	Reg name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	LF	lfact	p2cpdef							p1cpdef					pllcpl		
01	XO	xoch	xoc				xocf	suwait									
02	CAL_TIME	wait	tct					n/a		tkv1				tkv2			
03	VCO_CTRL	xtvco	ctavg		ctpol	clkpl	kvavg		kvrng	kvpol	xoi1	xoi2	xoi3	refst	icpup		n/a
04	CT_CAL1	p1ctgain			p1ctv					p1ct	p1ctdef						
05	CT_CAL2	p2ctgain			p2ctv					p2ct	p2ctdef						
06	PLL_CAL1	p1kv	p1dn									p1kvgain			p1sgn	n/a	
07	PLL_CAL2	p2kv	p2dn									p2kvgain			p2sgn	n/a	
08	VCO_AUTO	auto	ctmax							ctmin							n/a
09	PLL_CTRL	divby	clkdiv			pllst	tvco					lden	ldlev	relok	aloi	plldy	
0A	PLL_BIAS	n/a	p1loi				p1vcoi			n/a	p2loi				p2vcoi		
0B	MIX_CONT	fulld	p1mixidd			p2mixidd				n/a							
0C	P1_FREQ1	p1n									p1lodiv			p1presc		p1vcosel	
0D	P1_FREQ2	p1nmsb															
0E	P1_FREQ3	p1nlsb								n/a							
0F	P2_FREQ1	p2n									p2lodiv			p2presc		p2vcosel	
10	P2_FREQ2	p2nmsb															
11	P2_FREQ3	p2nlsb								n/a							
12	FN_CTRL	fnz	dithr	sdm		phaln	phsalngain			phsalndly		mode	dith	fm	dmode	tzps	n/a
13	EXT_MOD	modsetup	modstep					n/a									
14	FMOD	modulation															
15	SDI_CTRL	sipin	enbl	mode	4wire	addr	n/a									reset	n/a
16	GPO	p2gpio							p1gpio							gate	lock
17	T_VCO	curve_def_vco1			curve_def_vco2			curve_def_vco3			n/a						
18	IQMOD1	ctrl	bbgm	txlo	mod	modiv	modbias			lobias		calon	calnul	calblk	divbias	bufdc	
19	IQMOD2	bbatten				rctune						calatten		mod		modbuf	
1A	IQMOD3	bufdaci						bufdacq						dacen	n/a		
1B	IQMOD4	moddaci						moddacq						bufbias1		bufbias2	
1C	T_CTRL	tc_en		tbl_sel		fc_en	filt_ctrl		ref_sel	ext_filt	ldo_by	v_test	n/a				
1D	DEV_CTRL	readsel				rsmst	rsmstopst					cpu	cpd	dac	ctclk	bypas	n/a
1E	TEST	ten	tmux			tsel		lfsr	lfsrp	lfsrgatetime				lfsrt	rgbyp	rcbyp	n/a
1F	READBACK	readback (depends on setting of DEV_CTRL:readsel)															
readsel=0000		dev_id													rev_id		
readsel=0001		lock	ct_cal							cp_cal						ctfail	0
readsel=0010		v0_cal								v1_cal							
readsel=0011		rsm_state					f_errflag		0								
readsel=0100		vco_count_l															
readsel=0101		vco_count_h															
readsel=0110		calfbi	calfbq	0x0000													
readsel=0111		vco_sel		vco_tc_curve			0x000										
readsel=other		0x0000															

Not all registers are active in every device in this series of parts.

4.1 REGISTER CONTENT DESCRIPTION

4.1.1 LF - Loop Filter Configuration (00h)

Field Name	Bit Field	Function
lfact	15	active loop filter enable, 1=active 0=passive
p2cpdef	14:9	Charge pump setting. If p2_kv_en=1 this value sets charge pump current during KV compensation measurement. If p2_kv_en=0, this value is used at all times. Default value is 93µA.
p1cpdef	8:3	Charge pump setting. if p1_kv_en=1 this value sets charge pump current during KV compensation measurement. If p1_kv_en=0, this value is used at all times. Default value is 93µA.
pllcpl	2:0	charge pump leakage settings

4.1.2 XO - Crystal Oscillator Configuration (01h)

Field Name	Bit Field	Function
xoch	15	XO additional fixed capacitance
xoc	14:11	XO coarse tune
xocf	10	XO additional fixed capacitance
suwait	9:0	XO settling timer: 1LSB=128 reference clocks or 2.46µs at 52MHz

4.1.3 CAL_TIME - Calibration Timing (02h)

Field Name	Bit Field	Function
wait	15	If high then the RF sections are not enabled until the PLL calibrations complete
tct	14:10	Duration of CT acquisition
n/a	9:8	
tkv1	7:4	Timer for first KV settling
tkv2	3:0	Timer for second KV settling

4.1.4 VCO_CTRL - Calibration Control (03h)

Field Name	Bit Field	Function
xtvco	15	Enable external VCO
ctavg	14:13	Number of samples averaged to compute final value during CT Calibration: 0 = average 16 samples; 1 = average 32 samples; 2 = average 64 samples; 3 = average 128 samples
ctpol	12	polarity of VCO coarse-tune word 0 = increasing ct_val increases vco freq 1 = increasing ct_val decreases vco freq
clkpl	11	coarse tuning clock polarity 0 = in phase with reference; 1 = antiphase with reference
kvavg	10:9	Number of samples averaged to compute final value during KV compensation: 0 = average 16 samples; 1 = average 32 samples; 2 = average 64 samples; 3 = average 128 samples
kvrng	8	KV Range - Sets accuracy of Voltage measurement during KV cal
kvpol	7	VCO KV polarity: 0 = positive, VCO freq increases with increasing tuning voltage 1 = negative, VCO freq decreases with increasing tuning voltage
xoi1	6	XO current setting 1
xoi2	5	XO current setting 2
xoi3	4	XO current setting 3
refst	3	Reference oscillator standby mode
icpup	2:1	Override default charge pump-up settings
n/a	0	

4.1.5 CT_CAL1 - Path 1 Coarse Tuning Calibration (04h)

Field Name	Bit Field	Function
p1ctgain	15:13	Path 1 calibration loop gain. Each step changes gain by a factor of 2.
p1ctv	12:8	Path 1 VCO tuning target voltage
p1ct	7	VCO coarse tune enable, path 1 mode
p1ctdef	6:0	VCO coarse tuning default value, path 1 mode

4.1.6 CT_CAL2 - Path 2 Coarse Tuning Calibration (05h)

Field Name	Bit Field	Function
p2ctgain	15:13	Path 2 calibration loop gain. Each step changes gain by a factor of 2.
p2ctv	12:8	Path 2 VCO tuning target voltage
p2ct	7	VCO coarse tune enable, path2 mode
p2ctdef	6:0	VCO coarse tuning default value, path 2 mode

4.1.7 PLL_CAL1 - Path 1 PLL Calibration (06h)

Field Name	Bit Field	Function
p1kv	15	VCO tuning gain calibration enable, path 1 mode
p1dn	14:6	Change in N-divider value to give frequency step during KV compensation measurement in path 1 mode.
p1kvgain	5:3	Controls loop gain during KV compensation
p1sgn	2	Controls whether or not p1dn is added/subtracted in Path 1 mode. If 0 then subtract, otherwise add.
n/a	1:0	

4.1.8 PLL_CAL2 - Path 2 PLL Calibration (07h)

Field Name	Bit Field	Function
p2kv	15	VCO tuning gain calibration enable, path 2 mode
p2dn	14:6	Change in N-divider value to give frequency step during KV compensation measurement in path 2 mode
p2kvgain	5:3	Controls loop gain during KV compensation.
p2sgn	2	Controls whether or not p2dn is added/subtracted in Path 2 mode. If 0 then subtract, otherwise add
n/a	1:0	

4.1.9 VCO_AUTO - Auto VCO select control (08h)

Field Name	Bit Field	Function
auto	15	If high then the PLL state machine attempts to find the the correct VCO needed to lock to the desired frequency
ctmax	14:8	Maximum CT value for coarse tuning allowed. Used as the jump over threshold in auto VCO select mode
ctmin	7:1	Minimum CT value for coarse tuning allowed. Used as the jump over threshold in auto VCO select mode
n/a	0	

4.1.10 PLL_CTRL - PLL Control (09h)

Field Name	Bit Field	Function
divby	15	Force reference divider to divide by 1
clkdiv	14:12	Reference divider divide value
pllst	11	PLL standby mode (if high the PLL is always on)
tvco	10:6	VCO warm-up time. warm-up time [s] = tvco * 1/[fref*256]
lden	5	Enable lock detector circuitry
ldlev	4	Modify lock range for lock detector
relok	3	Self Clearing Bit. When this bit is set high it triggers a relock of the PLL and then clears
aloi	2	If low, the LO path current is automatically determined according to frequency. If high, the LO current is set according to the value of p2loi or P1loi in PLL_BIAS depending on mode
plldy	1:0	PLL reset delay

4.1.11 PLL_BIAS - PLL Bias Settings (0Ah)

Field Name	Bit Field	Function
n/a	15	
p1loi	14:11	LO path current setting, path 1 mode
p1vcoi	10:8	Path 1 VCO bias setting : 000=Min Current, 111=Max Current
n/a	7	
p2loi	6:3	LO path current setting, path 2 mode
p2vcoi	2:0	Path 2 VCO bias setting : 000=Min Current, 111=Max Current

4.1.12 MIX_CONT - Mixer Control (0Bh) [RFFC parts only]

Field Name	Bit Field	Function
fulld	15	Full duplex mode (dual mixer version only): 0 = half duplex, either path1 or path2 is enabled according to mode pin. 1 = full duplex, Path 1 and Path 2 are enabled.
p1mixidd	14:12	Path 1 mixer current: 000=min current, 111=max current
p2mixidd	11:9	Path 2 mixer current: 000=min current, 111=max current
n/a	8:0	

4.1.13 P1_FREQ1 - Path 1 Frequency 1 (0Ch)

Field Name	Bit Field	Function
p1n	15:7	Path 1 N-divider integer value
p1lodiv	6:4	Path 1 LO path divider setting: divide by 2^n (i.e. divide by 1 to divide by 32). 110 and 111 are reserved
p1presc	3:2	Path 1 VCO PLL feedback path divider setting: 01 = divide by 2, 10 = divide by 4 (00 and 11 are reserved)
p1vcosel	1:0	Path 1 VCO band select: 00 = vco1, 01 = vco2, 10 = vco3 (11 is reserved)

4.1.14 P1_FREQ2 - Path 1 Frequency 2 (0Dh)

Field Name	Bit Field	Function
p1nmsb	15:0	Path 1 N-divider numerator value, most significant 16 bits

4.1.15 P1_FREQ3 - Path 1 Frequency 3 (0Eh)

Field Name	Bit Field	Function
p1nlsb	15:8	Path 1 N divider numerator value, least significant 8 bits
n/a	7:0	

4.1.16 P2_FREQ1 - Path 2 Frequency 1 (0Fh)

Field Name	Bit Field	Function
p2n	15:7	Path 2 VCO divider integer value.
p2lodiv	6:4	Path2 LO path divider setting: divide by 2^n (i.e. divide by 1 to divide by 32). 110 and 111 are reserved
p2presc	3:2	Path 2 VCO PLL feedback path divider setting: 01 = divide by 2, 10 = divide by 4 (00 and 11 are reserved)
p2vcosel	1:0	Path 2 VCO band select: 00 = vco1, 01 = vco2, 10 = vco3 (11 is reserved)

4.1.17 P2_FREQ2 - Path 2 Frequency 2 (10h)

Field Name	Bit Field	Function
p2nmsb	15:0	Path 2 N divider numerator value, most significant 16 bits

4.1.18 P2_FREQ3 - Path 2 Frequency 3 (11h)

Field Name	Bit Field	Function
p2nlsb	15:8	Path 2 N divider numerator value, least significant 8 bits
n/a	7:0	

4.1.19 FN_CTRL - Frac-N Control (12h)

Field Name	Bit Field	Function
fnz	15	If programmed high the modulator to the fractional dividers is disabled. Test mode.
dithr	14	If high then the target frequency (reference of freq_det) is dither by the sigma delta
sdm	13:12	PLL sigma-delta modulator order: 00=first order accumulator, 01=2nd order MASH 1-1, 10=3rd order MASH 1-1-1 and 11=DSM modulator as defined by mode, dith, fm and dmode fields
phaln	11	Enable zero phase start
phsalngain	10:8	Gain Setting for zero phase start (N counts/LSB): 000=1/32, 001=1/16, 010=1/8, 011=1/4, 100=1/2, 101=1, 110=2 and 111: 4
phsalndly	7:6	Controls amount of synchronization(delay) of the BangBang PFD: 00=no synchronization, 01=1 cycle of delay, 10=2 cycles of delay and 11=bang bang PFD is off (no correction)
mode	5	DSM Modulator: 0=3rd order, and 1=5th order
dith	4	DSM modulator dither 1=dither enabled
fm	3	DSM modulator FM modulation (dithering option)
dmode	2	DSM modulator dithering mode 0 = stronger dithering, 1=distributed modulation
tzps	1	Loop filter pre-charge for zero-phase start (experimental)
n/a	0	

4.1.20 EXT_MOD - Frequency modulation control 1 (13h)

Field Name	Bit Field	Function
modsetup	15:14	Control how modulation is applied to frac-N: 00/10=modulation off, 01=modulation is analog, on every update of modulation the frac-N responds by adding value to frac-N and 11=modulation is binary when modpin is high modulation is added to frac-N
modstep	13:10	Modulation scale factor. Modulation is multiplied by 2^modstep before being added to frac-N. Maximum usable value is 8
n/a	9:0	

4.1.21 FMOD - Frequency modulation control 2 (14h)

Field Name	Bit Field	Function
modulation	15:0	Frequency Deviation applied to frac-N, functionallity determined by modstep and mod_setup

4.1.22 SDI_CTRL - SDI Control (15h)

Field Name	Bit Field	Function
sipin	15	1=ENBL and MODE pins are ignored and become available as GPO5 and GPO6
enbl	14	If sipin=1 this field will replace the functionality of the ENBL pin
mode	13	If sipin_ctrl=1 this field will replace the functionality of the MODE pin
4wire	12	1=4-wire SDI, i.e. SDATA is unidirectional and SDATA_out is routed to GPO4
addr	11	1=GPIO1,GPIO2 are inputs that map the register map to the address {GPO2,GPO1,SDI address}; this gives 4 possible addresses for the registers.
n/a	10:2	
reset	1	When this bit is taken high the part is reset
n/a	0	

4.1.23 GPO - General Purpose Outputs (16h)

Field Name	Bit Field	Function
p2gpo	15:9	GPOs for Path 2, 1=high, 0 = low. The mode pin or SDI field controls whether the value in p2gpo or p1gpo is used.
p1gpo	8:2	GPOs for Path 1, 1=high, 0 = low. The mode pin or SDI field controls whether the value in p2gpo or p1gpo is used.
gate	1	If low GPO's are ANDed with enable (forced to zero when the enable is low, if high the GPO's are available when enable is low
lock	0	Sends LOCK flag to GPO4

4.1.24 T_VCO - Temperature Compensation VCO Curves (17h)

Field Name	Bit Field	Function
curve_vco1	15:13	VCO1 temperature compensation curve
curve_vco2	12:10	VCO1 temperature compensation curve
curve_vco3	9:7	VCO3 temperature compensation curve
n/a	6:0	

4.1.25 IQMOD1 – Modulator Calibration (18h) [RFMD208x only]

Field Name	Bit Field	Function
ctrl	15:11	Individual circuit block power control
modbias	10:8	Modulator internal node DC bias
lobias	7:6	LO buffer bias current
calon	5	Calibration enable
calnul	4	
calblk	3	Isolates buffer and core during calibration
divbias	2	Reduces LO path gain, may be required at low LO frequencies
bufdc	1:0	Bias restoration in LO buffer

4.1.26 IQMOD2 – Modulator Control (19h) [RFMD208x only]

Field Name	Bit Field	Function
bbatten	15:12	Baseband attenuation [RFMD2080 only]
rctune	11:6	Input low pass filter bandwidth [RFMD2080 only]
calatten	5:4	Modulator attenuation during calibration
mod	3:2	Modulator attenuation
modbuf	1:0	Modulator buffer enable (usually the same as *mod*)

4.1.27 IQMOD3 - Modulator Buffer Control (1Ah) [RFMD2080 only]

Field Name	Bit Field	Function
bufdaci	15:10	I-channel buffer DC offset control
bufdacq	9:4	Q-channel buffer DC offset control
dacen	8	Enable DC offset control DACs

4.1.28 IQMOD4– Modulator Core Control (1Bh) [RFMD2080 only]

Field Name	Bit Field	Function
moddaci	15:10	I-channel mixer core DC offset control
moddacq	11:6	I-channel mixer core DC offset control
bufbias1	5:4	Buffer bias 1
bufbias2	3:2	Buffer bias 2

4.1.29 TEMPC_CTRL – Temperature compensation control (1Ch)

Field Name	Bit Field	Function
tc_en	15:14	Temp comp enable and mode 2'b00: disable temp comp 2'b01: enable closed loop temp comp 2'b10: enable open loop temp comp - manual mode 2'b11: enable open loop temp comp - automatic mode
tbl_sel	13:12	Temp comp table selection 2'b00: table 0 2'b01: table 1 2'b10: table 2 2'b11: table 3
fc_en	11	Temp comp fast charge (0=enabled, 1=disabled)
filtr_ctrl	10:9	Temp comp filter control 2'b0x: filter state automatically controlled 2'b10: filter always connected 2'b11: filter always bypassed
ref_sel	8	Reference selection for closed loop mode (0=fixed, 1=variable)
ext_filt	7	External filter cap option (0=no external cap, 1=external cap connected)
ldo_by	6	Temp comp voltage regulator control (0=regulator engaged, 1=regulator bypassed)
v_test	5	Temp comp test mode (0=disabled 1=enabled)

4.1.30 DEV_CTRL - Readback register and RSM Control (1Dh)

Field Name	Bit Field	Function
readsel	15:12	Controls what is readback through the READBACK register: 0000 > dev_id,mrev_id 0001 > lock,ct_cal,cp_cal,ct_failed 0010 > v0_cal,v1_cal 0011 > rsm_state,freqerrflag 0100 > vco_count_l[15:0] 0101 > vco_count_h[31:16] 0110 > cal_fbi,cal_fbq 0111 > vco_sel, tc_curve other > 0
rsmst	11	When this bit is high the PLL state machine stops in the state rsmstopstate
rsmstopst	10:6	This field defines the state we stop the state machine in when rsmst=1
cpu	5	Charge pump to pump up: 0=normal operation, 1=pump up
cpd	4	Charge pump to pump down: 0=normal operation, 1=pump down
dac	3	DAC test
ctclk	2	1=ct_clk is forced to always on, 0=clock turns on/off with state machine
bypas	1	If high, offsets mixer so that LO signal can be viewed at mixer output
n/a	0	

4.1.31 TEST - Test register (1Eh)

Field Name	Bit Field	Function
ten	15	Enables test mode
tmux	14:12	Test mux
tsel	11:10	
lfsr	9	Test mode, when high LFSR sclk is forced to always on and lfsr is enabled, when low it turns on/off with state machine
lfsrp	8	When high the phase (polarity) of lfsr_sclk is inverted relative to fr_clk
lfsrgatet	7:4	This sets the duration of the LFSR test timer (for production test), the number of fr_clk cycles=2^(10+lfsr_test_gate_time) (2^10 to 2^26 cycles). Intended for production test it could be used as a very accurate, but slow, lock detect
lfsrt	3	Self Clearing Bit. When this bit is set high LFSR BIST/Frequency Counter runs, and is self cleared when complete
rgbyp	2	Internal regulator bypass 1=bypassed
rcbyp	1	VCO Bias RC filter bypass 1=bypassed
lfsrd	0	LFSR detect mode

4.1.32 READBACK – Readback Register (1Fh)

Field Name	Bit Field	Function
		DEV_CTRL:readsel=0000
dev_id	15:3	Device identification
mrev_id	2:0	Chip revision
		DEV_CTRL: readsel=0001
lock	15	Synthesizer lock bit, can be routed to GPO4
ct_cal	14:8	Course tune calibration value
cp_cal	7:2	KV calibration charge pump current value
ctfail	1	Coarse tune calibration flag (1=CT cal failed)
		DEV_CTRL: readsel=0010
v0_cal	15:8	Min tuning voltage during cal
v1_cal	7:0	Max tuning voltage during cal
		DEV_CTRL: readsel=0011
rsm_state	15:11	State machine operating state
f_errflag	10:9	Flag indicating incorrect frequency
		DEV_CTRL: readsel=0100
vco_count_l	15:0	
		DEV_CTRL: readsel=0101
vco_count_h	15:0	
		DEV_CTRL: readsel=0110 [RFMD208x only]
cal_fbi	15	I-channel DC offset calibration complete flag
cal_fbq	14	Q-channel DC offset calibration complete flag
		DEV_CTRL:readsel=0111
vco_sel	15:14	Selected VCO
vco_tc_curve	13:11	Selected temperature compensation curve

4.2 DEFAULT REGISTER SETTINGS

#	Reg name	Revision 1	Revision 2
00	LF	0xBEFA	0xBEFA
01	XO	0x4064	0x4064
02	CAL_TIME	0x9055	0x9055
03	VCO_CTRL	0x2D02	0x2D02
04	CT_CAL1	0xB0BF	0xACBF
05	CT_CAL2	0xB0BF	0xACBF
06	PLL_CAL1	0x0028	0x0028
07	PLL_CAL2	0x0028	0x0028
08	VCO_AUTO	0xFC06	0xFF00
09	PLL_CTRL	0x8220	0x8220
0A	PLL_BIAS	0x0202	0x0202
0B	MIX_CONT	0x4800	0x4800
0C	P1_FREQ1	0x2324	0x1A94
0D	P1_FREQ2	0x6276	0xD89D
0E	P1_FREQ3	0x2700	0x8900
0F	P2_FREQ1	0x2F16	0x1E84
10	P2_FREQ2	0x3B13	0x89D8
11	P2_FREQ3	0xB100	0x9D00
12	FN_CTRL	0x2A80	0x2A80
13	EXT_MOD	0x0000	0x0000
14	FMOD	0x0000	0x0000
15	SDI_CTRL	0x0000	0x0000
16	GPO	0x0000	0x0000
17	T_VCO	n/a	0x4900
18	IQMOD1	0x0283	0x0281
19	IQMOD2	0xF00F	0xF00F
1A	IQMOD3	0x0000	0x0000
1B	IQMOD4	0x000F	0x0005
1C	T_CTRL	n/a	0xC840
1D	DEV_CTRL	0x1000	0x1000
1E	TEST	0x0001	0x0005

Revision 1 devices (mrev_id = 001): RFFC2071/2072/5071/5072, RFMD2080/2081
Revision 2 devices (mrev_id = 010): RFFC2071A/2072A/5071A/5072A

5. REFERENCES

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3. Integrated Synthesizer/Mixer Evaluation Board and GUI User Guide
4. Integrated Synthesizer/Mixer Programming Guide
5. Integrated Synthesizer and Modulator web site (http://www.rfmd.com/products/IntSynthModulator/)
6. IQ Modulator Programming Guide (RFMD2080/2081)