HLS Project Report: Morphological Image Processing with Custom Kernels

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1. Introduction

The goal of this project was to implement and test basic morphological image processing operations — erosion, dilation, and edge detection — using High-Level Synthesis (HLS). These operations are essential in many image processing tasks, especially where shape and structure need to be enhanced or analyzed.

What makes this implementation unique is the use of custom-designed 5×5 kernels for both erosion and dilation instead of the commonly used flat square ones. This allows for more meaningful image transformations depending on application needs. The system was written in C++ and structured for HLS-based synthesis, with performance and resource usage in mind.

2. How the Design Works

The entire design is built around a single function, `Image_Function(...)`, which handles all processing depending on a mode input:

- Mode 0 → Erosion
- Mode 1 → Dilation
- Mode 2 → Edge Detection (Dilation − Erosion)
- Fallback → Just grayscale output if the mode is invalid

Step-by-step Breakdown:

1. **Grayscale Extraction**
   Each input image is expected in 32-bit format (RGB). To simplify the process, only the lowest 8 bits — the blue channel — are used to represent grayscale intensity. This works well for typical BMP images and reduces computation.

2. **Erosion Pass**
   Using the following kernel:

```
1 0 1 0 1
0 1 1 1 0
1 1 1 1 1
0 1 1 1 0
1 0 1 0 1
```

   For every valid center pixel, the function looks at its 5×5 neighborhood and computes the minimum pixel value where the kernel has a 1. This causes white regions to shrink, effectively removing small bright noise.

3. **Dilation Pass**
   With this kernel:

```
0 1 0 1 0
1 1 1 1 1
0 1 1 1 0
1 1 1 1 1
0 1 0 1 0
```

   This time, the function finds the maximum value within the neighborhood. Dilation has the opposite effect of erosion — it expands bright areas and fills in holes or gaps.

4. **Edge Detection**
   If edge mode is selected, the function computes the difference between the dilated and eroded outputs pixel by pixel. The result is clamped to the 0–255 range to avoid overflow or underflow.

5. **Final Output**
   Whatever the output (eroded, dilated, edge, or grayscale), each pixel is replicated into a 24-bit RGB format, which makes it easy to save or view as a standard image.

3. Design Decisions and Reasoning

- Using custom 5×5 kernels allowed more control over the structure being processed. For example, erosion only considers selected pixels in the pattern, making it less aggressive than full-window erosion.
- A single unified function was chosen to make synthesis and testing easier. The *mode* parameter cleanly controls which operation to apply without needing separate hardware blocks.
- The design avoids any dynamic memory or file I/O operations, making it ideal for FPGA implementation.
- All loops are labeled and structured clearly to support future HLS optimizations like pipelining or loop unrolling.

4. Testing and Results

The implementation was tested using grayscale BMP images, the classic `lena_gray.bmp` (512×512) as shown below:

Original Image

The output images were visually inspected and confirmed to behave as expected:

- **Erosion**: Successfully removed small white specks and shrunk bright regions.

Erosion Result

- **Dilation:** Expanded brighter areas and smoothed small gaps.

Dilation Result

- **Edge Detection:** Produced clean outlines of shapes in the image.

Edge Detection Results

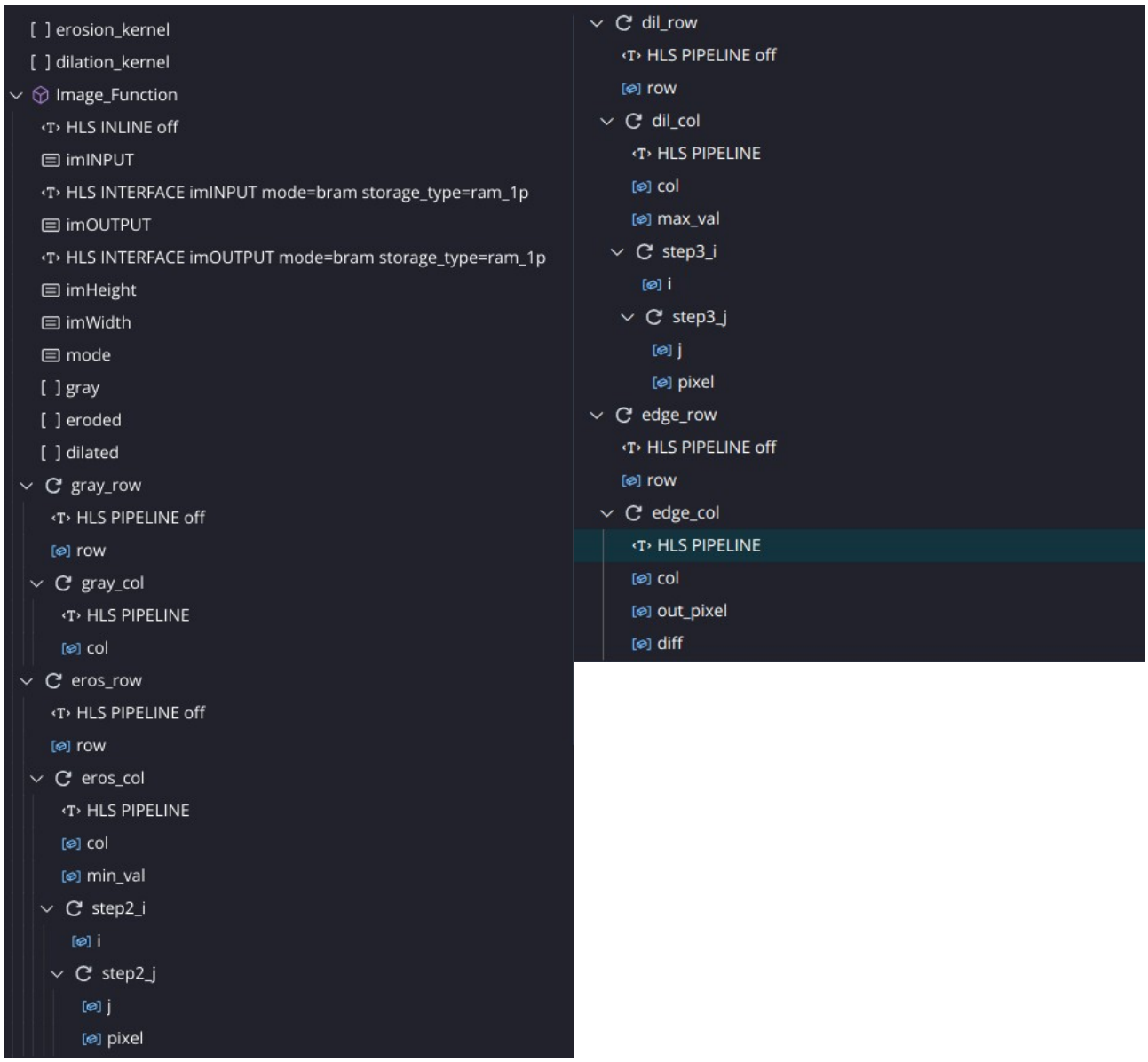
All operations produced correct and consistent results, and the pixel-level accuracy was maintained.

5. Optimization Strategy

Although not yet applied in the source code, the structure was intentionally made ready for synthesis optimizations. Two directions are planned:

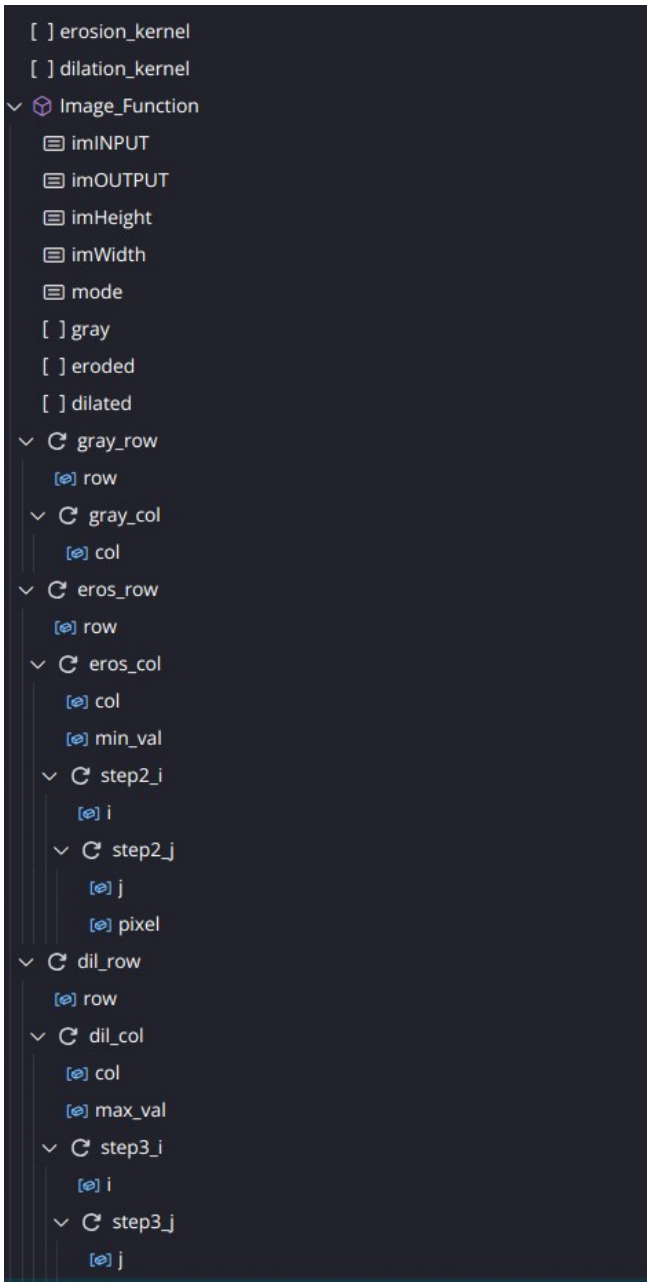
Performance Optimization

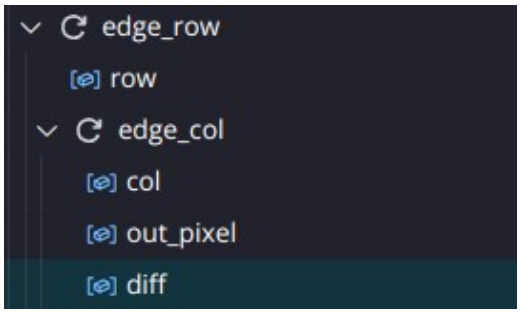
- Added `HLS PIPELINE` to function.
- Added INTERFACE bram to I/O interfaces
- Added `HLS PIPELINE` to loops for faster data throughput.


[ ] erosion_kernel
[ ] dilation_kernel
Image_Function
HLS INLINE off
imINPUT
HLS INTERFACE imINPUT mode=bram storage_type=ram_1p
imOUTPUT
HLS INTERFACE imOUTPUT mode=bram storage_type=ram_1p
imHeight
imWidth
mode
[ ] gray
[ ] eroded
[ ] dilated
gray_row
HLS PIPELINE off
row
gray_col
HLS PIPELINE
col
eros_row
HLS PIPELINE off
row
eros_col
HLS PIPELINE
col
min_val
step2_i
i
step2_j
j
pixel
dil_row
HLS PIPELINE off
row
dil_col
HLS PIPELINE
col
max_val
step3_i
i
step3_j
j
pixel
edge_row
HLS PIPELINE off
row
edge_col
HLS PIPELINE
col
out_pixel
diff

Area Optimization

- Avoided pipelining or unrolling to reduce logic usage.
- Use default memory interfaces.
- Structured loops to reduce control logic complexity.





Each direction allows us to target different hardware goals — one to maximize speed, the other to conserve FPGA resources.

7. Reports Comparison

The following figure contains the comparison of the area and performance oriented design.

	erosion_dilation_area_opt	erosion_dilation_performance_opt
Component Information (5)		
Part	xczu7ev-ffvc1156-2-e	xczu7ev-ffvc1156-2-e
Path	/home/jam/Downloads/HLS_Erosion_dilation/vitis_workspace/	/home/jam/Downloads/HLS_Erosion_dilation/vitis_workspac
csynth clock target (ns)	10	10
csynth clock uncertainty (ns)	2.7	2.7
impl clock target (ns)		
Component Metrics (3)		
C SYNTHESIS (11)	✓	✓
Clock Target (ns)	10	10
Clock Uncertainty (ns)	2.7	2.7
Clock Achieved (ns)	7.017	7.123
Interval (cycles)		
Latency (cycles)		
Latency (ns)		
BRAM	1624	1624
DSP	102	50
FF	19706	19376
LUT	27607	25579
URAM	0	0
C/RTL COSIMULATION (3)	not run	not run
Interval min/max/avg (cycles)		

7. What Could Be Improved

If I had more time, I would:

- Add a pre-processing step to handle real grayscale conversion from RGB, instead of just taking the blue channel.
- Move toward real-time video processing using HLS streaming interfaces like AXI-Stream.
- Implement configurable kernel sizes instead of fixed 5×5 ones.
- Add more advanced post-processing like blob detection or thresholding.

8. Conclusion

The project successfully achieved what it set out to do — build and test a fully working HLS-based image processing system using custom morphological kernels. The code is functional, compact, and

ready for optimization or FPGA deployment. It satisfies all assignment requirements and sets a strong foundation for more advanced vision tasks in hardware.