

1. Introduction

The central theme of this project, to be carried out using the Altera DE2-115 development kit, is the evaluation of how quickly (usually measured in milliseconds) a user reacts physically (by pressing a key) to visual stimuli. You can try tests of this type at <https://cps-check.com/en/reaction-test>, for example.

A typical elementary test cycle comprises the following steps:

1 - Start:

By pressing a button, the user sets a delay timer to activation with a random value (don) in milliseconds within a suitable range and starts it at that instant.

2 - Stimulus Activation:

After the delay don has elapsed, the visual stimulus is activated, starting the stopwatch that will measure the reaction time (treac) in milliseconds at that moment.

3 - Reaction to Stimulus:

The user must press a button (it can be the start button again) as soon as they observe the activation of the stimulus. At that moment, treac is recorded, the stopwatch is reset, and the stimulus is deactivated.

Note 1: It is essential that the delay don has a random duration to avoid predictability of the stimulus and consequent bias (even involuntary) of the results. However, a minimum limit must be imposed to ensure the readiness of the user in consecutive tests. Once these requirements are met, don should be brief to avoid biasing the results due to user fatigue and wasting time.

Suggestion: It is possible to meet these conditions based on a simple 'free-run' counting block: if the reading instant is determined manually, the read value will be random within the counting range, with a distribution as uniform as possible, the higher the clock frequency.

Note 2: In consecutive test cycles, step 3 of each cycle can constitute step 1 of the following cycle.

2. Specifications

It is intended to manage a competition consisting of a sequence of elementary test cycles (see structure described in the Introduction) applied simultaneously to two players. Both respond to the same stimulus in each cycle (lighting of

LEDG[7..0]), and one point is awarded to the player who achieves the shorter reaction time (regardless of the difference between times).

The winner will be the first to reach a given number of points, stipulated in an initial configuration stage, where the HEX3-HEX0 displays should show the indication 'ConF'. This number will be adjustable between 1 and 50 (10 by default) and displayed on the HEX7-HEX6 displays (which, at this stage, should blink at 1Hz). Adjustment should be efficient and comfortable for the user, using a single push button [Suggestion: combine unit increment with each brief touch with the ability to detect long touch (e.g., longer than 1s) and in that case apply rapid increment pulses (e.g., at 10Hz)]. The conclusion of this stage will be indicated by pressing another push button.

This will be followed by the competition stage, where HEX7-HEX6 should continue to display (now without blinking) the chosen target score. The HEX3-HEX0 displays should start by indicating 'tEst' and, from the first elementary test cycle, display the scores (of player A in HEX3-HEX2 and player B in HEX1-HEX0), with the number of the current test cycle presented in HEX5-HEX4.

In the test cycles, player A uses the KEY3 key and commands the deactivation of the left half of the stimulus, LEDG[7..4] while player B uses the KEY0 key and commands the deactivation of the right half of the stimulus, LEDG[3..0]. Note that, to accommodate this simultaneous competition format, the start of the cycles must be determined by the player who presses their key last.

In case of a tie in reaction times, no player scores (and the test cycle is not counted). Ensure that the system properly addresses this unlikely situation (use simulation to demonstrate).

If a player reacts prematurely to the stimulus, they will incur a penalty of 2 points, with disqualification if it results in a negative score (unless the opponent is in the same situation – in that case, the competition stage must be immediately restarted). The LEDR[7..4] or LEDR[3..0] groups should briefly light up (e.g., for 1s) to indicate premature reactions by player A or player B, respectively.

The competition ends when one of the players reaches the stipulated number of points, at which point the conclusion stage will consist of a victory celebration through a light effect lasting 5s on the LEDG[7..0] half corresponding to the winner. After this time, the system should return to the initial configuration stage.

3. Work Phases

A phased development approach is recommended, planning, building, and testing the various blocks/sets successively and gradually integrating the operating requirements, starting with the simplest ones. Below is a suggestion in this regard, with quotas presented as a guideline:

- 1 - [2] Single cycle with 1 user and display of reaction time (to verify functionality).
- 2 - [4] Single cycle with 2 players and indication of the result (victory of A, victory of B, or tie) ignoring premature reactions – MEF control should be applied (with careful design of the state diagram being crucial).
- 3 - [3] Competition with fixed score limit (e.g., 6), including the display of test cycle counts and points (ignoring penalties) and indication of the winner (A or B).
- 4 - [2] Adjustment of the target score (for the initial configuration stage).
- 5 - [2+1+1] General system control MEF (configuration, competition, and conclusion stages): integration of initial target score adjustment and victory celebration functionalities.
- 6 - [3] Refinement of phases 2 and 3 to detect premature reactions (phase 2) and apply the corresponding penalties (phase 3).
- 7 - [2] Addition of other relevant functionalities and/or options to improve the system.

4. General Recommendations

- A single clock signal (50MHz) should be applied to all sequential components.
- A general 'reset' input should be provided (protected against accidental activation) to return the system to the initial configuration stage.

General Requirements

All projects must, among other specific aspects:

They must have one or more finite state machines to control their operation, with the system's functioning corresponding to a sequence of states whose transitions depend on external or internal signals.

Follow a phased implementation strategy, according to the project specification. A single project (in Quartus Prime) must be created for which it is necessary:

Define a suitable architecture by elaborating a complete logic diagram with all constituent modules, ports, and connections.

Perform VHDL modeling of each of the blocks.

Simulate the behavior, based on VHDL-written testbenches, of the most relevant blocks and the global system.

Simulate the top level of the project.

Be based on VHDL models that use only the constructions covered in the LSD classes. Specifically, for-loops, while-loops, and the use of variables are not allowed.

Use a single clock signal throughout the entire system.