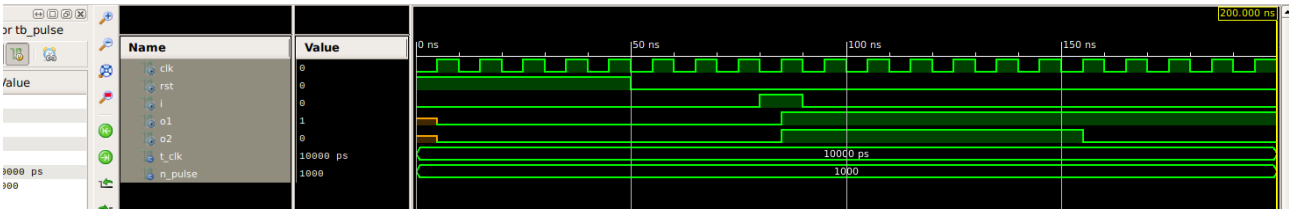
Project Solutions

1. The issue is in the arch of the pulse design. Because, cnt+1 never reaches to N_Pulse, therefore, desired result is not being achieved. This can be solved with a simple trick by replacing **cnt+1=N_PULSE** with **cnt+1=N_PULSE-1** in the ARCH_2 code line number 72.

```
52  --Copy the ARCH_1 to describe a new architecture ARCH_
53  --Modify the ARCH_2 according to the exercise
54
55  architecture ARCH_2 of PULSE is
56  constant N_BITS: integer:=F_NBITS(N_PULSE);
57  signal cnt: unsigned(N_BITS-1 downto 0);
58  signal start,started,finished: std_logic;
59  begin
60     start<=i;
61     o<=started;
62
63     fsm: process
64     begin
65        wait until rising_edge(clk);
66        if rst='1' then
67           started<='0';
68           finished<='0';
69        elsif start='1' then
70           started<='1';
71           finished<='0';
72        elsif (cnt+1=N_PULSE-1) then
73           started<='0';
74           finished<='1';
75        end if;
76     end process;
77
78     counter: process
79     begin
80        wait until rising_edge(clk);
81        cnt<=(others=>'0');
82        if started='1' and finished='0' then
83           cnt<=cnt+1;
84        end if;
85     end process;
86  end architecture;
```



We can see in the simulation that correct ARCH_2 output o2 is as required but arch_1 output o1 is wrong.

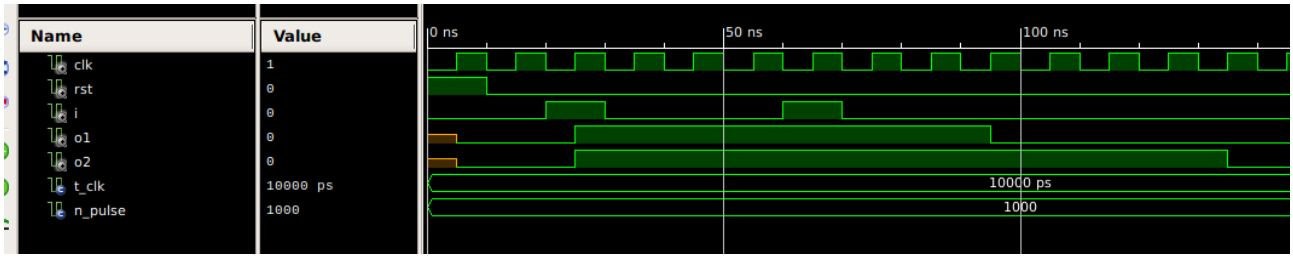
2. To achieve the double click, following code lines of the test bench has been modified.

```
105  begin
106     clk<=not clk after T_CLK/2;
107     rst<='1', '0' after 1*T_CLK; --part 2 modified from 5*T_CLK to 1*T_CLK
108
109     --part 2 solution modified
110     i<='0', '1' after 2*T_CLK, '0' after 3*T_CLK, '1' after 6*T_CLK, '0' after 7*T_CLK;
111
```

This makes sure start is pressed twice after *2*T_CLK* and *6*T_CLK*.
Next, line 72 of arch_1 is also changed to make it work.
Now, to make sure arch_2 output is enlarged as required, its counter (cnt) is being reset every time a start is pressed.

```
begin
   wait until rising_edge(clk);
   cnt<=(others=>'0');
   if start = '1' then --part 2 modification, resets cnt every time star is pressed
      cnt <= "000"; --part 2 modification
   elsif started='1' and finished='0' then
      cnt<=cnt+1;
```

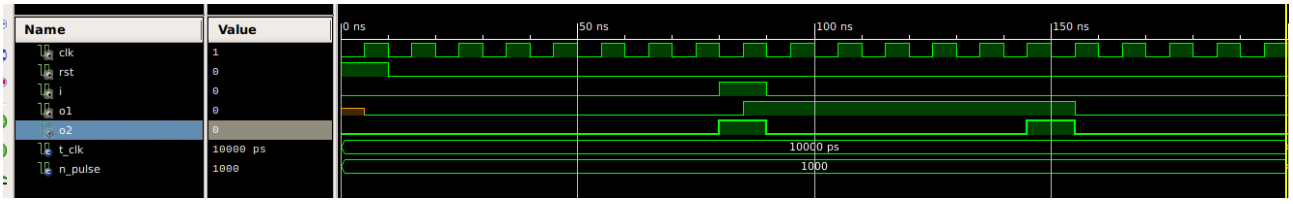
The commented line makes sure, arch_2 is enlarged than arch_1 output. Simulation result below shows the achieved result.



3. In order to activate arche_2 output o2 at the start and end of pulse, we only need to assign o2 as 1 when pulse is active or count of arche_2 (cnt+1=N_PULSE-1) has reached required number of pulses. This can be done by modifying 61 of the pulse as shown in the screenshot below.

As a result, desired output pulse at o2 is achieved.

```
58  signal start,started,finished: std_logic;
59  begin
60     start<=i;
61        o <= '1' when(i = '1' or cnt+1=N_PULSE-1) else '0';--part 3 modification: replacing o<=started with (i = '1' or cnt+1=N_PULSE-1)
62
63
```



4.

100×106Hz×100×10−3s = 10,000,000 clock cycles to produce 100ms pulse

top level code modified.

```
1  NET fpga_clk TNM_NET = clk_net;
2  TIMESPEC TS_clk_net = PERIOD clk_net 100 MHz;
3
4  NET fpga_clk            LOC=C10; #100MHz clock input
5  NET fpga_rst            LOC=V4;     #USER PUSH-BUTTON
6
7  NET switch              LOC=B3;  # DIP1 Switch1 of the LX9 MICROBOARD
8  NET led              LOC=D2;     # LED1 of the LX9 MICROBOARD
9
```

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	26	11440	0%
Number of Slice LUTs	61	5720	1%
Number of fully used LUT-FF pairs	26	61	42%
Number of bonded IOBs	4	200	2%
Number of BUFG/BUFGCTRLs	1	16	6%

Device utilization summary:

Selected Device : 6slx9csg324-3

Slice Logic Utilization:
 Number of Slice Registers: 26 out of 11440 0%
 Number of Slice LUTs: 61 out of 5720 1%
 Number used as Logic: 61 out of 5720 1%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used: 61
 Number with an unused Flip Flop: 35 out of 61 57%
 Number with an unused LUT: 0 out of 61 0%
 Number of fully used LUT-FF pairs: 26 out of 61 42%
 Number of unique control sets: 2

IO Utilization:
 Number of IOs: 4
 Number of bonded IOBs: 4 out of 200 2%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs: 1 out of 16 6%