1. PWM Bit Resolution should be 8 bits

$$Switching\ Frequency\ =\ \frac{1}{2^{R}\times(T_{Sys}\times(Timer\ Final\ Value+1)}$$ where the lowest

$T_{Sys} = 0.5ns$; can you confirm this from the data sheet?

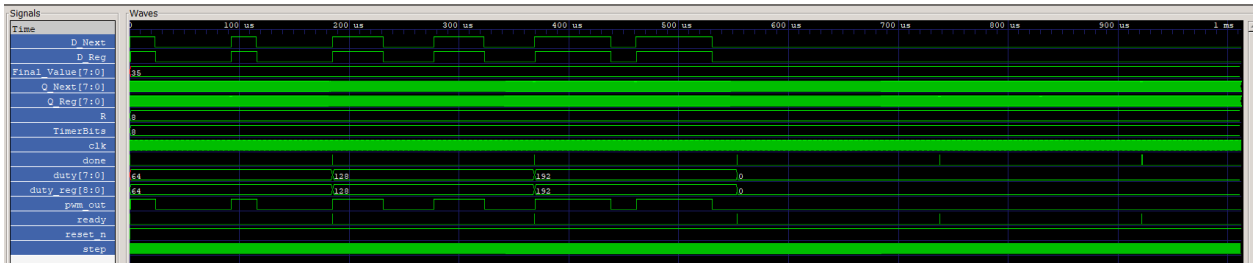
$$Switching\ Frequency\ =\ 3.9MHz$$

In our case, we need up to 3.5 MHz so 8 bit should be good instead of 15 bit. I believe you have to change the bit resolution in a couple modules (Pwm_In, top_level, etc.)

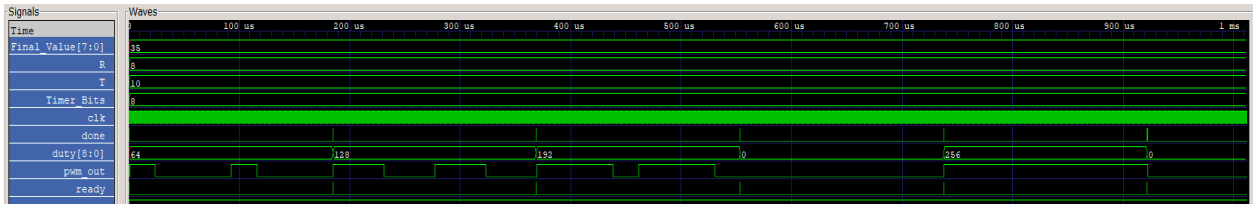
2. Pwm_In module duty logic

```
module Pwm_In
    #(parameter R = 8, TimerBits = 15)(
    input clk,
    input reset_n,
    input [R - 1:0] duty, // Control the Duty Cycle
    input [TimerBits - 1:0] Final_Value, // Control the switching frequency
```

You have [R - 1:0] duty for the input, however it should be [R:0]duty because if we test 100% duty cycle, we will get a duty cycle of 0%. If you read the testbench I wrote, there should be a 100% duty cycle near the end.



Simulation with [R - 1:0] duty above



Simulation with [R - 1:0] duty above

3. Make sure the DEPTH and WIDTH are correct for the sync_fifo module for what we need. I don't see much change from the default values of the modules.
4. Are we sure the PWM_RegInterface and PWM_RegInterfacefifo are correct? No testbench.
5. I am using GTK Wave so I need the $dumpfile and $dumpvars. However, the top_level_tb simulation window is still not opening so I am not sure what is wrong. I have added a $finish after the $stop on line 82.

```
initial begin

  $dumpfile ("top_level_tb.vcd");
  $dumpvars (0, top_level_tb);


// Initialize signals
      spi_tx_data = 16'h0000;
      spi_tx_valid = 0;
```

```
FST info: dumpfile top_level_tb.vcd opened for output.
```

6. In addition to the problem with loading the simulation window, I have a bunch of warnings about the bit sizes while running the top_level module tb.

```
Desktop/VPWM/ffpga/src/top_level.v:55: warning: Port 10 (i_tx_data) of spi_master expects 8 bits, got 16.
Desktop/VPWM/ffpga/src/top_level.v:55:        : Pruning 8 high bits of the expression.
Desktop/VPWM/ffpga/src/top_level.v:55: warning: Port 12 (o_rx_data) of spi_master expects 8 bits, got 16.
Desktop/VPWM/ffpga/src/top_level.v:55:        : Padding 8 high bits of the expression.
Desktop/VPWM/ffpga/src/top_level.v:73: warning: Port 9 (i_tx_data) of spi_slave expects 8 bits, got 16.
Desktop/VPWM/ffpga/src/top_level.v:73:        : Pruning 8 high bits of the expression.
Desktop/VPWM/ffpga/src/top_level.v:73: warning: Port 12 (o_rx_data) of spi_slave expects 8 bits, got 16.
Desktop/VPWM/ffpga/src/top_level.v:73:        : Padding 8 high bits of the expression.
Desktop/VPWM/ffpga/src/top_level.v:135: warning: Port 4 (Final_Value) of Pwm_In expects 15 bits, got 16.
Desktop/VPWM/ffpga/src/top_level.v:135:        : Pruning 1 high bits of the expression.
Desktop/VPWM/ffpga/src/top_level.v:150: warning: Port 4 (Final_Value) of Pwm_In expects 15 bits, got 16.
Desktop/VPWM/ffpga/src/top_level.v:150:        : Pruning 1 high bits of the expression.
Desktop/VPWM/ffpga/src/top_level.v:163: warning: Port 4 (Final_Value) of Pwm_In expects 15 bits, got 16.
Desktop/VPWM/ffpga/src/top_level.v:163:        : Pruning 1 high bits of the expression.
Desktop/VPWM/ffpga/src/top_level.v:177: warning: Port 4 (Final_Value) of Pwm_In expects 15 bits, got 16.
Desktop/VPWM/ffpga/src/top_level.v:177:        : Pruning 1 high bits of the expression.
Desktop/VPWM/ffpga/sim/top_level_tb.vt:99: error: reg fifo_read_enable; cannot be driven by primitives or continuous assignment.
Desktop/VPWM/ffpga/sim/top_level_tb.vt:91: error: Could not find variable ``uut.spi_master.i_tx_data'' in ``top_level_tb''
Desktop/VPWM/ffpga/sim/top_level_tb.vt:92: error: Could not find variable ``uut.spi_master.i_tx_data_valid'' in ``top_level_tb''
Desktop/VPWM/ffpga/sim/top_level_tb.vt:94: error: Could not find variable ``uut.spi_master.i_tx_data_valid'' in ``top_level_tb''
```