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1

REV.

DESCRIPTION

DATE

DESIGNER

CHECKED BY

ENGINEER

1

PRELIMINARY

7/19/2021

J. Bohenek

CKR

ENG

2

UNLESS OTHERWISE SPECIFIED  
ALL DIMENSIONS ARE IN INCHES  
DIMENSIONS IN BRACKETS [X.XX] (WHERE PRESENT)  
ARE MILLIMETERS AND ARE FOR REFERENCE ONLY  
INTERPRET DRAWING AS PER ANSI Y14.5-1994 OR Y32.2-1975

DRAWN BY

J. Mead

DR DATE

CHECKED BY

J. Hammond

CH DATE

VACUUM APPROVAL

NA

ENGINEER APPROVAL

J. Mead

EN DATE

SUPERVISOR APPROVAL

D. Padrazo

SP DATE

ES&H APPROVAL

LES&H APP

QA DATE

QA APPROVAL

QA APP

ES DATE

SCHEMATIC DIAGRAM

RF zuBPM-II

Zynq UltraScale+ DFE

B

LT-EL-SR-EU-BPM-0614-03

2

SH

REVISION

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS, 1%, 100PPM.

2. ALL CAPACITOR VALUES ARE IN MICROFARADS, 50V.

3 ALL INDUCTOR VALUES ARE IN MICROHENRIES.

PROJECT:

THIRD ANGLE PROJECTION

SCALE: N/A

WBS# -

ESH&Q RISK LEVEL A-3

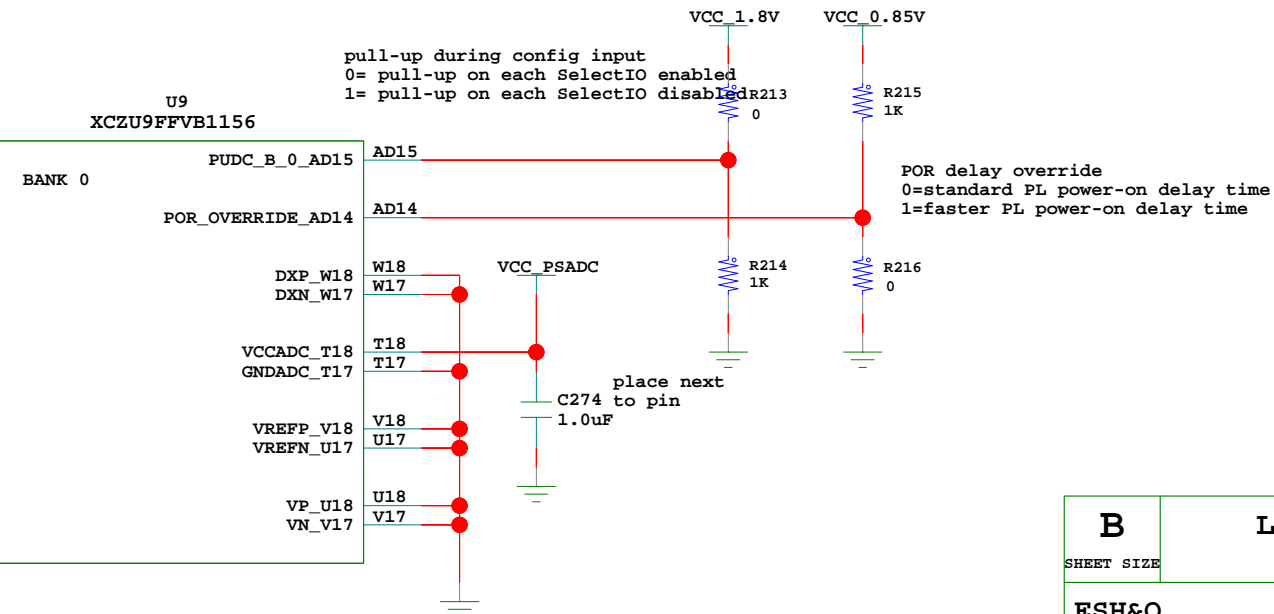
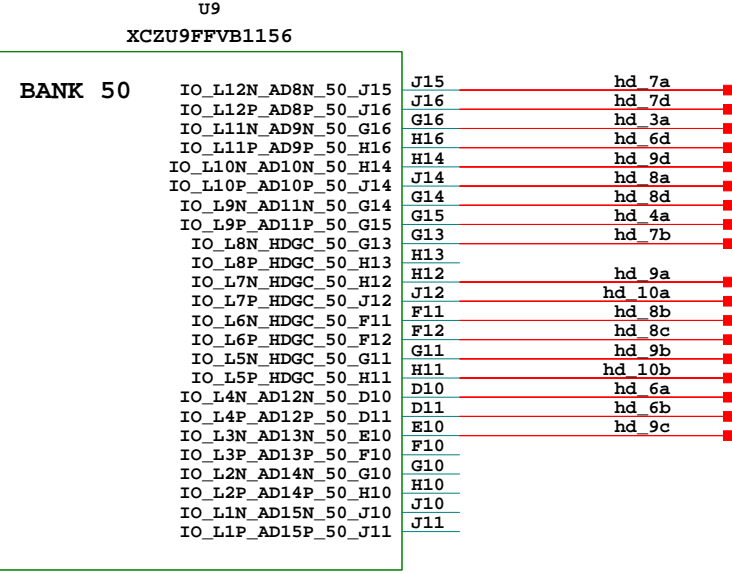
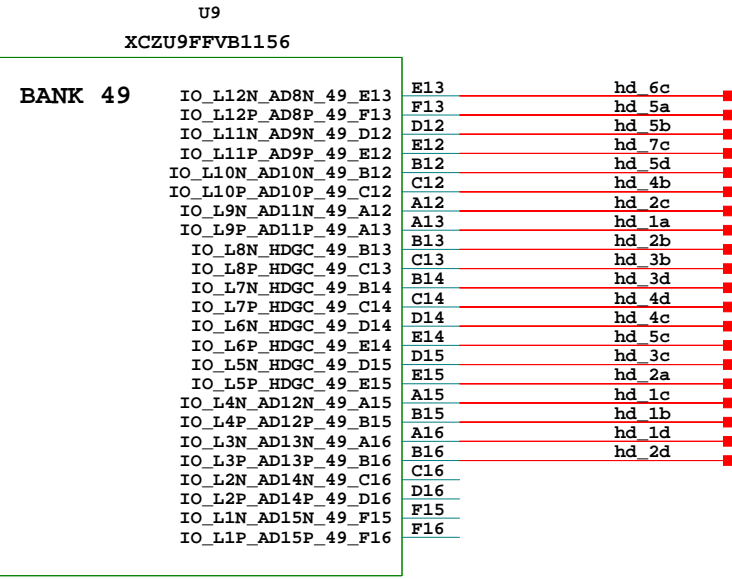
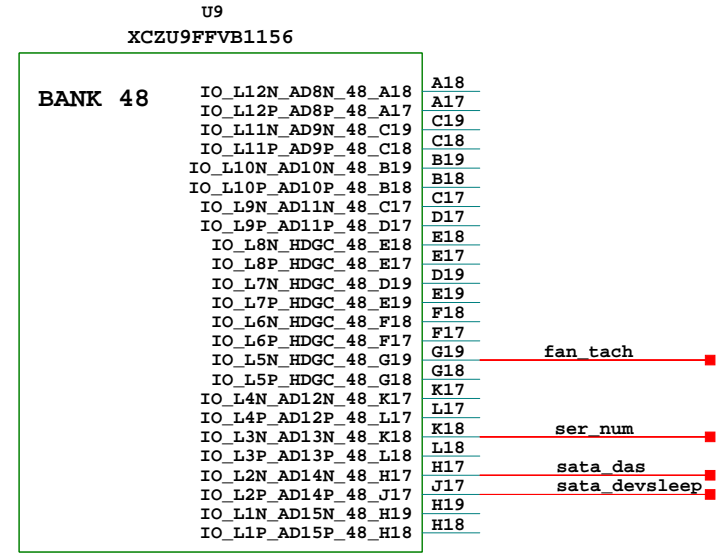
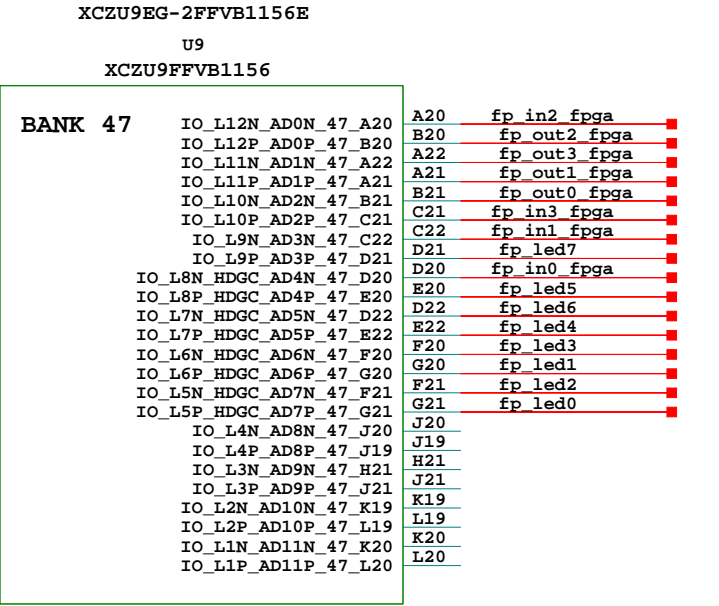
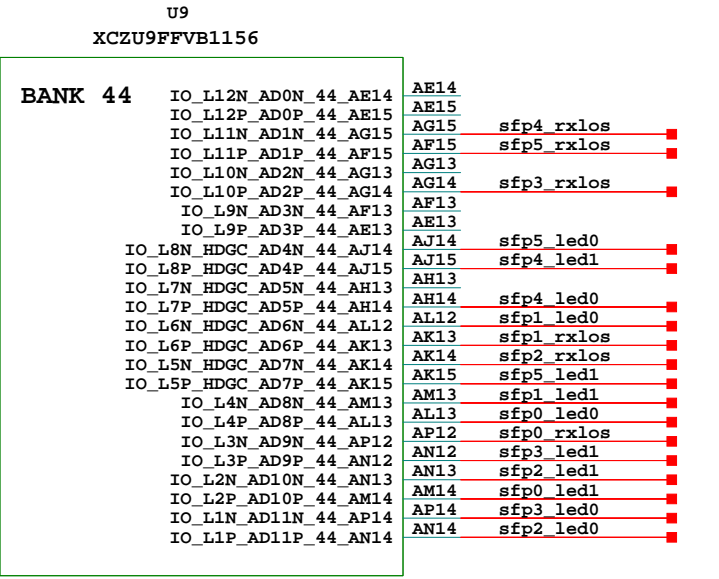
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FPGA - Bank 0 & HD Banks



FPGA - HP Banks

U9 XCZU9FFVB1156	
BANK 64	IO_T3U_N12_64_AP1
	IO_L24N_T3U_N11_64_AK2
	IO_L24P_T3U_N10_64_AK3
	IO_L23N_T3U_N9_64_AL1
	IO_L23P_T3U_N8_64_AK1
IO_L22N_T3U_N7_DBC_AD0N_64_AL2	
IO_L22P_T3U_N6_DBC_AD0P_64_AL3	
IO_L21N_T3L_N5_AD8N_64_AN1	
IO_L21P_T3L_N4_AD8P_64_AM1	
IO_L20N_T3L_N3_AD1N_64_AP3	
IO_L20P_T3L_N2_AD1P_64_AN3	
IO_L19N_T3L_N1_DBC_AD9N_64_AP2	
IO_L19P_T3L_N0_DBC_AD9P_64_AN2	
IO_T2U_N12_64_AM3	
IO_L18N_T2U_N11_AD2N_64_AK4	
IO_L18P_T2U_N10_AD2P_64_AK5	
IO_L17N_T2U_N9_AD10N_64_AN4	
IO_L17P_T2U_N8_AD10P_64_AM4	
IO_L16N_T2U_N7_QBC_AD3N_64_AP6	
IO_L16P_T2U_N6_QBC_AD3P_64_AN6	
IO_L15N_T2L_N5_AD11N_64_AP4	
IO_L15P_T2L_N4_AD11P_64_AP5	
IO_L14N_T2L_N3_GC_64_AM5	
IO_L14P_T2L_N2_GC_64_AM6	
IO_L13N_T2L_N1_GC_QBC_64_AL5	
IO_L13P_T2L_N0_GC_QBC_64_AL6	
IO_T1U_N12_64_AJ7	
IO_L12N_T1U_N11_GC_64_AL7	
IO_L12P_T1U_N10_GC_64_AL8	
IO_L11N_T1U_N9_GC_64_AK7	
IO_L11P_T1U_N8_GC_64_AK8	
IO_L10N_T1U_N7_QBC_AD4N_64_AP7	
IO_L10P_T1U_N6_QBC_AD4P_64_AN7	
IO_L9N_T1L_N5_AD12N_64_AK9	
IO_L9P_T1L_N4_AD12P_64_AJ9	
IO_L8N_T1L_N3_AD5N_64_AM8	
IO_L8P_T1L_N2_AD5P_64_AM9	
IO_L7N_T1L_N1_QBC_AD13N_64_AP8	
IO_L7P_T1L_N0_QBC_AD13P_64_AN8	
IO_T0U_N12_VRP_64_AN11	
IO_L6N_T0U_N11_AD6N_64_AK10	
IO_L6P_T0U_N10_AD6P_64_AJ10	
IO_L5N_T0U_N9_AD14N_64_AP9	
IO_L5P_T0U_N8_AD14P_64_AN9	
IO_L4N_T0U_N7_DBC_AD7N_64_AP10	
IO_L4P_T0U_N6_DBC_AD7P_64_AP11	
IO_L3N_T0L_N5_AD15N_64_AM10	
IO_L3P_T0L_N4_AD15P_64_AL10	
IO_L2N_T0L_N3_64_AM11	
IO_L2P_T0L_N2_64_AL11	
IO_L1N_T0L_N1_DBC_64_AK12	
IO_L1P_T0L_N0_DBC_64_AJ12	
VREF_64_AJ11	

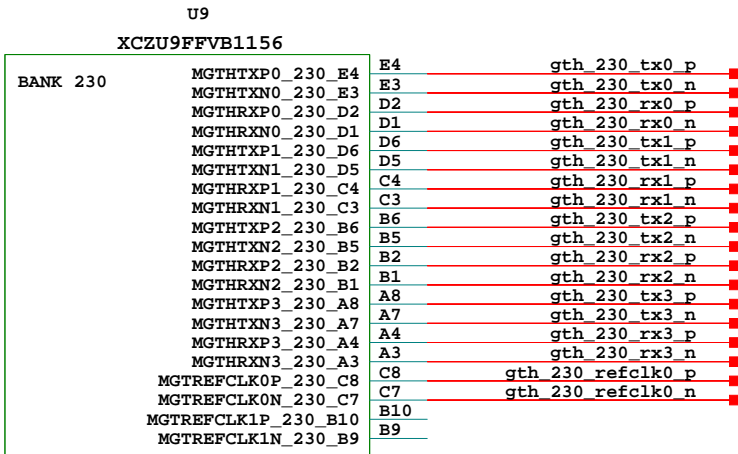
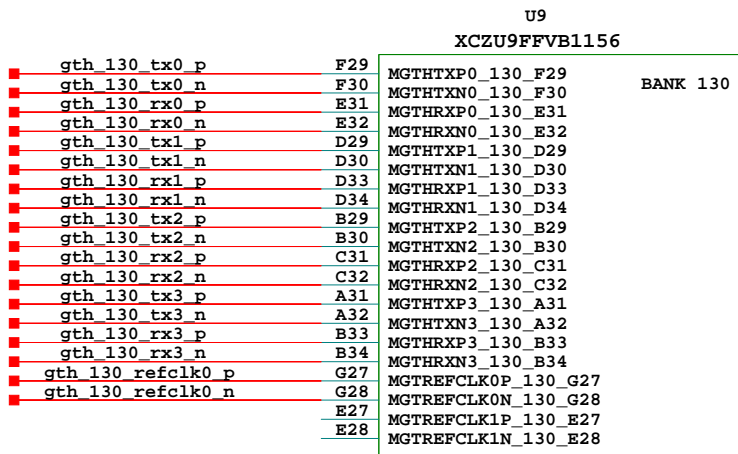
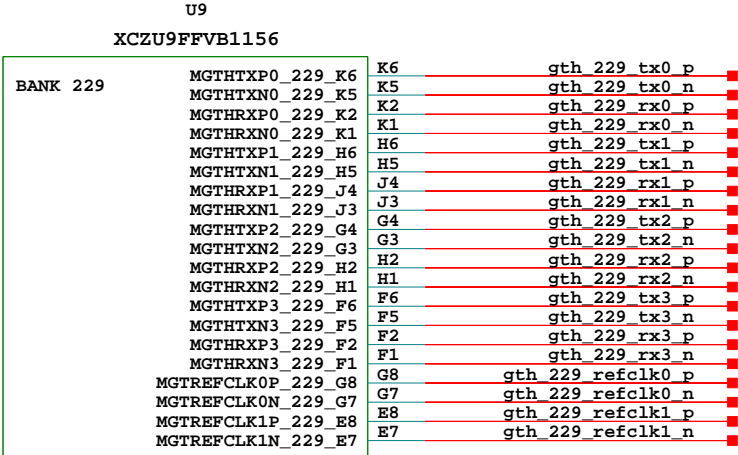
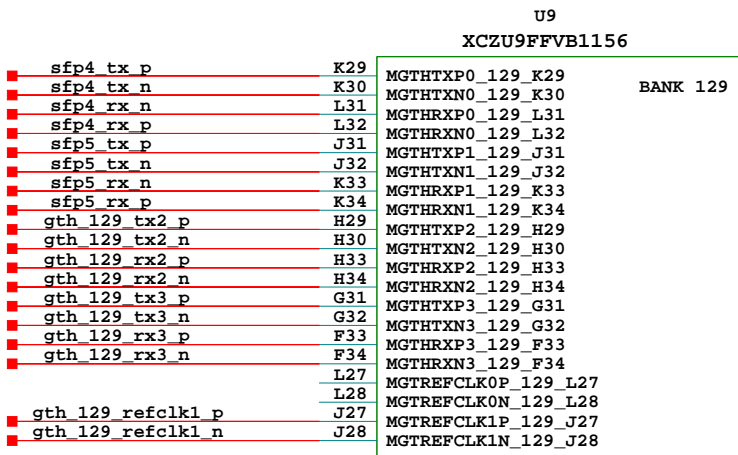
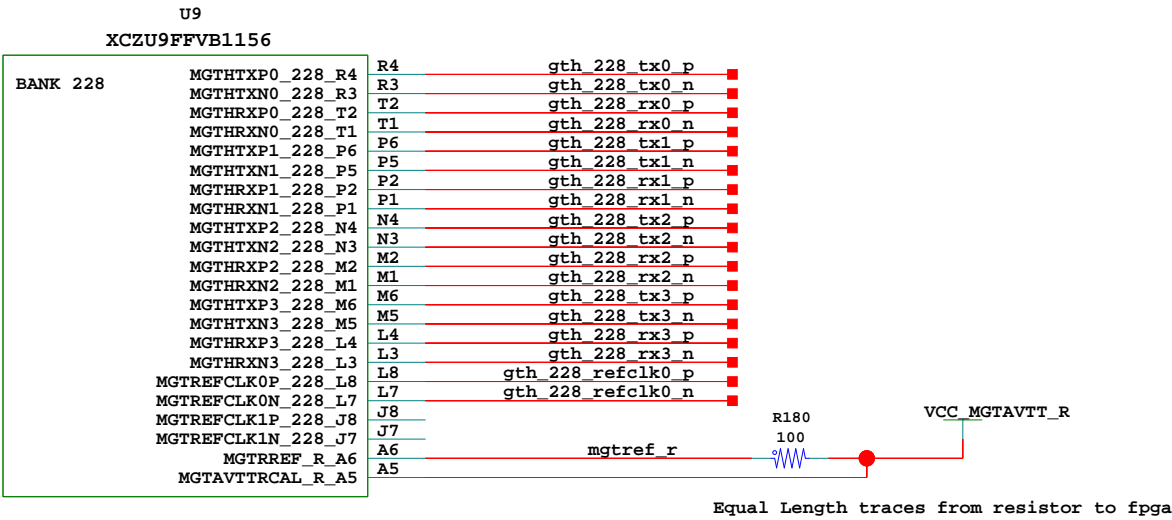
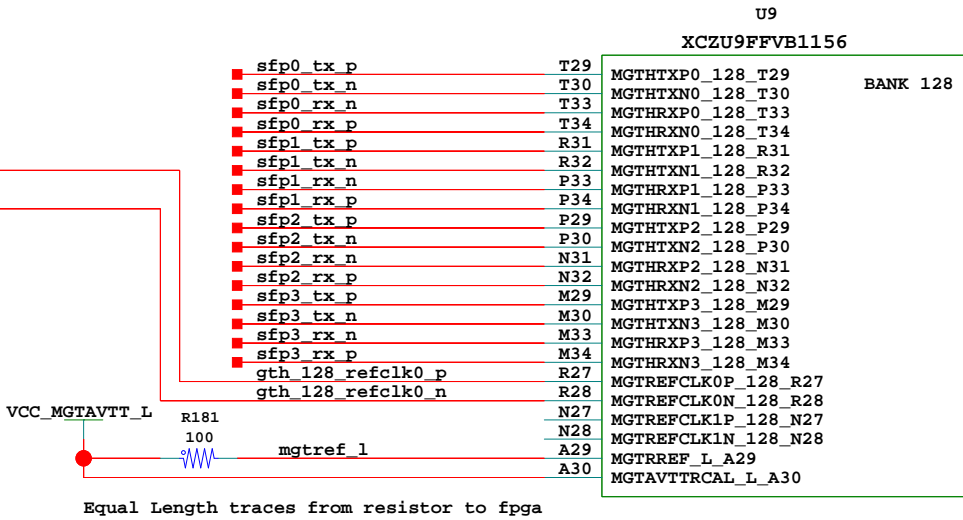
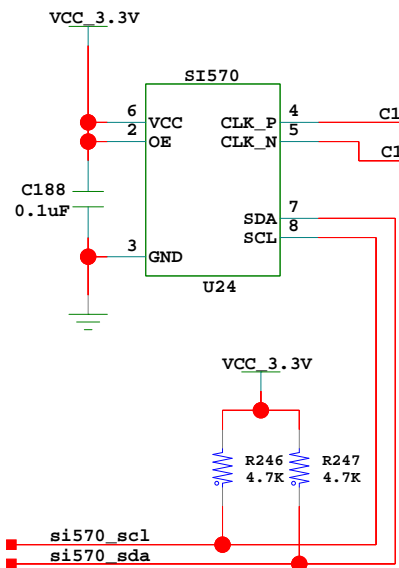
U9 XCZU9FFVB1156	
BANK 65	IO_T3U_N12_65_AG1
	IO_L24N_T3U_N11_PERSTN0_65_AE1
	IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65_AE2
	IO_L23N_T3U_N9_65_AD1
	IO_L23P_T3U_N8_I2C_SCLK_65_AD2
IO_L22N_T3U_N7_DBC_AD0N_65_AJ1	
IO_L22P_T3U_N6_DBC_AD0P_65_AH1	
IO_L21N_T3L_N5_AD8N_65_AF1	
IO_L21P_T3L_N4_AD8P_65_AF2	
IO_L20N_T3L_N3_AD1N_65_AH3	
IO_L20P_T3L_N2_AD1P_65_AG3	
IO_L19N_T3L_N1_DBC_AD9N_65_AJ2	
IO_L19P_T3L_N0_DBC_AD9P_65_AH2	
IO_T2U_N12_65_AD5	
IO_L18N_T2U_N11_AD2N_65_AE4	
IO_L18P_T2U_N10_AD2P_65_AD4	
IO_L17N_T2U_N9_AD10N_65_AF3	
IO_L17P_T2U_N8_AD10P_65_AE3	
IO_L16N_T2U_N7_QBC_AD3N_65_AJ5	
IO_L16P_T2U_N6_QBC_AD3P_65_AJ6	
IO_L15N_T2L_N5_AD11N_65_AJ4	
IO_L15P_T2L_N4_AD11P_65_AH4	
IO_L14N_T2L_N3_GC_65_AG4	
IO_L14P_T2L_N2_GC_65_AG5	
IO_L13N_T2L_N1_GC_QBC_65_AF5	
IO_L13P_T2L_N0_GC_QBC_65_AE5	
IO_T1U_N12_65_AH9	
IO_L12N_T1U_N11_GC_65_AF7	
IO_L12P_T1U_N10_GC_65_AE7	
IO_L11N_T1U_N9_GC_65_AG6	
IO_L11P_T1U_N8_GC_65_AF6	
IO_L10N_T1U_N7_QBC_AD4N_65_AF8	
IO_L10P_T1U_N6_QBC_AD4P_65_AE8	
IO_L9N_T1L_N5_AD12N_65_AD6	
IO_L9P_T1L_N4_AD12P_65_AD7	
IO_L8N_T1L_N3_AD5N_65_AH8	
IO_L8P_T1L_N2_AD5P_65_AG8	
IO_L7N_T1L_N1_QBC_AD13N_65_AH6	
IO_L7P_T1L_N0_QBC_AD13P_65_AH7	
IO_T0U_N12_VRP_65_AD9	
IO_L6N_T0U_N11_AD6N_65_AE9	
IO_L6P_T0U_N10_AD6P_65_AD10	
IO_L5N_T0U_N9_AD14N_65_AG9	
IO_L5P_T0U_N8_AD14P_65_AG10	
IO_L4N_T0U_N7_DBC_AD7N_65_AG11	
IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65_AF11	
IO_L3N_T0L_N5_AD15N_65_AF12	
IO_L3P_T0L_N4_AD15P_65_AE12	
IO_L2N_T0L_N3_65_AH11	
IO_L2P_T0L_N2_65_AH12	
IO_L1N_T0L_N1_DBC_65_AF10	
IO_L1P_T0L_N0_DBC_65_AE10	
VREF_65_AD11	

FPGA - HP Banks

U9 XCZU9FFVB1156	
BANK 66	
IO_T3U_N12_66_AB1	AB1
IO_L24N_T3U_N11_66_W1	W1
IO_L24P_T3U_N10_66_W2	W2
IO_L23N_T3U_N9_66_V1	V1
IO_L23P_T3U_N8_66_V2	V2
IO_L22N_T3U_N7_DBC_AD0N_66_Y1	Y1
IO_L22P_T3U_N6_DBC_AD0P_66_Y2	Y2
IO_L21N_T3L_N5_AD8N_66_AA1	AA1
IO_L21P_T3L_N4_AD8P_66_AA2	AA2
IO_L20N_T3L_N3_AD1N_66_AC3	AC3
IO_L20P_T3L_N2_AD1P_66_AB3	AB3
IO_L19N_T3L_N1_DBC_AD9N_66_AC1	AC1
IO_L19P_T3L_N0_DBC_AD9P_66_AC2	AC2
IO_T2U_N12_66_AA3	AA3
IO_L18N_T2U_N11_AD2N_66_U4	U4
IO_L18P_T2U_N10_AD2P_66_U5	U5
IO_L17N_T2U_N9_AD10N_66_V3	V3
IO_L17P_T2U_N8_AD10P_66_V4	V4
IO_L16N_T2U_N7_QBC_AD3N_66_AC4	AC4
IO_L16P_T2U_N6_QBC_AD3P_66_AB4	AB4
IO_L15N_T2L_N5_AD11N_66_W4	W4
IO_L15P_T2L_N4_AD11P_66_W5	W5
IO_L14N_T2L_N3_GC_66_AA5	AA5
IO_L14P_T2L_N2_GC_66_Y5	Y5
IO_L13N_T2L_N1_GC_QBC_66_Y3	Y3
IO_L13P_T2L_N0_GC_QBC_66_Y4	Y4
IO_T1U_N12_66_AA8	AA8
IO_L12N_T1U_N11_GC_66_AA6	AA6
IO_L12P_T1U_N10_GC_66_AA7	AA7
IO_L11N_T1U_N9_GC_66_Y7	Y7
IO_L11P_T1U_N8_GC_66_Y8	Y8
IO_L10N_T1U_N7_QBC_AD4N_66_AB5	AB5
IO_L10P_T1U_N6_QBC_AD4P_66_AB6	AB6
IO_L9N_T1L_N5_AD12N_66_W6	W6
IO_L9P_T1L_N4_AD12P_66_W7	W7
IO_L8N_T1L_N3_AD5N_66_AC8	AC8
IO_L8P_T1L_N2_AD5P_66_AB8	AB8
IO_L7N_T1L_N1_QBC_AD13N_66_AC6	AC6
IO_L7P_T1L_N0_QBC_AD13P_66_AC7	AC7
IO_T0U_N12_VRP_66_W9	W9
IO_L6N_T0U_N11_AD6N_66_Y9	Y9
IO_L6P_T0U_N10_AD6P_66_Y10	Y10
IO_L5N_T0U_N9_AD14N_66_AA12	AA12
IO_L5P_T0U_N8_AD14P_66_Y12	Y12
IO_L4N_T0U_N7_DBC_AD7N_66_AC9	AC9
IO_L4P_T0U_N6_DBC_AD7P_66_AB9	AB9
IO_L3N_T0L_N5_AD15N_66_AA10	AA10
IO_L3P_T0L_N4_AD15P_66_AA11	AA11
IO_L2N_T0L_N3_66_AB10	AB10
IO_L2P_T0L_N2_66_AB11	AB11
IO_L1N_T0L_N1_DBC_66_AC11	AC11
IO_L1P_T0L_N0_DBC_66_AC12	AC12
VREF_66_AD12	AD12

U9 XCZU9FFVB1156	
BANK 67	
IO_T3U_N12_67_K14	K14
IO_L24N_T3U_N11_67_K15	K15
IO_L24P_T3U_N10_67_L15	L15
IO_L23N_T3U_N9_67_K13	K13
IO_L23P_T3U_N8_67_L13	L13
IO_L22N_T3U_N7_DBC_AD0N_67_M13	M13
IO_L22P_T3U_N6_DBC_AD0P_67_N13	N13
IO_L21N_T3L_N5_AD8N_67_N12	N12
IO_L21P_T3L_N4_AD8P_67_P12	P12
IO_L20N_T3L_N3_AD1N_67_M14	M14
IO_L20P_T3L_N2_AD1P_67_M15	M15
IO_L19N_T3L_N1_DBC_AD9N_67_K16	K16
IO_L19P_T3L_N0_DBC_AD9P_67_L16	L16
IO_T2U_N12_67_K10	K10
IO_L18N_T2U_N11_AD2N_67_K12	K12
IO_L18P_T2U_N10_AD2P_67_L12	L12
IO_L17N_T2U_N9_AD10N_67_L11	L11
IO_L17P_T2U_N8_AD10P_67_M11	M11
IO_L16N_T2U_N7_QBC_AD3N_67_N8	N8
IO_L16P_T2U_N6_QBC_AD3P_67_N9	N9
IO_L15N_T2L_N5_AD11N_67_L10	L10
IO_L15P_T2L_N4_AD11P_67_M10	M10
IO_L14N_T2L_N3_GC_67_P9	P9
IO_L14P_T2L_N2_GC_67_P10	P10
IO_L13N_T2L_N1_GC_QBC_67_N11	N11
IO_L13P_T2L_N0_GC_QBC_67_P11	P11
IO_T1U_N12_67_V9	V9
IO_L12N_T1U_N11_GC_67_R8	R8
IO_L12P_T1U_N10_GC_67_T8	T8
IO_L11N_T1U_N9_GC_67_R9	R9
IO_L11P_T1U_N8_GC_67_R10	R10
IO_L10N_T1U_N7_QBC_AD4N_67_T6	T6
IO_L10P_T1U_N6_QBC_AD4P_67_T7	T7
IO_L9N_T1L_N5_AD12N_67_U8	U8
IO_L9P_T1L_N4_AD12P_67_U9	U9
IO_L8N_T1L_N3_AD5N_67_U6	U6
IO_L8P_T1L_N2_AD5P_67_V6	V6
IO_L7N_T1L_N1_QBC_AD13N_67_V7	V7
IO_L7P_T1L_N0_QBC_AD13P_67_V8	V8
IO_T0U_N12_VRP_67_W10	W10
IO_L6N_T0U_N11_AD6N_67_T11	T11
IO_L6P_T0U_N10_AD6P_67_U11	U11
IO_L5N_T0U_N9_AD14N_67_V11	V11
IO_L5P_T0U_N8_AD14P_67_V12	V12
IO_L4N_T0U_N7_DBC_AD7N_67_R12	R12
IO_L4P_T0U_N6_DBC_AD7P_67_T12	T12
IO_L3N_T0L_N5_AD15N_67_T10	T10
IO_L3P_T0L_N4_AD15P_67_U10	U10
IO_L2N_T0L_N3_67_R13	R13
IO_L2P_T0L_N2_67_T13	T13
IO_L1N_T0L_N1_DBC_67_W11	W11
IO_L1P_T0L_N0_DBC_67_W12	W12
VREF_67_N14	N14

FPGA - PL Transceivers





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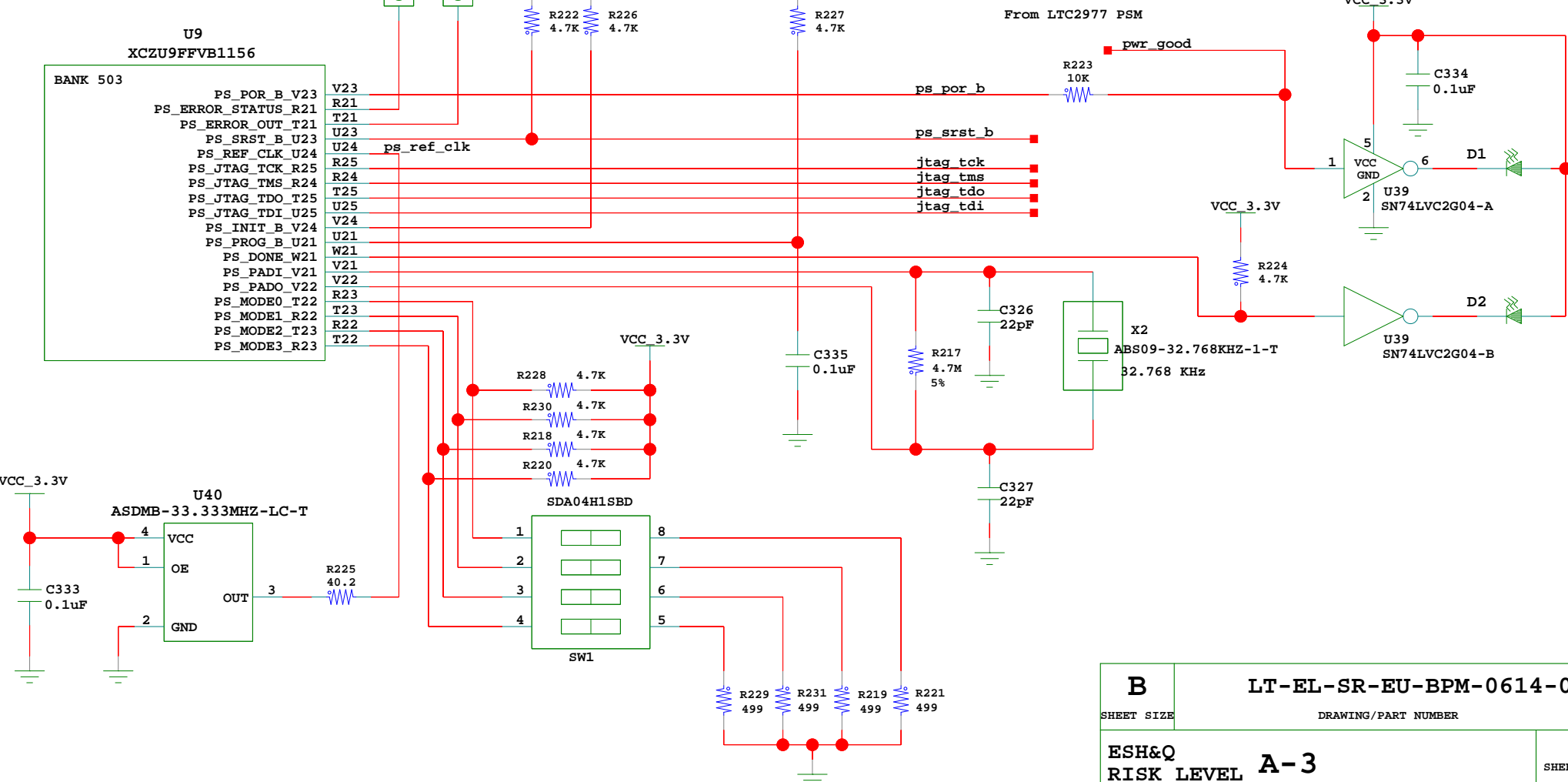
FPGA - PS Banks

U9 XCZU9FFVB1156		
BANK 500	PS_MIO25_AE19	AE19
	PS_MIO24_AE20	AE20
	PS_MIO23_AD19	AD19
	PS_MIO22_AD20	AD20
	PS_MIO21_AF18	AF18
	PS_MIO20_AD18	AD18
	PS_MIO19_AL17	AL17
	PS_MIO18_AE18	AE18
	PS_MIO17_AP16	AP16
	PS_MIO16_AM16	AM16
	PS_MIO15_AN16	AN16
	PS_MIO14_AL16	AL16
	PS_MIO13_AK17	AK17
	PS_MIO12_AJ17	AJ17
	PS_MIO11_AF17	AF17
	PS_MIO10_AH17	AH17
	PS_MIO9_API5	API5
	PS_MIO8_AE17	AE17
	PS_MIO7_AD17	AD17
	PS_MIO6_AL15	AL15
	PS_MIO5_AM15	AM15
	PS_MIO4_AH16	AH16
	PS_MIO3_AG16	AG16
	PS_MIO2_AD16	AD16
	PS_MIO1_AJ16	AJ16
	PS_MIO0_AF16	AF16

U9 XCZU9FFVB1156		
BANK 502	PS_MIO77_F25	F25
	PS_MIO76_H25	H25
	PS_MIO75_D25	D25
	PS_MIO74_G25	G25
	PS_MIO73_H24	H24
	PS_MIO72_E25	E25
	PS_MIO71_C27	C27
	PS_MIO70_C26	C26
	PS_MIO69_B27	B27
	PS_MIO68_B26	B26
	PS_MIO67_B25	B25
	PS_MIO66_A27	A27
	PS_MIO65_A26	A26
	PS_MIO64_A25	A25
	PS_MIO63_D24	D24
	PS_MIO62_G24	G24
	PS_MIO61_C24	C24
	PS_MIO60_E24	E24
	PS_MIO59_B24	B24
	PS_MIO58_G23	G23
	PS_MIO57_A23	A23
	PS_MIO56_C23	C23
	PS_MIO55_B23	B23
	PS_MIO54_F23	F23
	PS_MIO53_E23	E23
	PS_MIO52_F22	F22
	PS_MIO77_F25	F25
	PS_MIO76_H25	H25
	PS_MIO75_D25	D25
	PS_MIO74_G25	G25
	PS_MIO73_H24	H24
	PS_MIO72_E25	E25
	PS_MIO71_C27	C27
	PS_MIO70_C26	C26
	PS_MIO69_B27	B27
	PS_MIO68_B26	B26
	PS_MIO67_B25	B25
	PS_MIO66_A27	A27
	PS_MIO65_A26	A26
	PS_MIO64_A25	A25
	PS_MIO63_D24	D24
	PS_MIO62_G24	G24
	PS_MIO61_C24	C24
	PS_MIO60_E24	E24
	PS_MIO59_B24	B24
	PS_MIO58_G23	G23
	PS_MIO57_A23	A23
	PS_MIO56_C23	C23
	PS_MIO55_B23	B23
	PS_MIO54_F23	F23
	PS_MIO53_E23	E23
	PS_MIO52_F22	F22

U9 XCZU9FFVB1156		
BANK 505	PS_MGTRTXP0_505_AB29	AB29
	PS_MGTRTXN0_505_AB30	AB30
	PS_MGTRRXXP0_505_AB33	AB33
	PS_MGTRRXN0_505_AB34	AB34
	PS_MGTRTXP1_505_Y29	Y29
	PS_MGTRTXN1_505_Y30	Y30
	PS_MGTRRXXP1_505_AA31	AA31
	PS_MGTRRXN1_505_AA32	AA32
	PS_MGTRTXP2_505_W31	W31
	PS_MGTRTXN2_505_W32	W32
	PS_MGTRRXXP2_505_Y33	Y33
	PS_MGTRRXN2_505_Y34	Y34
	PS_MGTRTXP3_505_V29	V29
	PS_MGTRTXN3_505_V30	V30
	PS_MGTRRXXP3_505_V33	V33
	PS_MGTRRXN3_505_V34	V34
	PS_MGTREFCLK0P_505_AA27	AA27
	PS_MGTREFCLK0N_505_AA28	AA28
	PS_MGTREFCLK1P_505_W27	W27
	PS_MGTREFCLK1N_505_W28	W28
	PS_MGTREFCLK2P_505_U27	U27
	PS_MGTREFCLK2N_505_U28	U28
	PS_MGTREFCLK3P_505_U31	U31
	PS_MGTREFCLK3N_505_U32	U32
	PS_MGTRREF_505_AB28	AB28
	gtrl_sata_tx_p	
	gtrl_sata_tx_n	
	gtrl_sata_rx_p	
	gtrl_sata_rx_n	
	gtr_refclk1_p	
	gtr_refclk1_n	
	ps_mgtrref	
	R193 500	

U9 XCZU9FFVB1156		
BANK 501	PS_MIO51_N25	N25
	PS_MIO50_P25	P25
	PS_MIO49_K25	K25
	PS_MIO48_M25	M25
	PS_MIO47_L25	L25
	PS_MIO46_J25	J25
	PS_MIO45_P24	P24
	PS_MIO44_N24	N24
	PS_MIO43_K24	K24
	PS_MIO42_M24	M24
	PS_MIO41_J24	J24
	PS_MIO40_M23	M23
	PS_MIO39_N23	N23
	PS_MIO38_L23	L23
	PS_MIO37_N22	N22
	PS_MIO36_K23	K23
	PS_MIO35_P22	P22
	PS_MIO34_L22	L22
	PS_MIO33_H23	H23
	PS_MIO32_H22	H22
	PS_MIO31_J22	J22
	PS_MIO30_L21	L21
	PS_MIO29_K22	K22
	PS_MIO28_N21	N21
	PS_MIO27_M21	M21
	PS_MIO26_P21	P21
	mio51_sd_clk	
	mio50_sd_cmd	
	mio49_sd_d3	
	mio48_sd_d2	
	mio47_sd_d1	
	mio46_sd_d0	
	mio45_sd_cd	
	mio44_sd_wp	
	mio35_uart_tx	
	mio34_uart_rx	
	mio27_i2c_sda	
	mio26_i2c_scl	



FPGA - PS DDR4 Bank

refer to UG583 - Chapter 2 for routing guidance

XCZU9FFVB1156

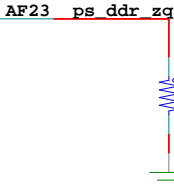
BANK 504

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PS_DDR4_A3	AP27
PS_DDR4_A4	AP25
PS_DDR4_A5	AN24
PS_DDR4_A6	AM29
PS_DDR4_A7	AM28
PS_DDR4_A8	AM26
PS_DDR4_A9	AM25
PS_DDR4_A10	AL28
PS_DDR4_A11	AK27
PS_DDR4_A12	AJ25
PS_DDR4_A13	AL25
PS_DDR4_A14	AK25
PS_DDR4_A15	AK24
PS_DDR4_A16	AM24
PS_DDR4_BA0	AF25
PS_DDR4_BA1	AH26
PS_DDR4_ACTN	AG26
PS_DDR4_ALERTN	AF22
PS_DDR4_PARITY	AF20
PS_DDR4_RAM_RSTN	AF21
PS_DDR4_BG0	AK28
PS_DDR4_CS0N	AN28
PS_DDR4_CK0_P	AN26
PS_DDR4_CK0_N	AN27
PS_DDR4_CKE0	AL26
PS_DDR4_ODT0	AL27
PS_DDR4_DQS0_P	AN29
PS_DDR4_DQS0_N	AJ27
PS_DDR4_DQS1_P	AM30
PS_DDR4_DQS1_N	AJ26
PS_DDR4_DQS2_P	AN18
PS_DDR4_DQS2_N	AN19
PS_DDR4_DQS3_P	AN21
PS_DDR4_DQS3_N	AN22
PS_DDR4_DQS4_P	AH19
PS_DDR4_DQS4_N	AJ19
PS_DDR4_DQS5_P	AH22
PS_DDR4_DQS5_N	AH23
PS_DDR4_DQS6_P	AH28
PS_DDR4_DQS6_N	AH29
PS_DDR4_DQS7_P	AE28
PS_DDR4_DQS7_N	AE29
PS_DDR4_DM0	AJ32
PS_DDR4_DM1	AK32
PS_DDR4_DM2	AE33
PS_DDR4_DM3	AE32
PS_DDR4_DM4	AN32
PS_DDR4_DM5	AN33
PS_DDR4_DM6	AN17
PS_DDR4_DM7	AM21
PS_DDR4_DM8	AK19
PS_DDR4_DM9	AH24
PS_DDR4_DM10	AH31
PS_DDR4_DM11	AE30
PS_DDR4_DM12	AJ31
PS_DDR4_DM13	AE34
PS_DDR4_DM14	AN34

PS_DDR_A0_AP29	PS_DDR_A0_AP29
PS_DDR_A1_AP30	PS_DDR_A1_AP30
PS_DDR_A2_AP26	PS_DDR_A2_AP26
PS_DDR_A3_AP27	PS_DDR_A3_AP27
PS_DDR_A4_AP25	PS_DDR_A4_AP25
PS_DDR_A5_AN24	PS_DDR_A5_AN24
PS_DDR_A6_AM29	PS_DDR_A6_AM29
PS_DDR_A7_AM28	PS_DDR_A7_AM28
PS_DDR_A8_AM26	PS_DDR_A8_AM26
PS_DDR_A9_AM25	PS_DDR_A9_AM25
PS_DDR_A10_AL28	PS_DDR_A10_AL28
PS_DDR_A11_AK27	PS_DDR_A11_AK27
PS_DDR_A12_AJ25	PS_DDR_A12_AJ25
PS_DDR_A13_AL25	PS_DDR_A13_AL25
PS_DDR_A14_AK25	PS_DDR_A14_AK25
PS_DDR_A15_AK24	PS_DDR_A15_AK24
PS_DDR_A16_AM24	PS_DDR_A16_AM24
PS_DDR_A17_AF25	PS_DDR_A17_AF25
PS_DDR_BA0_AH26	PS_DDR_BA0_AH26
PS_DDR_BA1_AG26	PS_DDR_BA1_AG26
PS_DDR_ACTN_AG25	PS_DDR_ACTN_AG25
PS_DDR_ALERTN_AF22	PS_DDR_ALERTN_AF22
PS_DDR_PARITY_AF20	PS_DDR_PARITY_AF20
PS_DDR_RAM_RSTN_AF21	PS_DDR_RAM_RSTN_AF21
PS_DDR_BG0_AK28	PS_DDR_BG0_AK28
PS_DDR_CS0N_AN28	PS_DDR_CS0N_AN28
PS_DDR_CK0_P_AN26	PS_DDR_CK0_P_AN26
PS_DDR_CK0_N_AN27	PS_DDR_CK0_N_AN27
PS_DDR_CKE0_AL26	PS_DDR_CKE0_AL26
PS_DDR_ODT0_AL27	PS_DDR_ODT0_AL27
PS_DDR_DQS0_P_AN29	PS_DDR_DQS0_P_AN29
PS_DDR_DQS0_N_AJ27	PS_DDR_DQS0_N_AJ27
PS_DDR_DQS1_P_AM30	PS_DDR_DQS1_P_AM30
PS_DDR_DQS1_N_AJ26	PS_DDR_DQS1_N_AJ26
PS_DDR_DQS2_P_AN18	PS_DDR_DQS2_P_AN18
PS_DDR_DQS2_N_AN19	PS_DDR_DQS2_N_AN19
PS_DDR_DQS3_P_AN21	PS_DDR_DQS3_P_AN21
PS_DDR_DQS3_N_AN22	PS_DDR_DQS3_N_AN22
PS_DDR_DQS4_P_AH19	PS_DDR_DQS4_P_AH19
PS_DDR_DQS4_N_AJ19	PS_DDR_DQS4_N_AJ19
PS_DDR_DQS5_P_AH22	PS_DDR_DQS5_P_AH22
PS_DDR_DQS5_N_AH23	PS_DDR_DQS5_N_AH23
PS_DDR_DQS6_P_AH28	PS_DDR_DQS6_P_AH28
PS_DDR_DQS6_N_AH29	PS_DDR_DQS6_N_AH29
PS_DDR_DQS7_P_AE28	PS_DDR_DQS7_P_AE28
PS_DDR_DQS7_N_AE29	PS_DDR_DQS7_N_AE29
PS_DDR_DM0_AJ32	PS_DDR_DM0_AJ32
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PS_DDR_DM2_AE33	PS_DDR_DM2_AE33
PS_DDR_DM3_AE32	PS_DDR_DM3_AE32
PS_DDR_DM4_AN32	PS_DDR_DM4_AN32
PS_DDR_DM5_AN33	PS_DDR_DM5_AN33
PS_DDR_DM6_AN17	PS_DDR_DM6_AN17
PS_DDR_DM7_AM21	PS_DDR_DM7_AM21
PS_DDR_DM8_AK19	PS_DDR_DM8_AK19
PS_DDR_DM9_AH24	PS_DDR_DM9_AH24
PS_DDR_DM10_AH31	PS_DDR_DM10_AH31
PS_DDR_DM11_AE30	PS_DDR_DM11_AE30
PS_DDR_DM12_AJ31	PS_DDR_DM12_AJ31
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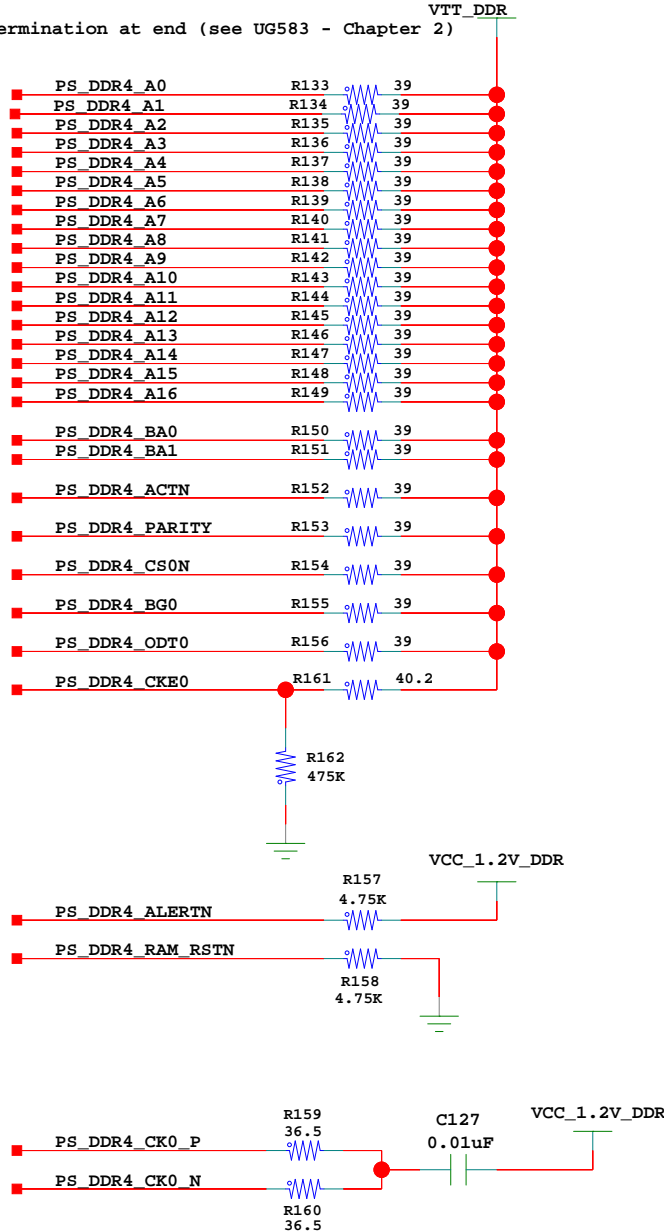
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PS_DDR_DQ5_AM19	PS_DDR_DQ5_AM19
PS_DDR_DQ6_AM18	PS_DDR_DQ6_AM18
PS_DDR_DQ7_AL18	PS_DDR_DQ7_AL18
PS_DDR_DQ8_AP22	PS_DDR_DQ8_AP22
PS_DDR_DQ9_AP21	PS_DDR_DQ9_AP21
PS_DDR_DQ10_AP24	PS_DDR_DQ10_AP24
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PS_DDR_DQ12_AL21	PS_DDR_DQ12_AL21
PS_DDR_DQ13_AL22	PS_DDR_DQ13_AL22
PS_DDR_DQ14_AM23	PS_DDR_DQ14_AM23
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PS_DDR_DQ23_AG18	PS_DDR_DQ23_AG18
PS_DDR_DQ24_AG21	PS_DDR_DQ24_AG21
PS_DDR_DQ25_AH21	PS_DDR_DQ25_AH21
PS_DDR_DQ26_AG24	PS_DDR_DQ26_AG24
PS_DDR_DQ27_AG23	PS_DDR_DQ27_AG23
PS_DDR_DQ28_AK22	PS_DDR_DQ28_AK22
PS_DDR_DQ29_AJ21	PS_DDR_DQ29_AJ21
PS_DDR_DQ30_AJ22	PS_DDR_DQ30_AJ22
PS_DDR_DQ31_AK23	PS_DDR_DQ31_AK23
PS_DDR_DQ32_AG31	PS_DDR_DQ32_AG31
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PS_DDR_DQ38_AK30	PS_DDR_DQ38_AK30
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PS_DDR_DQ40_AE27	PS_DDR_DQ40_AE27
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PS_DDR_DQ57_AG34	PS_DDR_DQ57_AG34
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PS_DDR_DQ59_AF33	PS_DDR_DQ59_AF33
PS_DDR_DQ60_AD31	PS_DDR_DQ60_AD31
PS_DDR_DQ61_AD32	PS_DDR_DQ61_AD32
PS_DDR_DQ62_AD34	PS_DDR_DQ62_AD34
PS_DDR_DQ63_AD33	PS_DDR_DQ63_AD33
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PS_DDR_DQ65_AP31	PS_DDR_DQ65_AP31
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PS_DDR_DQ69_AM33	PS_DDR_DQ69_AM33
PS_DDR_DQ70_AM34	PS_DDR_DQ70_AM34
PS_DDR_DQ71_AL33	PS_DDR_DQ71_AL33

PS\_DDR\_ZQ\_AF23



AF23 ps ddr zq

Fly by routing, termination at end (see UG583 - Chapter 2)



4

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XCZU9FFVB1156

VCCO Bank Power

Core Power

FPGA - PL Power

VCC\_3.3V

VCC\_0.85V

VCC\_1.8V

VCC\_1.8V

VCC\_MGT\_0.9V

VCC\_MGT\_0.9V

VCC\_MGT\_1.2V

VCC\_MGT\_1.2V

VCC\_MGT\_1.8V

VCC\_MGT\_1.8V

Transceiver Power

U9

B

LT-EL-SR-EU-BPM-0614-03

2

SHEET SIZE

DRAWING/PART NUMBER

REVISION

ESH&amp;Q

RISK LEVEL A-3

SHEET 8 OF 31

4

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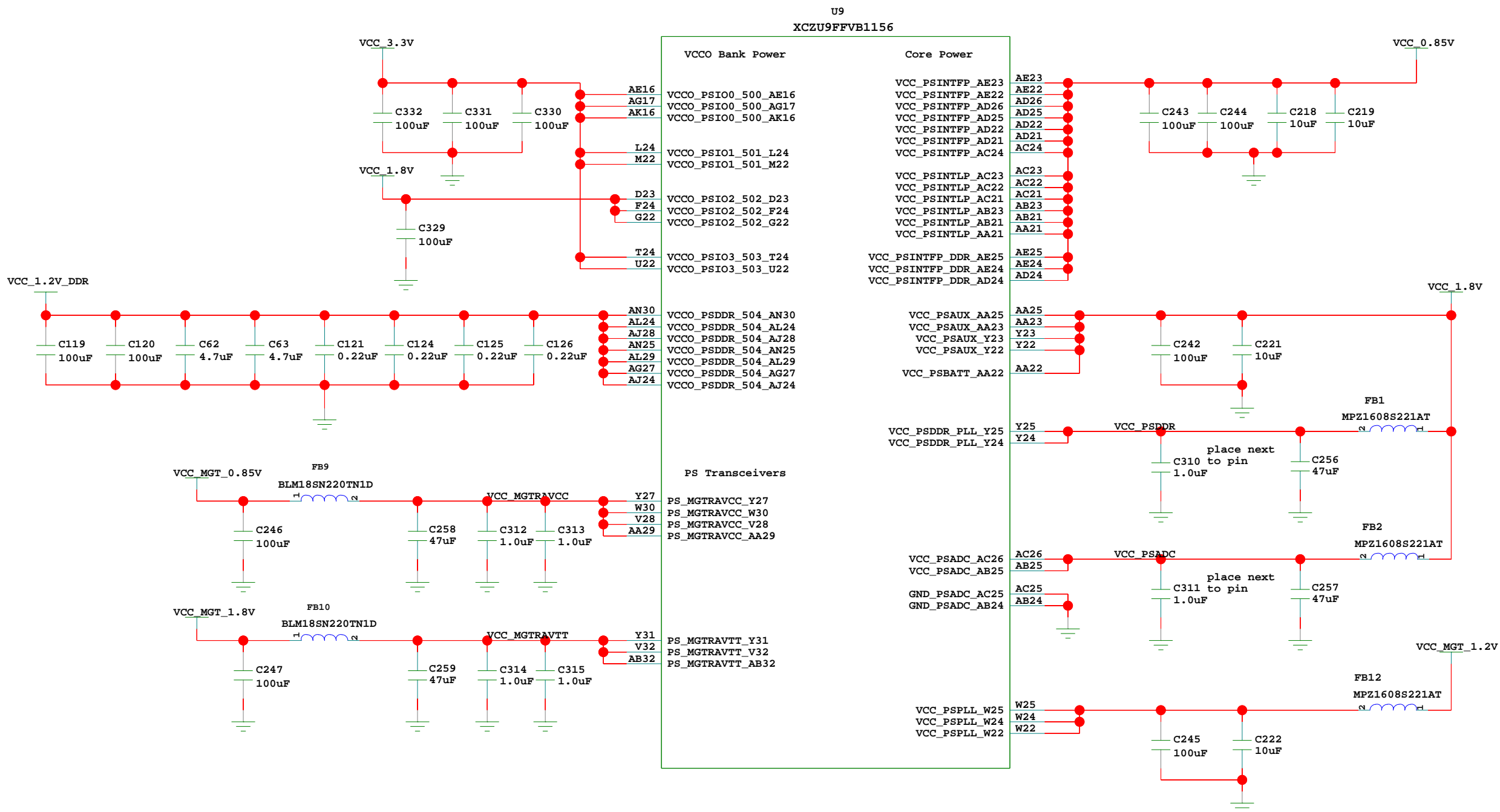
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FPGA - PS Power



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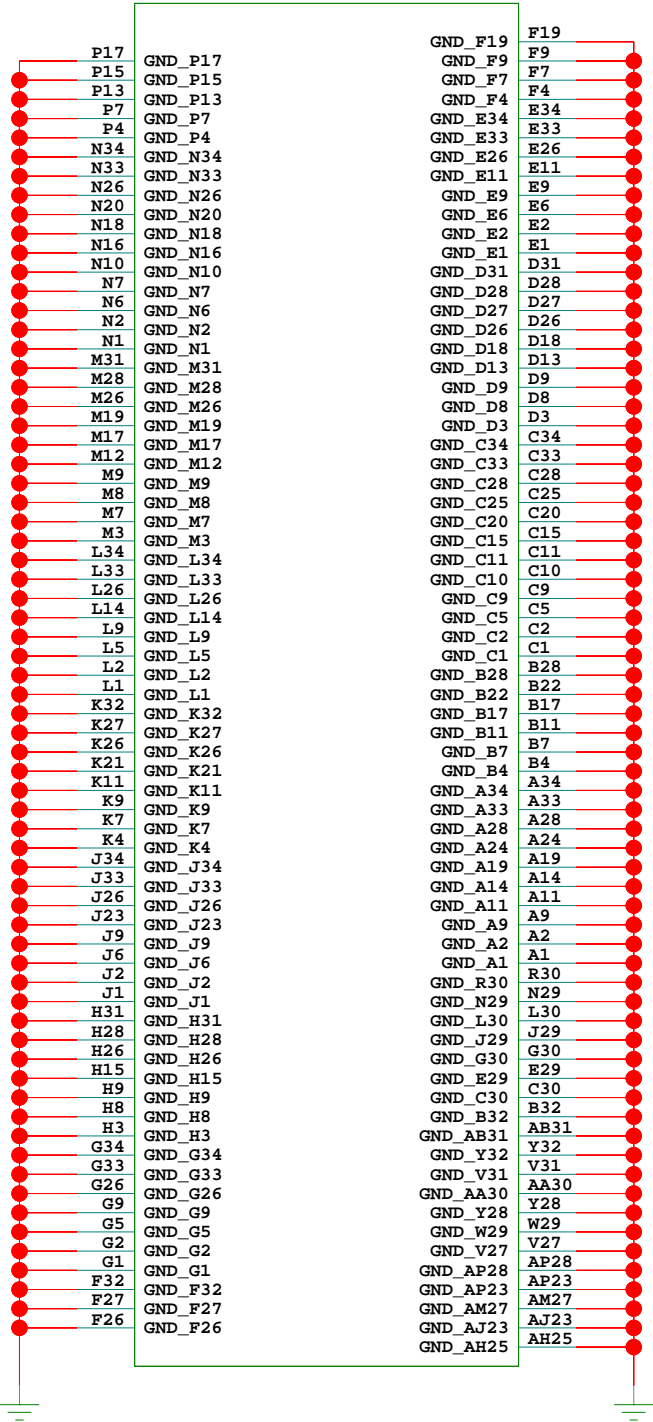
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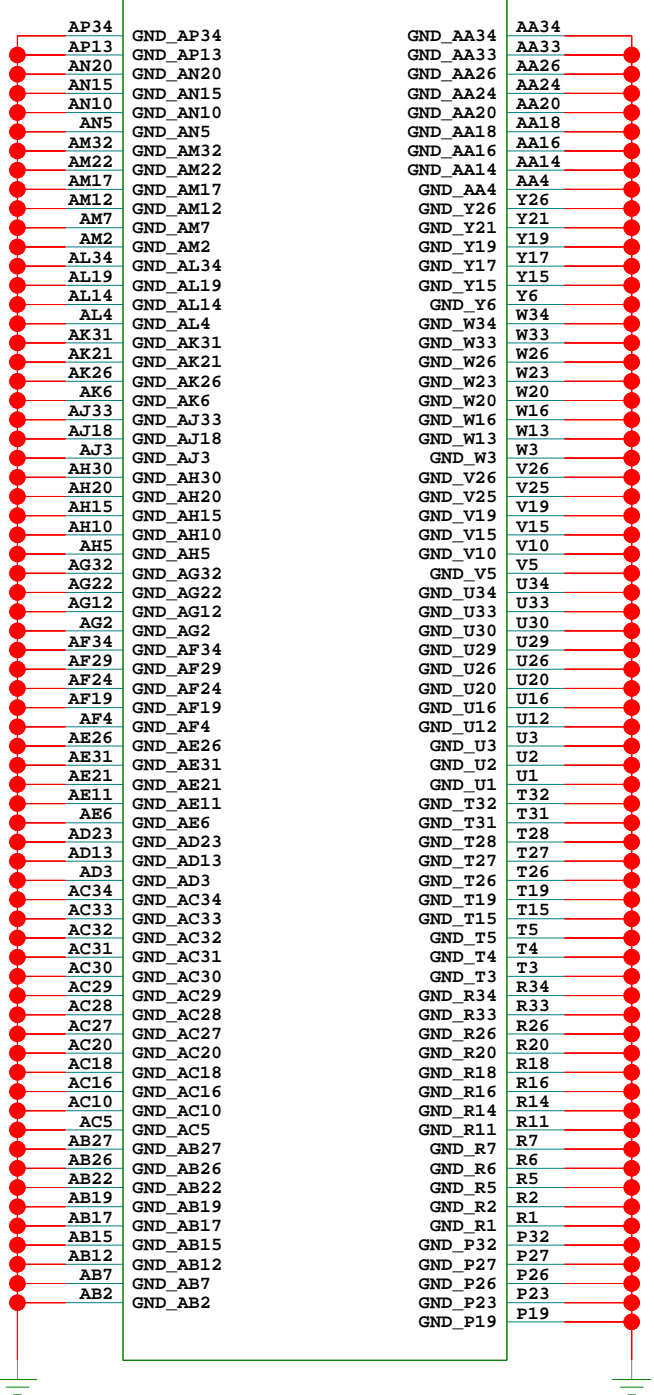
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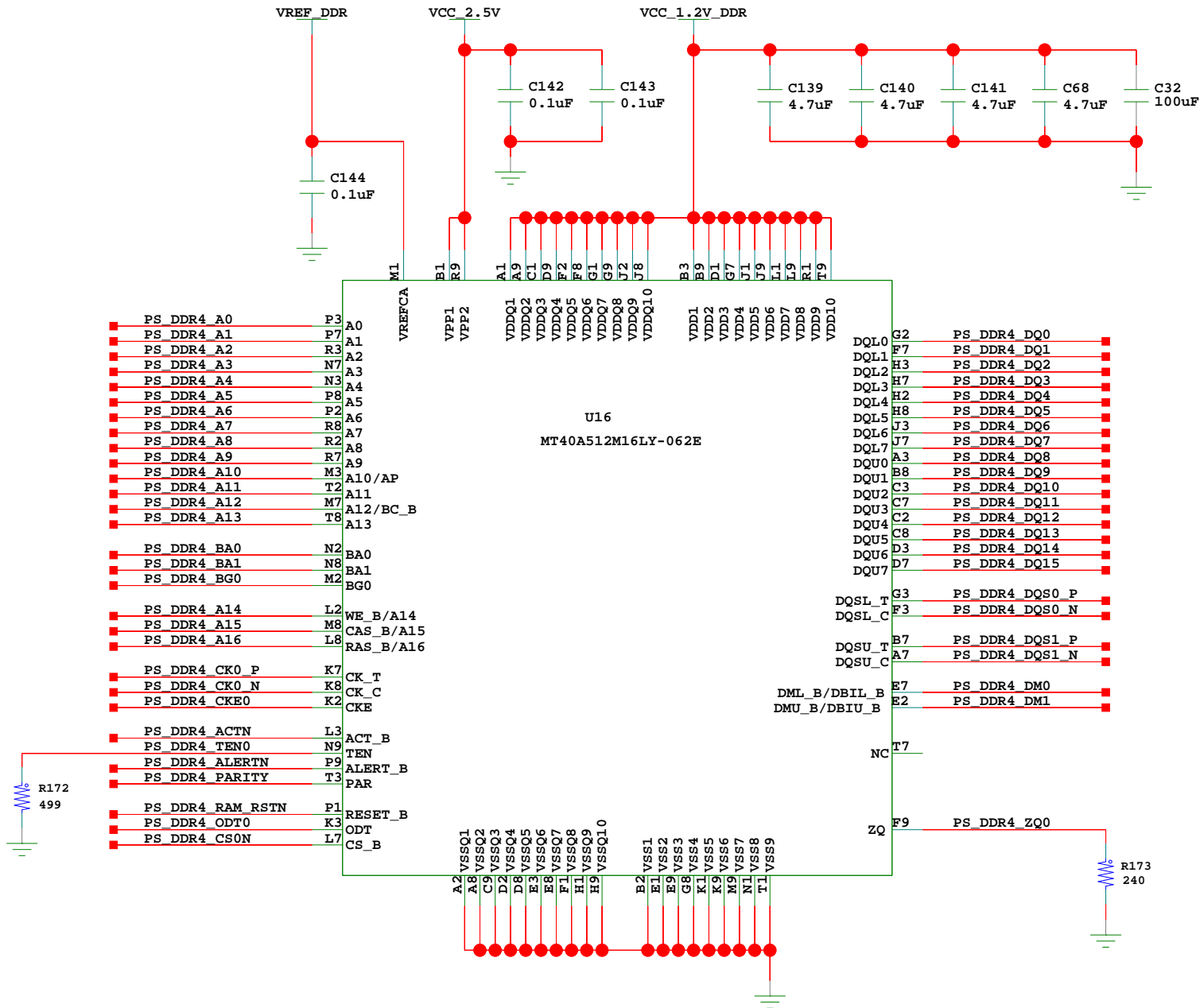
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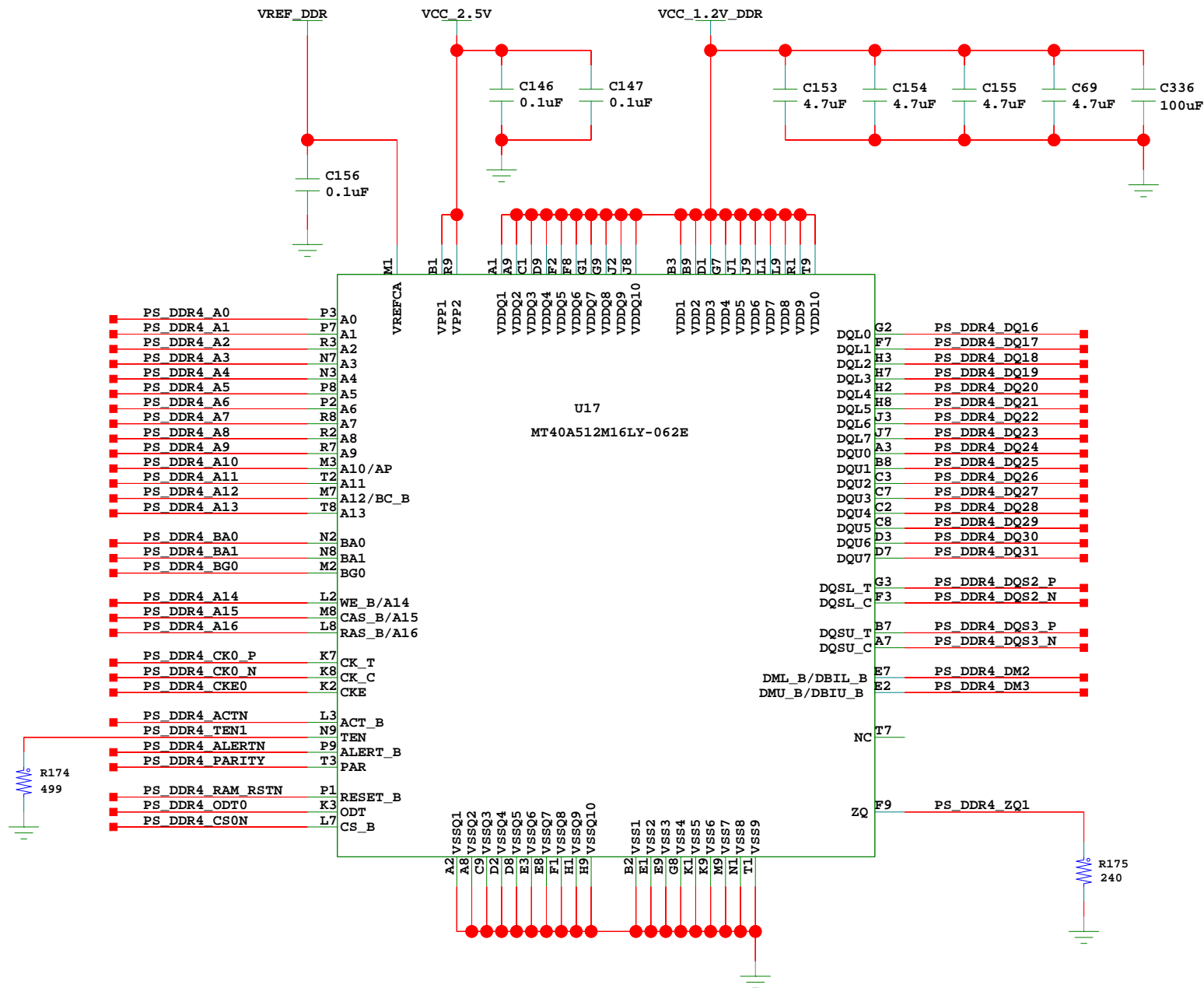
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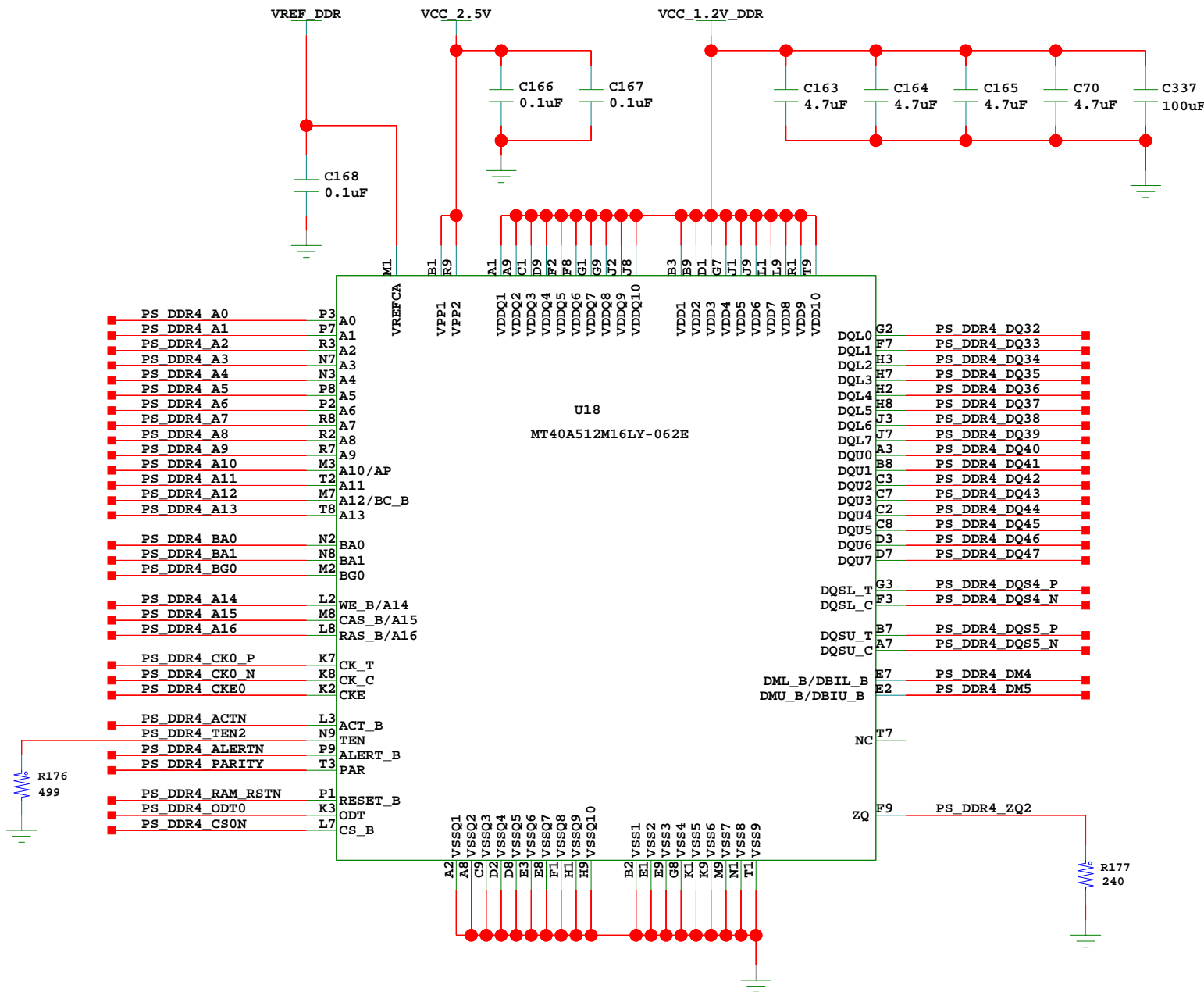
PS DDR4 Device 0



PS DDR4 Device 1

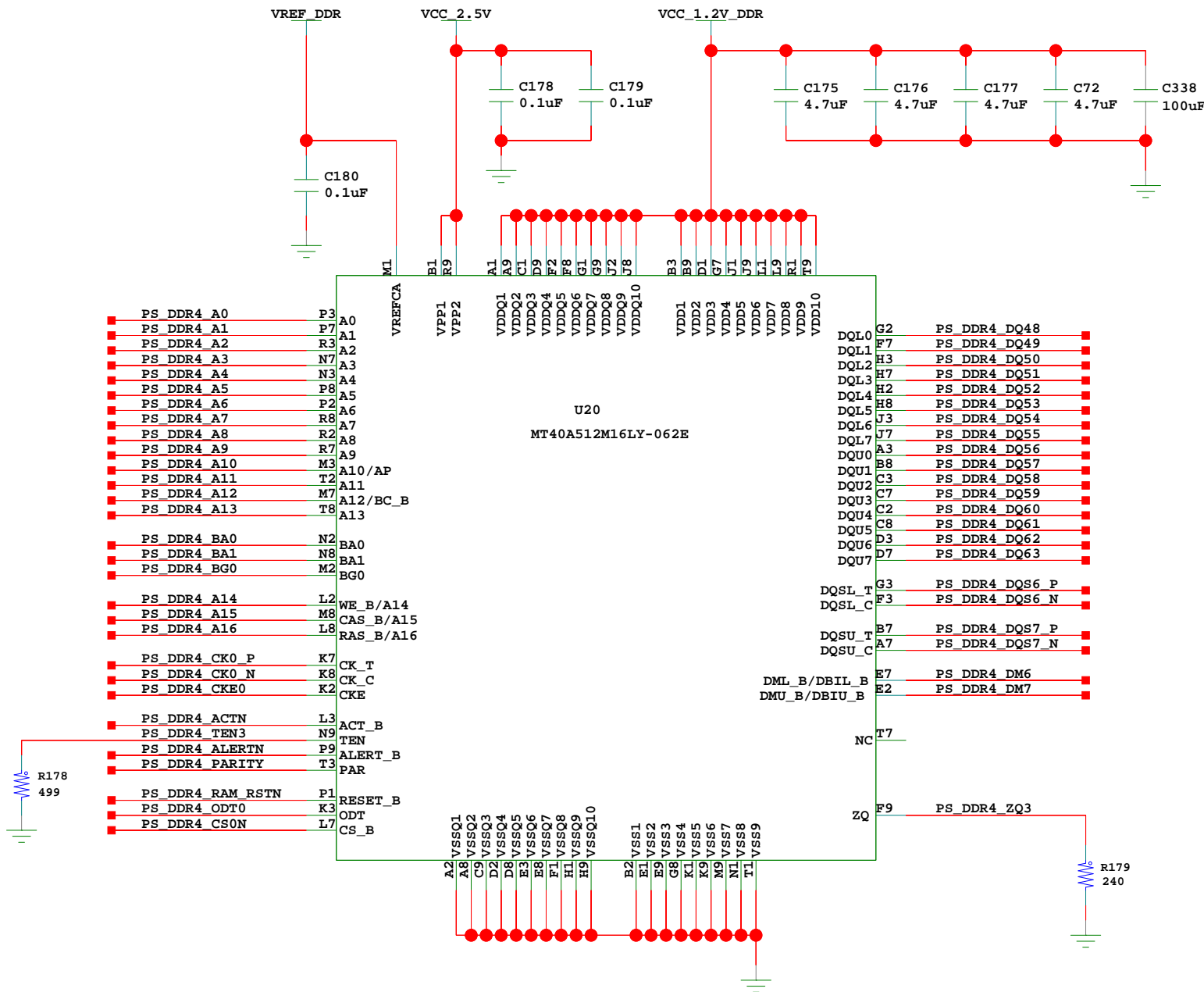


PS DDR4 Device 2

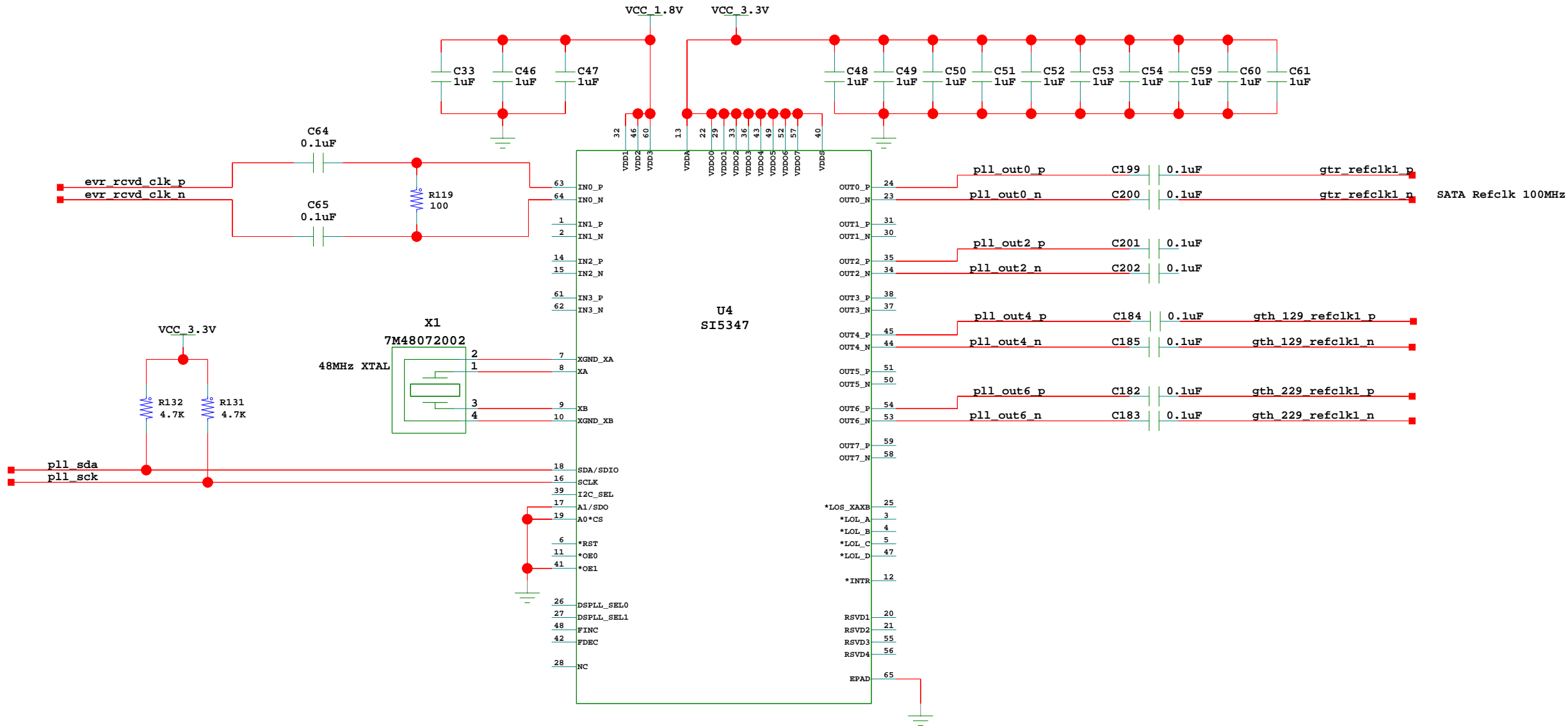




PS DDR4 Device 3



PLL Clock Generator



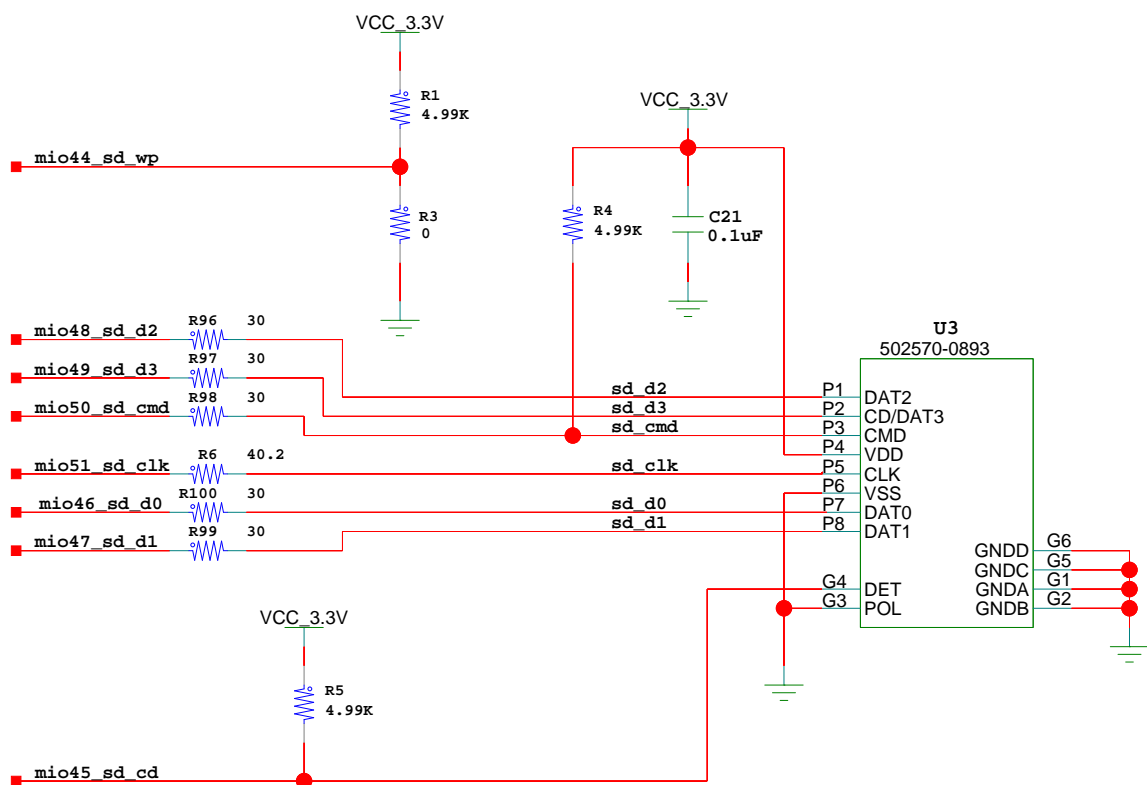
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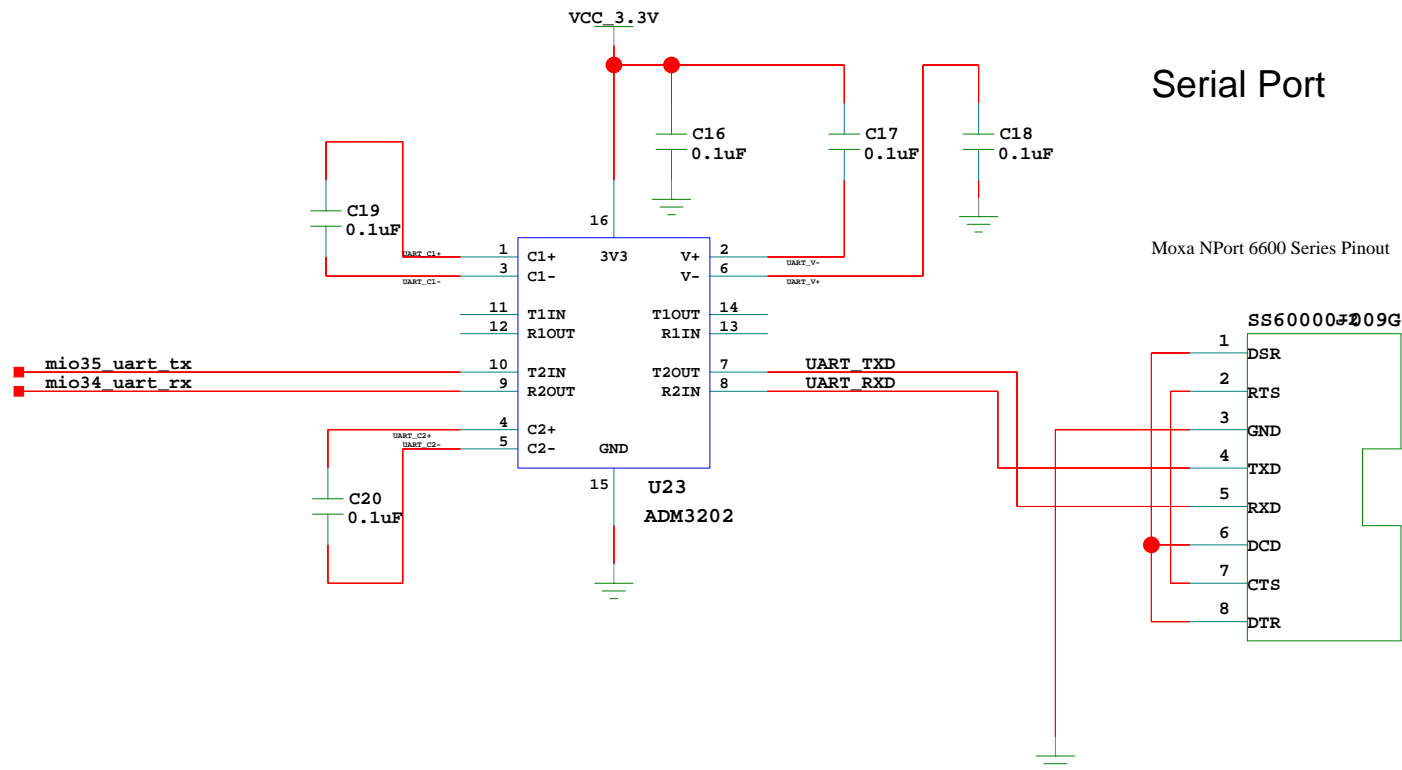
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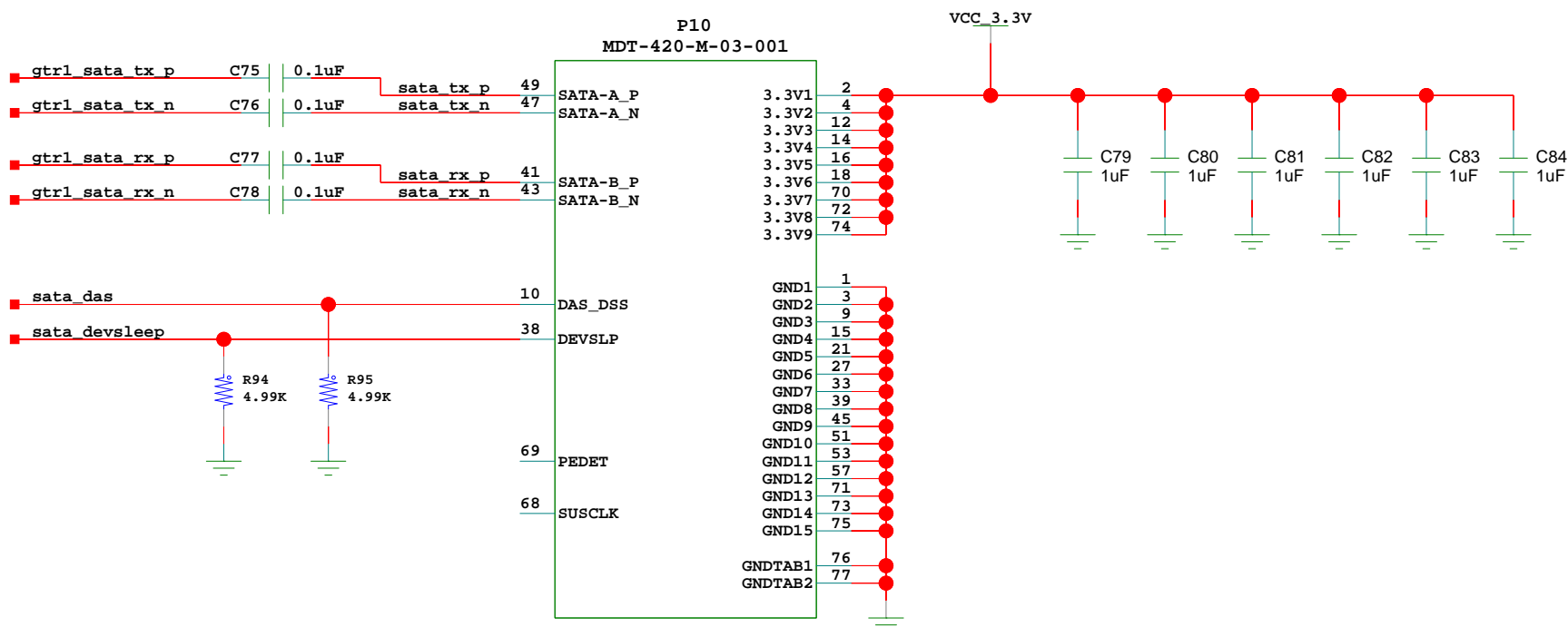
## SD card



## Serial Port



## M.2 SATA



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SHEET SIZE	DRAWING/PART NUMBER	REVISION
ESH&Q	RISK LEVEL A-3	SHEET 16 OF 31

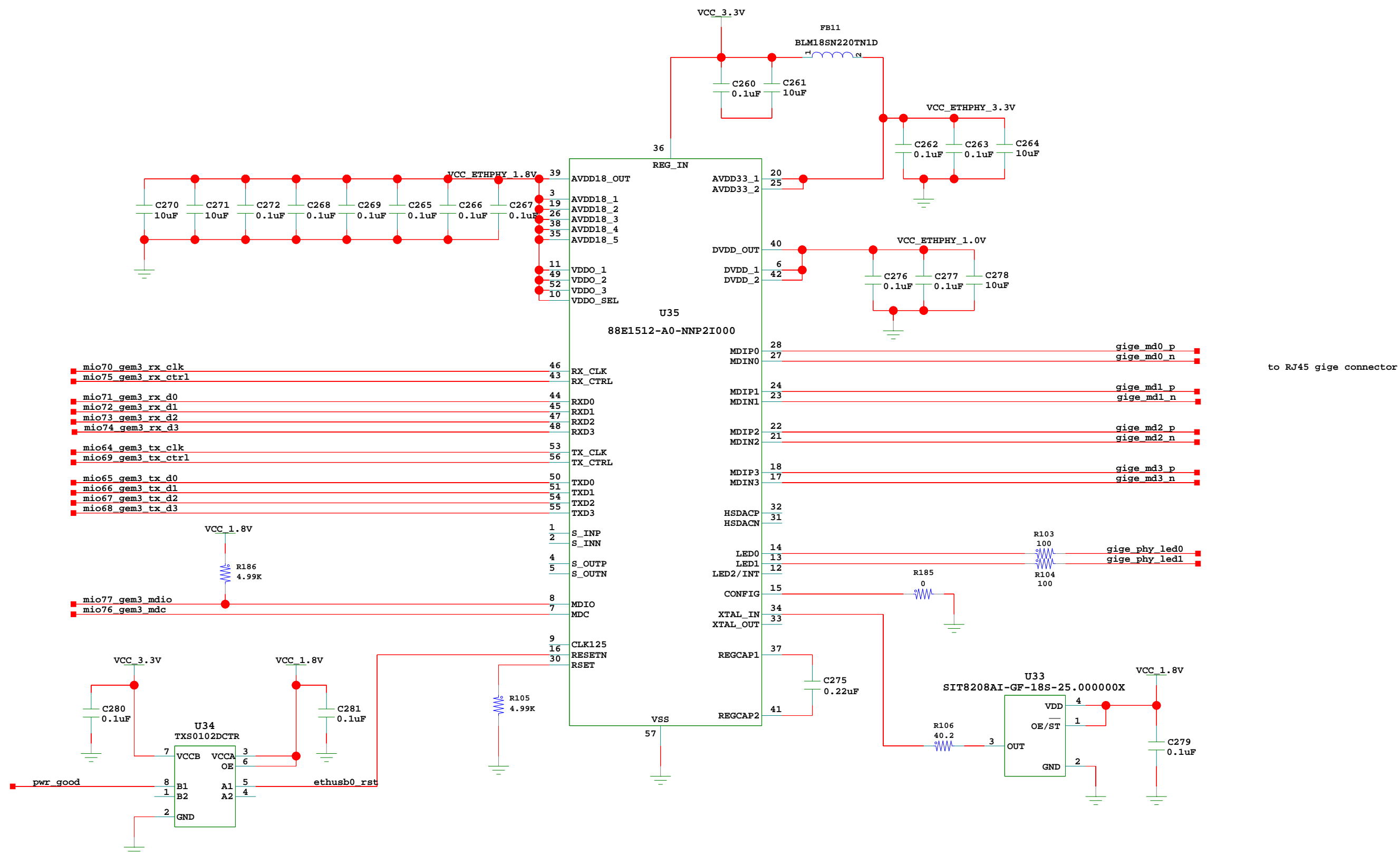
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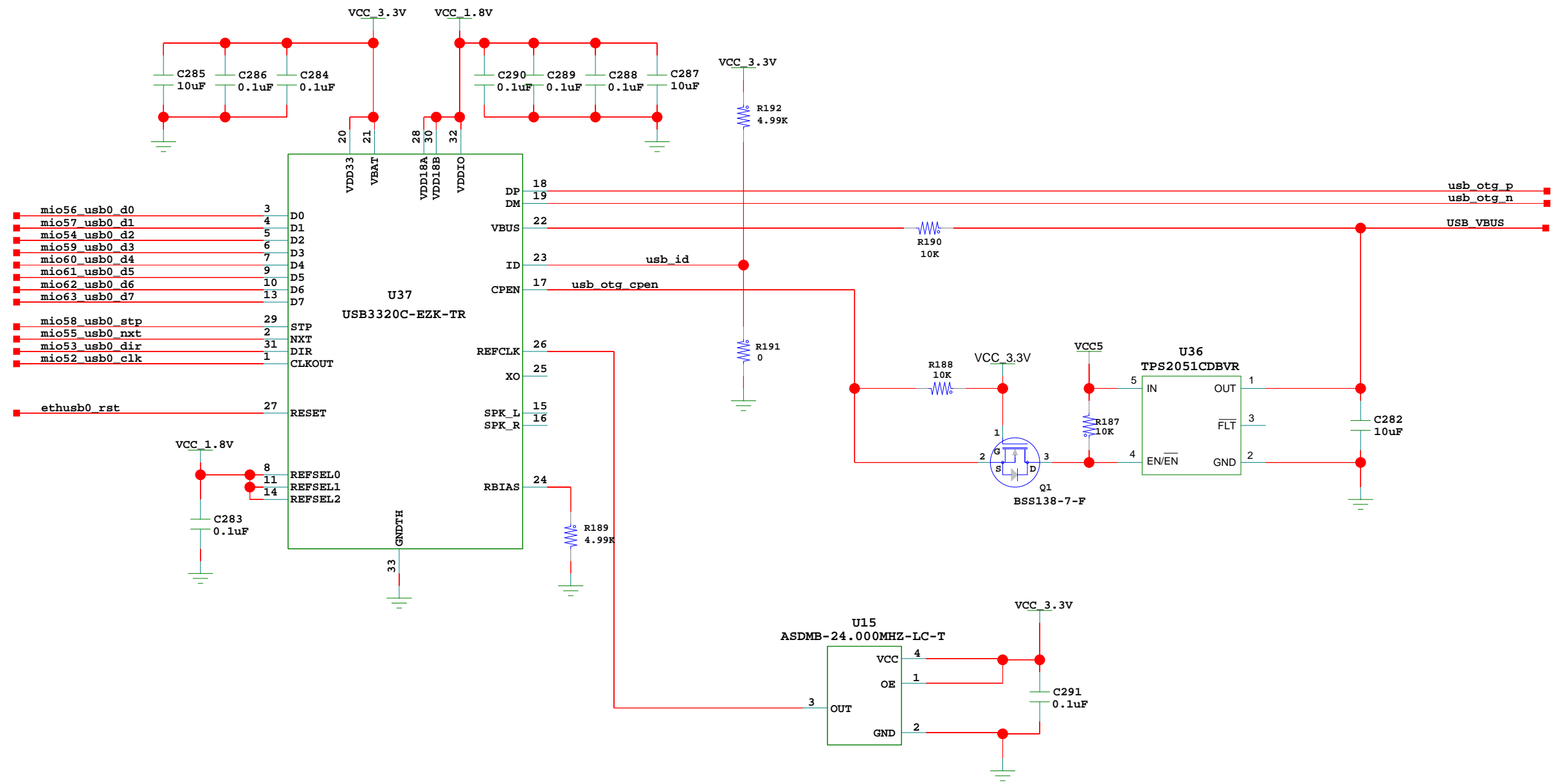
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## Gigabit Ethernet PHY



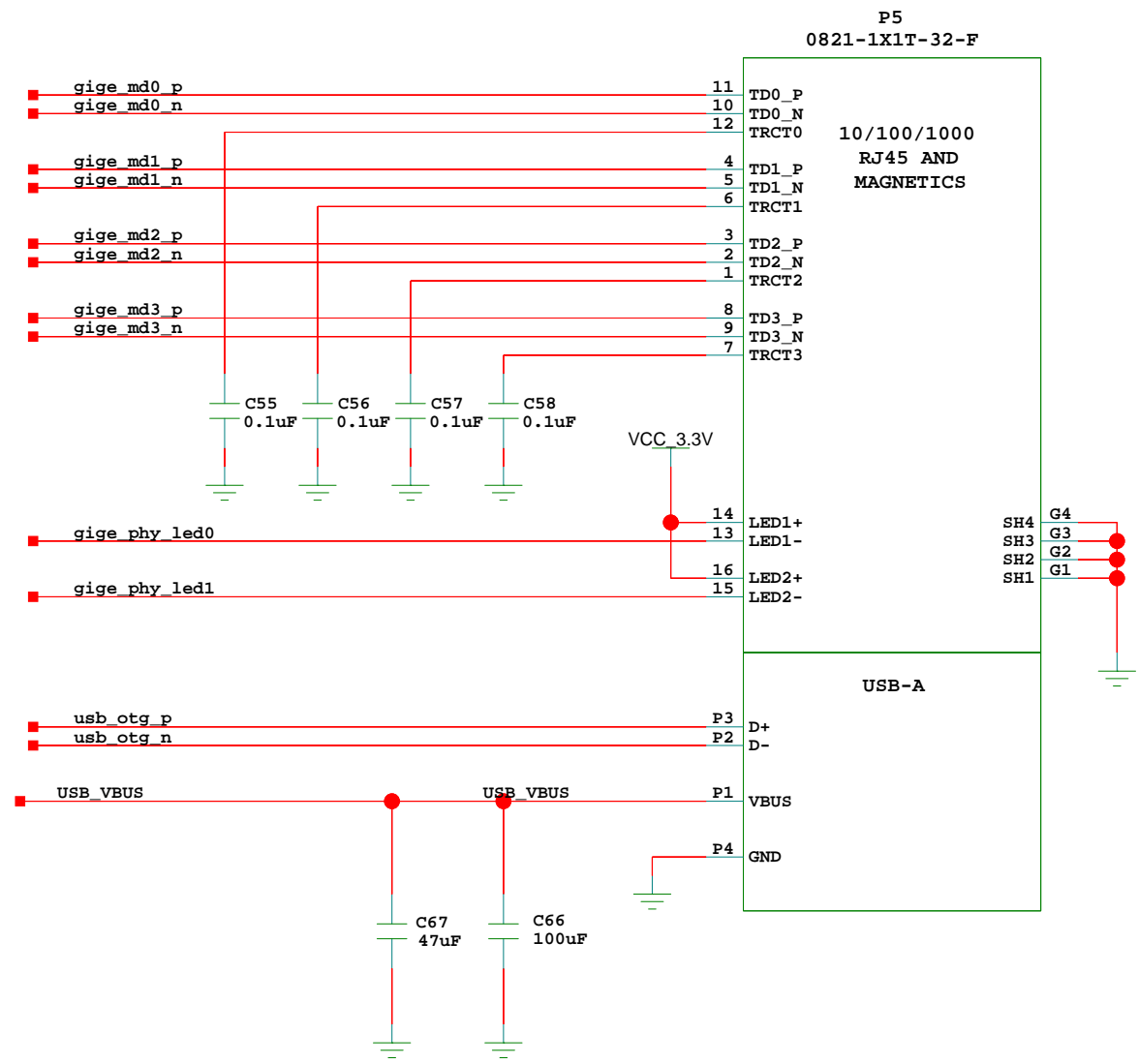
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SHEET SIZE	DRAWING/PART NUMBER	REVISION
<b>ESH&amp;Q</b> <b>RISK LEVEL A-3</b>		SHEET <b>17</b> OF <b>31</b>

USB PHY





Gigabit Ethernet / USB Connector



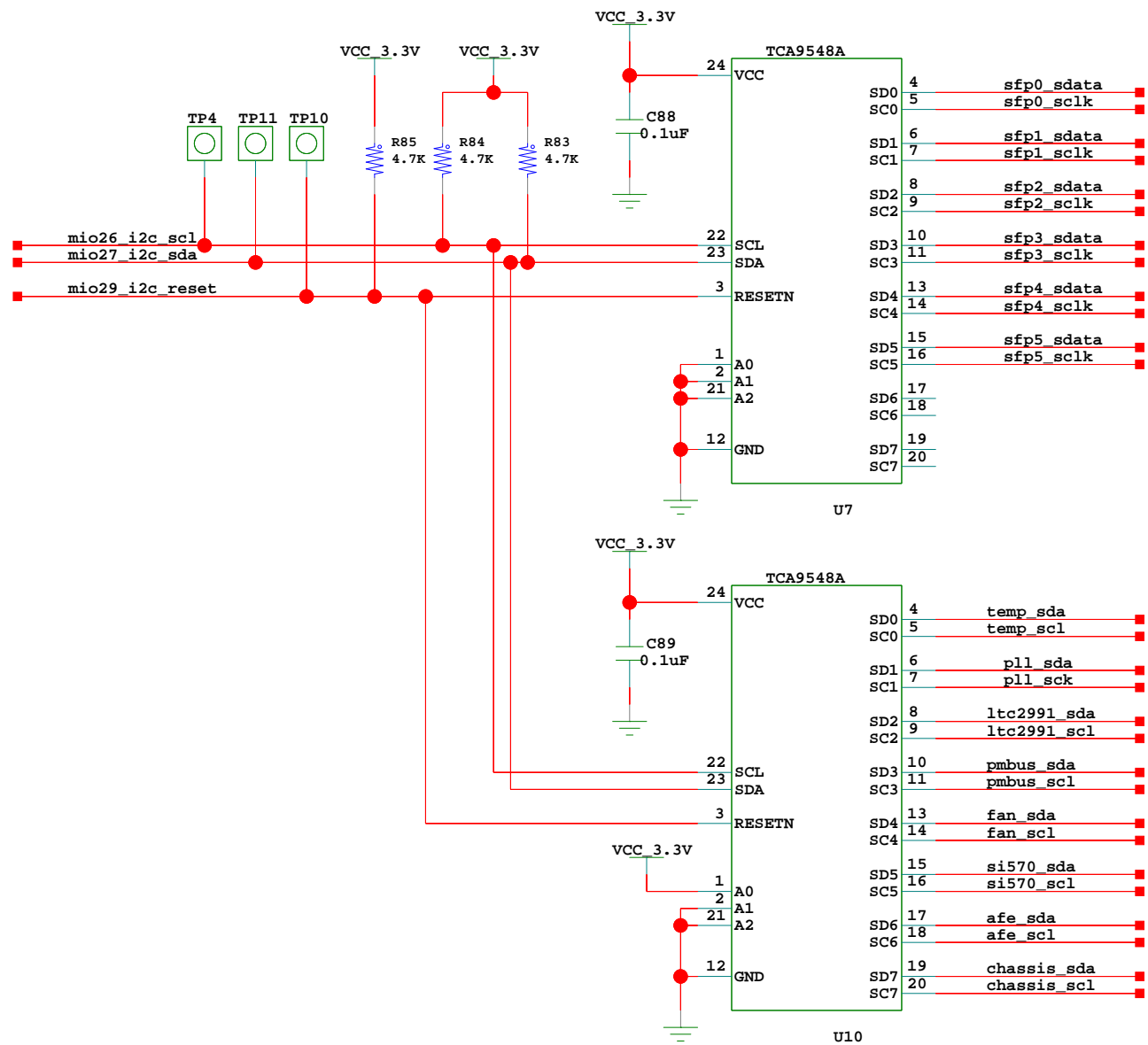
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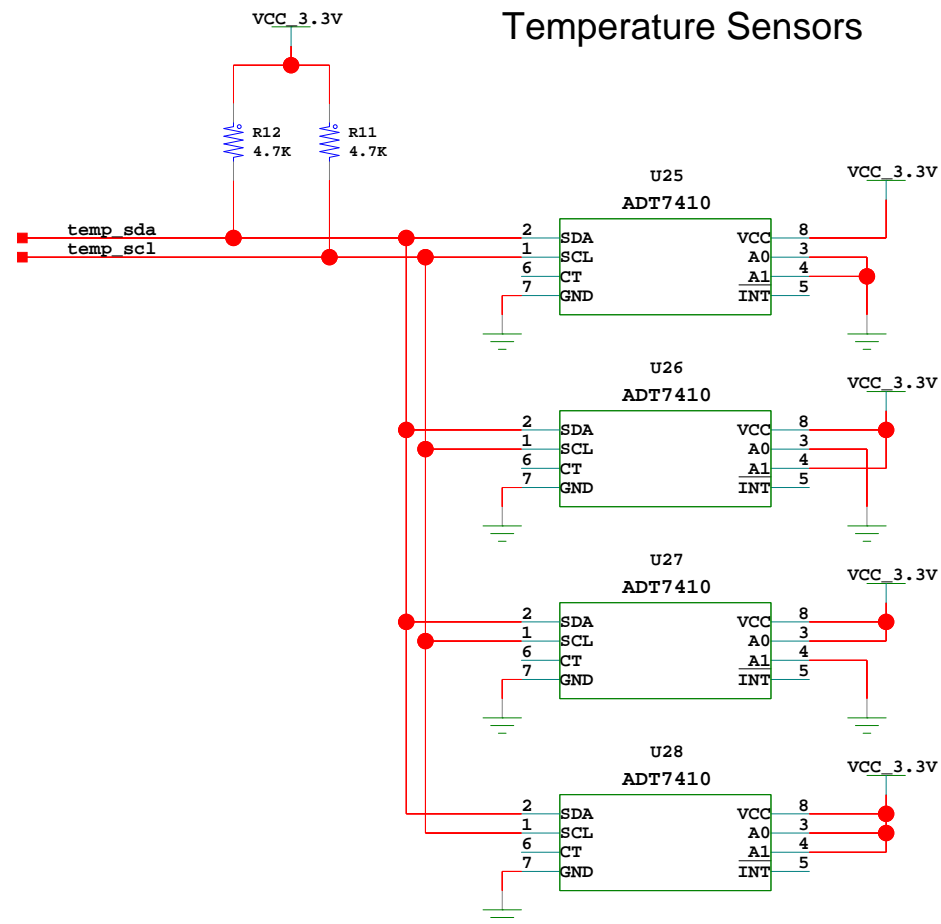
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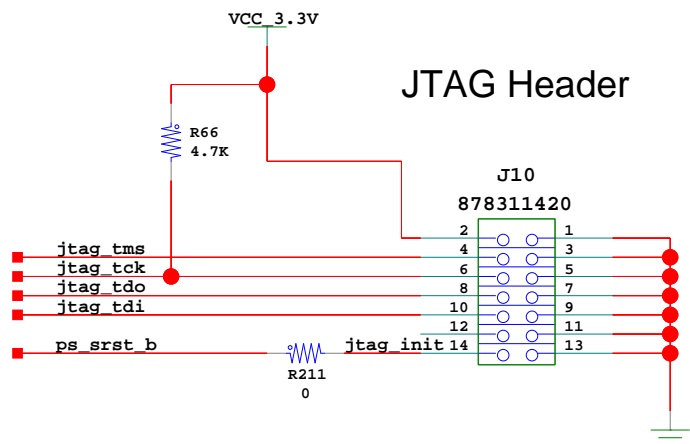
## i2c expander



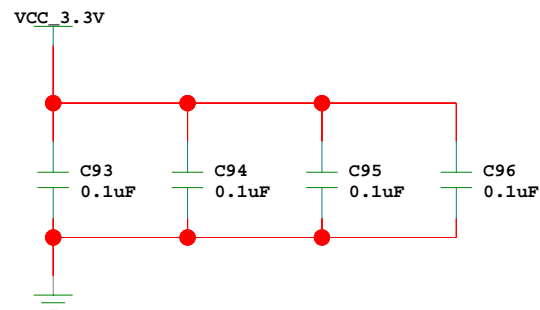
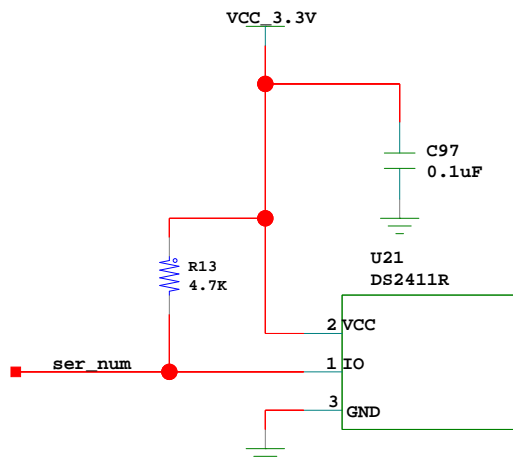
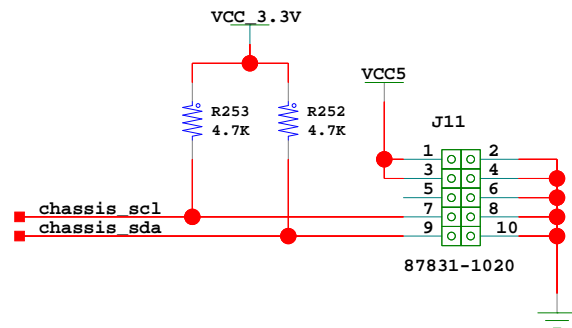
## Temperature Sensors



## JTAG Header



## Chassis Fan Header



B

LT-EL-SR-EU-BPM-0614-03

2

SHEET SIZE

DRAWING/PART NUMBER

REVISION

ESH&amp;Q

RISK LEVEL A-3

SHEET 20 OF 31

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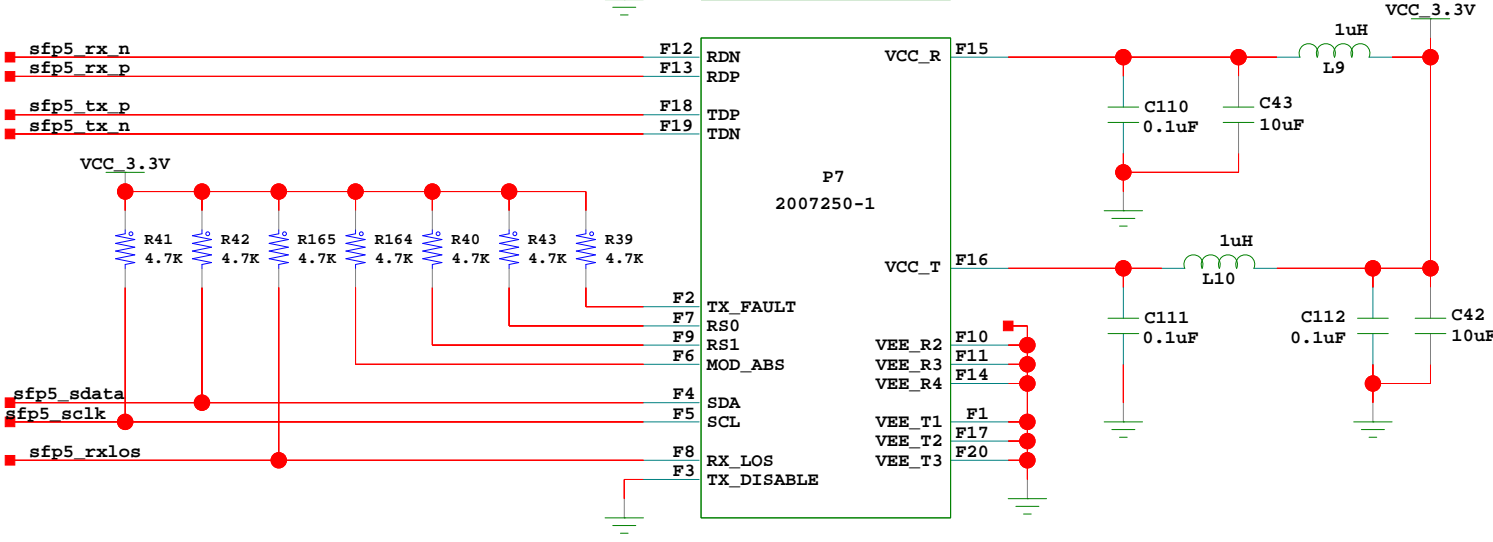
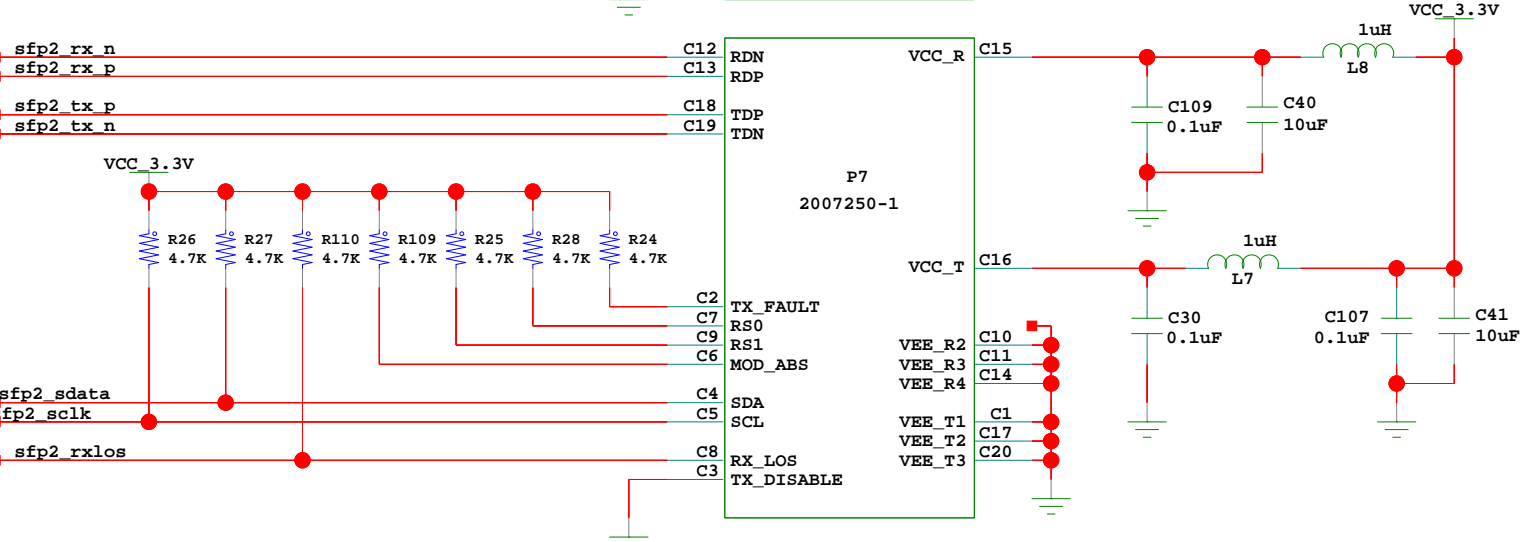
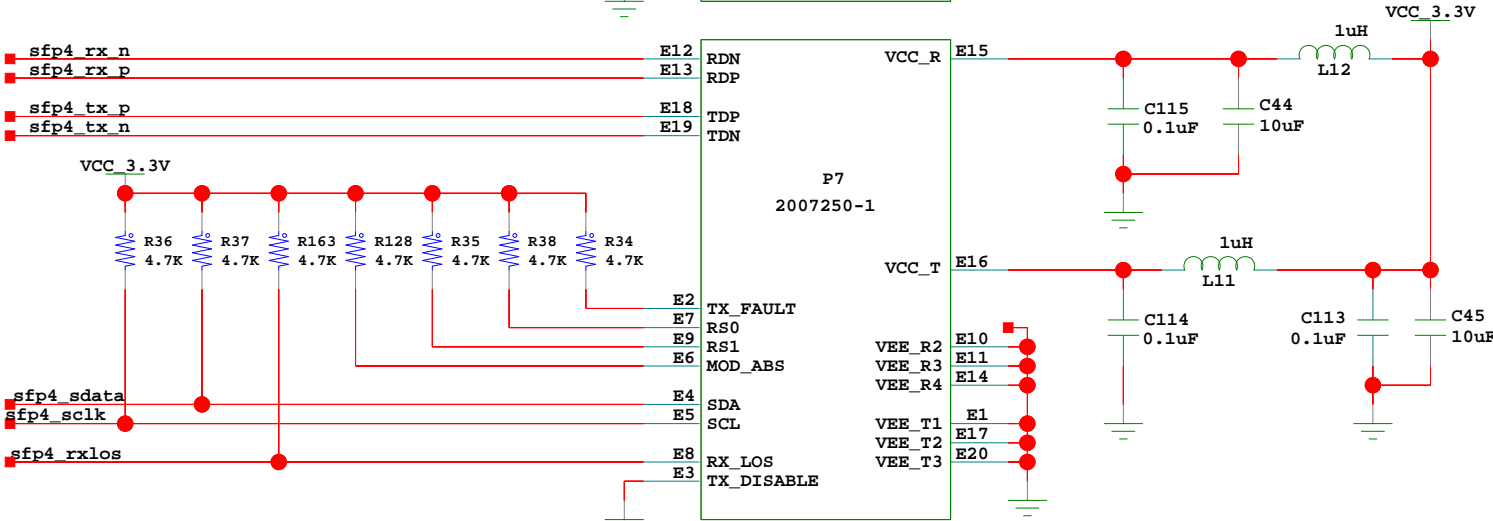
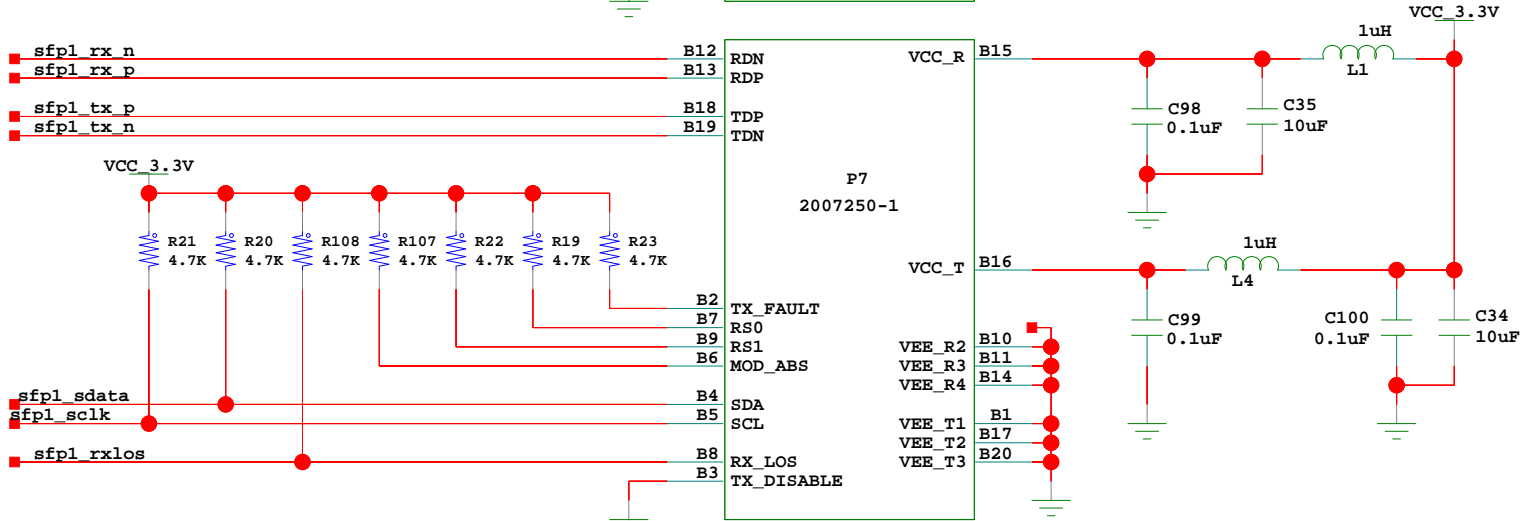
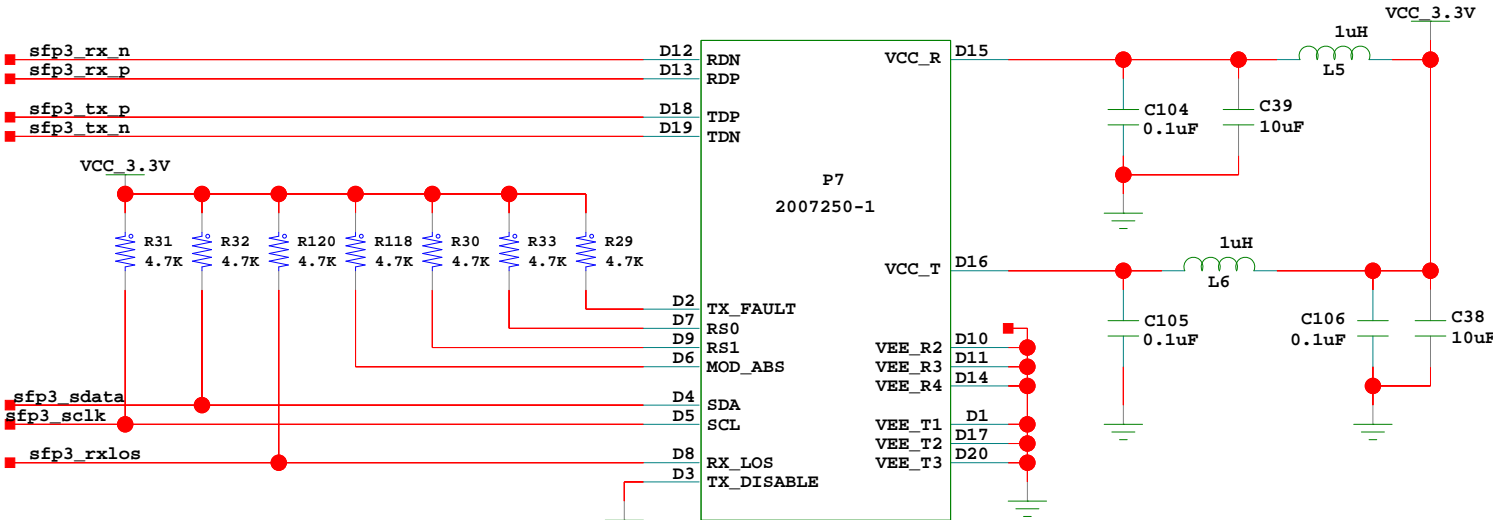
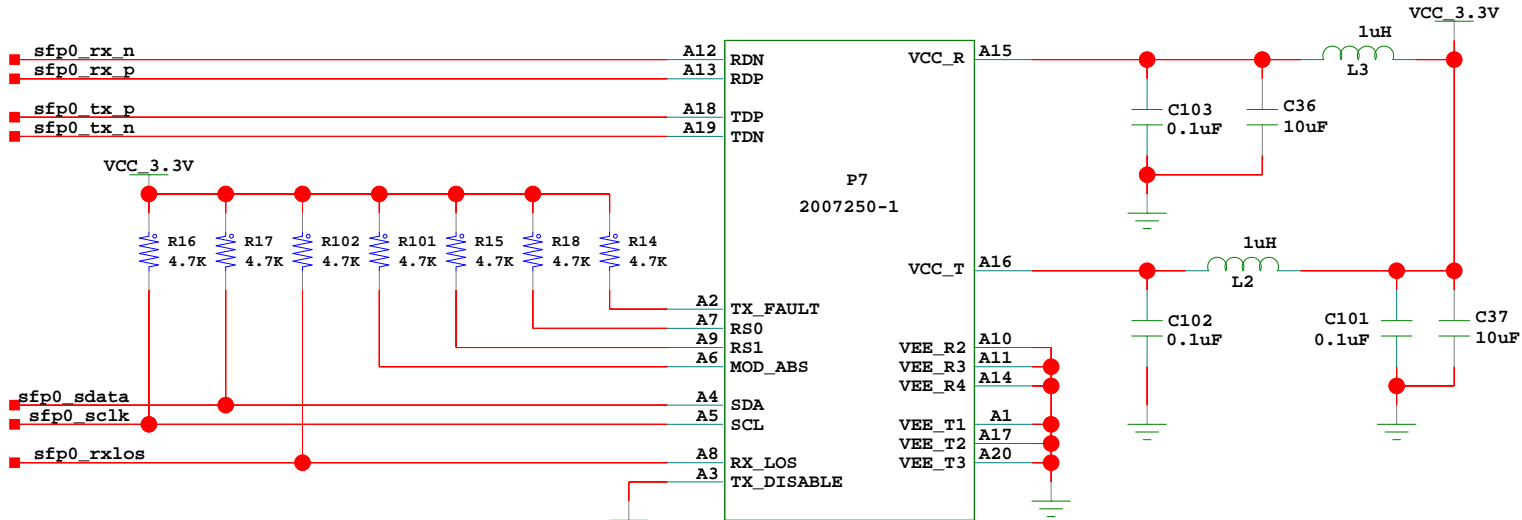
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1

6 gang SFP connector



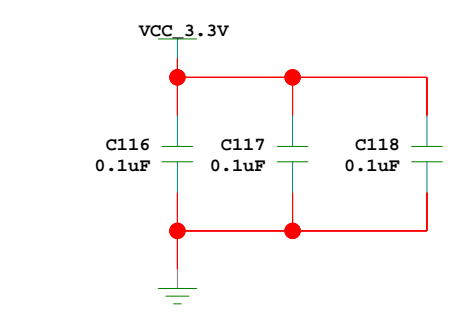
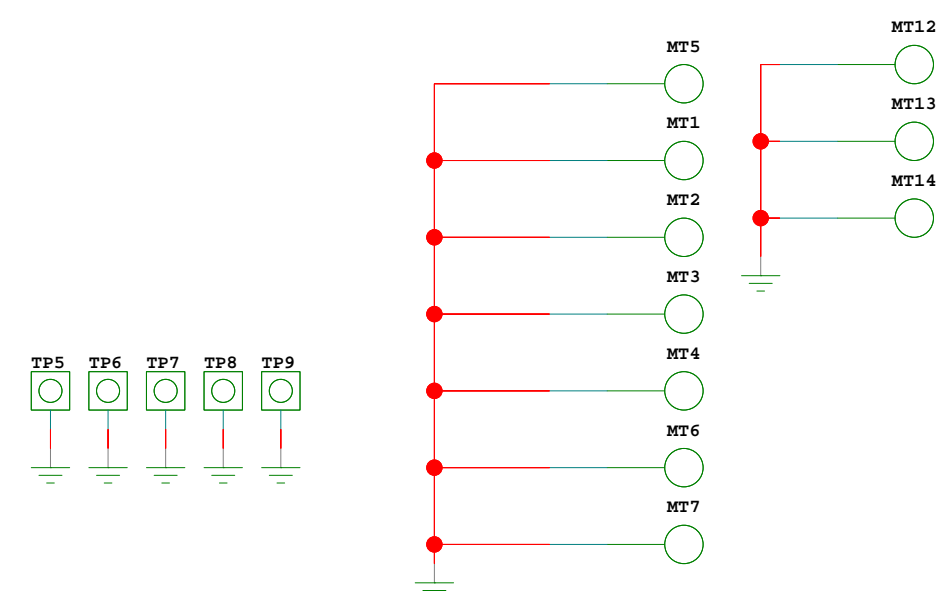
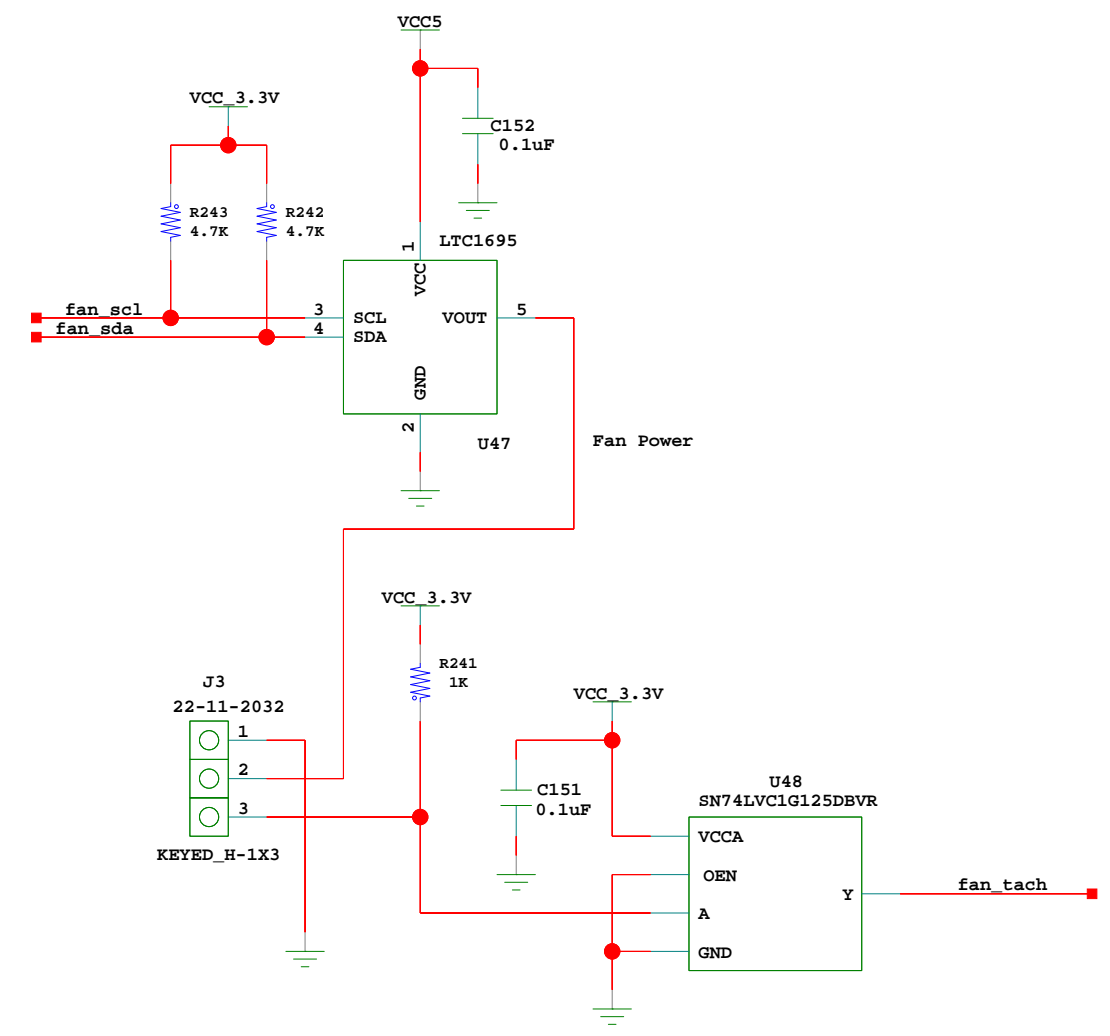
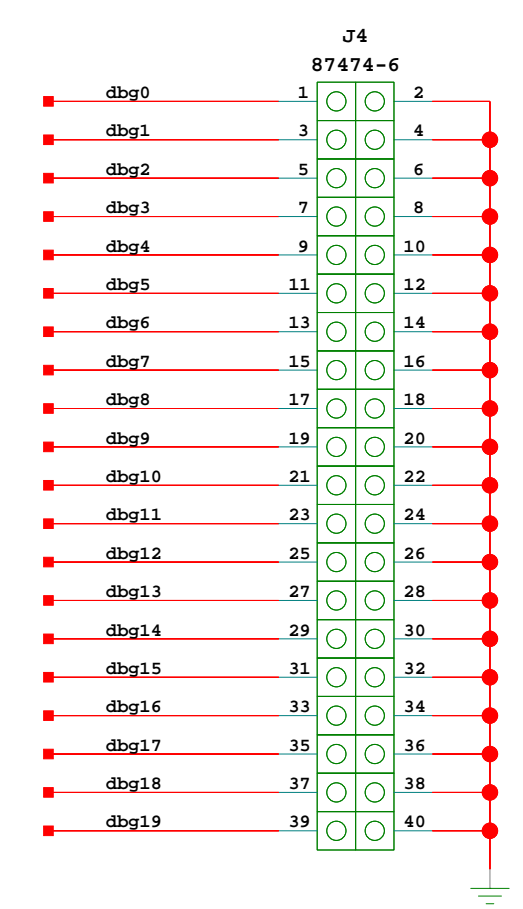
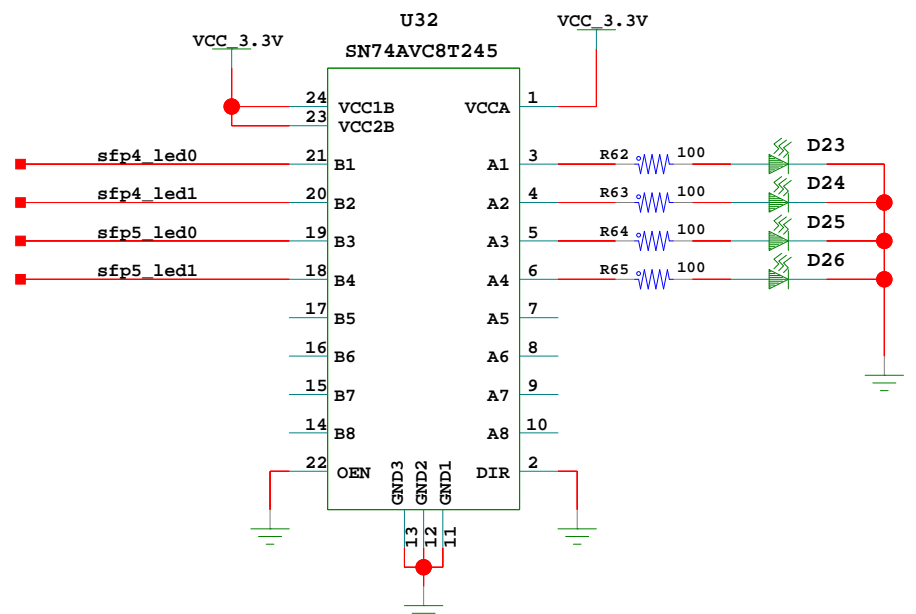
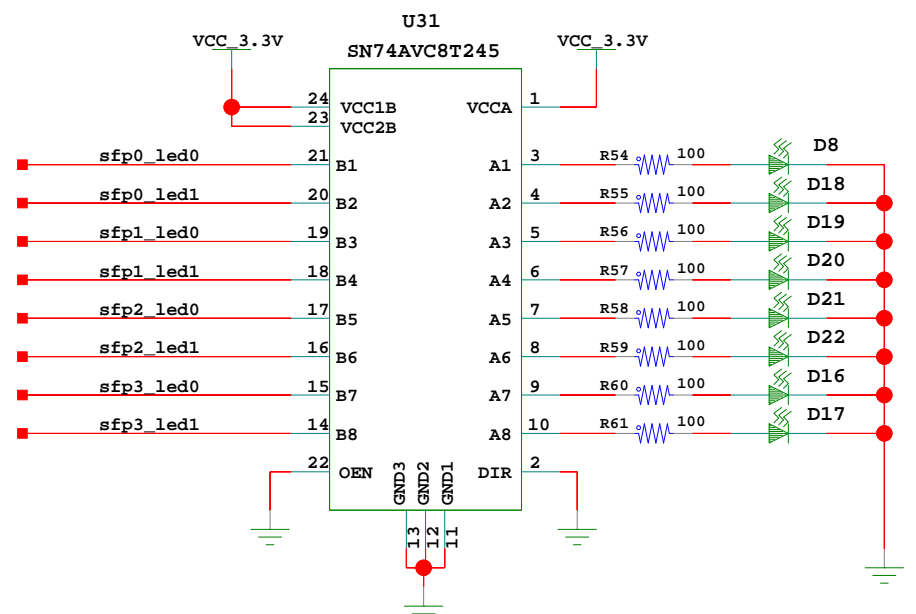
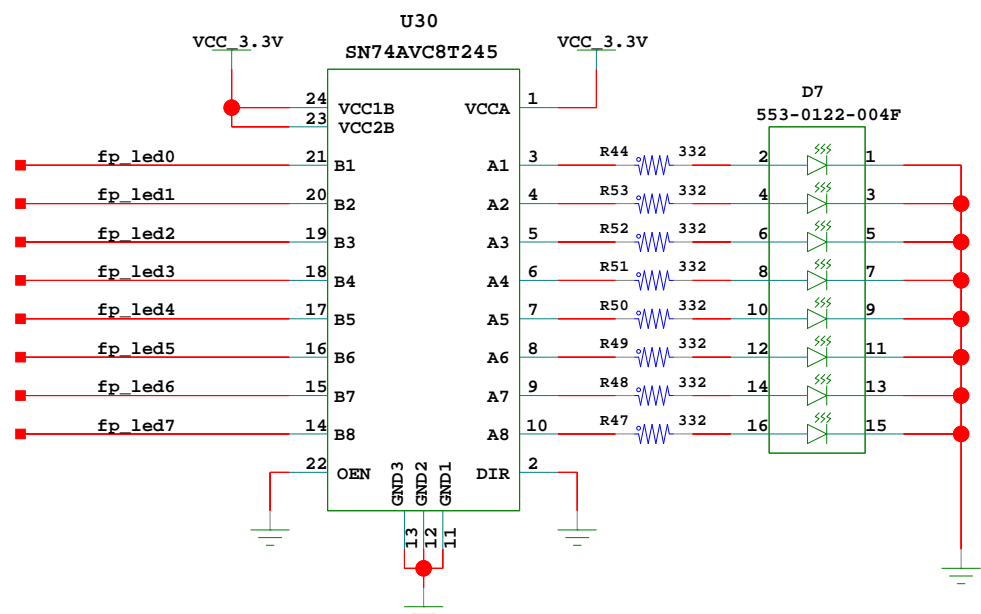
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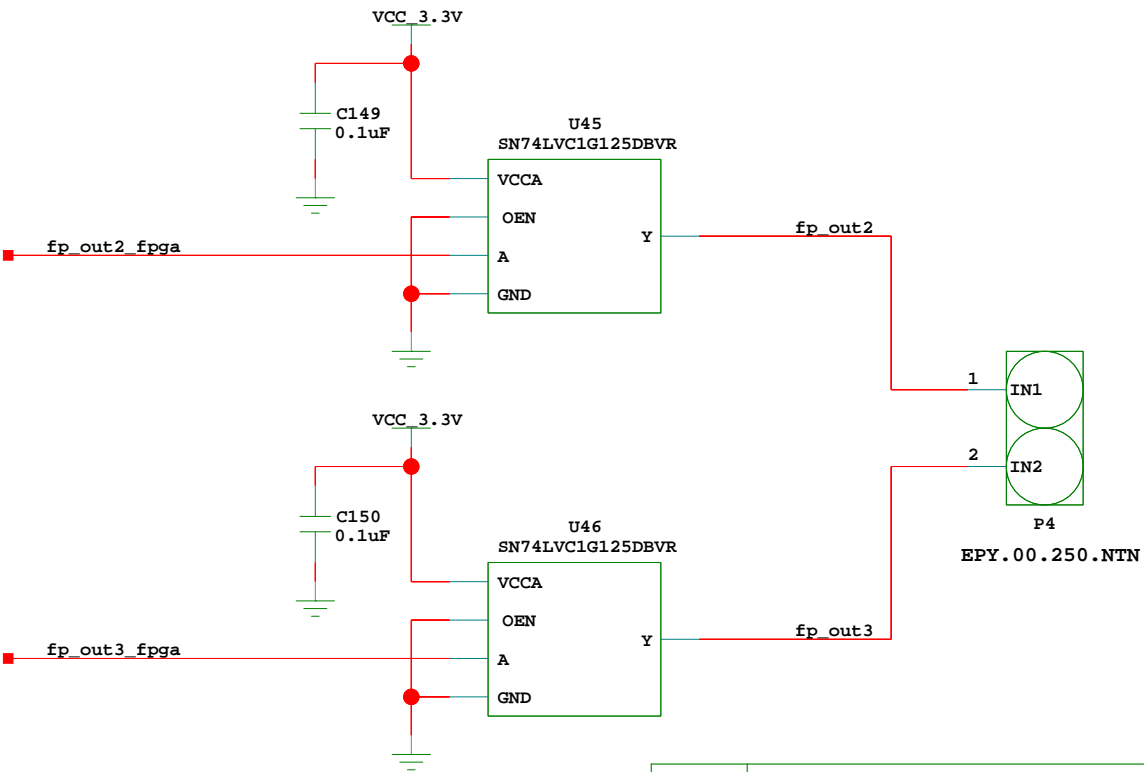
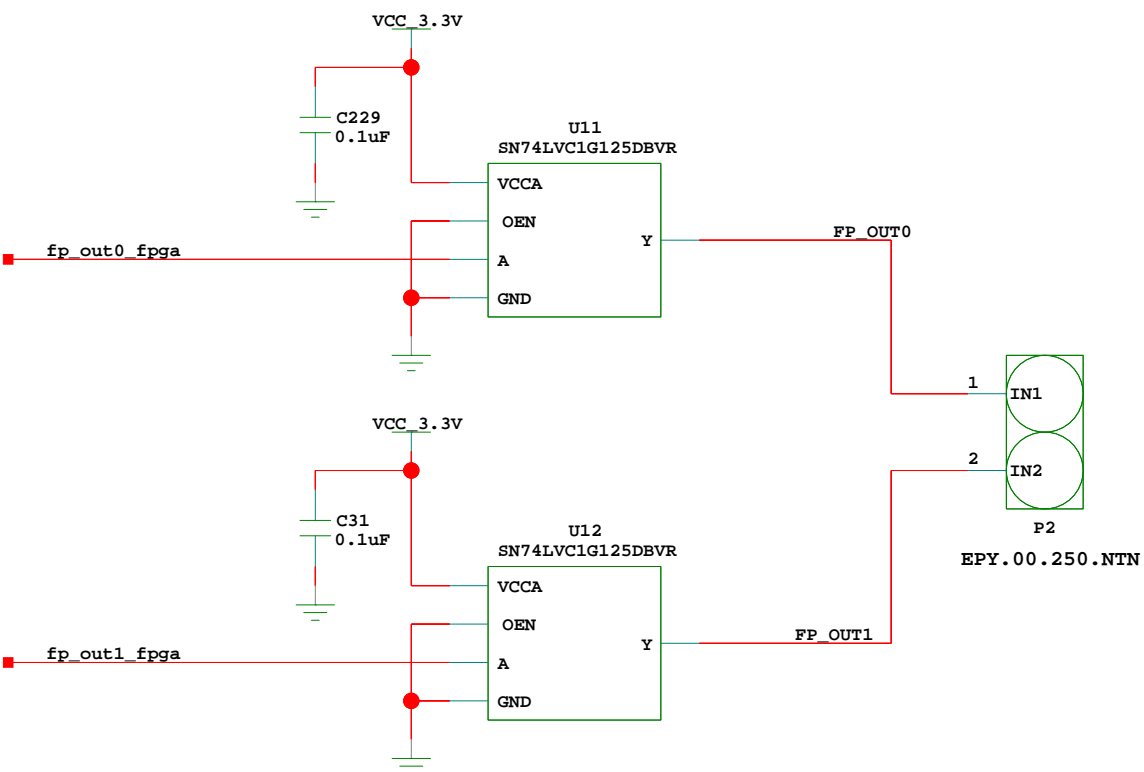
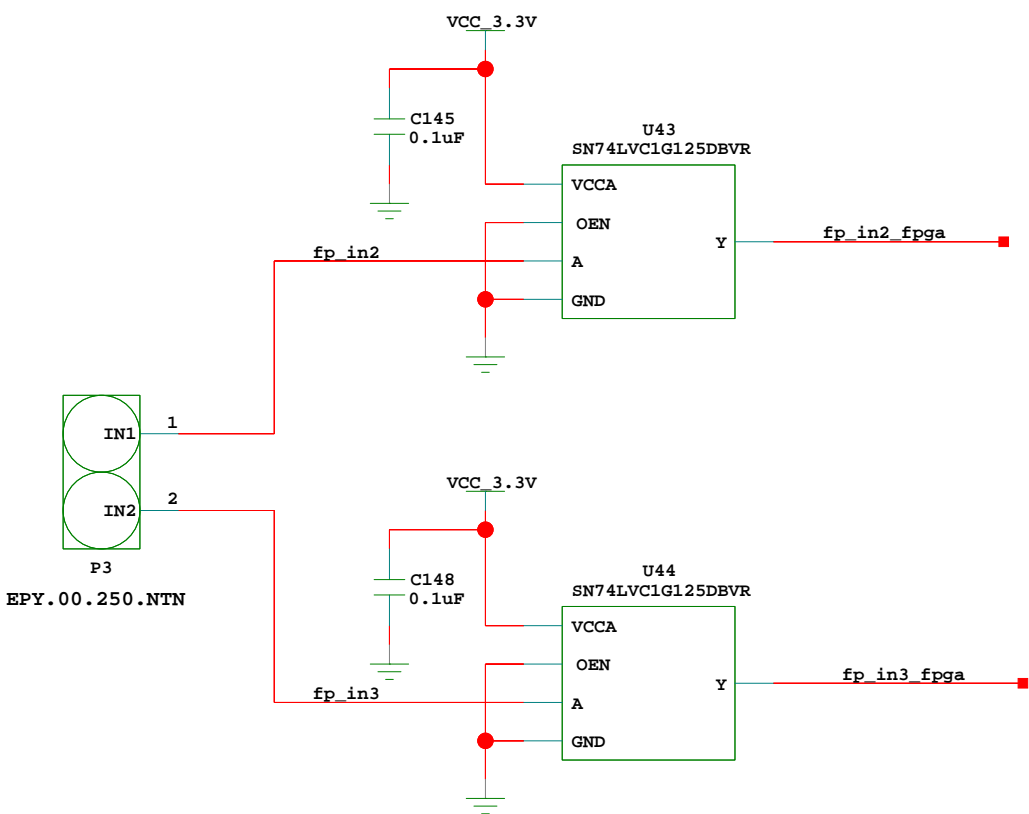
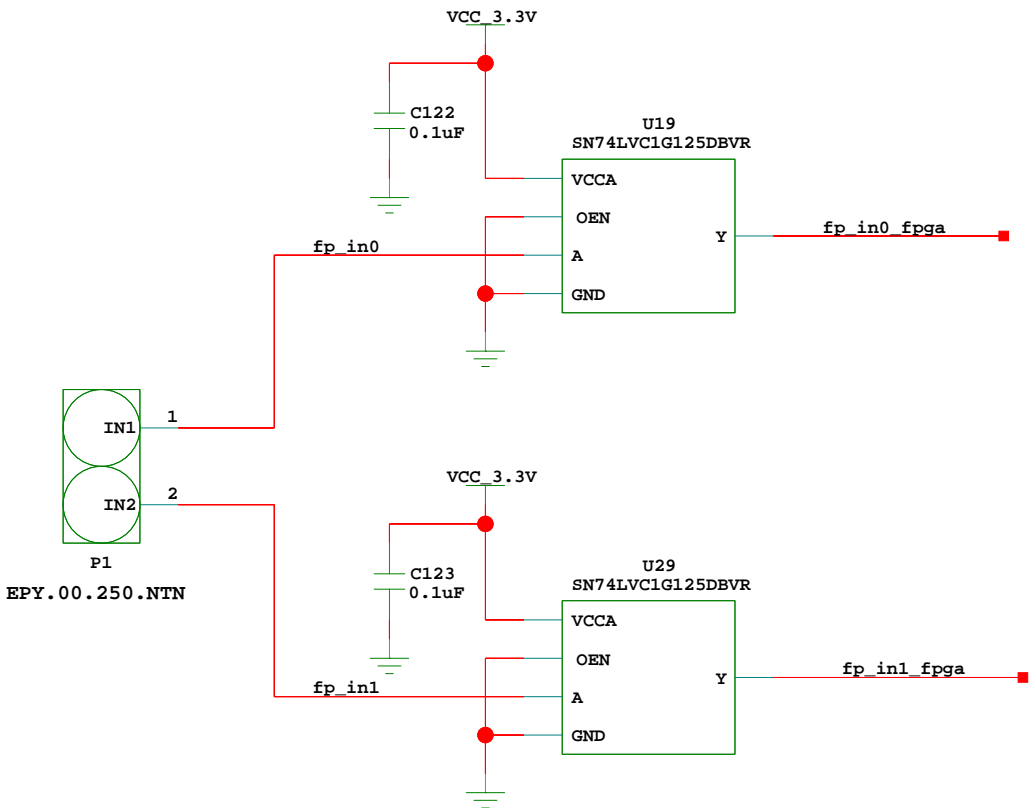
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1

LED's, Debug Header, Fan Speed



Front panel LEMO I/O  
4 inputs, 4 outputs





4

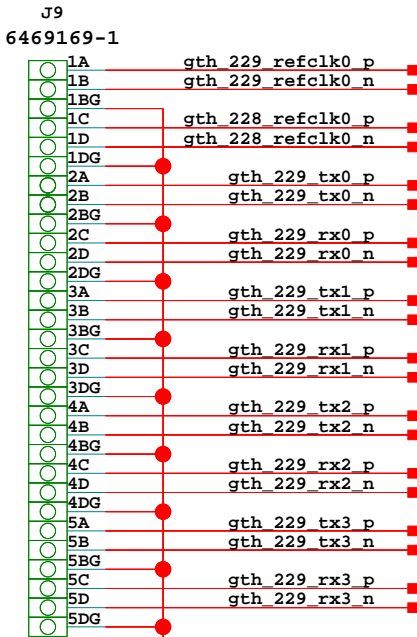
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2

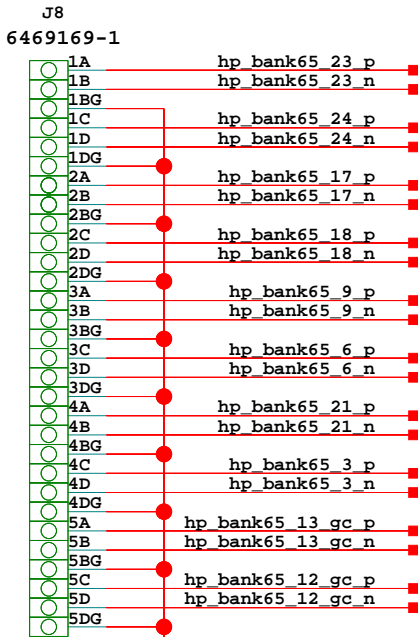
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AFE Connectors

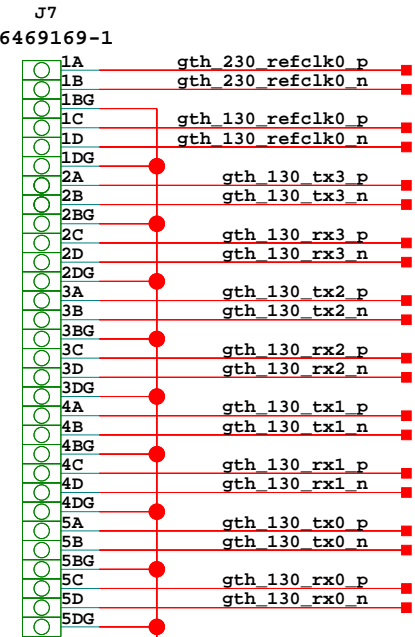
GTH Transceivers



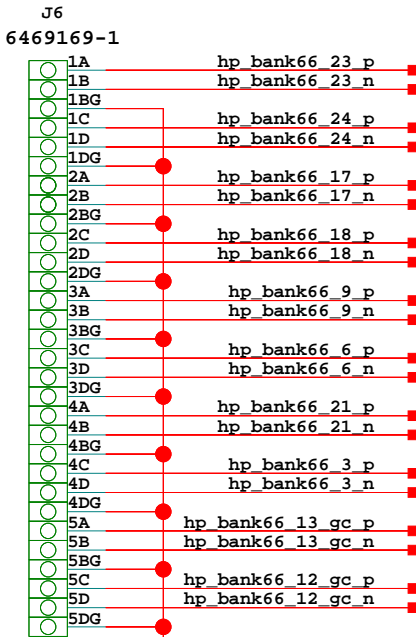
HP I/O (Bank 65)



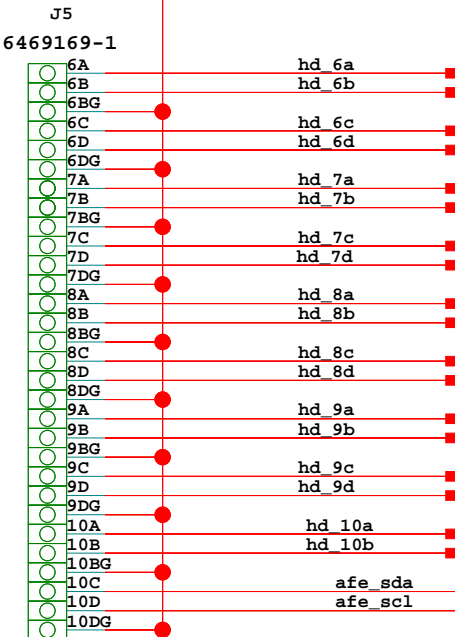
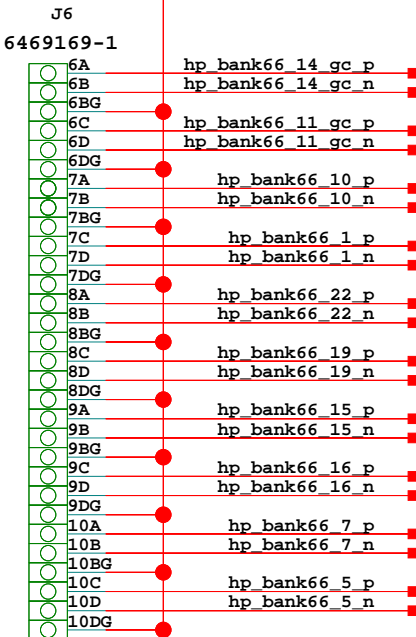
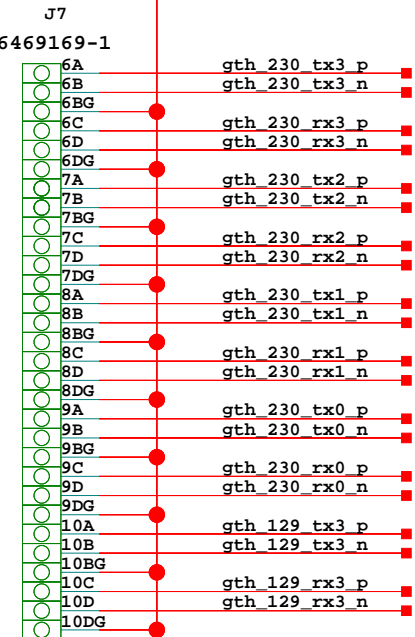
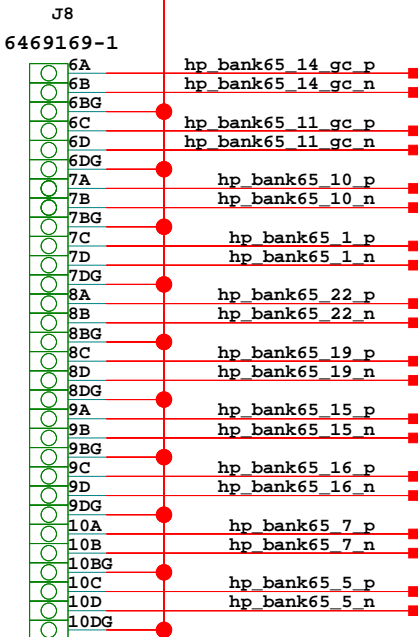
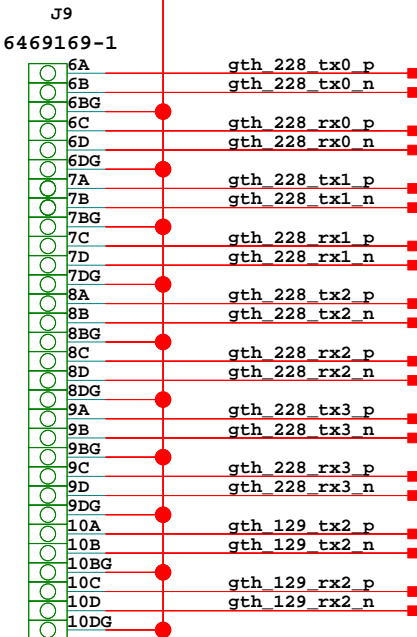
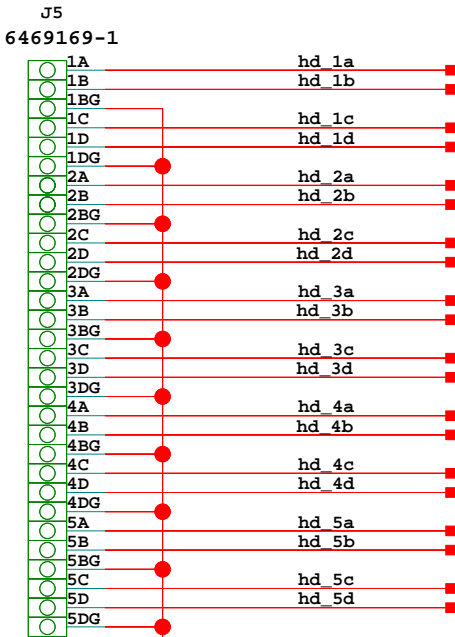
GTH Transceivers



HP I/O (Bank 66)



HD I/O



VCC 3.3V

R244  
4.7K

R245  
4.7K

B

LT-EL-SR-EU-BPM-0614-03

2

SHEET SIZE

DRAWING/PART NUMBER

REVISION

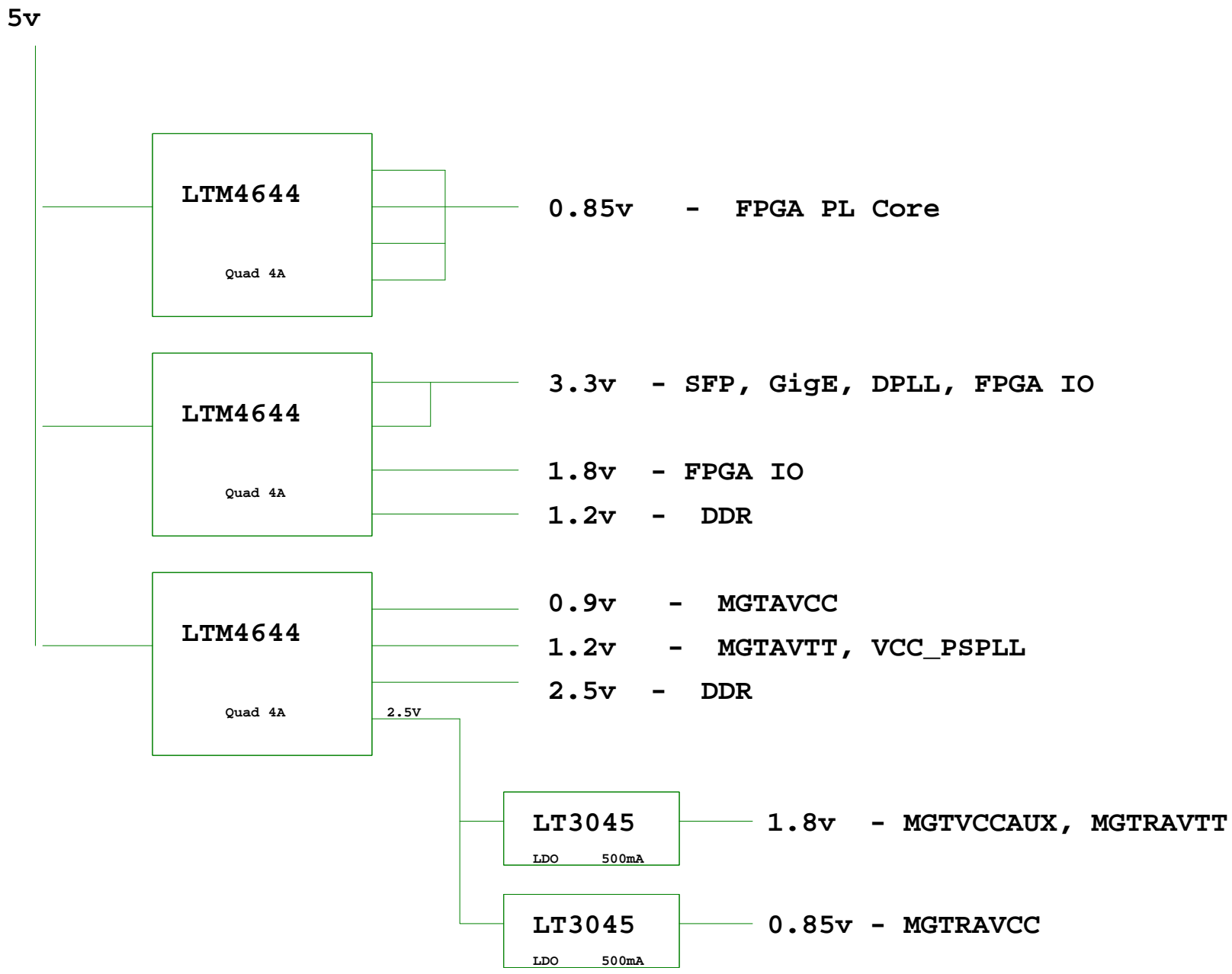
ESH&Q

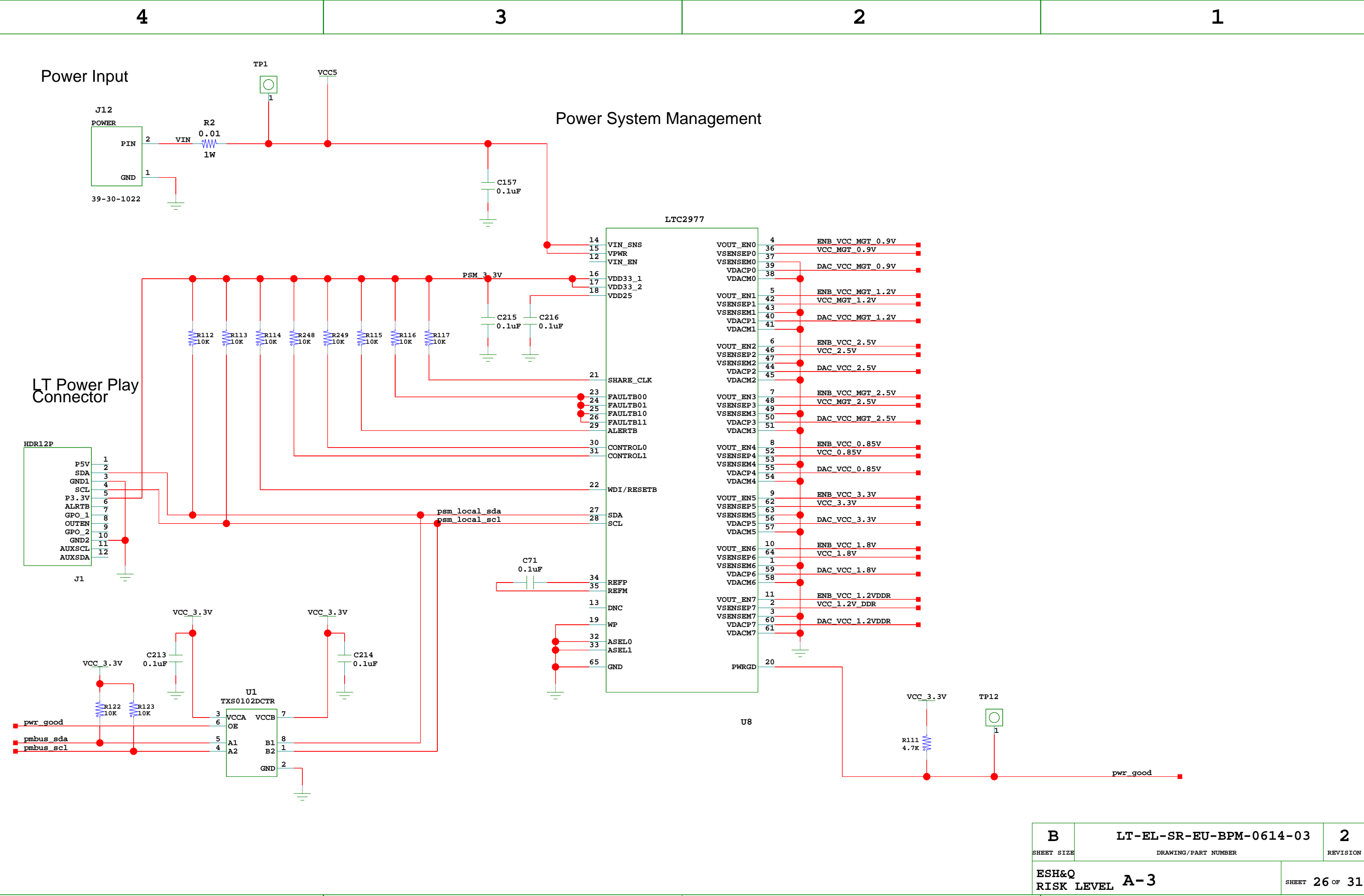
RISK LEVEL

A-3

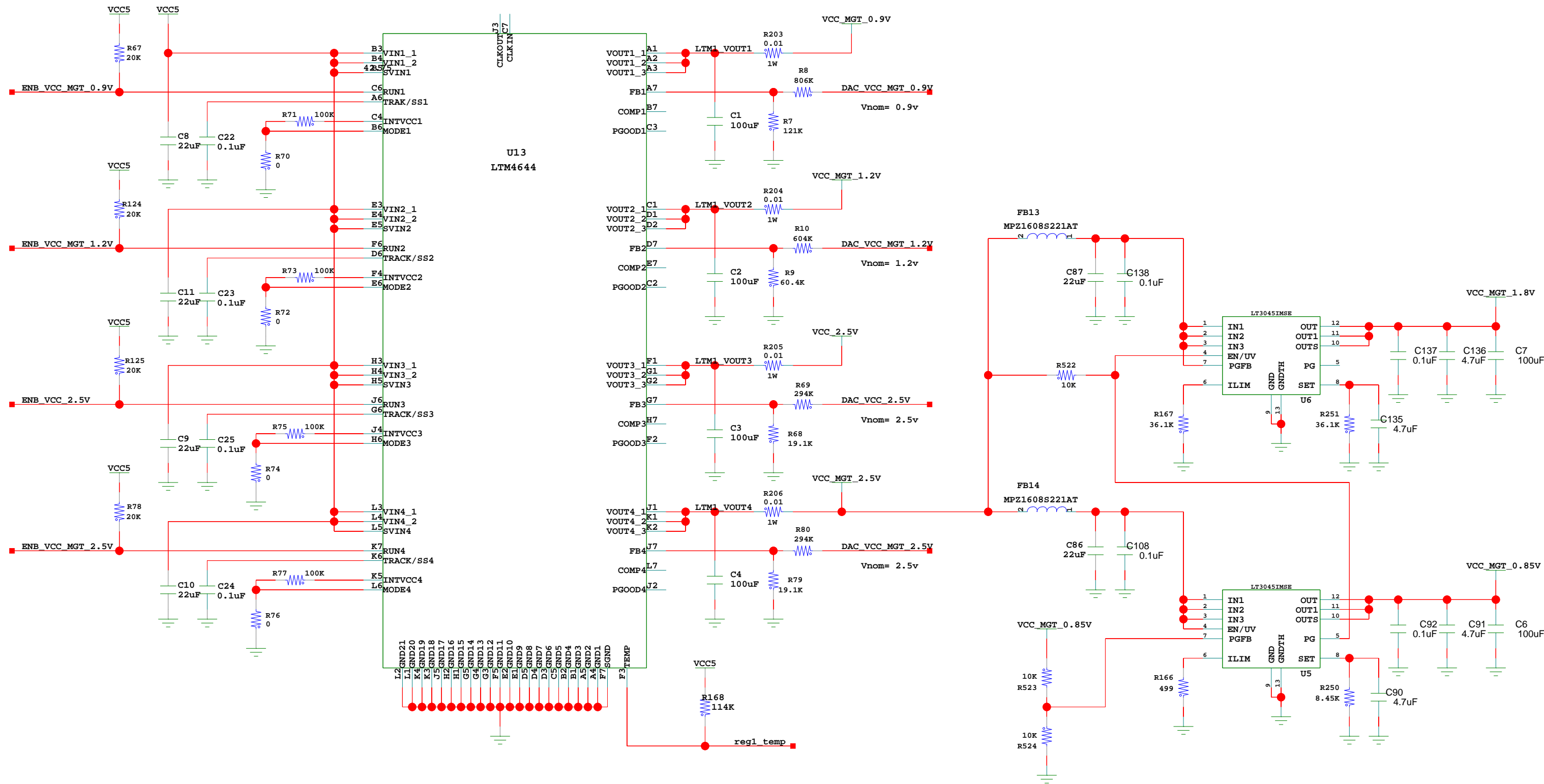
SHEET 24 OF 31

Regulator Configuration

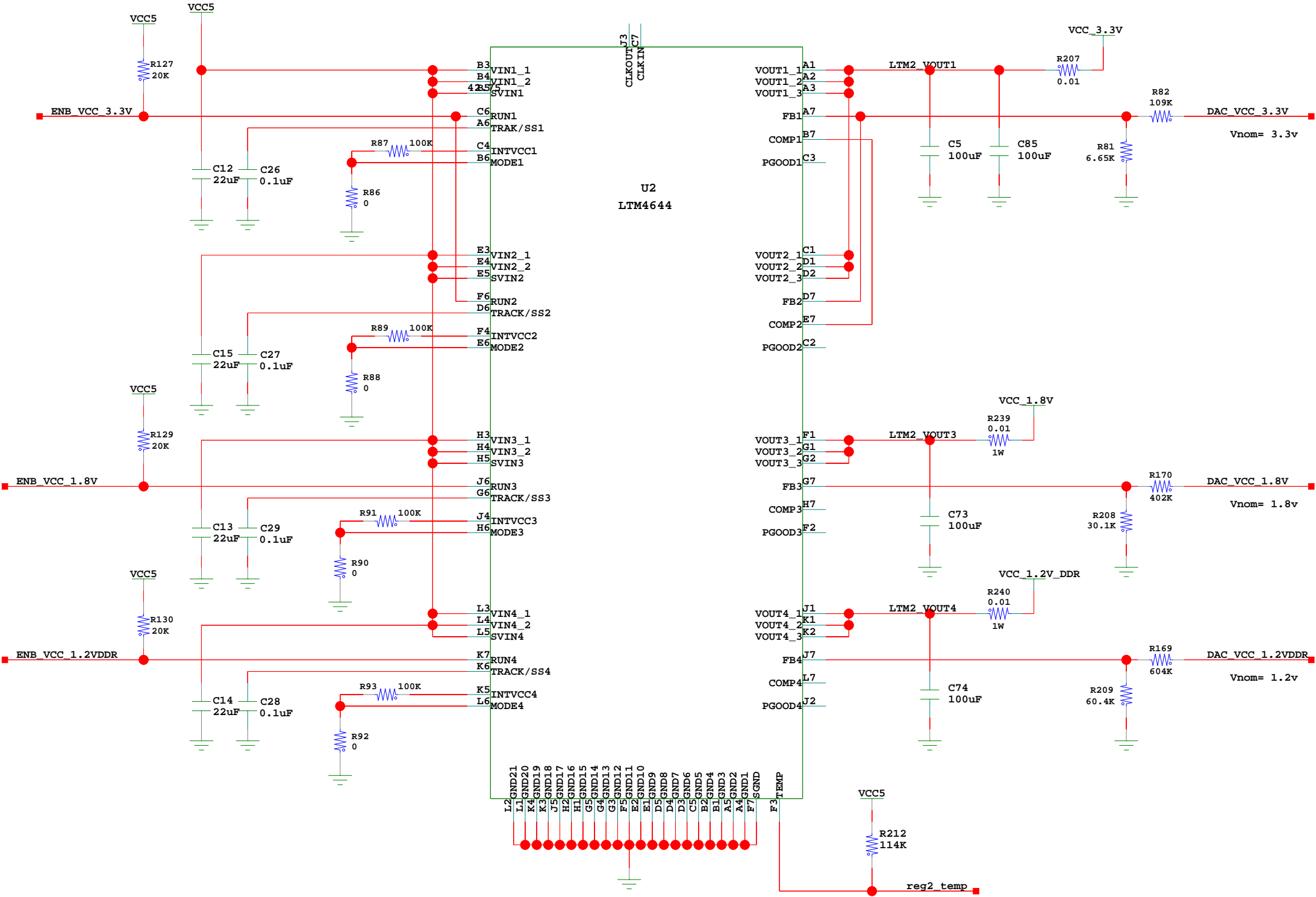




Regulators: MGT / MGTR

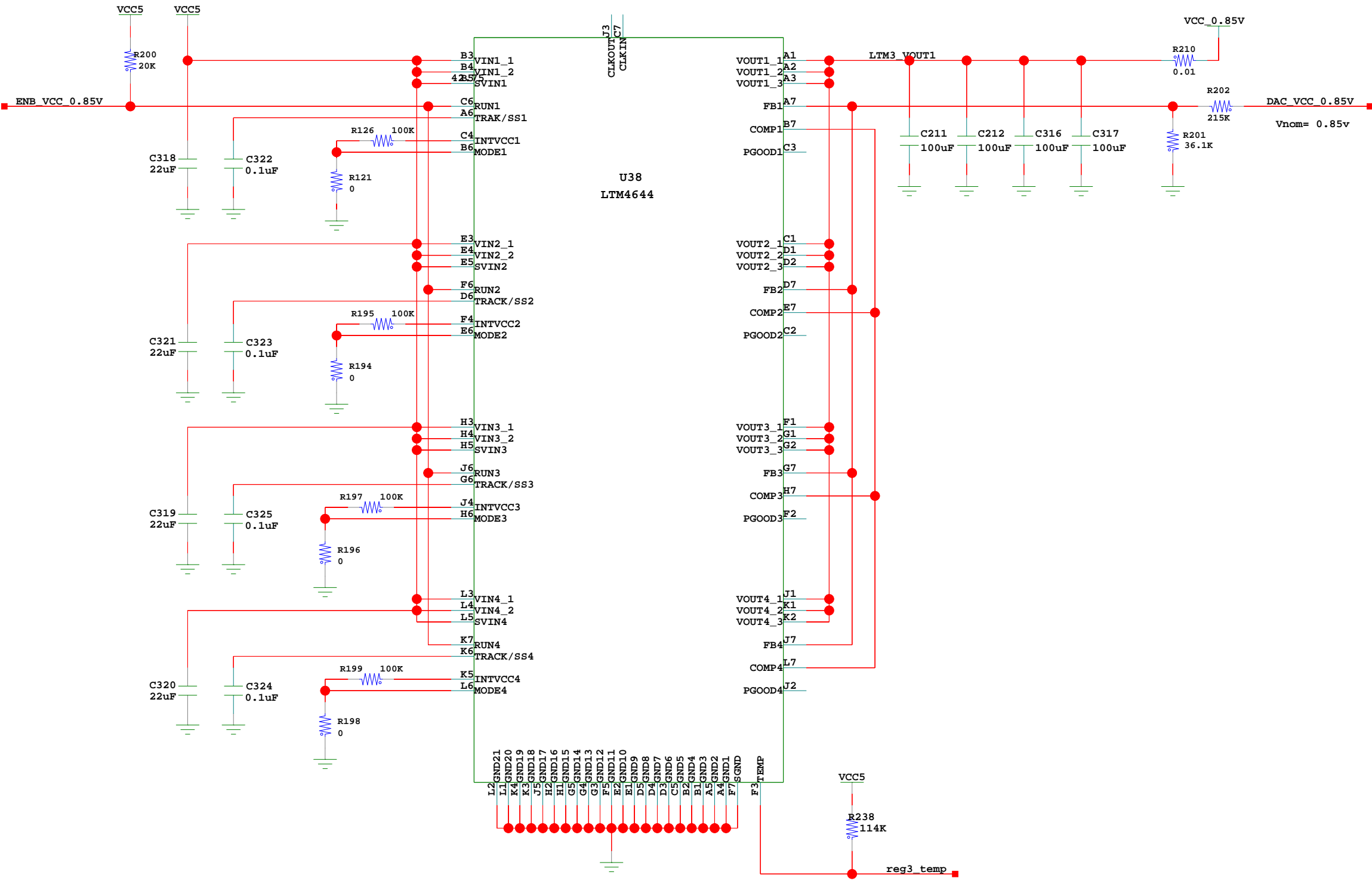


Regulators: DDR4 ,3.3v, 1.8v



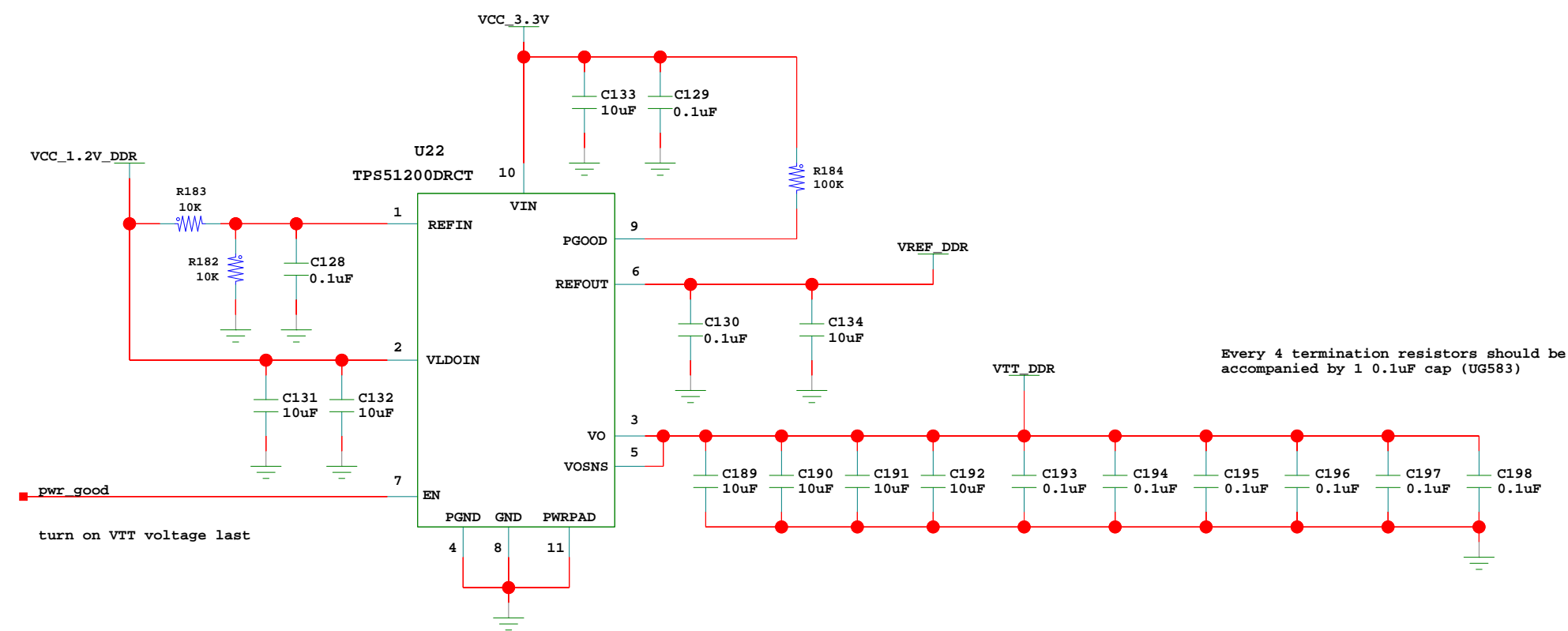


Regulators: PL/PS Core



B	LT-EL-SR-EU-BPM-0614-03	2
SHEET SIZE	DRAWING/PART NUMBER	REVISION
ESH&Q RISK LEVEL A-3		SHEET 29 OF 31

Regulators: DDR4 Termination Voltage



Regulators: Current Measurement

