REV.	DESCRIPTION	DATE	DESIGNER	CHECKED BY	ENGINEER
	PRELIMINARY RELEASE		JM	AD	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS, 1%, 100PPM.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, 50V.
3 ALL INDUCTOR VALUES ARE IN MICROHENRIES.

UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS ARE IN INCHES
DIMENSIONS IN BRACKETS [X.XX] (WHERE PRESENT)
ARE MILLIMETERS AND ARE FOR REFERENCE ONLY
INTERPRET DRAWING AS PER ANSI Y14.5-1994 OR Y32.2-1975

DIMENSIONAL TOLERANCES
X. ± 0.060
.X ± 0.030
.XX ± 0.015
.XXX ± 0.005

ANGULAR TOLERANCE
±0.5°

FINISH: 125

BREAK EDGES & SHARP CORNERS 0.005 MIN. TO 0.030 MAX

NEXT ASSY:

PROJECT:

THIRD ANGLE PROJECTION

SCALE: N/A

WBS#

BROOKHAVEN NATIONAL LABORATORY
BROOKHAVEN SCIENCE ASSOCIATES
UPTON, N.Y. 11973
Exploring Life's Mysteries,
Protecting its Future

DRAWN BY	J. Mead	
CHECKED BY	T. Caracappa	
VACUUM APPROVAL	NA	
ENGINEER APPROVAL	J. Mead	
SUPERVISOR APPROVAL	D. Padrazo	
ES&H APPROVAL		
QA APPROVAL	E. Cheswick	

SCHEMATIC DIAGRAM
APS BESOCM

SHEET SIZE	DRAWING/PART NUMBER	REVISION
B		

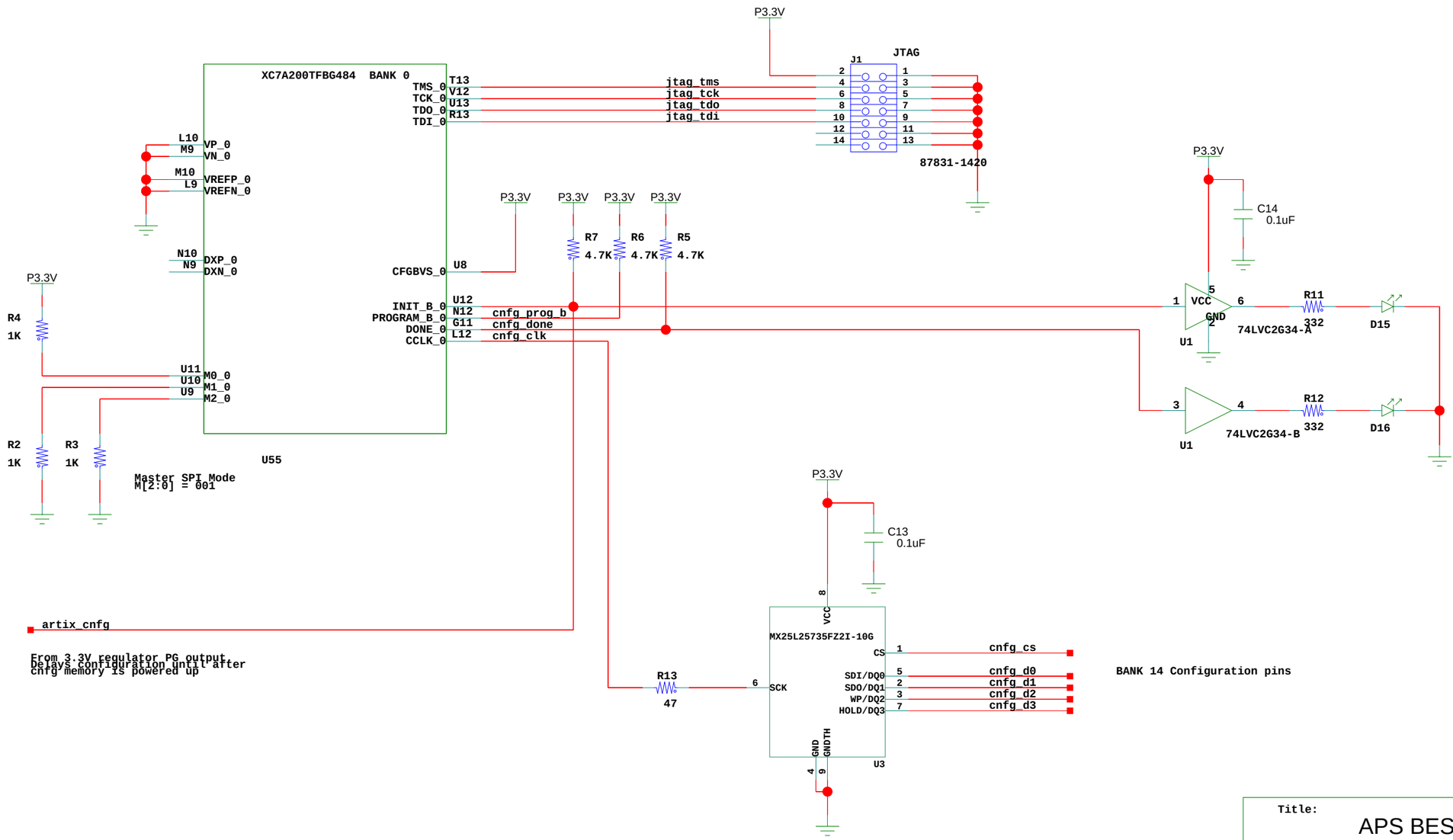
ESH&Q RISK LEVEL A-2

SHEET 1 OF 23

DWG #

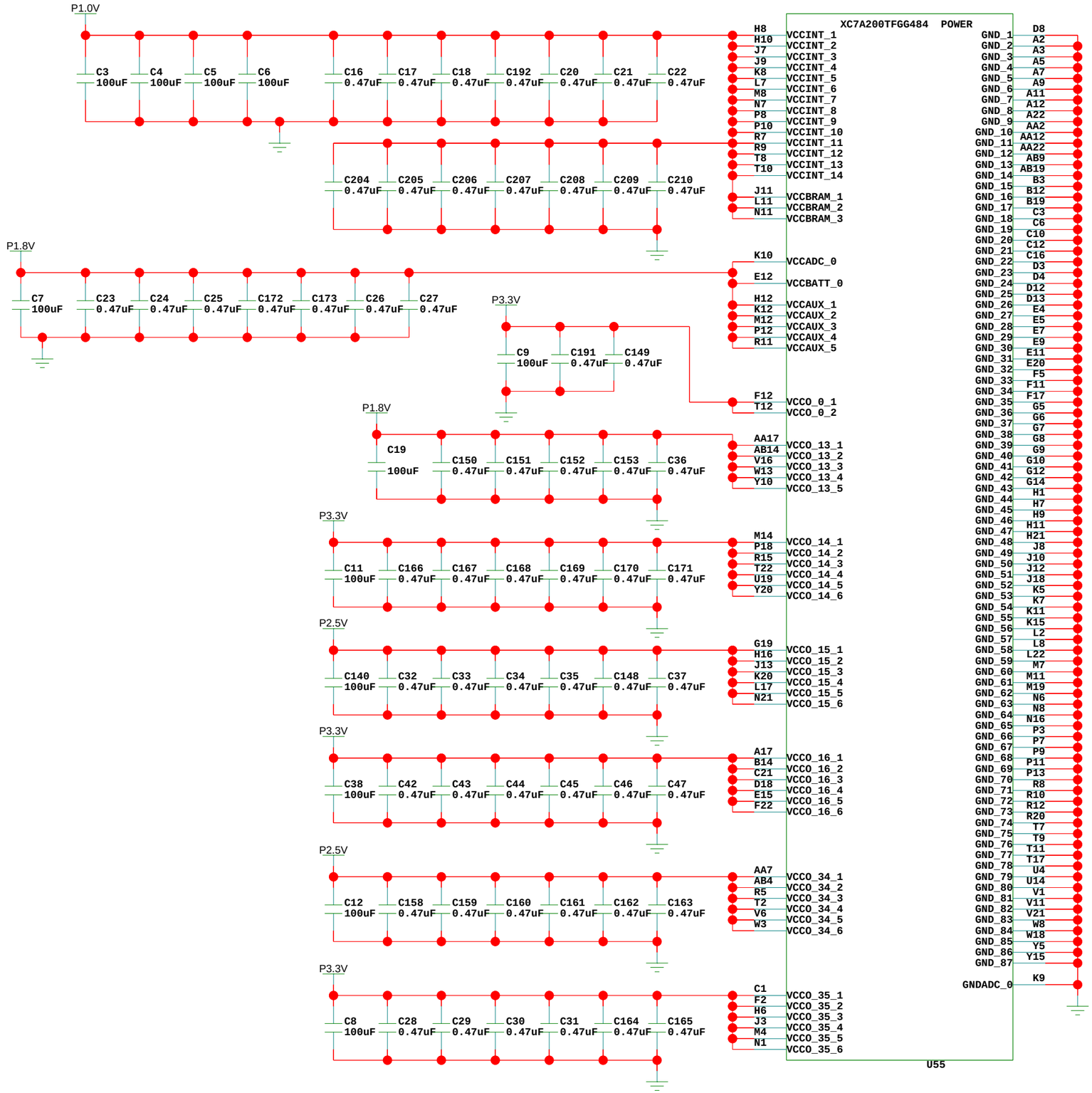
Artix 7 FPGA Configuration

JTAG Header



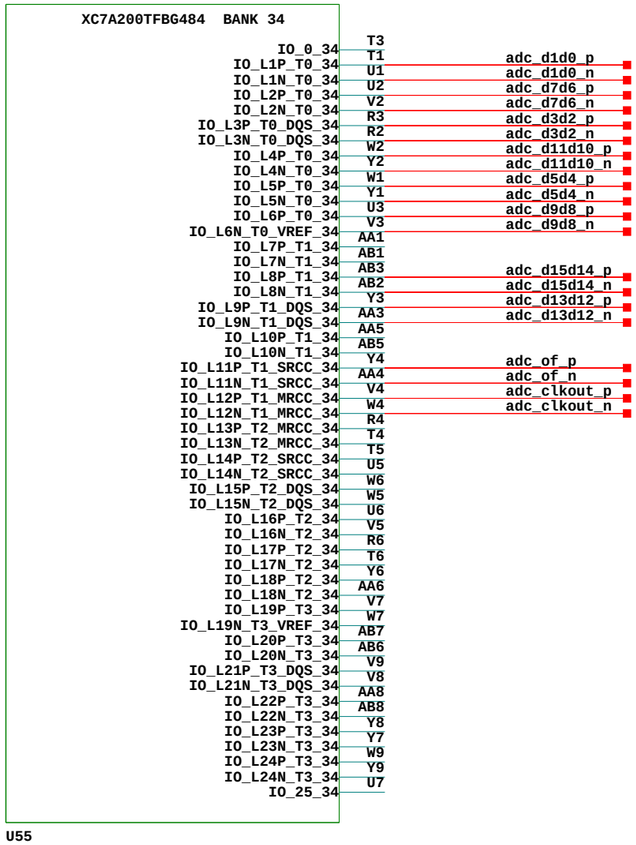
Title: APS BESOCM FPGA BOARD	
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 2 of 23	Drawn By J. Mead

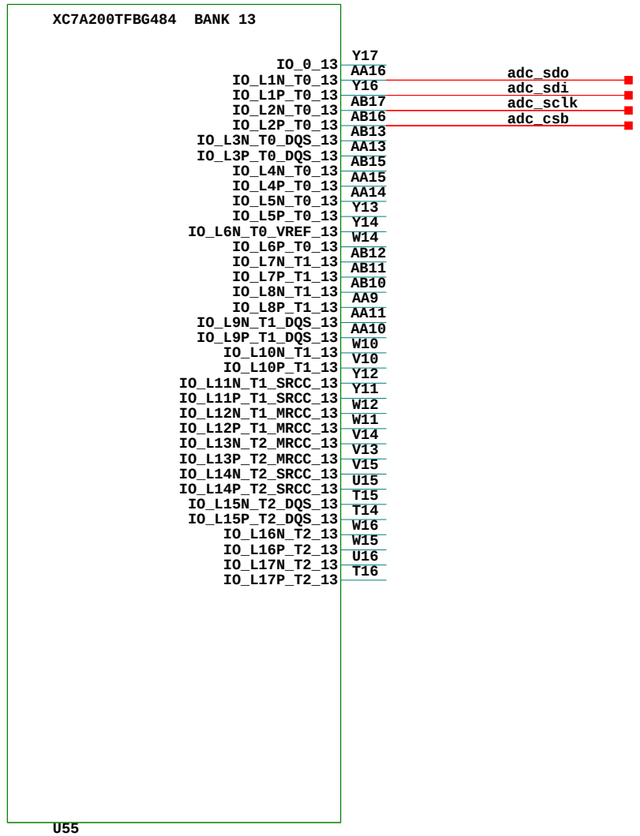
Artix 7 FPGA Power

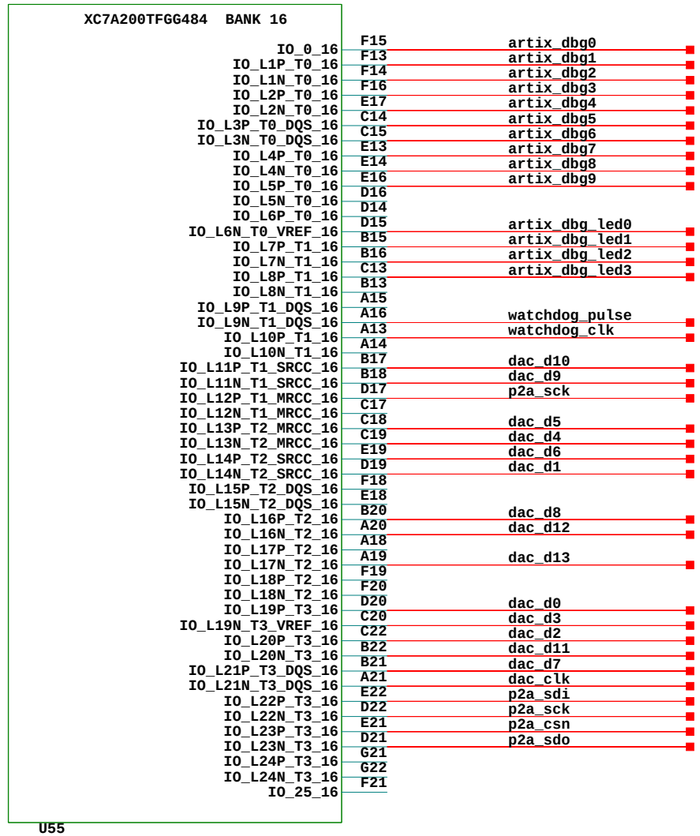


Title:	APS BESOCM FPGA BOARD
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 3 of 23	Drawn By J. Mead

Artix 7 FPGA I/O







Title:	APS BESOCM FPGA BOARD		
Date:	11-1-21	Ver:	
Sheet Size: B		Rev: A	
Sheet 4 of 23		Drawn By	J. Mead

Artix 7 FPGA I/O

P3.3V

PUDC - Pull High for 3state I/O during configuration

R8

4.7K

XC7A200TFBG484 BANK 14

IO_0_14	P20	
IO_L1P_T0_D00_MOSI_14	P22	cnfg_d0
IO_L1N_T0_D01_DIN_14	R22	cnfg_d1
IO_L2P_T0_D02_14	P21	cnfg_d2
IO_L2N_T0_D03_14	R21	cnfg_d3
IO_L3P_T0_DQS_PUDC_B_14	U22	
IO_L3N_T0_DQS_EMCCLK_14	V22	fault_fpga_7
IO_L4P_T0_D04_14	T21	fault_fpga_9_lat
IO_L4N_T0_D05_14	U21	fault_fpga_9
IO_L5P_T0_D06_14	P19	fault_fpga_8
IO_L5N_T0_D07_14	R19	fault_fpga_8_lat
IO_L6P_T0_FCS_B_14	T19	cnfg_cs
IO_L6N_T0_D08_VREF_14	T20	fault_fpga_5_lat
IO_L7P_T1_D09_14	W21	fault_fpga_10
IO_L7N_T1_D10_14	W22	fault_fpga_7_lat
IO_L8P_T1_D11_14	AA20	fault_no_clock_lat
IO_L8N_T1_D12_14	AA21	fault_fpga_11
IO_L9P_T1_DQS_14	Y21	fault_fpga_10_lat
IO_L9N_T1_DQS_D13_14	Y22	fault_bad_power_lat
IO_L10P_T1_D14_14	AB21	fault_fpga_11_lat
IO_L10N_T1_D15_14	AB22	fault_bad_power
IO_L11P_T1_SRCC_14	U20	fault_fpga_5
IO_L11N_T1_SRCC_14	V20	fault_fpga_6
IO_L12P_T1_MRCC_14	W19	fault_no_clock_lat
IO_L12N_T1_MRCC_14	W20	fault_fpga_6_lat
IO_L13P_T2_MRCC_14	Y18	fault_fpga_2_lat
IO_L13N_T2_MRCC_14	Y19	fault_fpga_0_lat
IO_L14P_T2_SRCC_14	V18	fault_fpga_3
IO_L14N_T2_SRCC_14	V19	fault_fpga_0
IO_L15P_T2_DQS_RDWR_B_14	AA19	fault_fpga_1
IO_L15N_T2_DQS_DOUT_CSO_B_14	AB20	fault_no_clock
IO_L16P_T2_CSI_B_14	V17	fault_no_trig
IO_L16N_T2_A15_D31_14	W17	fault_no_trig_lat
IO_L17P_T2_A14_D30_14	AA18	fault_fpga_2
IO_L17N_T2_A13_D29_14	AB18	fault_fpga_1_lat
IO_L18P_T2_A12_D28_14	U17	acis_resetn
IO_L18N_T2_A11_D27_14	U18	fault_fpga_3_lat
IO_L19P_T3_A10_D26_14	P14	fault_no_pulse_lat
IO_L19N_T3_A09_D25_VREF_14	R14	fault_no_pulse
IO_L20P_T3_A08_D24_14	R18	fault_fpga_4
IO_L20N_T3_A07_D23_14	T18	acis_fault_rdbk
IO_L21P_T3_DQS_14	N17	trigger_pulse
IO_L21N_T3_DQS_A06_D22_14	P17	beam_pulse_detect_led
IO_L22P_T3_A05_D21_14	P15	trigger_pulse_detect_led
IO_L22N_T3_A04_D20_14	R16	trigger_pulse_fp
IO_L23P_T3_A03_D19_14	N13	fault_fpga_4_lat
IO_L23N_T3_A02_D18_14	N14	acis_faultn
IO_L24P_T3_A01_D17_14	P16	acis_reset
IO_L24N_T3_A00_D16_14	R17	acis_force_trip
IO_25_14	N15	acis_keylock

U55

XC7A200TFBG484 BANK 35

IO_0_35	F4	
IO_L1P_T0_AD4P_35	B1	eeprom_csn0
IO_L1N_T0_AD4N_35	A1	eeprom_sck0
IO_L2P_T0_AD12P_35	C2	eeprom_sdi0
IO_L2N_T0_AD12N_35	B2	eeprom_holdn0
IO_L3P_T0_DQS_AD5P_35	E1	eeprom_sdo0
IO_L3N_T0_DQS_AD5N_35	D1	
IO_L4P_T0_35	E2	eeprom_csn1
IO_L4N_T0_35	D2	eeprom_sck1
IO_L5P_T0_AD13P_35	G1	eeprom_sdi1
IO_L5N_T0_AD13N_35	F1	eeprom_holdn1
IO_L6P_T0_35	F3	eeprom_sdo1
IO_L6N_T0_VREF_35	E3	
IO_L7P_T1_AD6P_35	K1	dac_tp_d8
IO_L7N_T1_AD6N_35	J1	dac_tp_d5
IO_L8P_T1_AD14P_35	H2	dac_tp_d3
IO_L8N_T1_AD14N_35	G2	dac_tp_d1
IO_L9P_T1_DQS_AD7P_35	K2	dac_tp_d7
IO_L9N_T1_DQS_AD7N_35	J2	dac_tp_d4
IO_L10P_T1_AD15P_35	J5	
IO_L10N_T1_AD15N_35	H5	
IO_L11P_T1_SRCC_35	H3	dac_tp_d2
IO_L11N_T1_SRCC_35	G3	dac_tp_d0
IO_L12P_T1_MRCC_35	H4	
IO_L12N_T1_MRCC_35	G4	
IO_L13P_T2_MRCC_35	K4	
IO_L13N_T2_MRCC_35	J4	
IO_L14P_T2_SRCC_35	L3	dac_tp_d10
IO_L14N_T2_SRCC_35	K3	dac_tp_d6
IO_L15P_T2_DQS_35	M1	dac_tp_clk
IO_L15N_T2_DQS_35	L1	dac_tp_d9
IO_L16P_T2_35	M3	dac_tp_d11
IO_L16N_T2_35	M2	dac_tp_d12
IO_L17P_T2_35	K6	
IO_L17N_T2_35	J6	
IO_L18P_T2_35	L5	
IO_L18N_T2_35	L4	dac_tp_d13
IO_L19P_T3_35	N4	tpdac_sdo
IO_L19N_T3_VREF_35	N3	tp_sw0
IO_L20P_T3_35	R1	tpdac_sdin
IO_L20N_T3_35	P1	tpdac_ldacn
IO_L21P_T3_DQS_35	P5	
IO_L21N_T3_DQS_35	P4	tpdac_sclk
IO_L22P_T3_35	P2	tpdac_syncn
IO_L22N_T3_35	N2	tp_sw1
IO_L23P_T3_35	M6	tp_sw2
IO_L23N_T3_35	M5	tp_sw3
IO_L24P_T3_35	P6	
IO_L24N_T3_35	N5	tpdac_clrn
IO_25_35	L6	

U55

XC7A200TFBG484 BANK 15

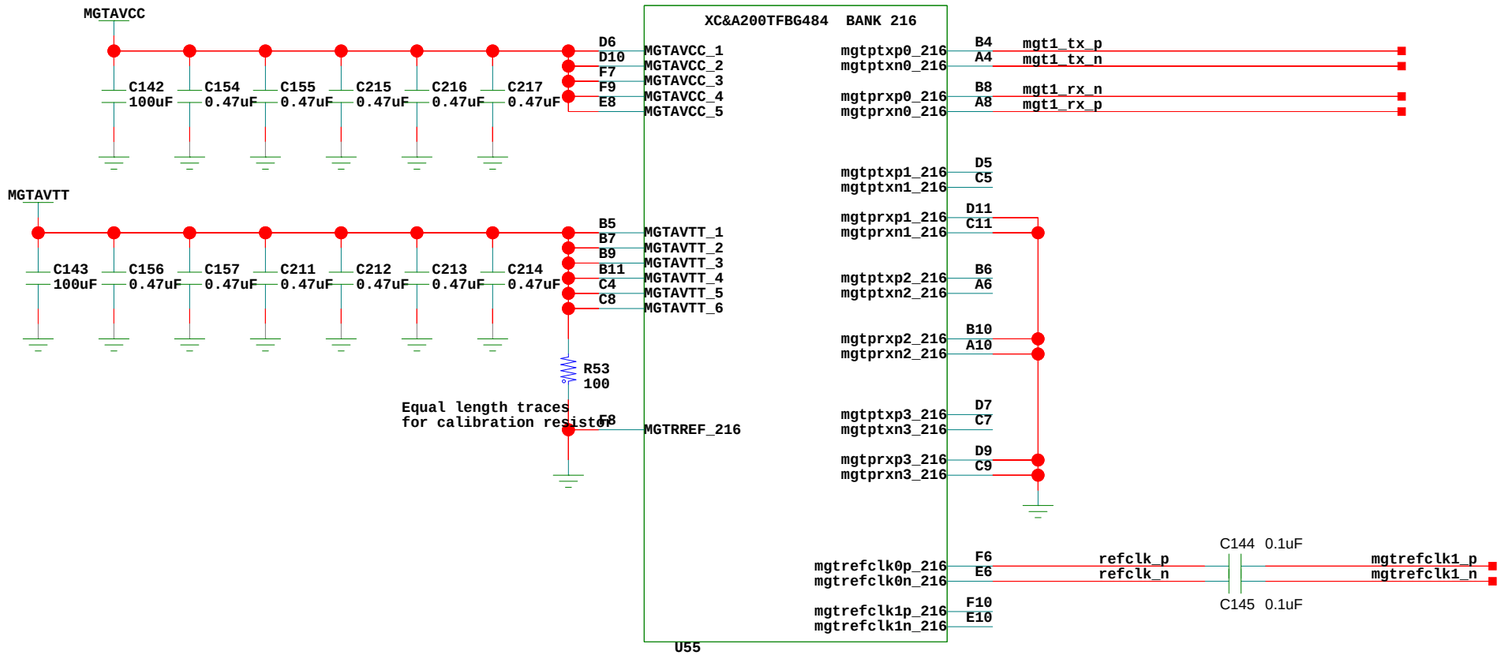
IO_0_15	J16	
IO_L1P_T0_AD0P_15	H13	
IO_L1N_T0_AD0N_15	G13	
IO_L2P_T0_AD8P_15	G15	a2p_d1_p
IO_L2N_T0_AD8N_15	G16	a2p_d1_n
IO_L3P_T0_DQS_AD1P_15	J14	a2p_d2_p
IO_L3N_T0_DQS_AD1N_15	H14	a2p_d2_n
IO_L4P_T0_15	G17	a2p_d3_p
IO_L4N_T0_15	G18	a2p_d3_n
IO_L5P_T0_AD9P_15	J15	a2p_d4_p
IO_L5N_T0_AD9N_15	H15	a2p_d4_n
IO_L6P_T0_15	H17	a2p_d5_p
IO_L6N_T0_VREF_15	H18	a2p_d5_n
IO_L7P_T1_AD2P_15	J22	a2p_d6_p
IO_L7N_T1_AD2N_15	H22	a2p_d6_n
IO_L8P_T1_AD10P_15	H20	a2p_d0_p
IO_L8N_T1_AD10N_15	G20	a2p_d0_n
IO_L9P_T1_DQS_AD3P_15	K21	a2p_d8_p
IO_L9N_T1_DQS_AD3N_15	K22	a2p_d8_n
IO_L10P_T1_AD11P_15	M21	a2p_d9_p
IO_L10N_T1_AD11N_15	L21	a2p_d9_n
IO_L11P_T1_SRCC_15	J20	a2p_d10_p
IO_L11N_T1_SRCC_15	J21	a2p_d10_n
IO_L12P_T1_MRCC_15	J19	a2p_d7_p
IO_L12N_T1_MRCC_15	H19	a2p_d7_n
IO_L13P_T2_MRCC_15	K18	a2p_d11_p
IO_L13N_T2_MRCC_15	K19	a2p_d11_n
IO_L14P_T2_SRCC_15	L19	a2p_d12_p
IO_L14N_T2_SRCC_15	L20	a2p_d12_n
IO_L15P_T2_DQS_15	N22	a2p_d13_p
IO_L15N_T2_DQS_ADV_B_15	M22	a2p_d13_n
IO_L16P_T2_A28_15	M18	a2p_d14_p
IO_L16N_T2_A27_15	L18	a2p_d14_n
IO_L17P_T2_A26_15	N18	a2p_d15_p
IO_L17N_T2_A25_15	N19	a2p_d15_n
IO_L18P_T2_A24_15	N20	a2p_sel_p
IO_L18N_T2_A23_15	M20	a2p_sel_n
IO_L19P_T3_A22_15	K13	a2p_enb_p
IO_L19N_T3_A21_VREF_15	K14	a2p_enb_n
IO_L20P_T3_A20_15	M13	
IO_L20N_T3_A19_15	L13	
IO_L21P_T3_DQS_15	K17	
IO_L21N_T3_DQS_A18_15	J17	
IO_L22P_T3_A17_15	L14	
IO_L22N_T3_A16_15	L15	
IO_L23P_T3_FOE_B_15	L16	a2p_clk_p
IO_L23N_T3_FWE_B_15	K16	a2p_clk_n
IO_L24P_T3_RS1_15	M15	
IO_L24N_T3_RS0_15	M16	
IO_25_15	M17	

U55

Title: APS BESOCM FPGA BOARD

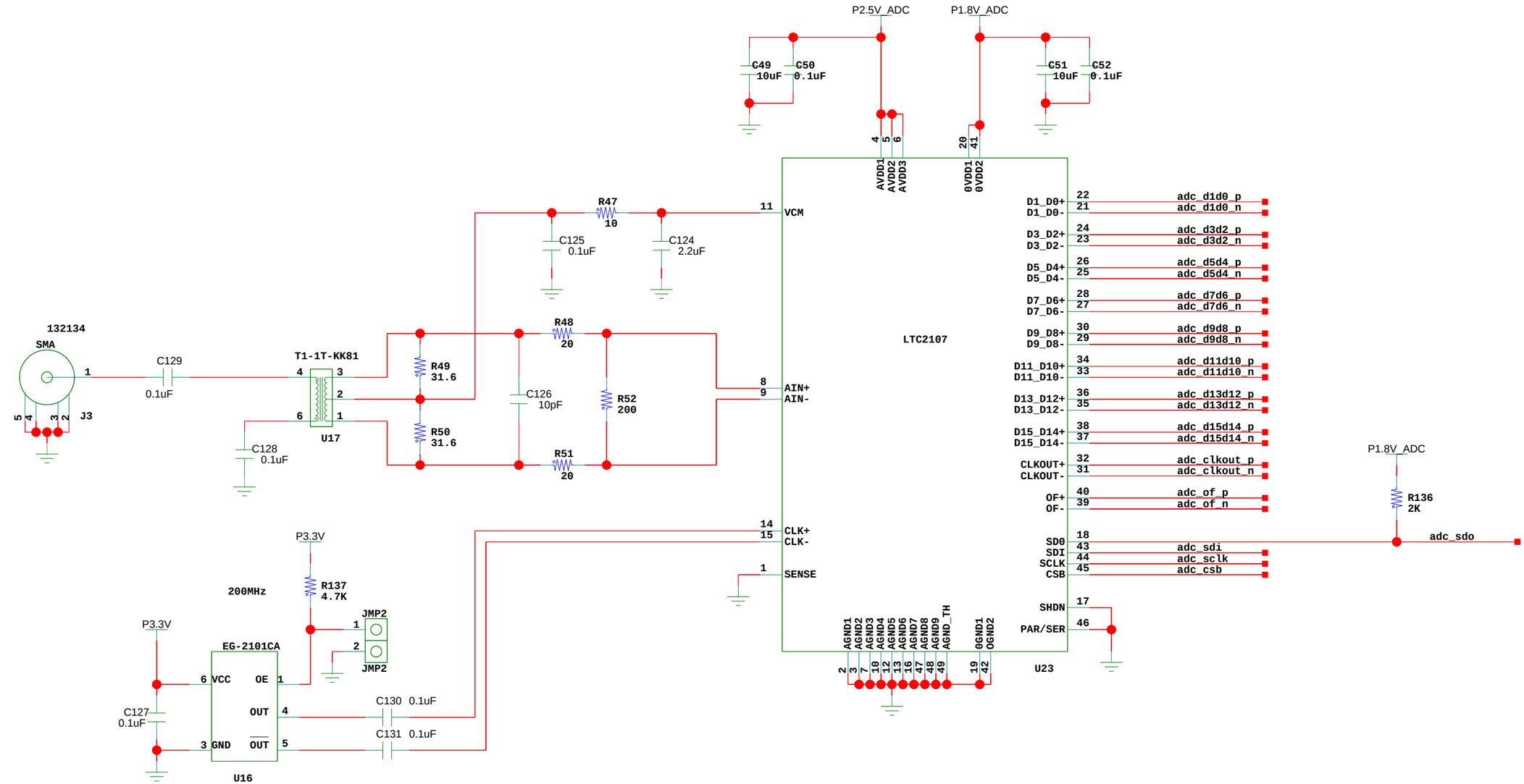
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 5 of 23	Drawn By J. Mead

Artix 7 FPGA MGT



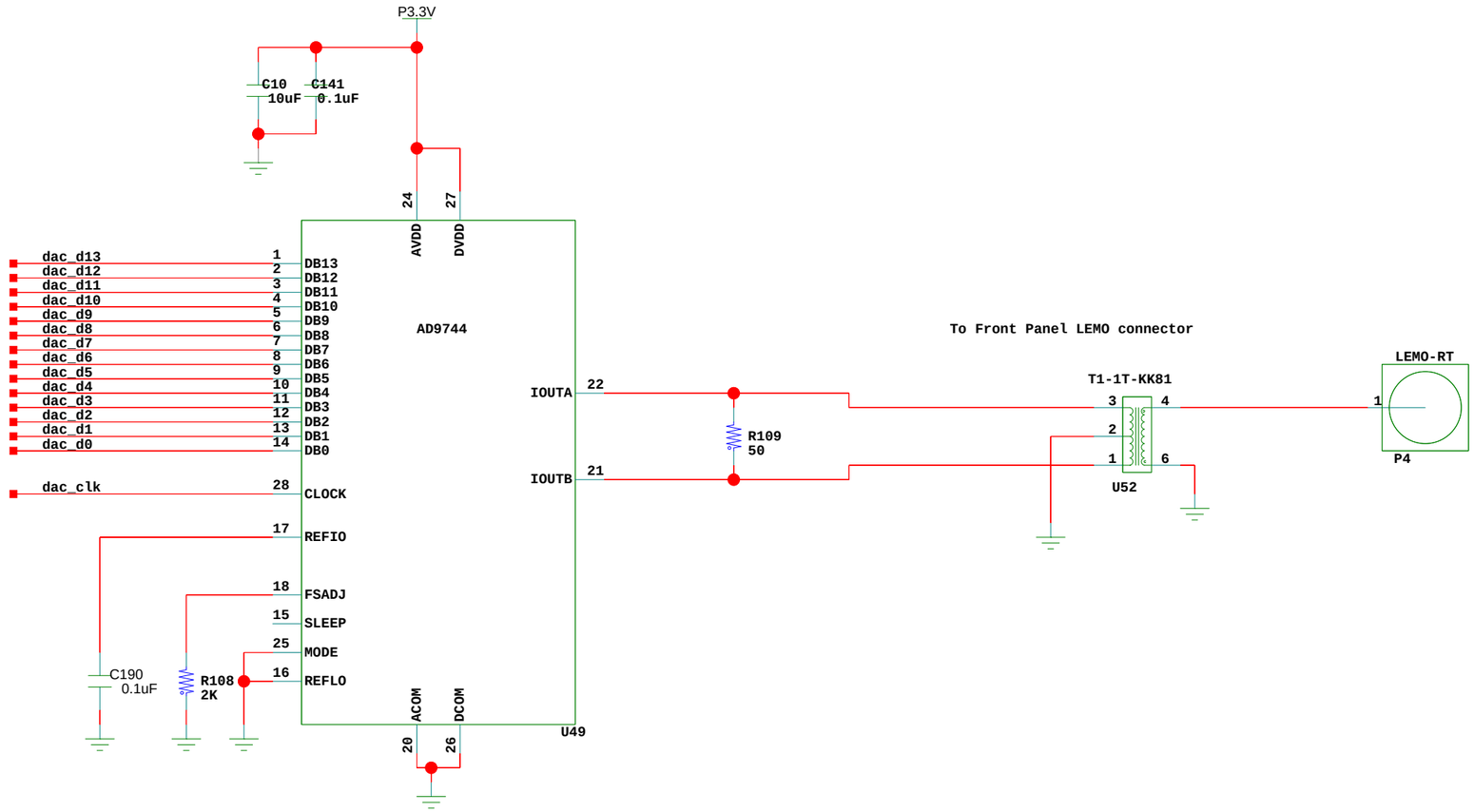
Title: APS BESOCM FPGA BOARD	
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 6 of 23	Drawn By J. Mead

LTC2107 ADC



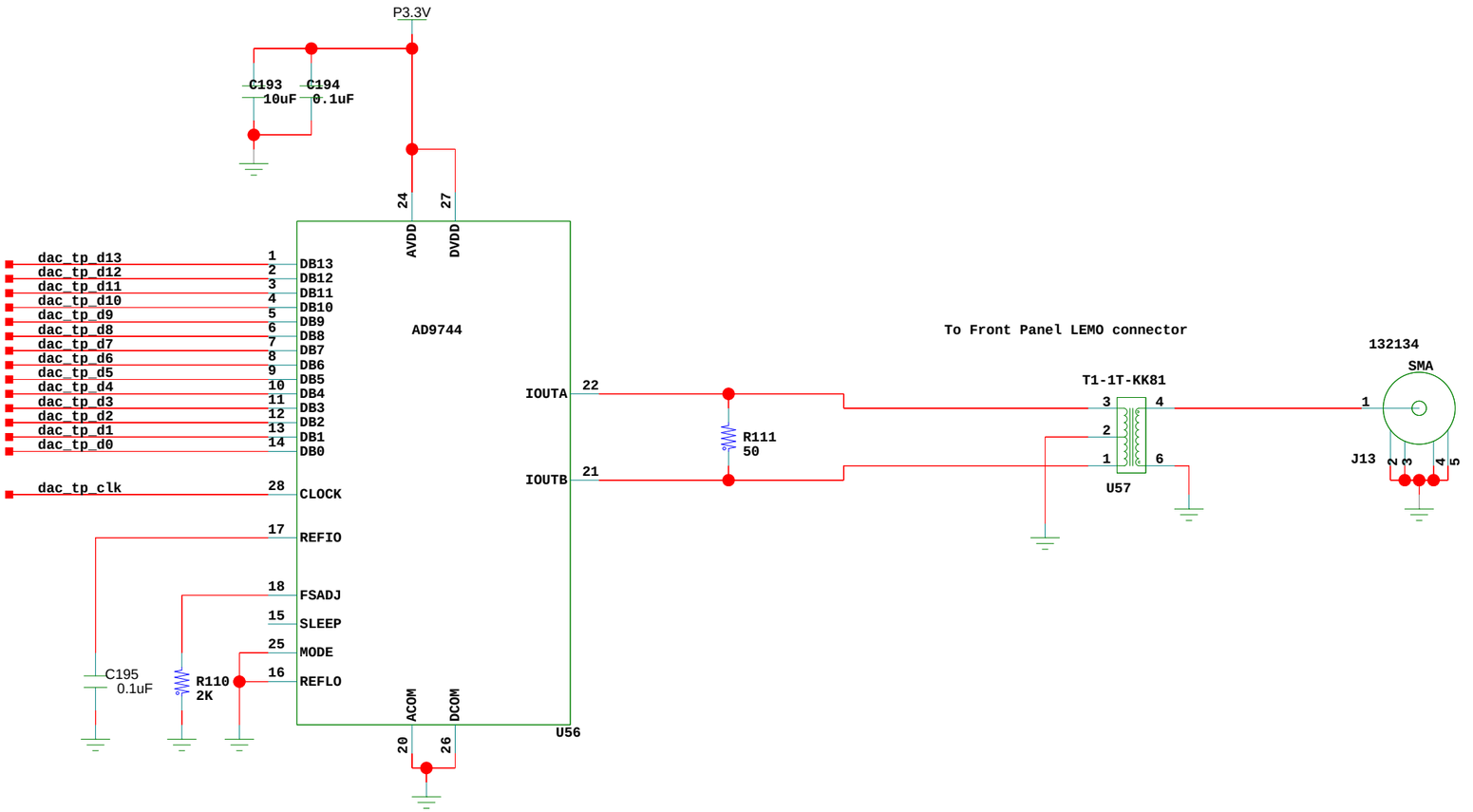
Title:	APS BESOCM FPGA BOARD
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 7 of 23	Drawn By J. Mead

Raw ADC Front Panel Test Port AD9744 DAC

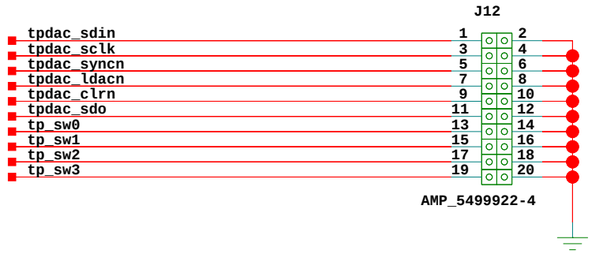


Title: APS BESOCM FPGA BOARD	
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 8 of 23	Drawn By J. Mead

Test Pulse Generation AD9744 DAC

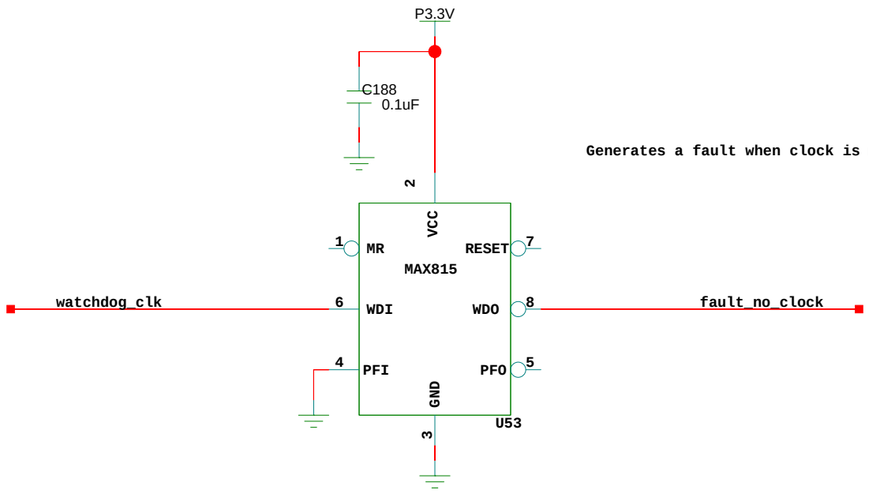


Test Pulse Gen Control Signals

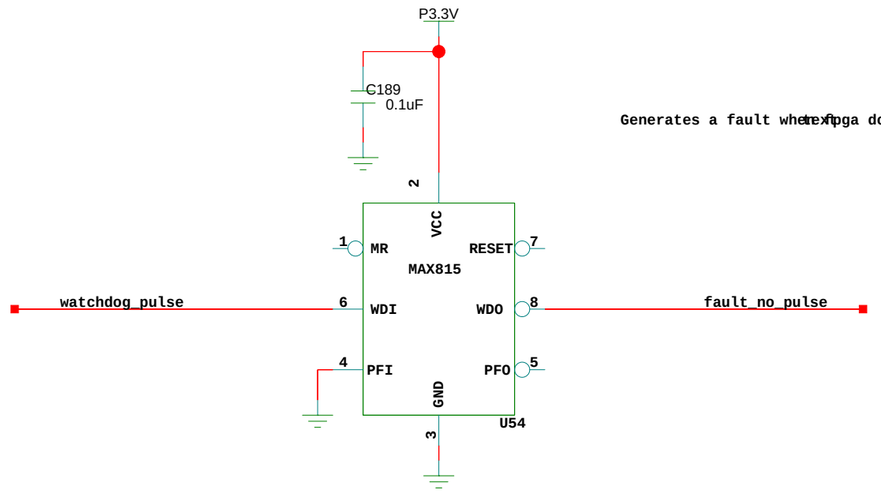


Title: APS BESOCM FPGA BOARD	
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 9 of 23	Drawn By J. Mead

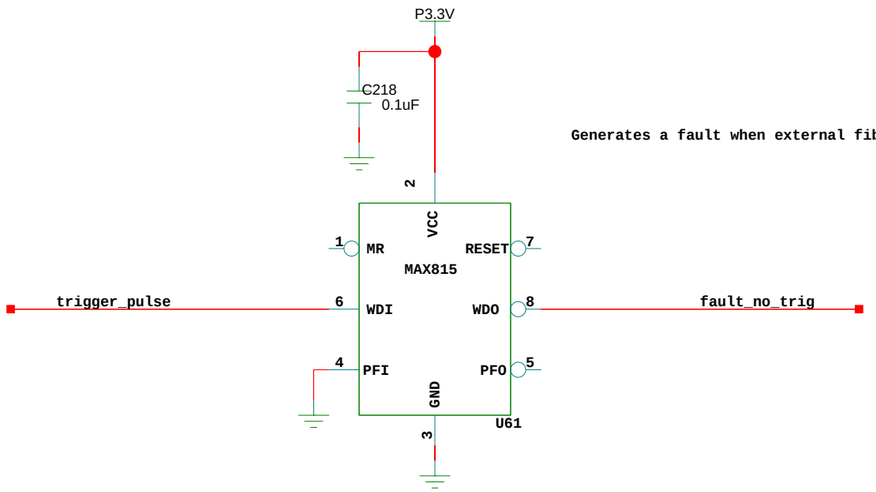
Clock and Gate Watch Dog Timers



Generates a fault when clock is missing or slow



Generates a fault when fpga doesn't see external trigge



Generates a fault when external fiber trigger pulse is missing

Title: APS BESOCM FPGA BOARD	
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 10 of 23	Drawn By J. Mead

Fiber Trigger Input

Trigger Input

P5.0V
P3.3V
C146 0.1uF
R139 560
HFBR-2412T
VCC
DOUT
GND1
GND2
U27
C132 0.1uF
74LVC1G125
U25

Trigger select

1-2: Gate taken from Fiber
2-3 : Gate taken from companion board

JMP3
J6

to fpga
trigger_pulse

To Companion board
132134
SMA
J11
C175 0.1uF
74LVC1G125
U51

From Companion board
132134
SMA
J8

P3.3V
C147 0.1uF
74LVC1G125
U26
trig_raw_out

To Front Panel
Raw External Trigger Gate
132134
SMA
J9

Trigger & Beam Status LEDs

P3.3V
C39 0.1uF
trigger_pulse_detect_led
VCC
GND
74LVC2G04-A
U45
R92 332
D3

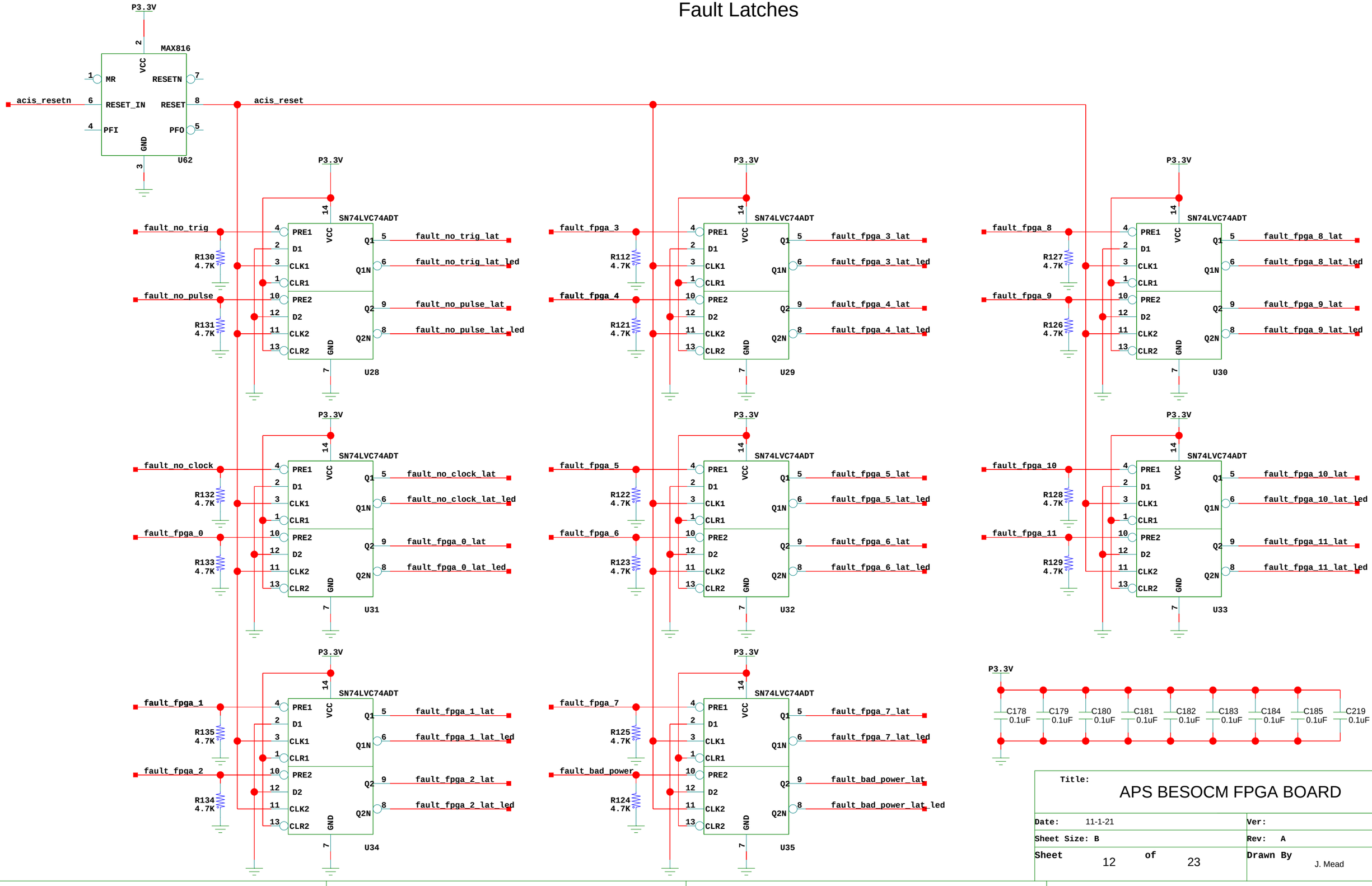
beam_pulse_detect_led
74LVC2G04-B
U45
R93 332
D4

P3.3V
C174 0.1uF
From FPGA
trigger_pulse_fp
74LVC1G125
U50

Front Panel Lemo
Internal Trigger
LEMO-RT
P3

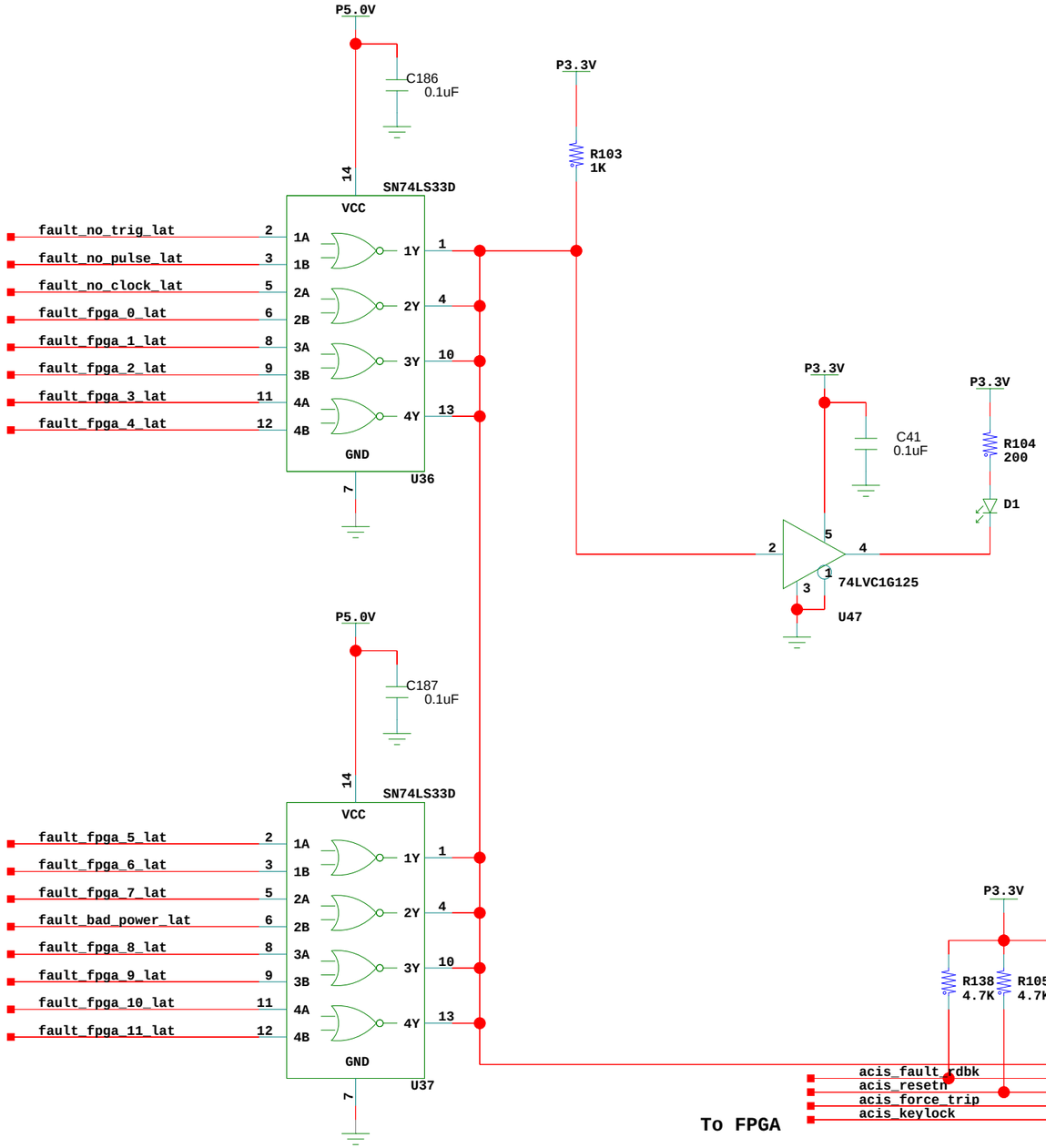
Title:	APS BESOCM FPGA BOARD		
Date:	11-1-21	Ver:	
Sheet Size: B		Rev: A	
Sheet	11 of 23	Drawn By	J. Mead

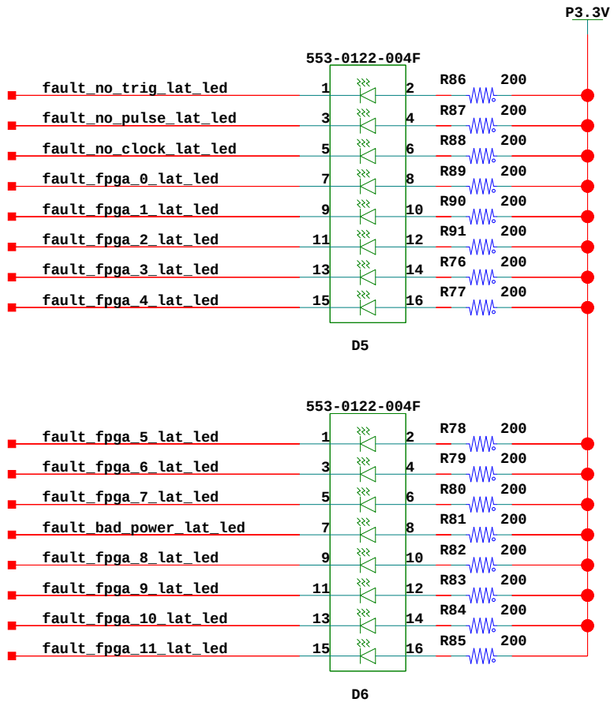
Fault Latches

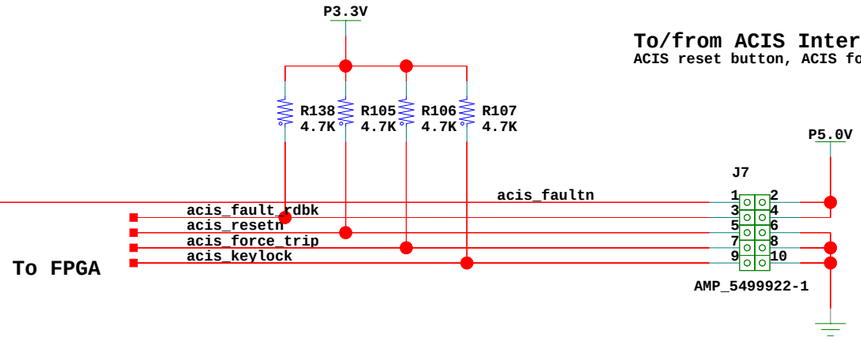


Title: APS BESOCM FPGA BOARD	
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 12 of 23	Drawn By J. Mead

ACIS Fault



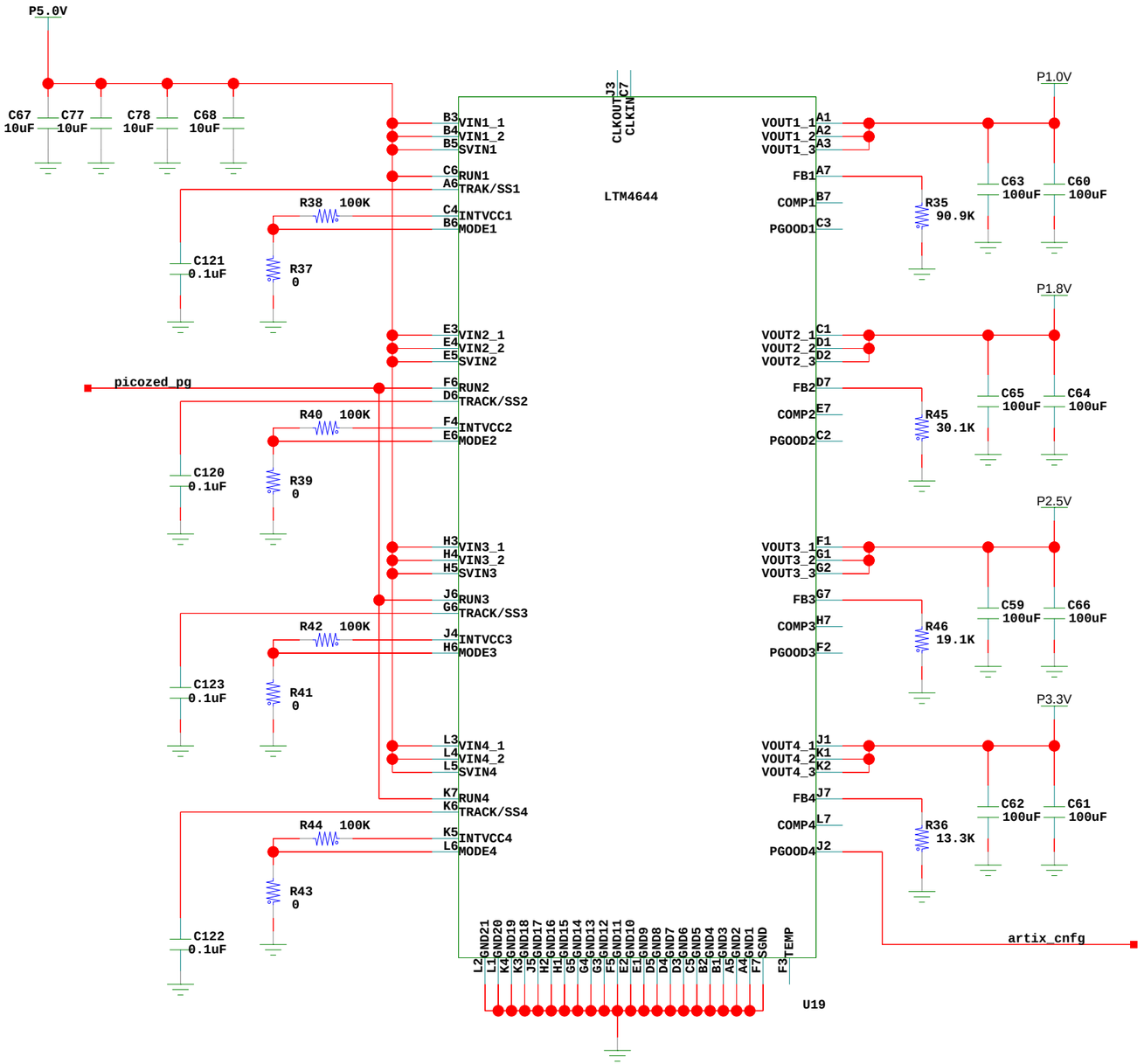


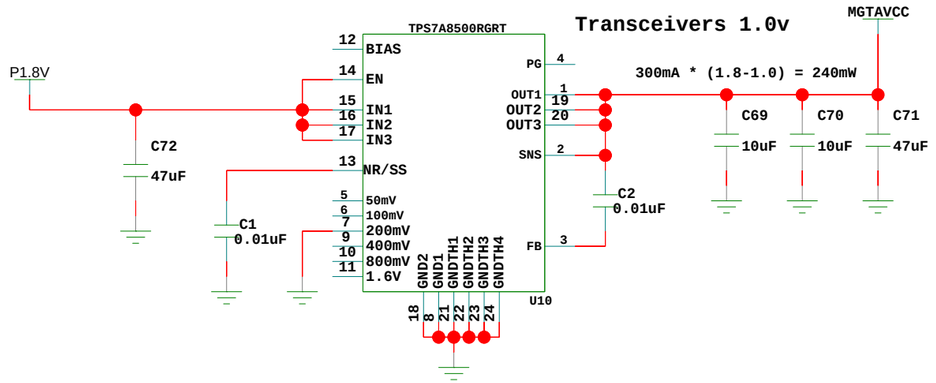


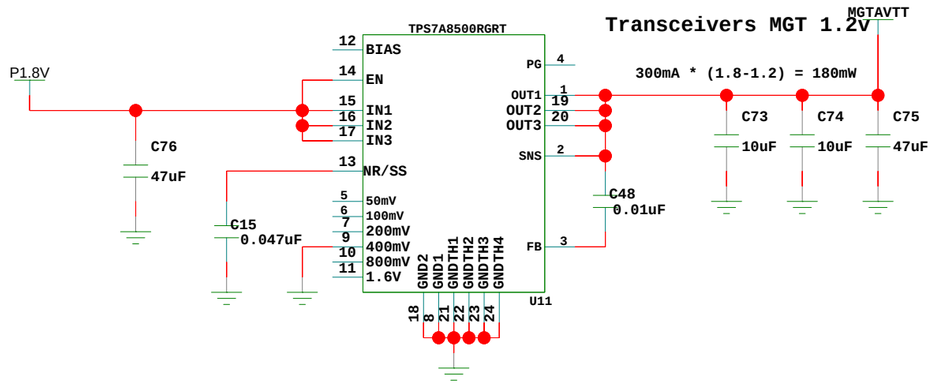
To/from ACIS Interface board.
ACIS reset button, ACIS force trip buttons and keylock wire to ACIS interface board

Title: APS BESOCM FPGA BOARD	
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 13 of 23	Drawn By J. Mead

Artix and picoZed Regulators

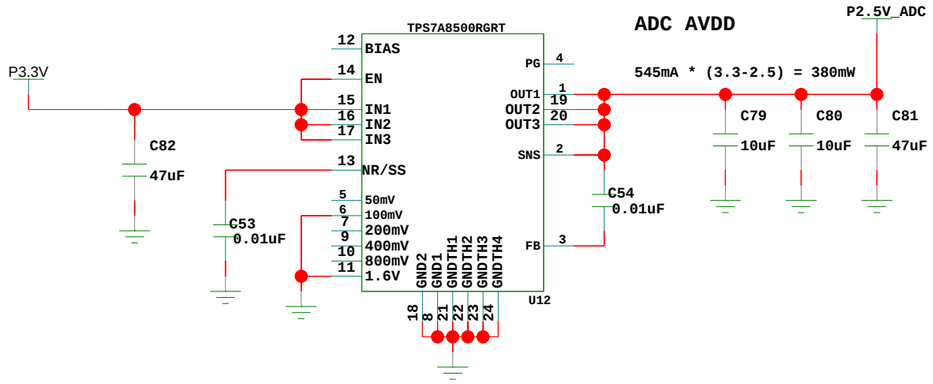


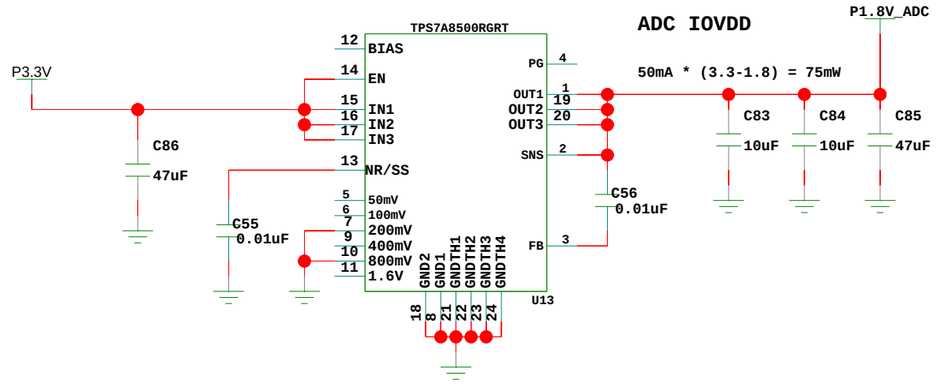




Title: APS BESOCM FPGA BOARD			
Date: 11-1-21		Ver:	
Sheet Size: B		Rev: A	
Sheet 14	of 23	Drawn By J. Mead	

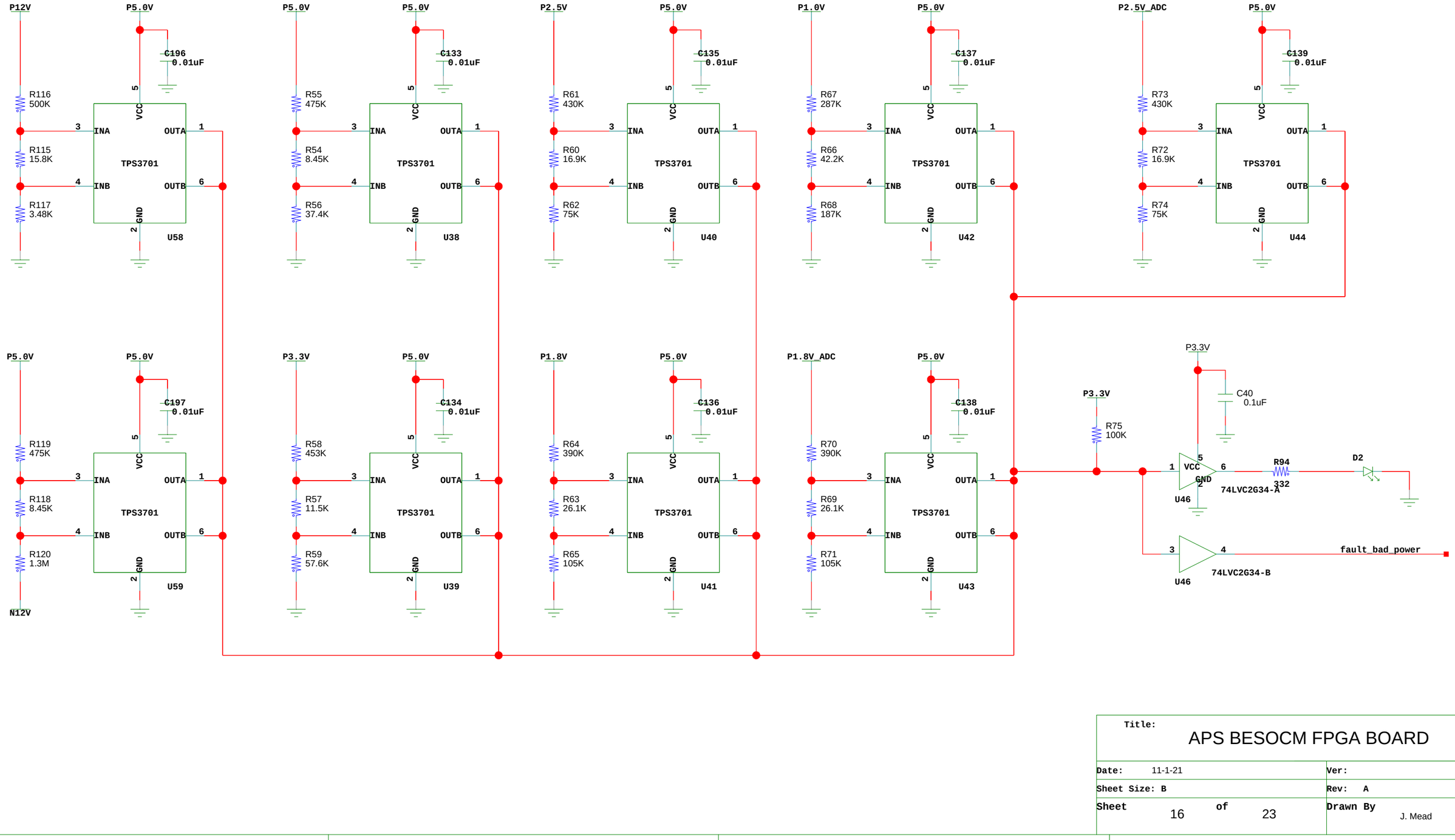
LTC2107 Linear Regulators





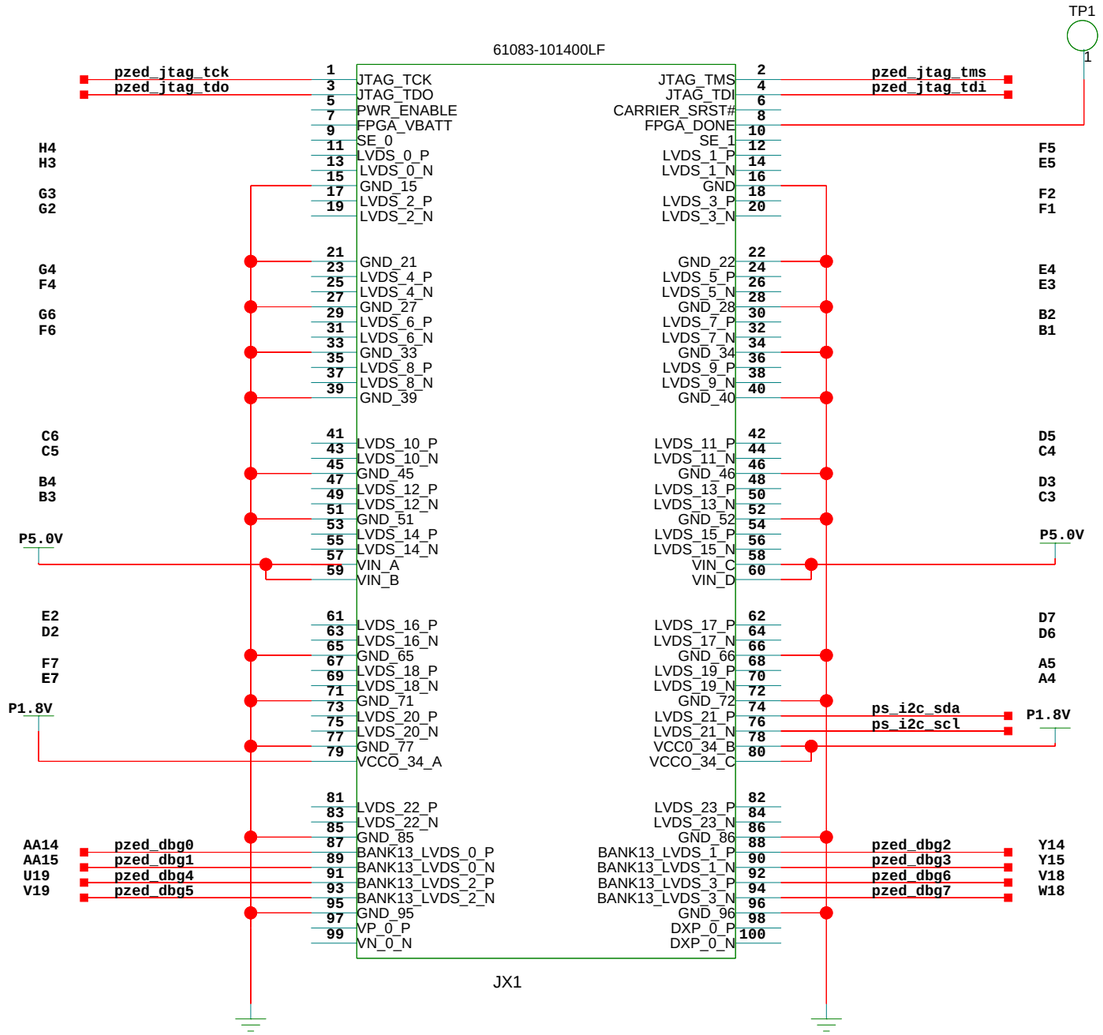
Title: APS BESOCM FPGA BOARD	
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 15 of 23	Drawn By J. Mead

Voltage OV and UV Monitors

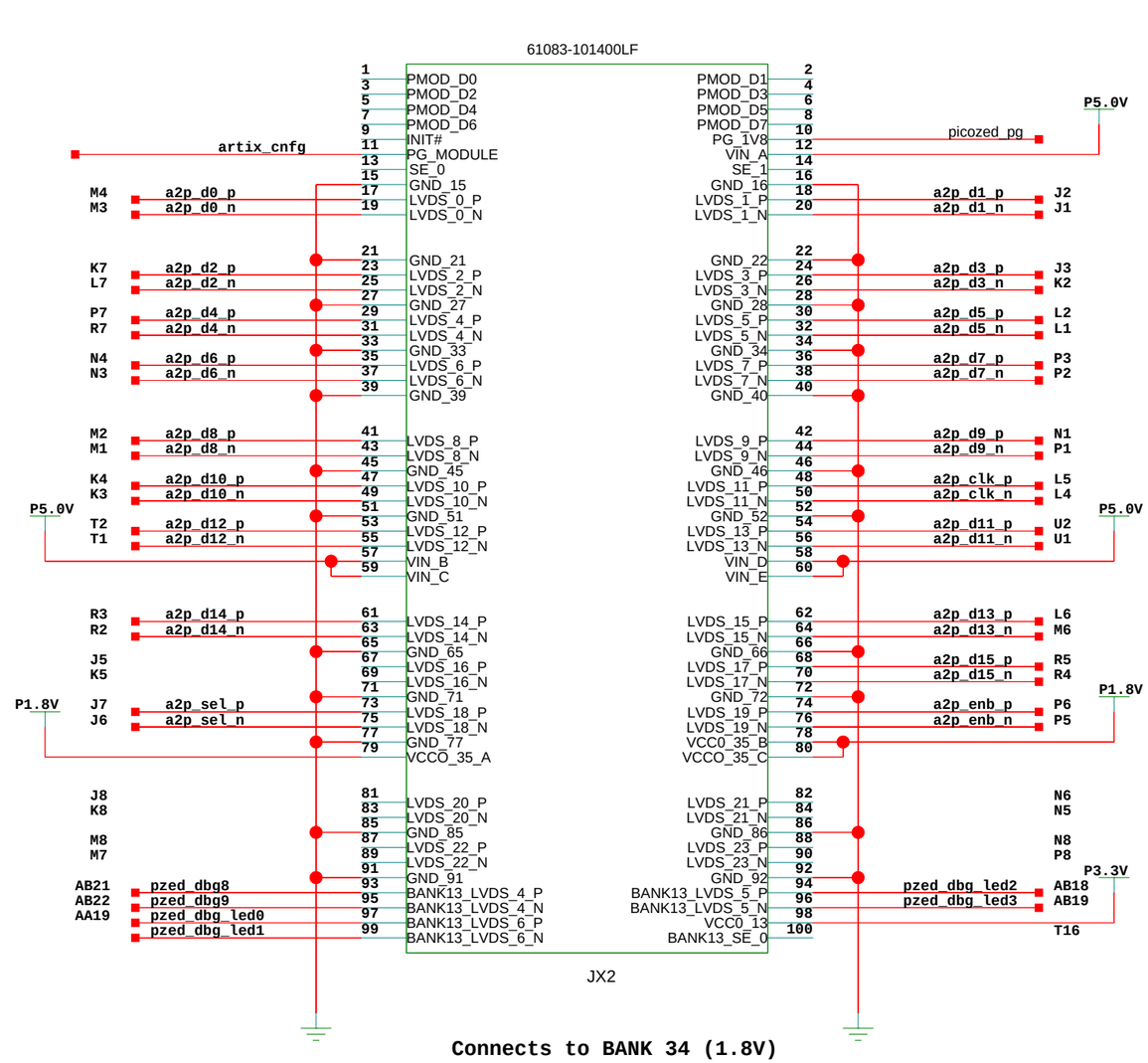


Title: APS BESOCM FPGA BOARD	
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 16 of 23	Drawn By J. Mead

picoZED Connectors JX1 & JX2



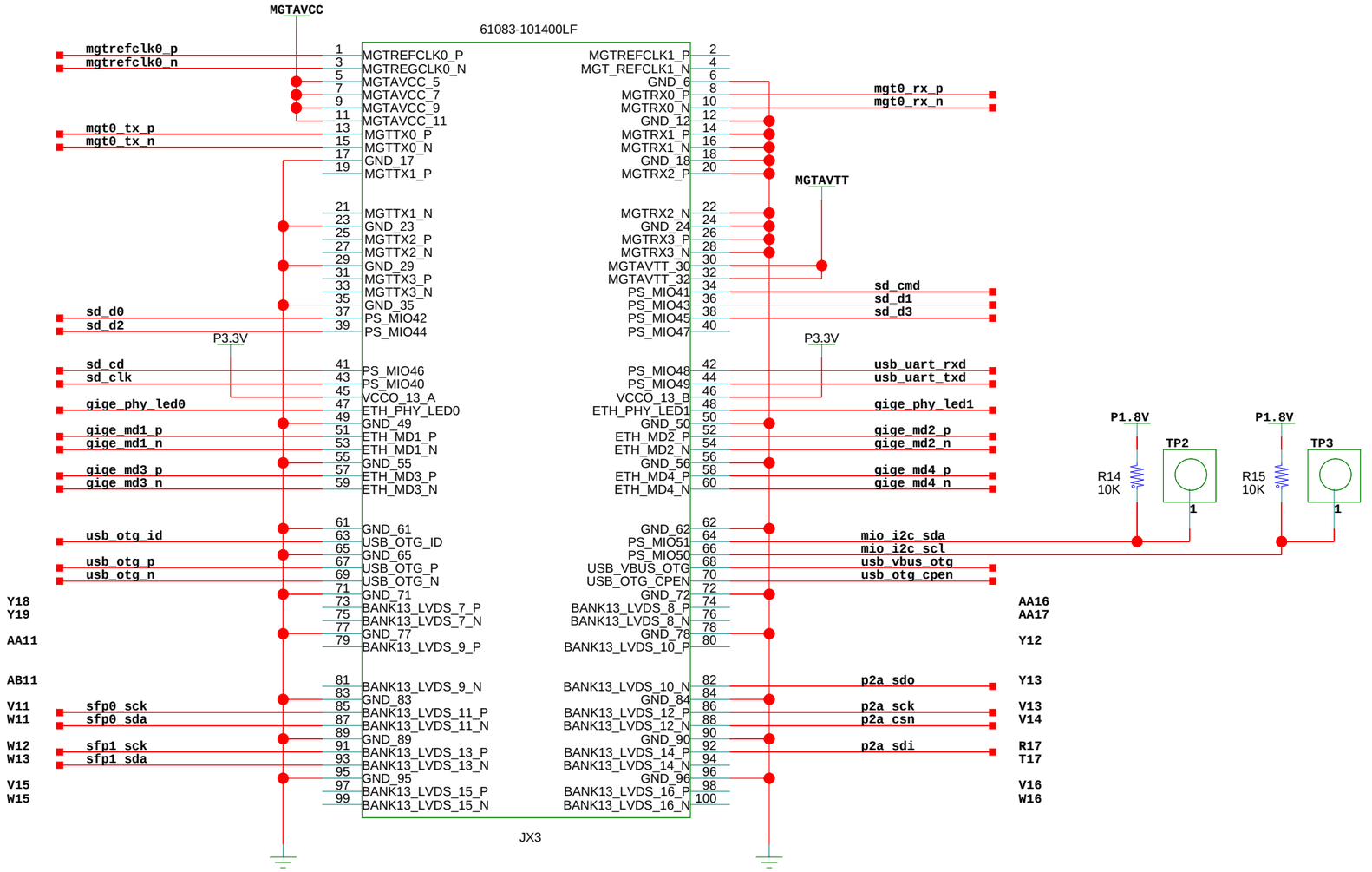
Connects to BANK 35 (1.8V) LVDS



Connects to BANK 34 (1.8V)

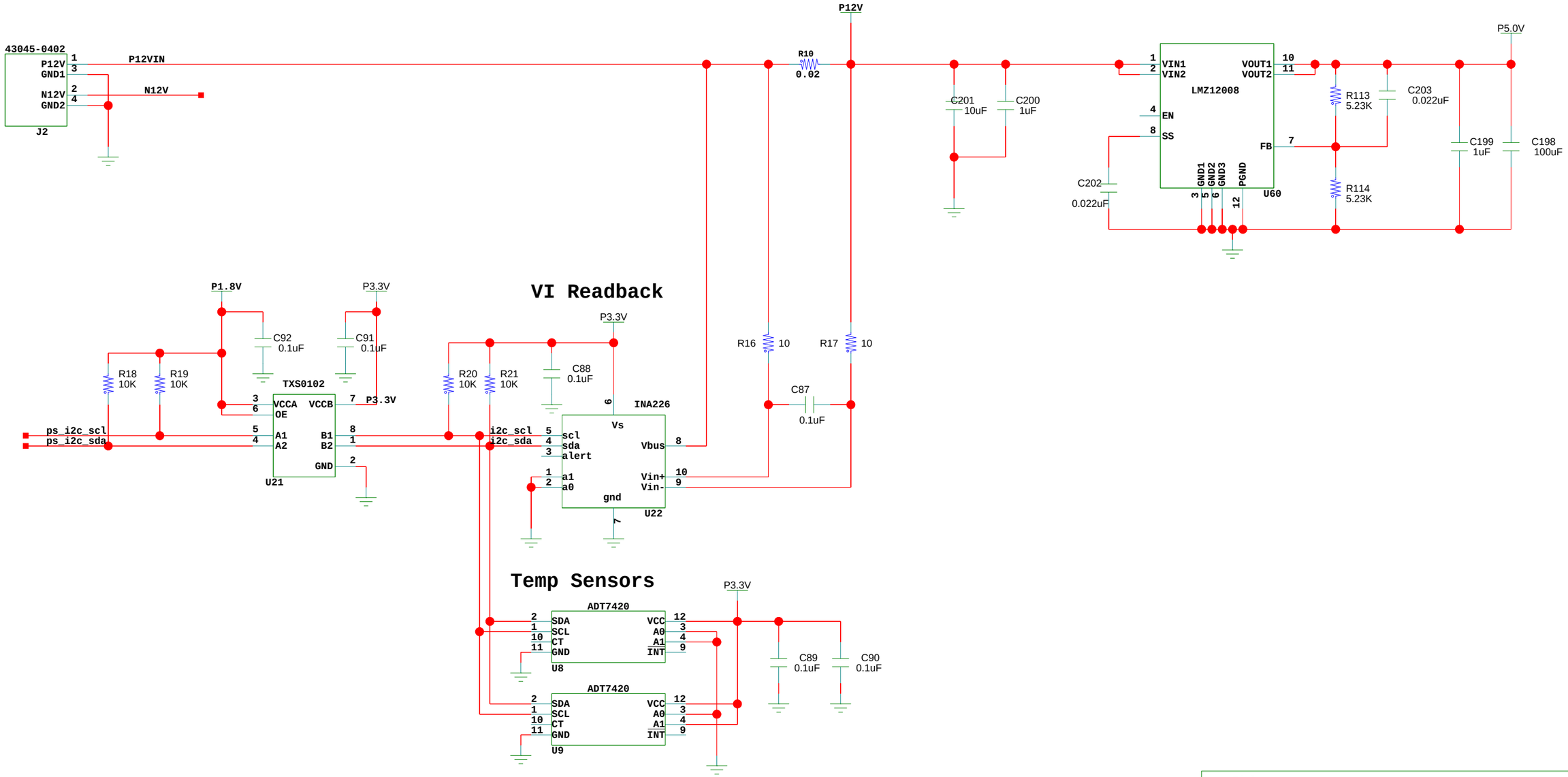
Title:	APS BESOCM FPGA BOARD		
Date:	11-1-21	**Ver:**	
Sheet Size: B		**Rev:** A	
Sheet	17 of 23	**Drawn By**	J. Mead

picoZED Connector JX3



Title: APS BESOCM FPGA BOARD			
Date: 11-1-21		Ver:	
Sheet Size: B		Rev: A	
Sheet 18	of 23	Drawn By J. Mead	

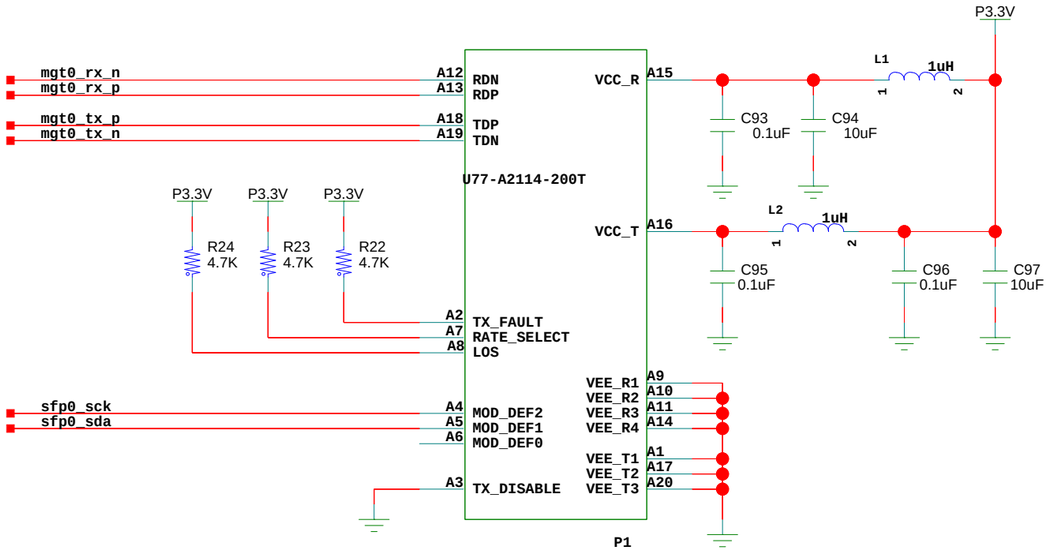
Power Input



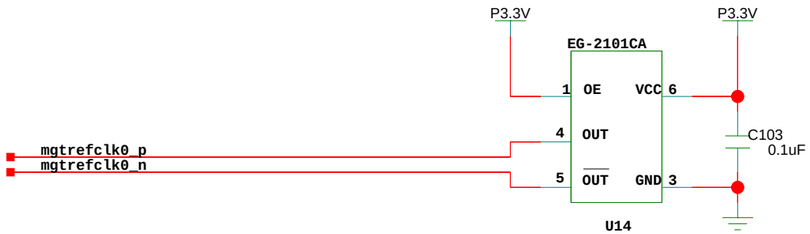
Title:	APS BESOCM FPGA BOARD
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 19 of 23	Drawn By J. Mead

SFP Connecters

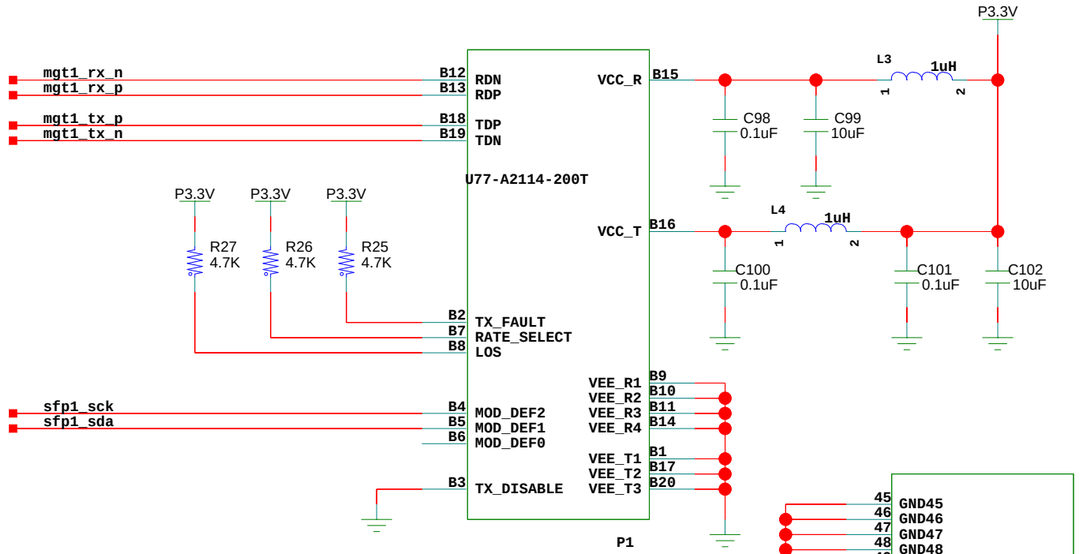
Event Receiver



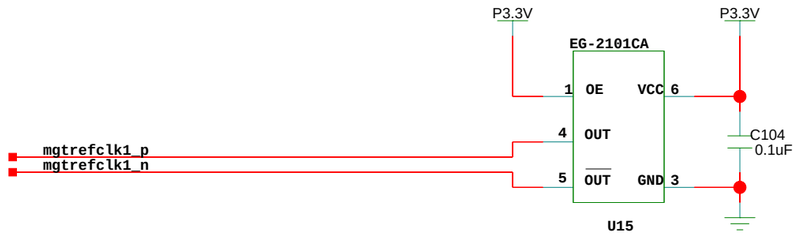
124.92MHz

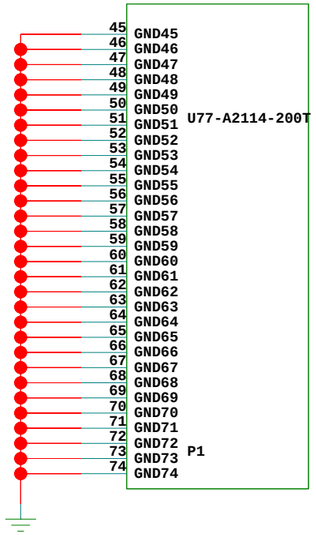


Data Transceiver



200MHz

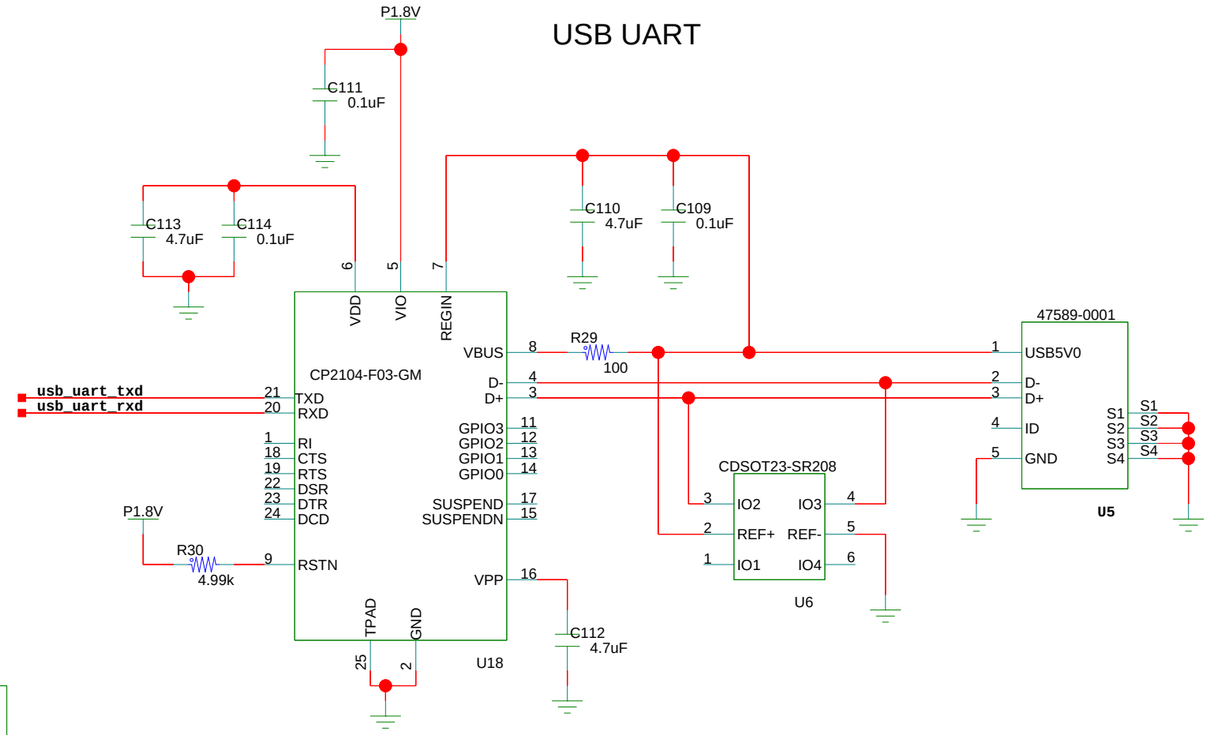




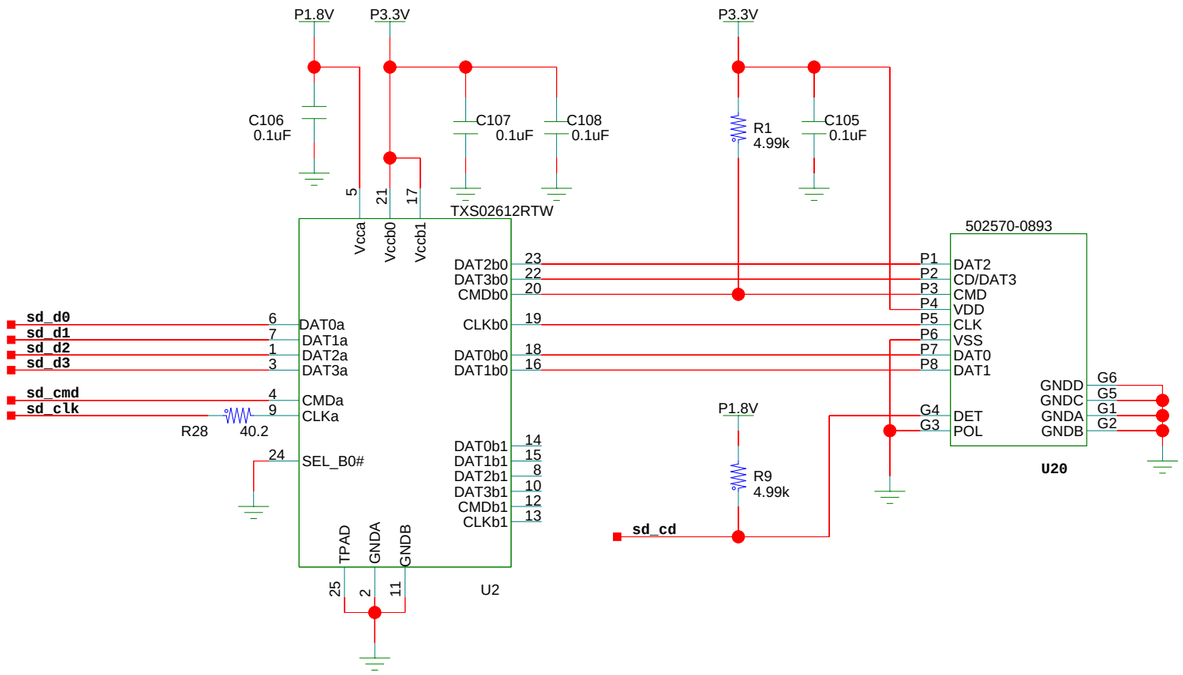
Title: APS BESOCM FPGA BOARD	
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 20 of 23	Drawn By J. Mead

Zynq Peripherals : SDCARD / UART

USB UART

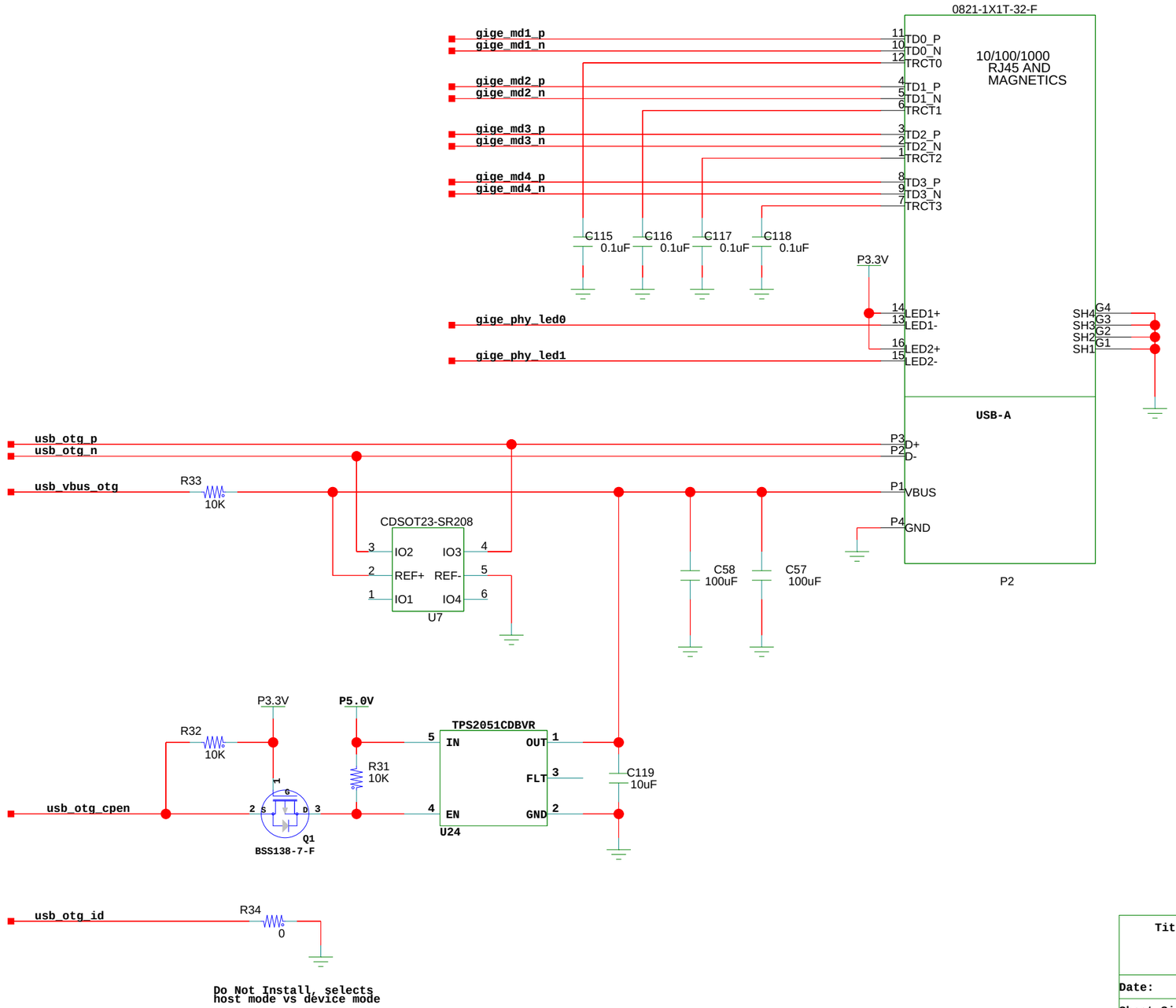


SD card



Title:	APS BESOCM FPGA BOARD		
Date:	11-1-21	**Ver:**	
Sheet Size:	B	**Rev:**	A
Sheet	21 of 23	**Drawn By**	J. Mead

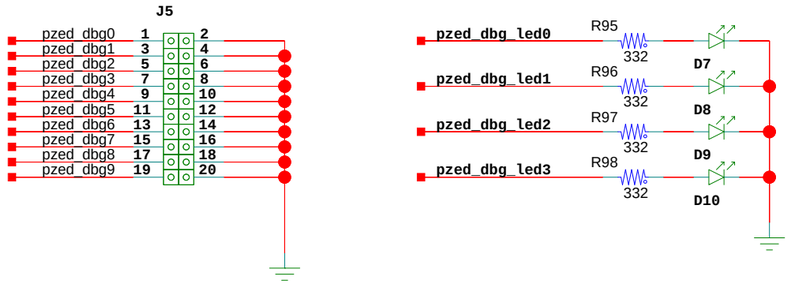
Zynq Peripherals : Gigabit Ethernet / USB



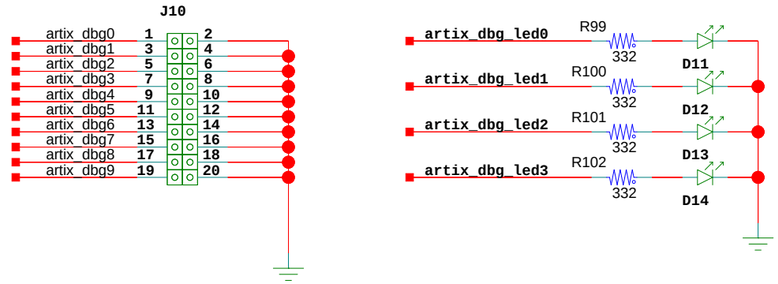
Title: APS BESOCM FPGA BOARD			
Date: 11-1-21		Ver:	
Sheet Size: B		Rev: A	
Sheet 22	of 23	Drawn By J. Mead	

Miscellaneous

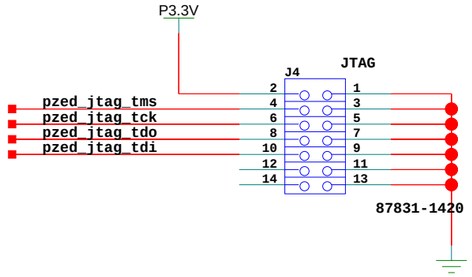
picoZed Debug Header

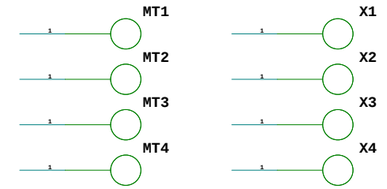


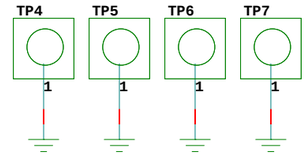
Artix Debug Header



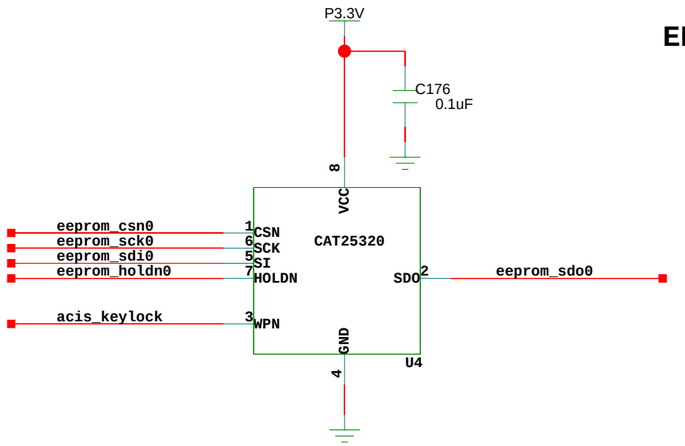
picZed JTAG Header

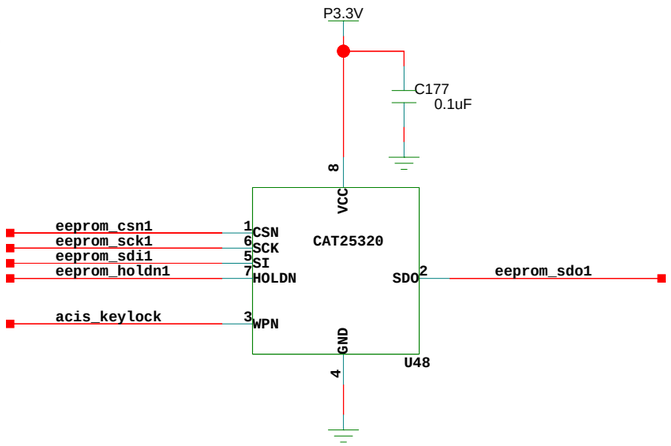






EEPROM's





Title: APS BESOCM FPGA BOARD	
Date: 11-1-21	Ver:
Sheet Size: B	Rev: A
Sheet 23 of 23	Drawn By J. Mead