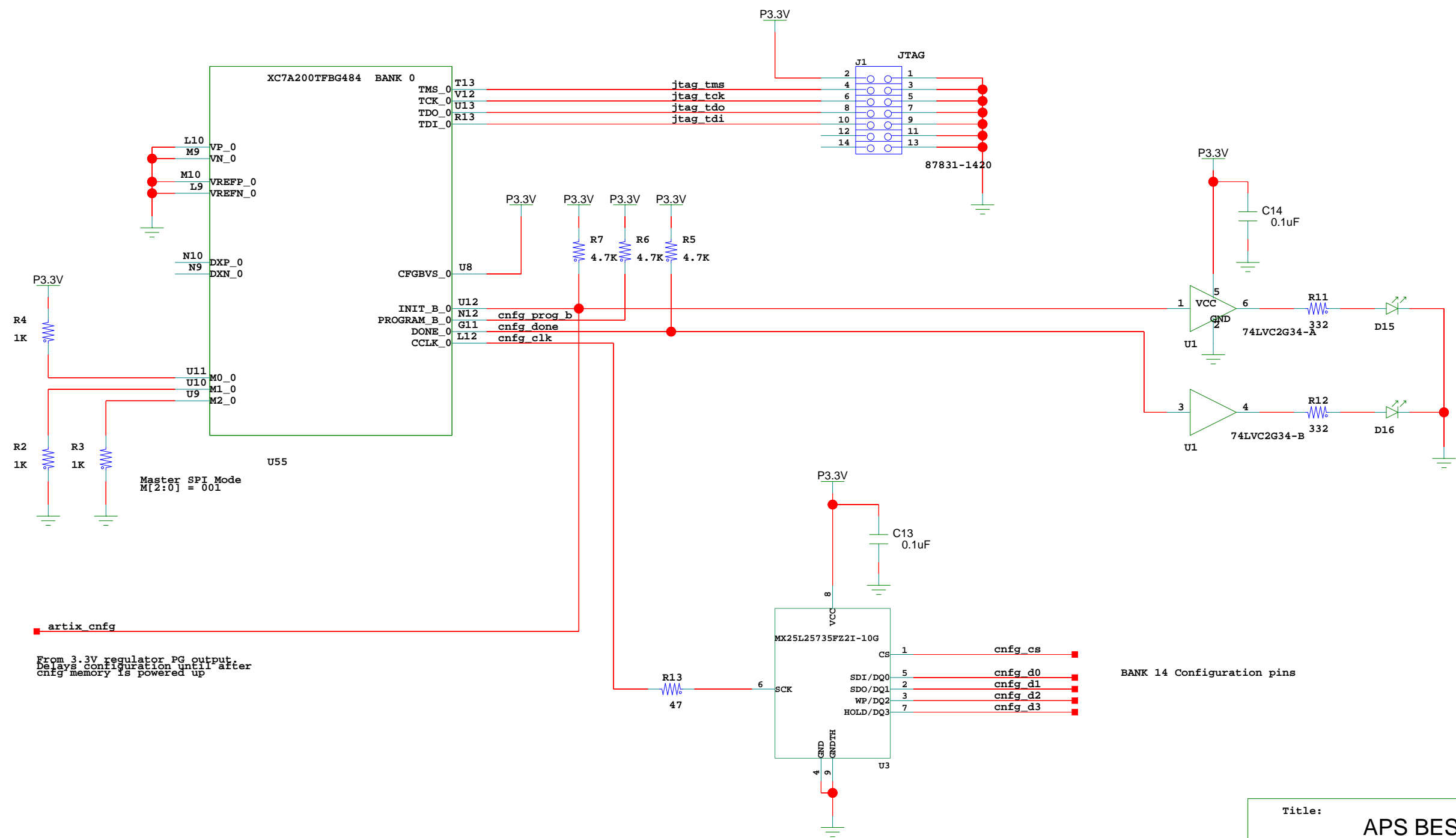


Artix 7 FPGA Configuration

JTAG Header

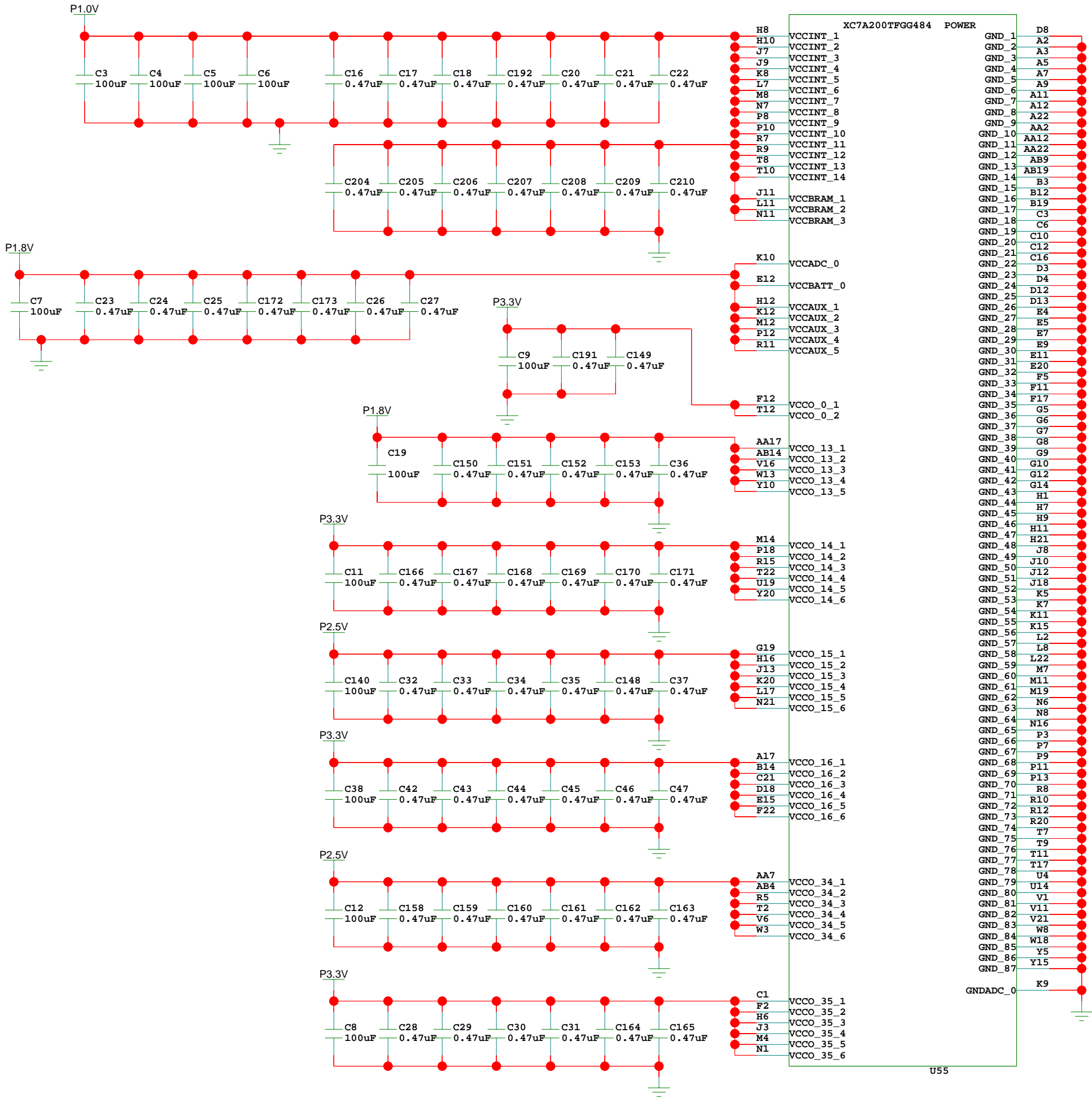


From 3.3V regulator PG output.
Delays configuration until after
cnfg memory is powered up

BANK 14 Configuration pins

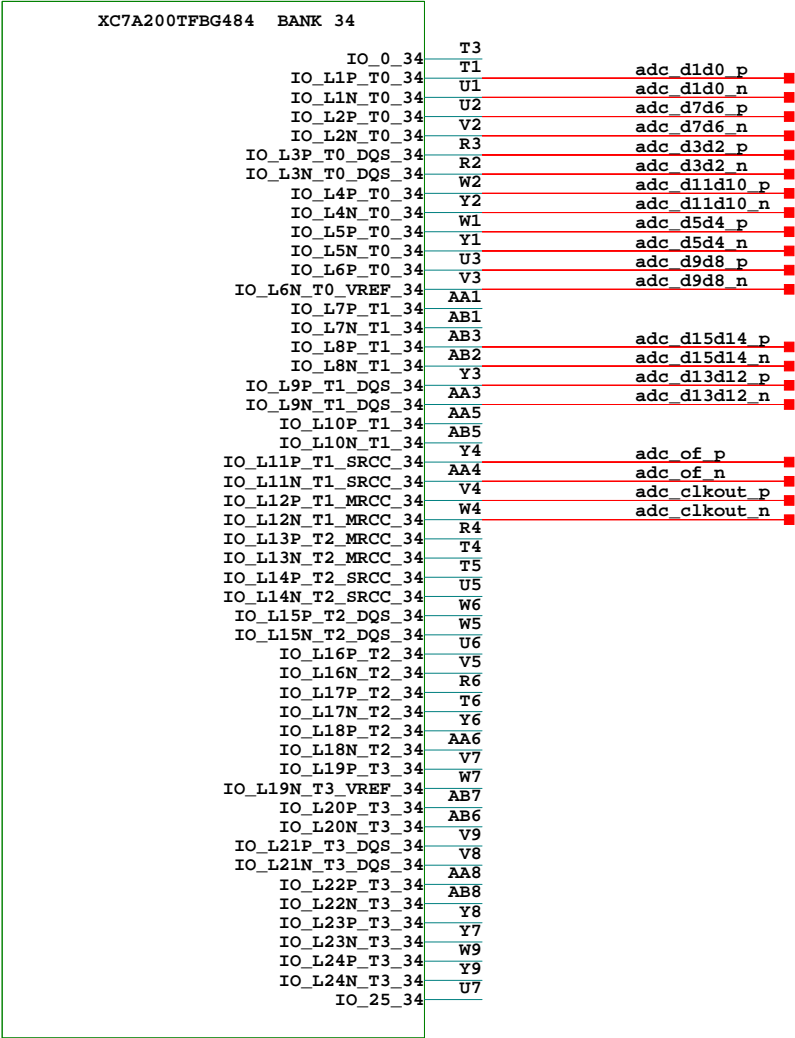
Title: APS BESOCM FPGA BOARD			
Date: 8-22-22		Ver: B	
Sheet Size: B		Rev: B	
Sheet 2 of 23		Drawn By J. Mead	

Artix 7 FPGA Power

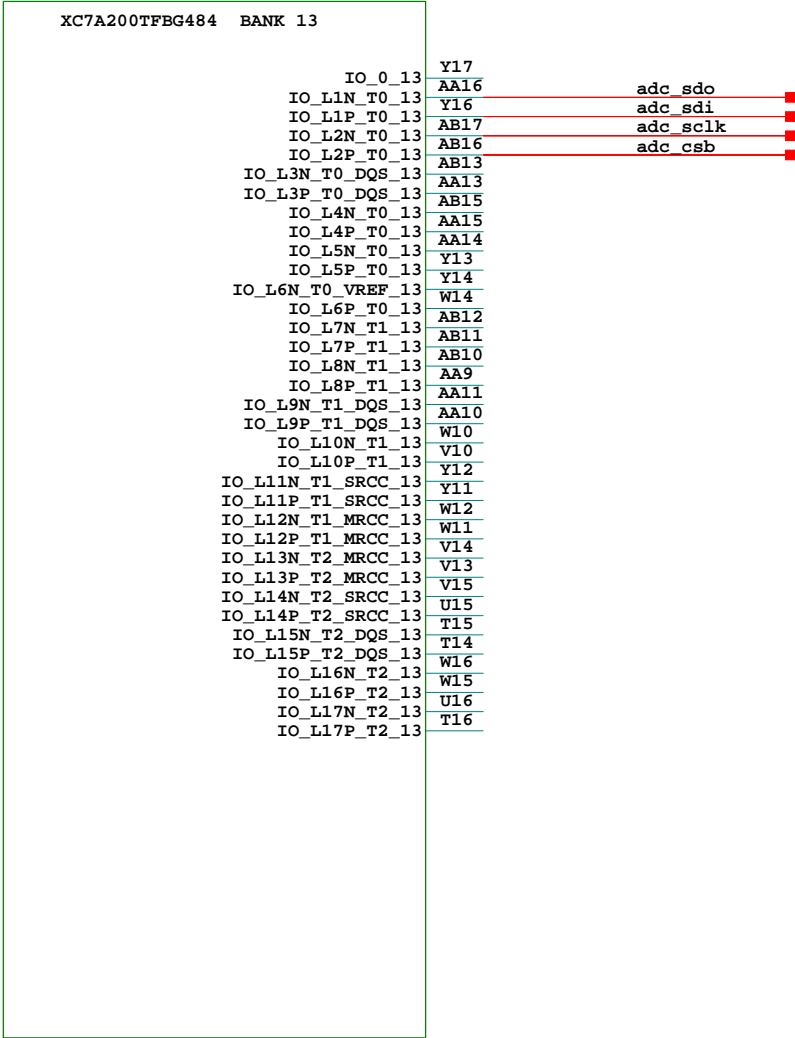


Title: APS BESOCM FPGA BOARD	
Date: 8-22-22	Ver:
Sheet Size: B	Rev: B
Sheet 3 of 23	Drawn By J. Mead

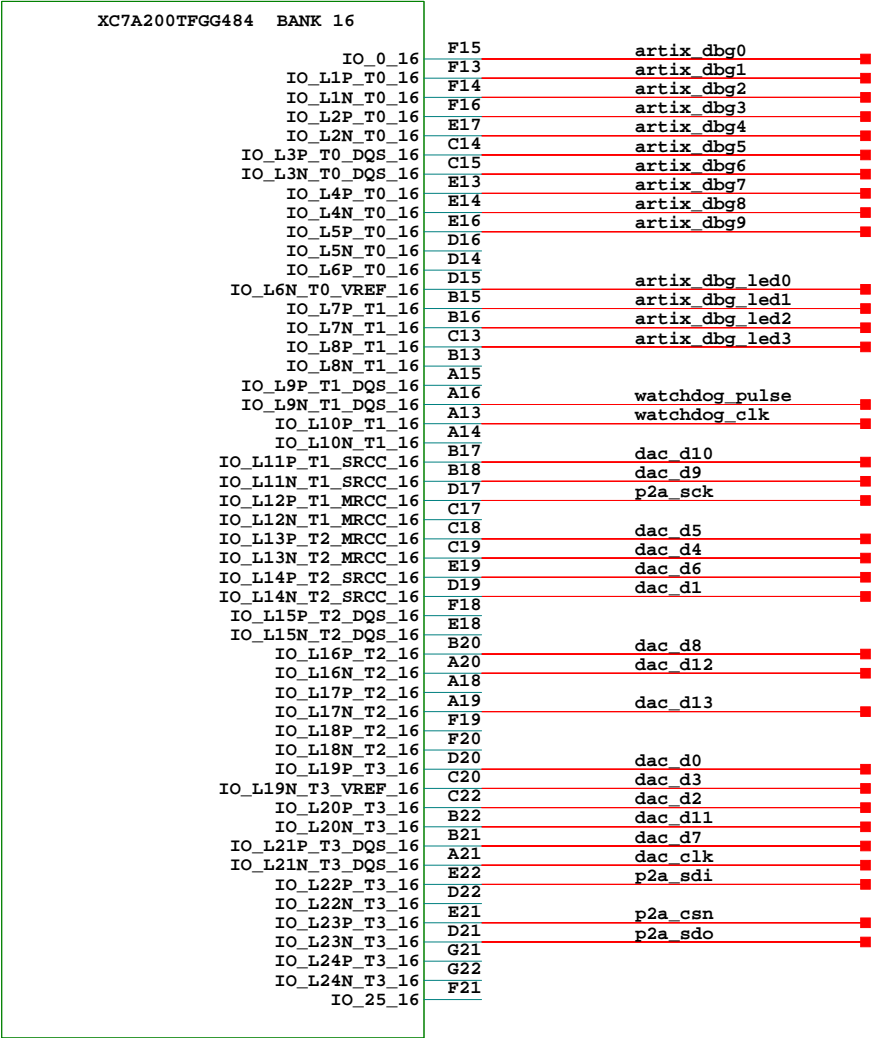
Artix 7 FPGA I/O



U55



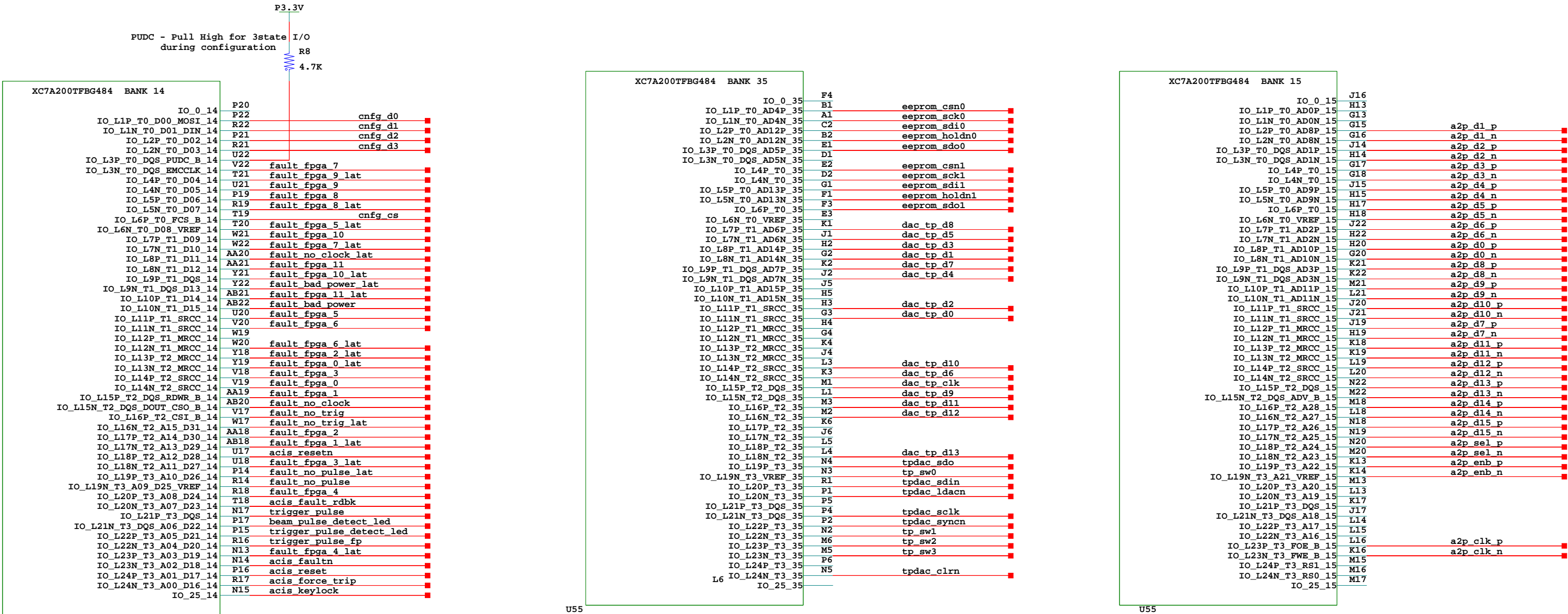
U55



U55

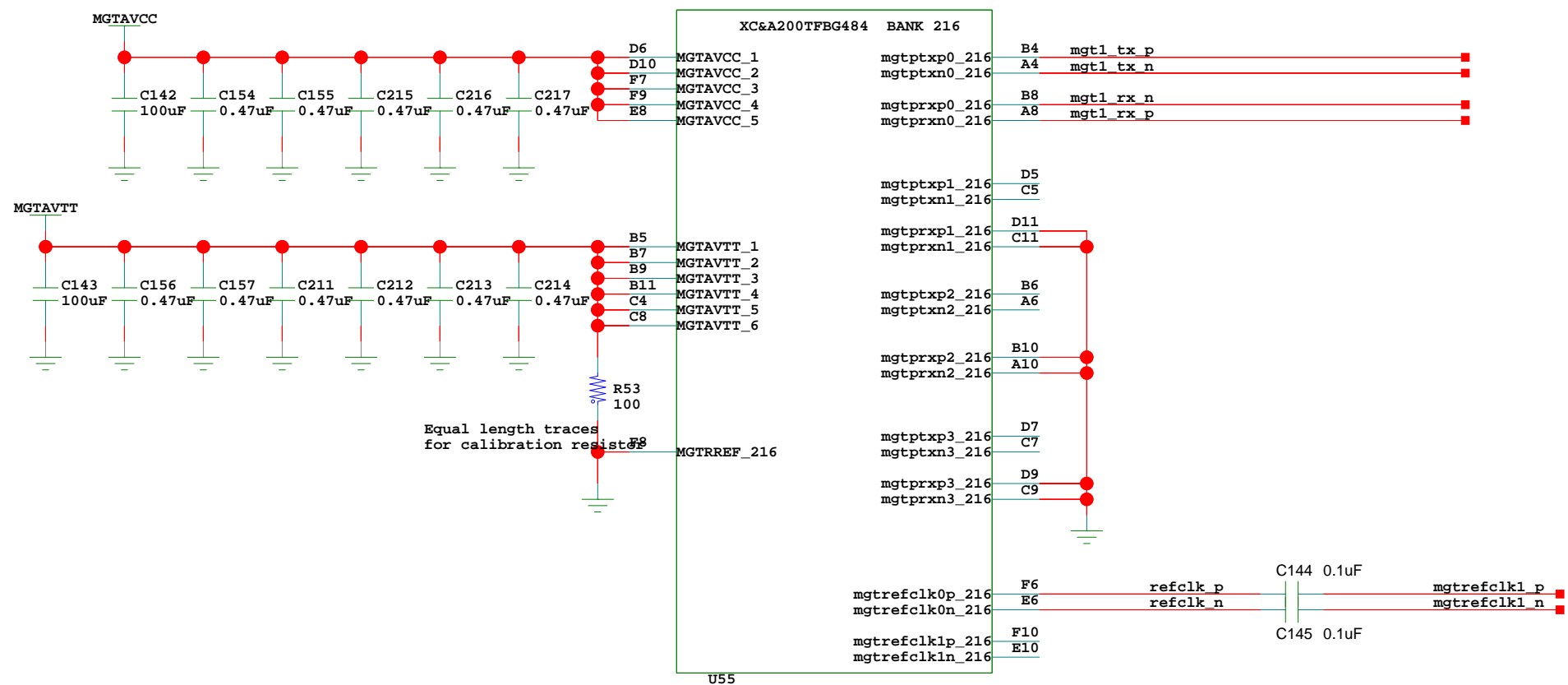
Title: APS BESOCM FPGA BOARD			
Date: 8-22-22			Ver:
Sheet Size: B			Rev: B
Sheet 4 of 23	Drawn By J. Mead		

Artix 7 FPGA I/O



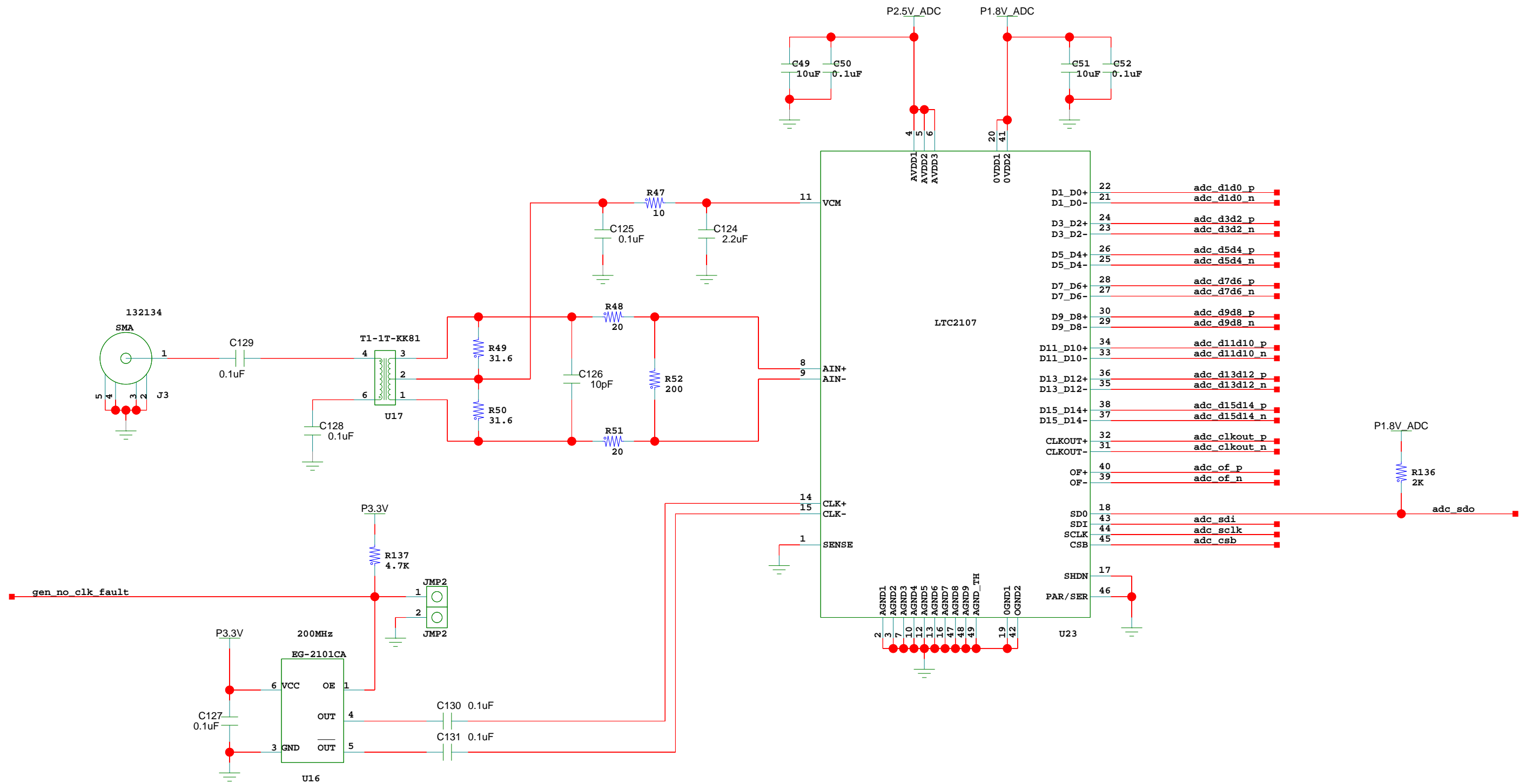
Title: APS BESOCM FPGA BOARD			
Date: 8-22-22	Ver:		
Sheet Size: B	Rev: B		
Sheet 5 of 23	Drawn By J. Mead		

Artix 7 FPGA MGT



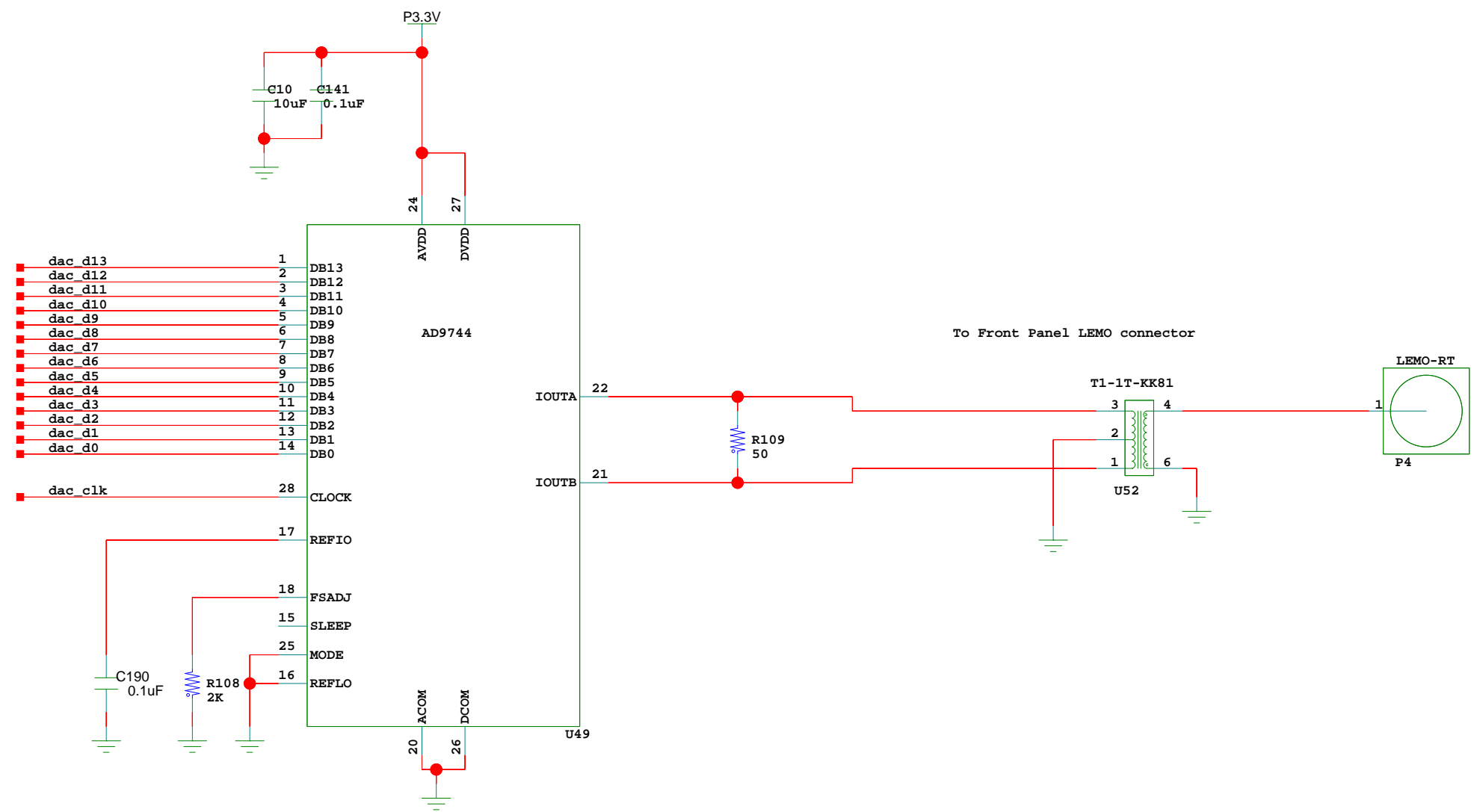
Title: APS BESOCM FPGA BOARD			
Date: 8-22-22	Rev: B		Ver: B
Sheet 6 of 23	Drawn By J. Mead		

LTC2107 ADC



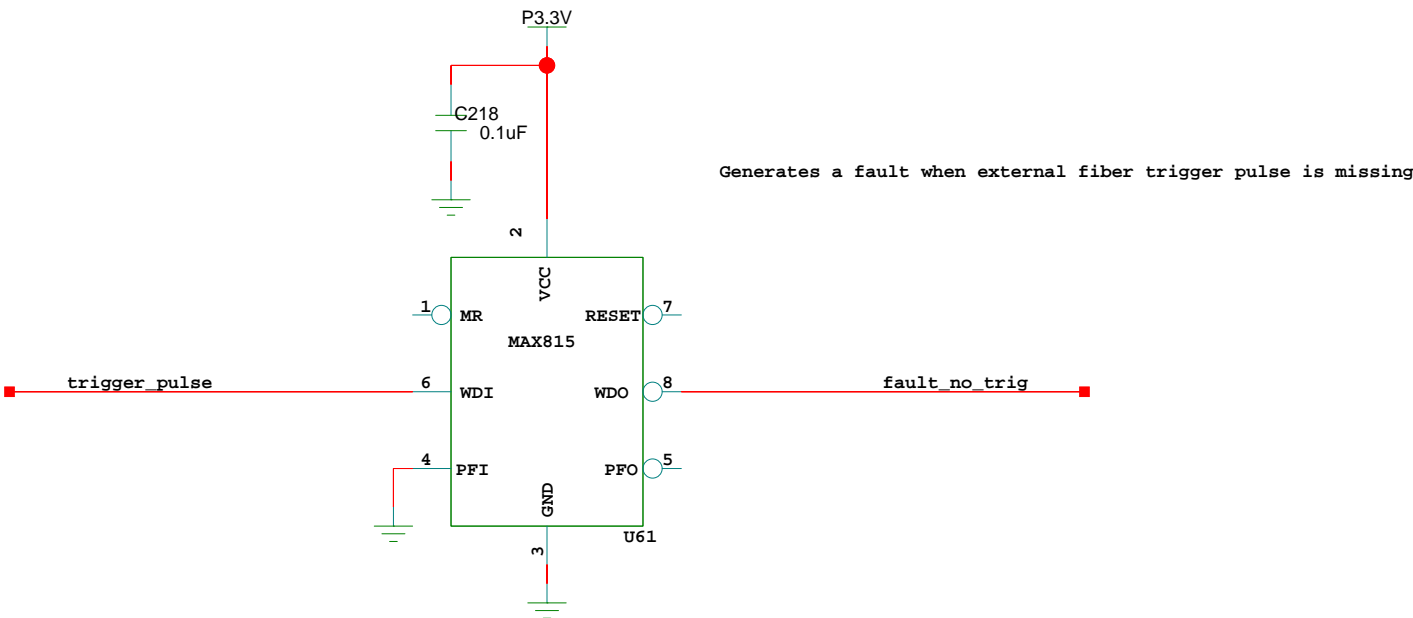
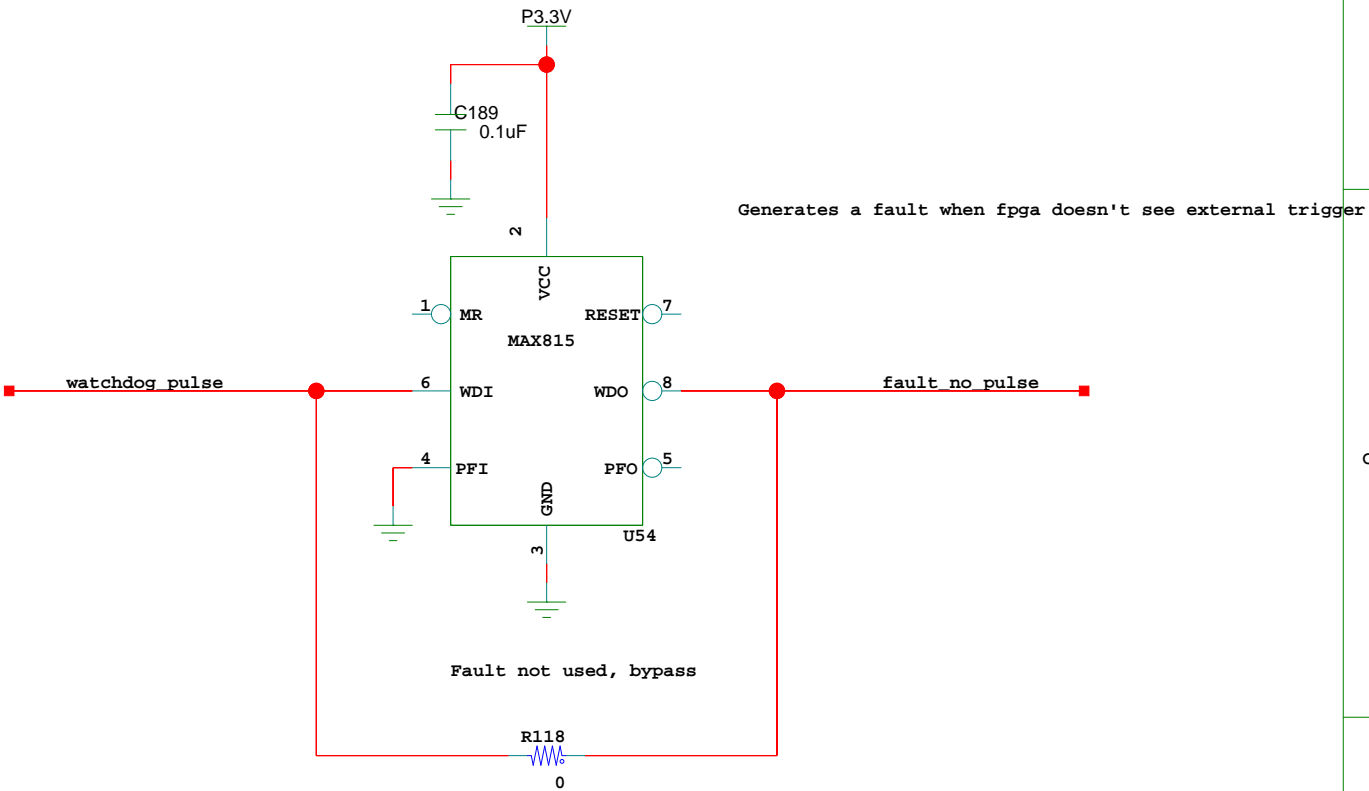
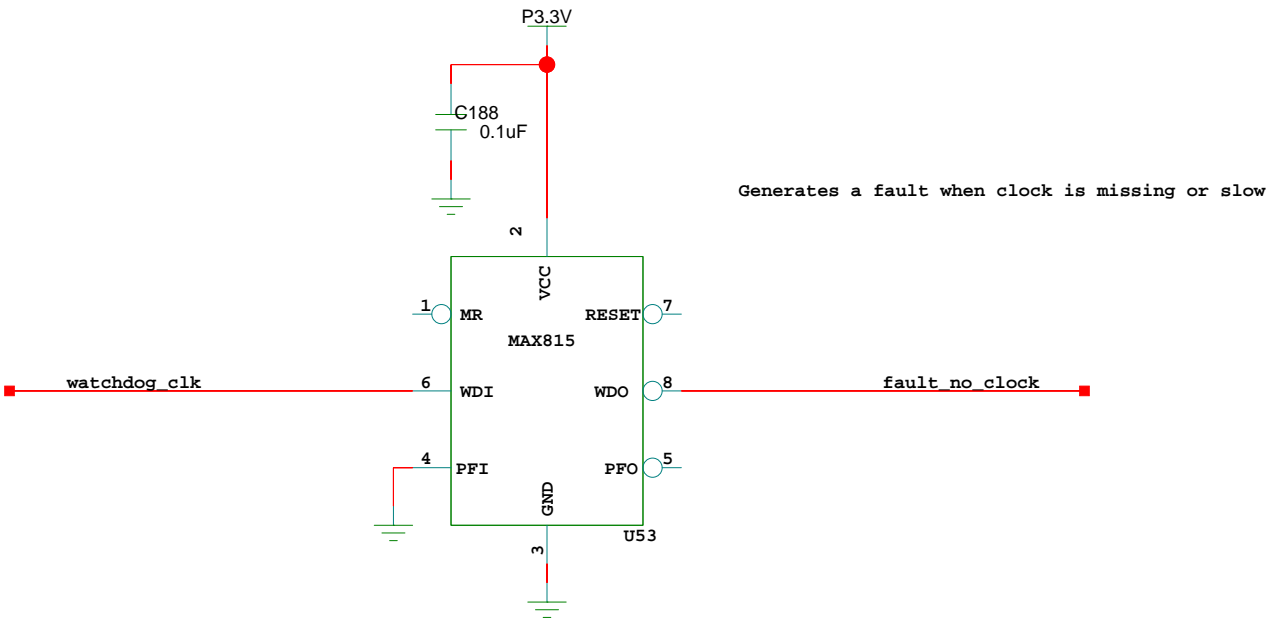
Title:		APS BESOCM FPGA BOARD	
Date:	8-22-22	Ver:	
Sheet Size:	B	Rev:	B
Sheet	7 of 23	Drawn By	J. Mead

Raw ADC Front Panel Test Port AD9744 DAC



Title: APS BESOCM FPGA BOARD	
Date: 8-22-22	Ver: B
Sheet Size: B	Rev: B
Sheet 8 of 23	Drawn By J. Mead

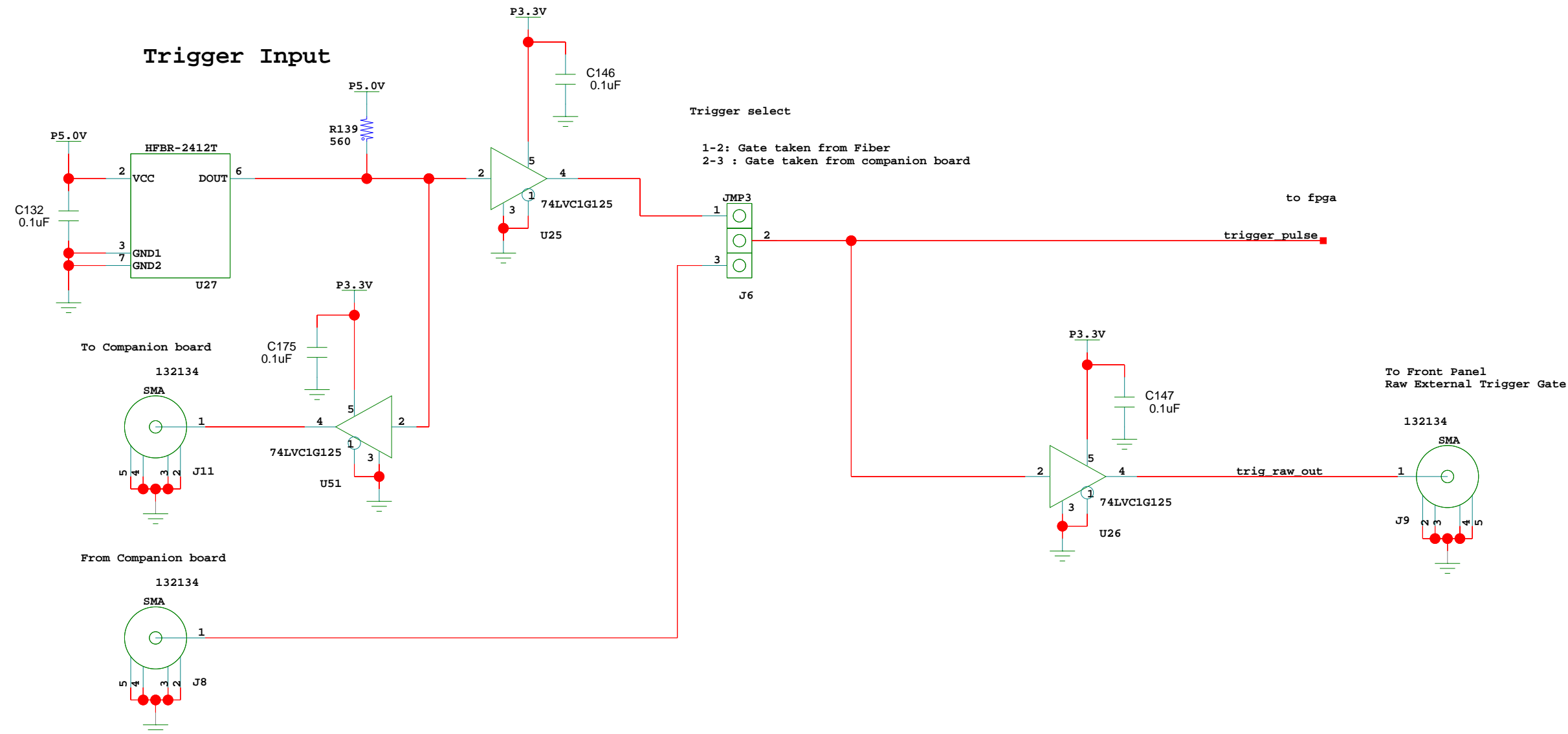
Clock and Gate Watch Dog Timers



Title:		APS BESOCM FPGA BOARD	
Date:	8-22-22	Ver:	
Sheet Size:	B	Rev:	B
Sheet	10 of 23	Drawn By	J. Mead

Fiber Trigger Input

Trigger Input

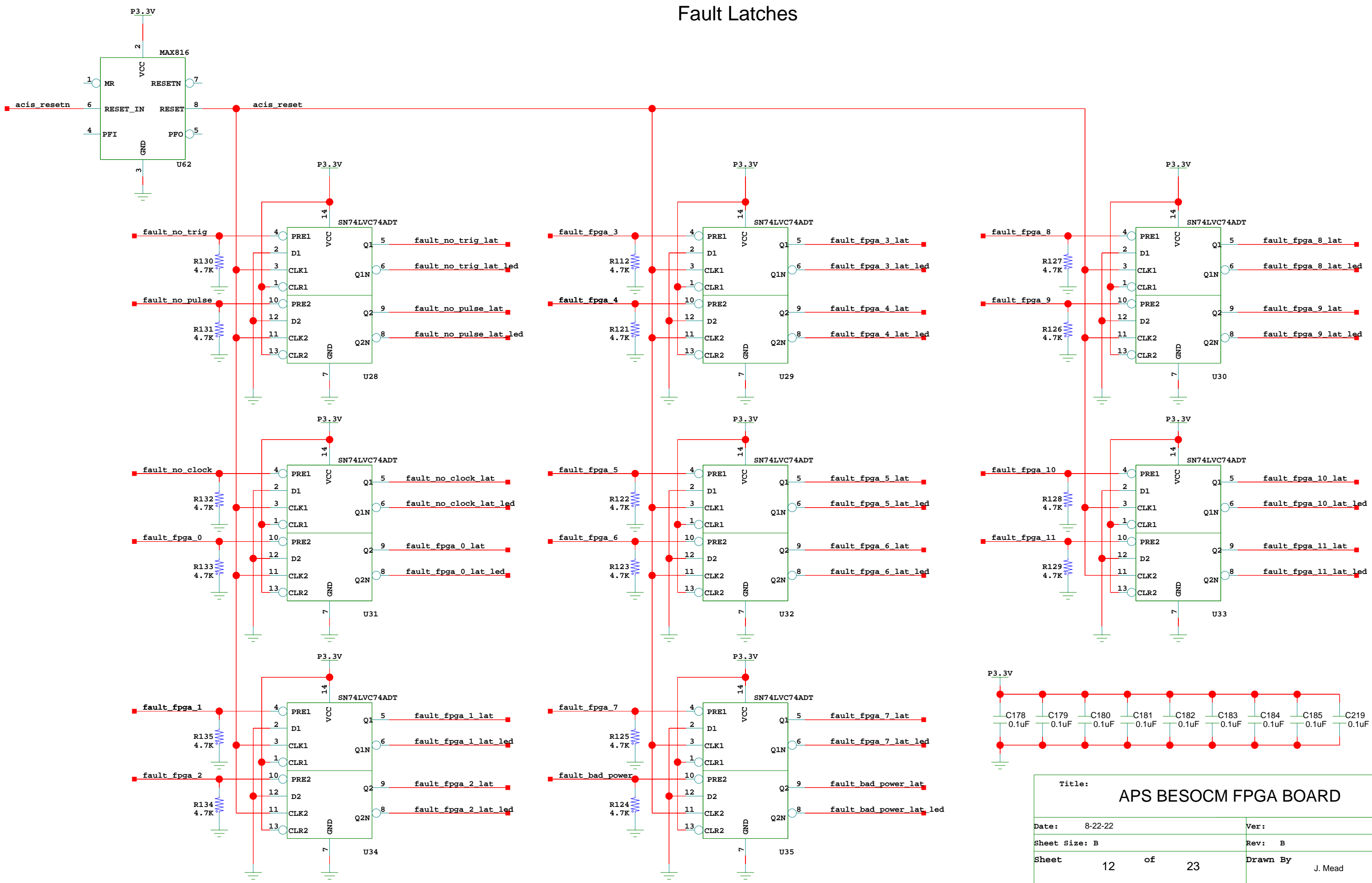


Trigger & Beam Status LEDs



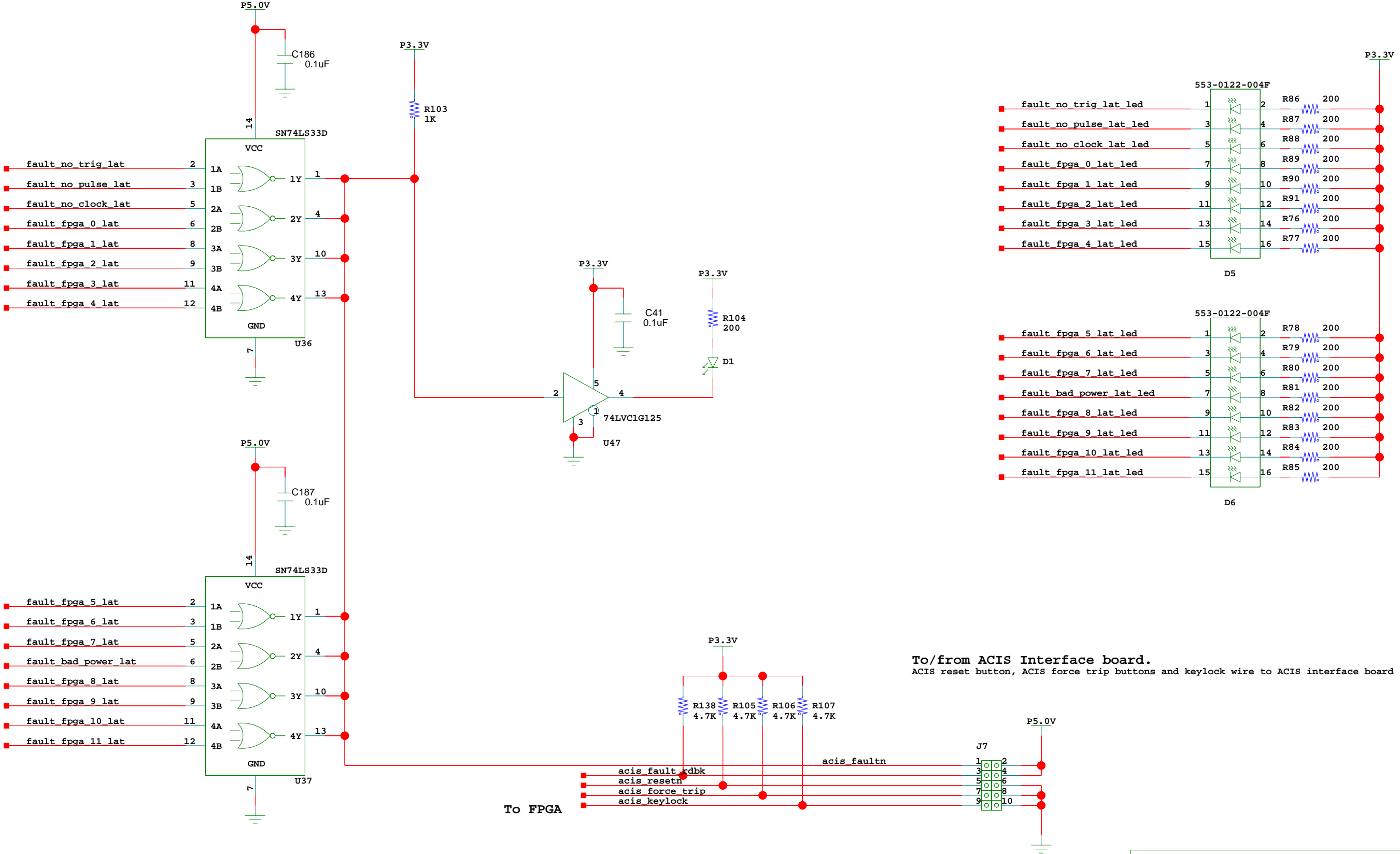
Title: APS BESOCM FPGA BOARD			
Date: 8-22-22	Ver: B		
Sheet Size: B	Rev: B		
Sheet 11 of 23	Drawn By J. Mead		

Fault Latches



Title: APS BESOCM FPGA BOARD			
Date: 8-22-22		Ver:	
Sheet Size: B		Rev: B	
Sheet	12	of	23
Drawn By		J. Mead	

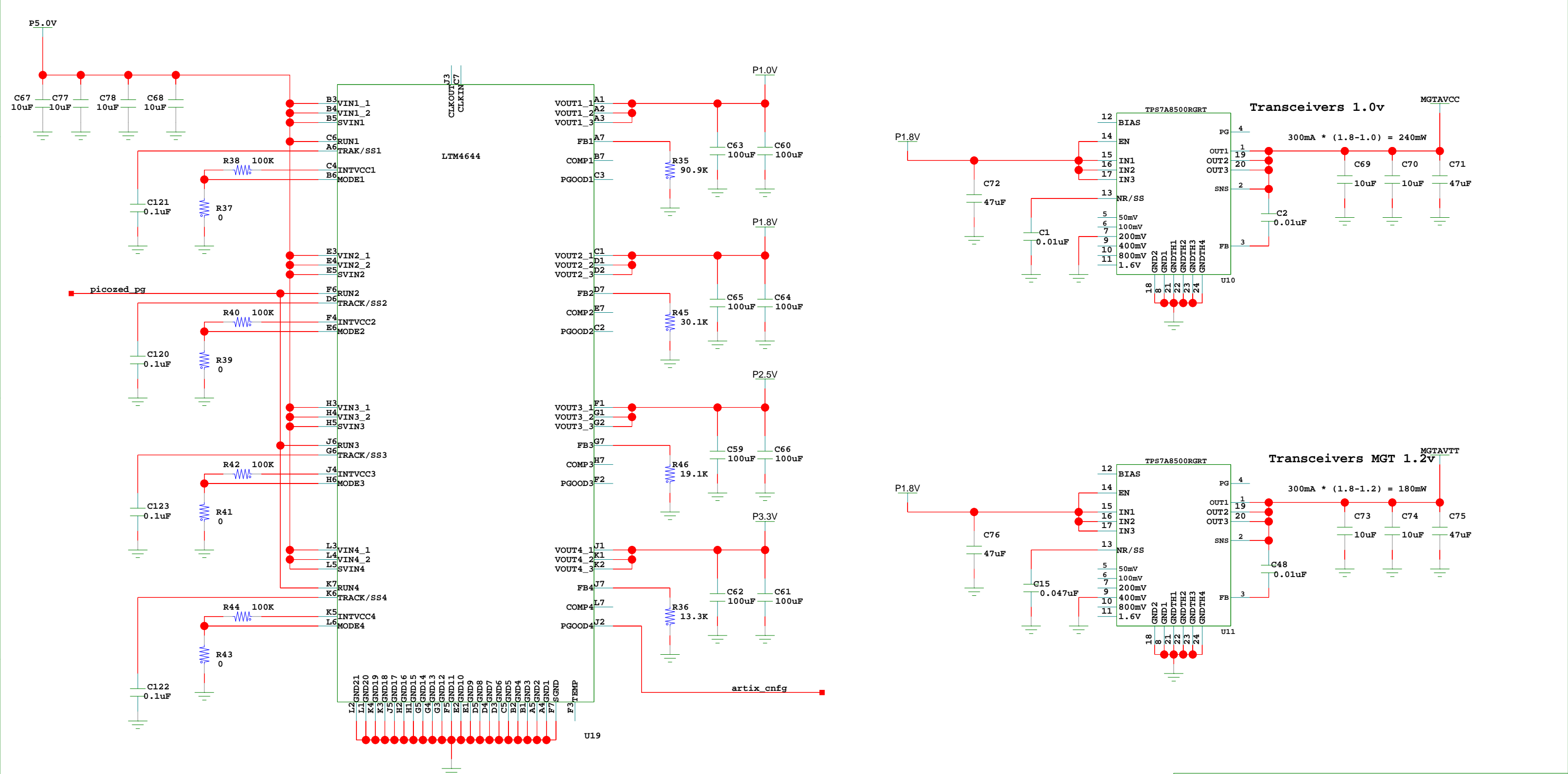
ACIS Fault



To/from ACIS Interface board.
ACIS reset button, ACIS force trip buttons and keylock wire to ACIS interface board

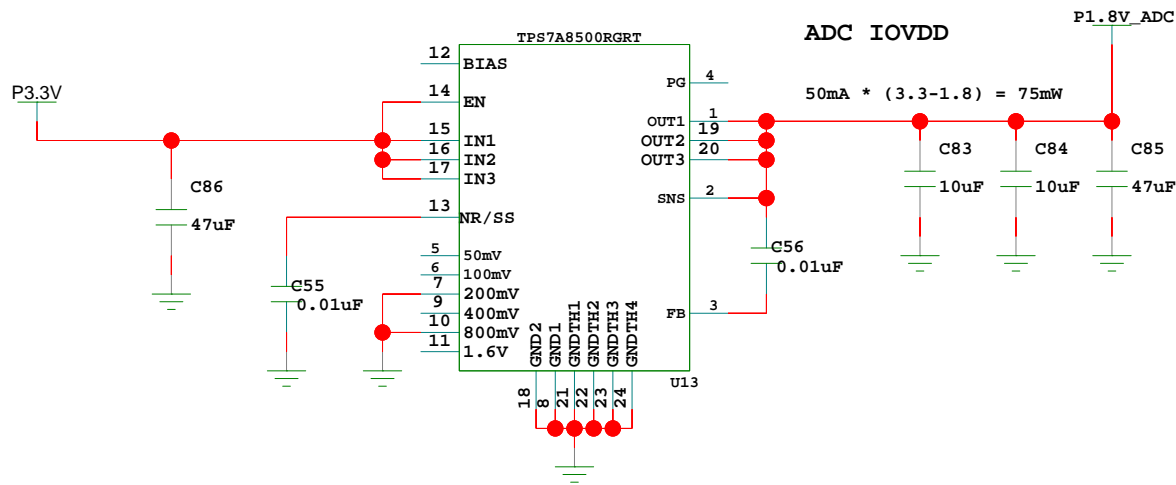
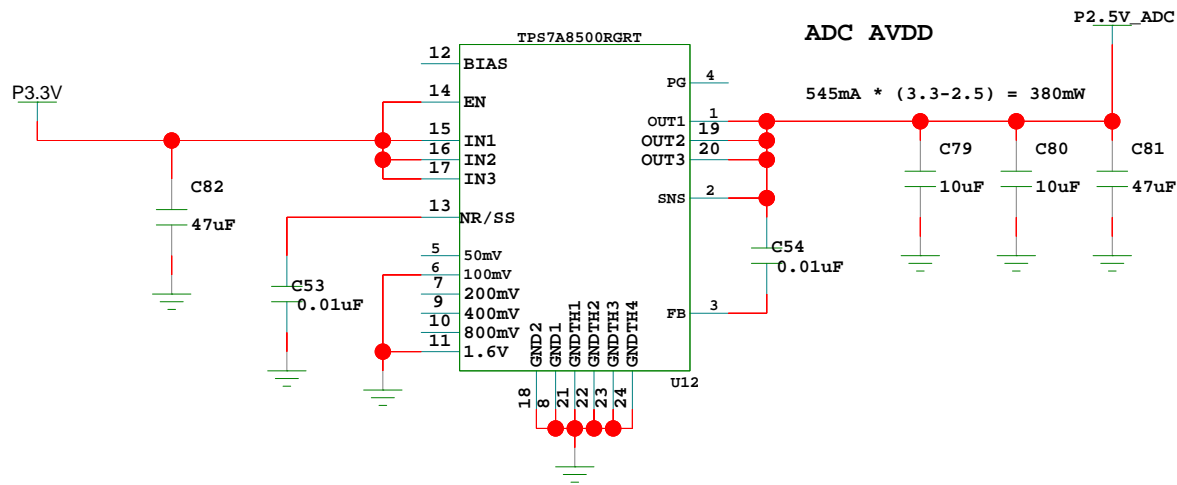
Title: APS BESOCM FPGA BOARD			
Date: 8-22-22	Ver:		
Sheet Size: B	Rev: B		
Sheet 13 of 23	Drawn By J. Mead		

Artix and picoZed Regulators



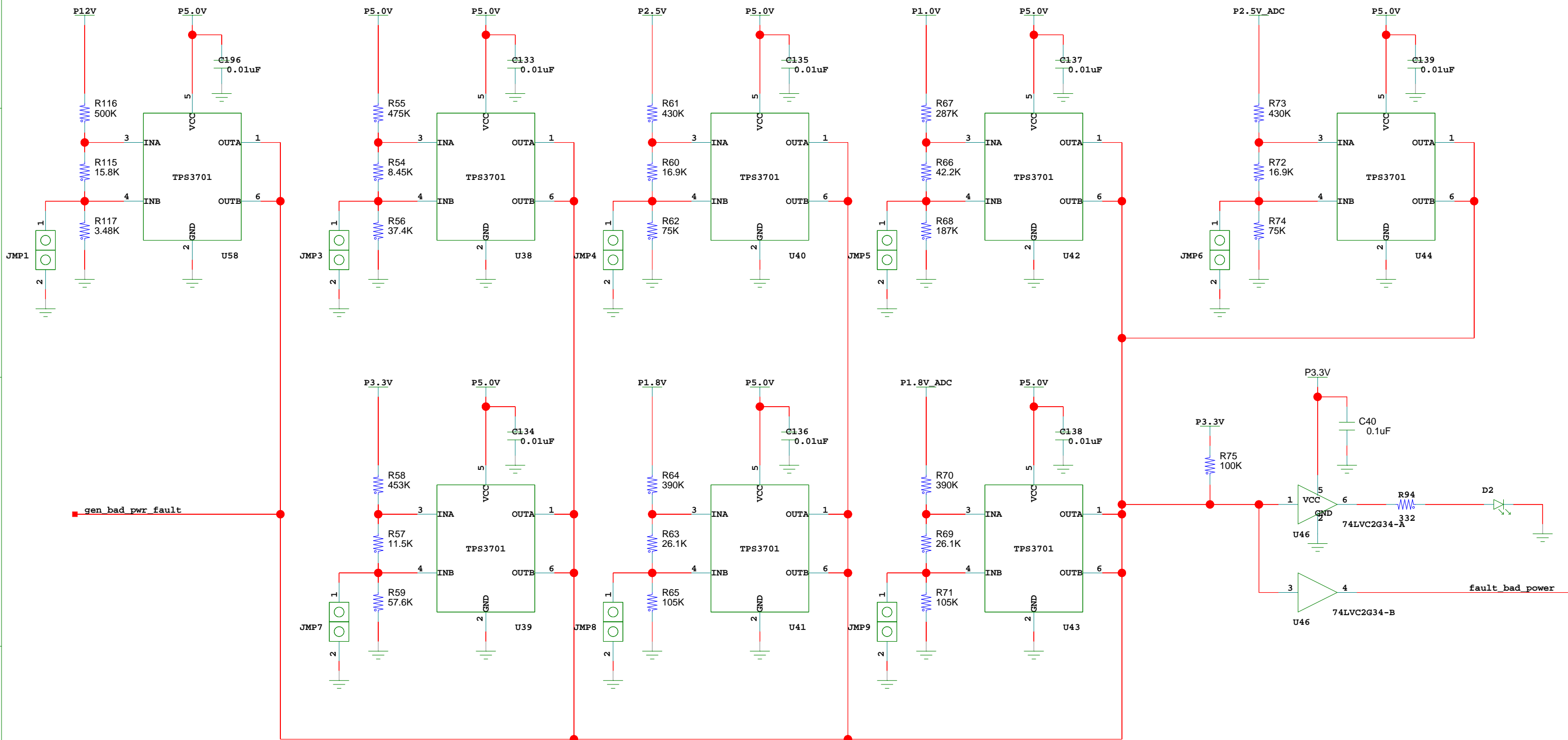
Title:		APS BESOCM FPGA BOARD	
Date:	8-22-22	Ver:	
Sheet Size:	B	Rev:	B
Sheet	14	of	23
Drawn By		J. Mead	

LTC2107 Linear Regulators



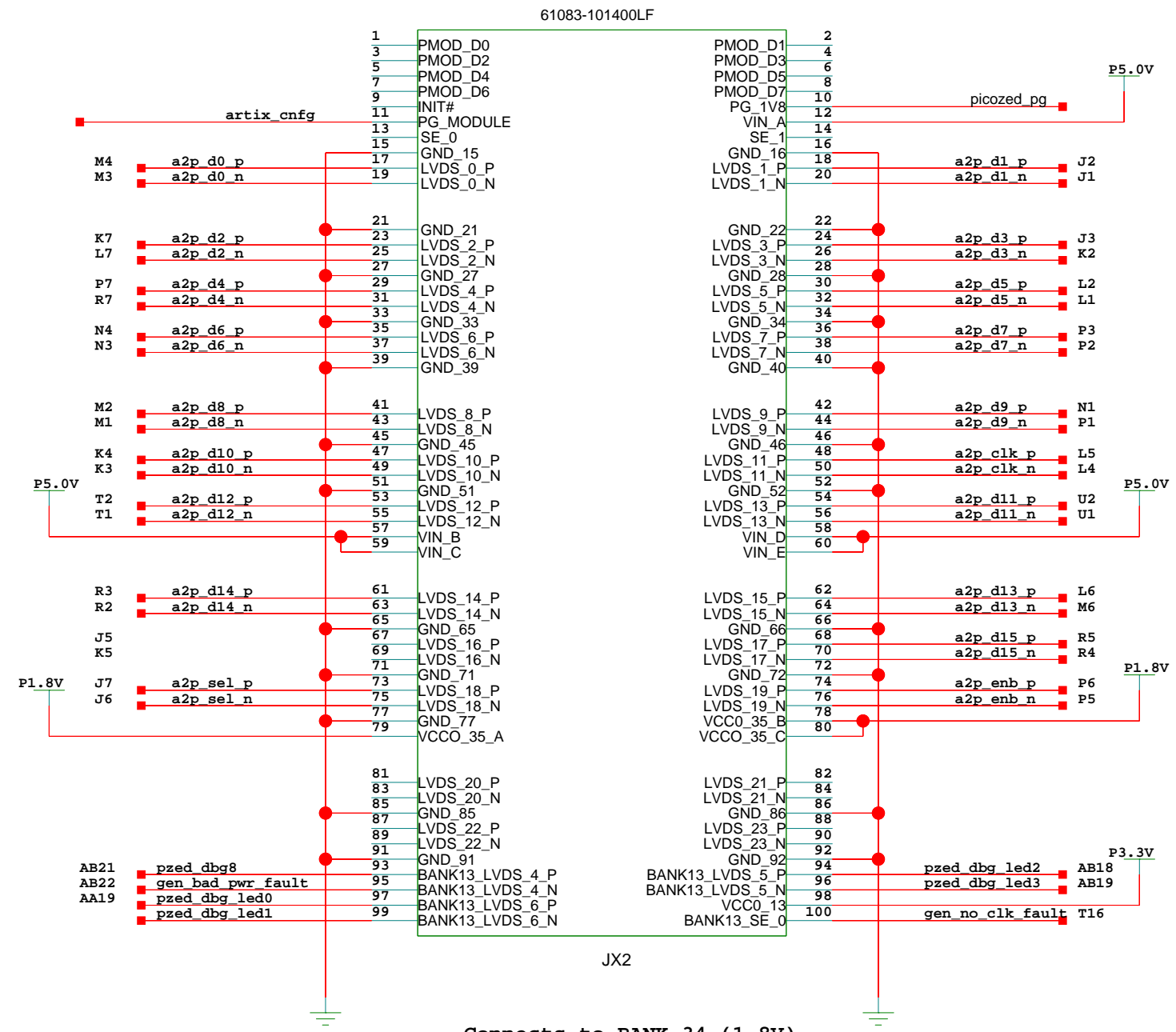
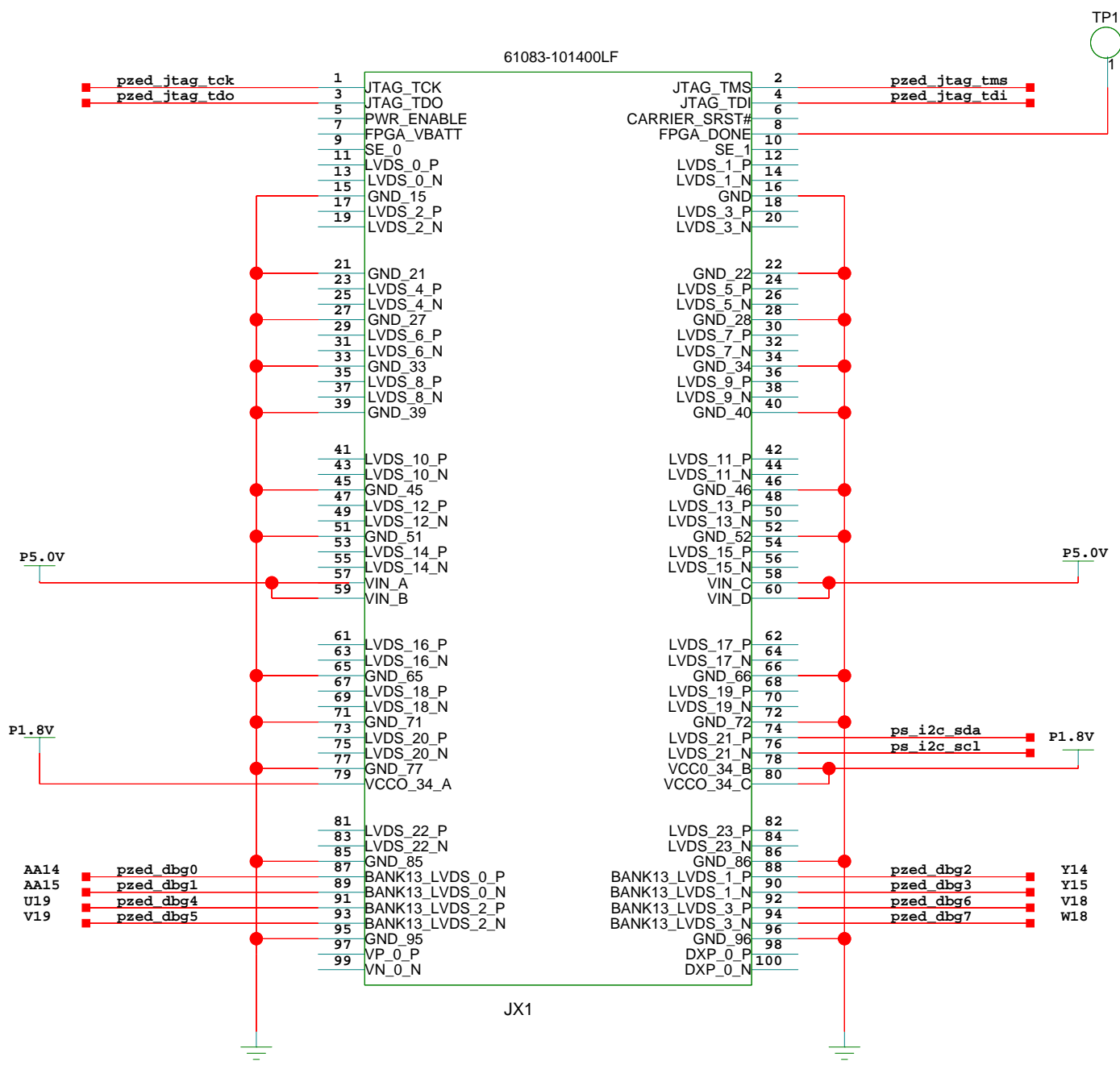
Title: APS BESOCM FPGA BOARD	
Date: 8-22-22	Ver:
Sheet Size: B	Rev: B
Sheet 15 of 23	Drawn By J. Mead

Voltage OV and UV Monitors



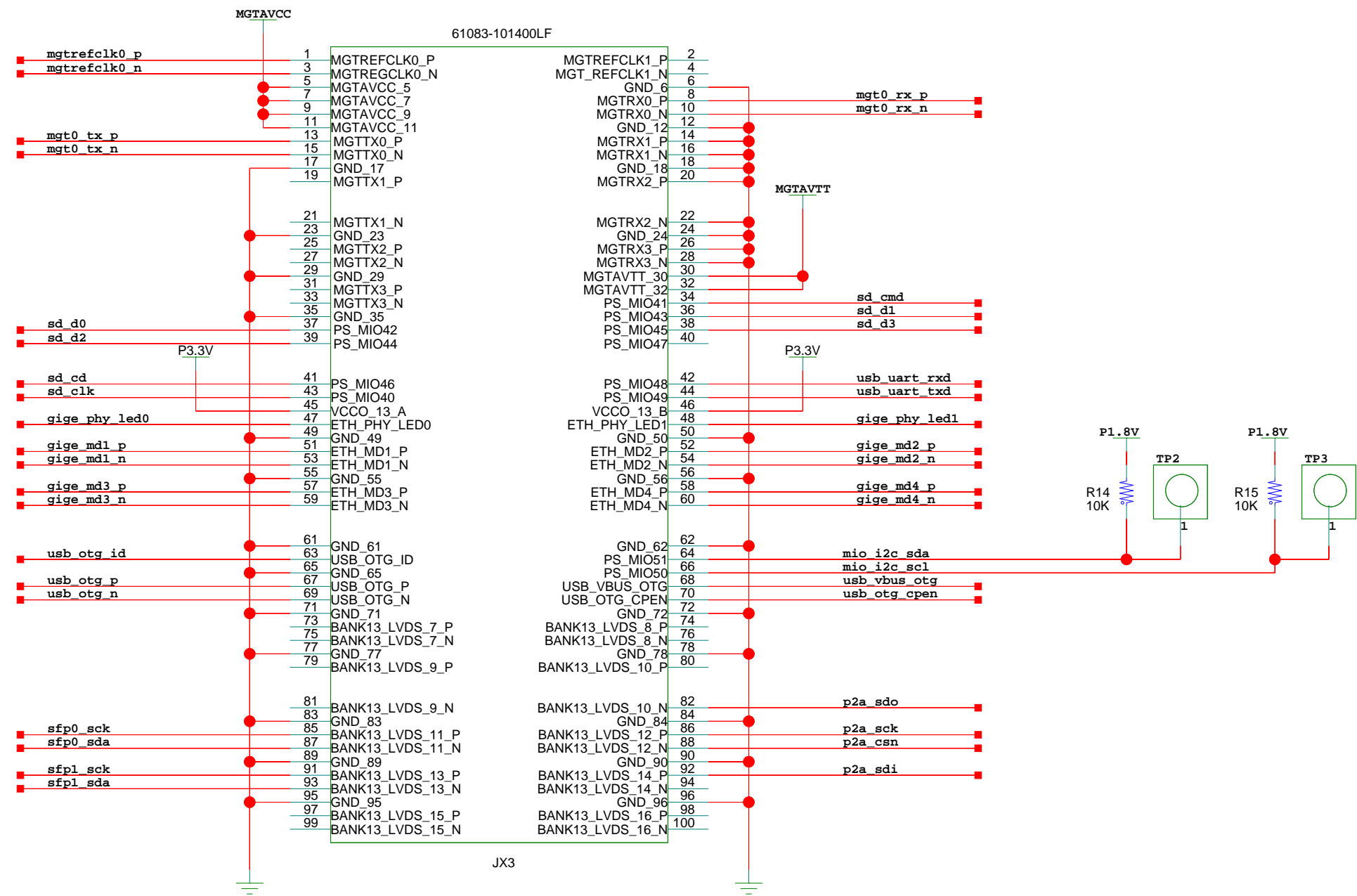
Title: <div style="text-align: center; font-size: 2em; font-weight: bold;">APS BESOCM FPGA BOARD</div>	
Date: 8-22-22	Ver:
Sheet Size: B	Rev: B
Sheet 16 of 23	Drawn By J. Mead

picoZED Connectors JX1 & JX2



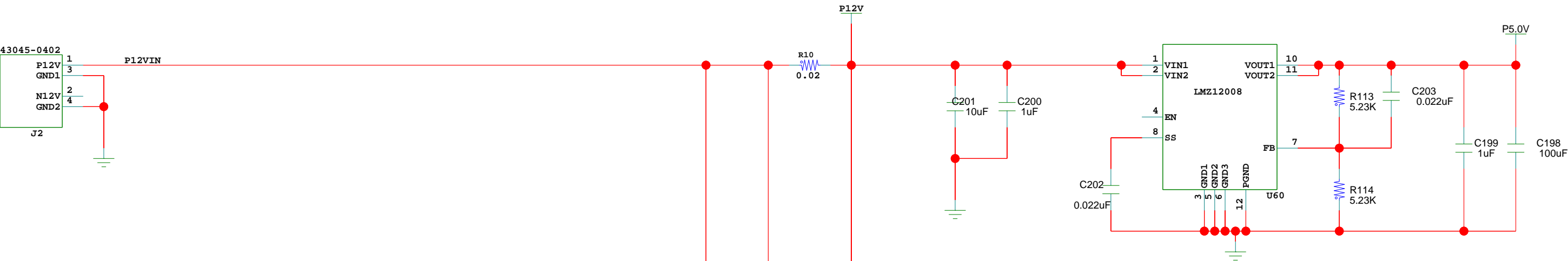
Title: APS BESOCM FPGA BOARD			
Date: 8-22-22	Ver:		
Sheet Size: B	Rev: B		
Sheet 17 of 23	Drawn By J. Mead		

picoZED Connector JX3

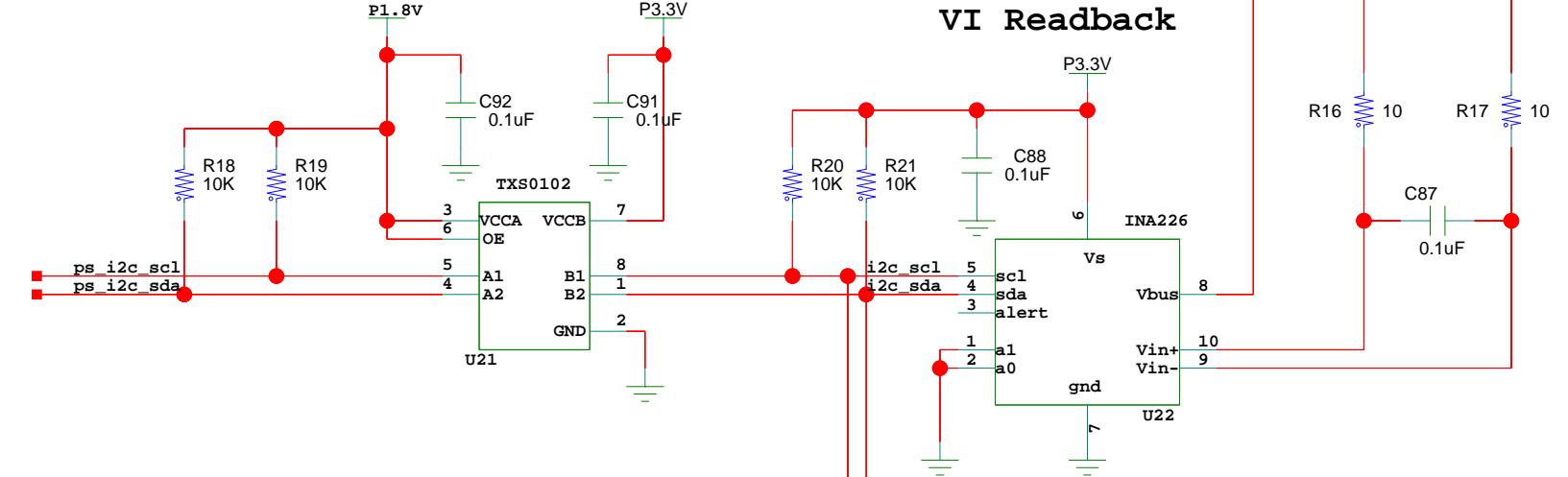


Title:		APS BESOCM FPGA BOARD	
Date:	8-22-22	Ver:	
Sheet Size:	B	Rev:	B
Sheet	18	of	23
Drawn By		J. Mead	

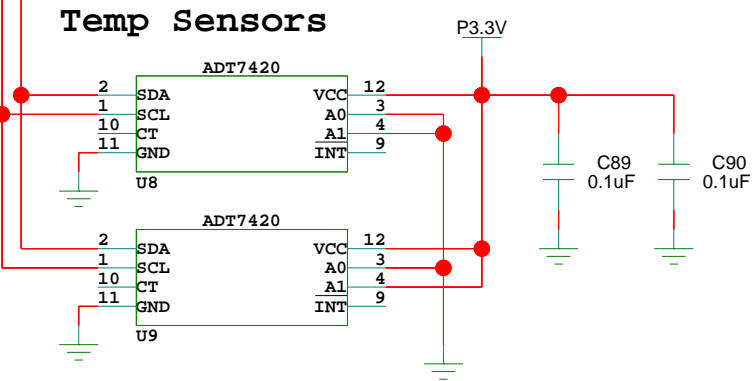
Power Input



VI Readback



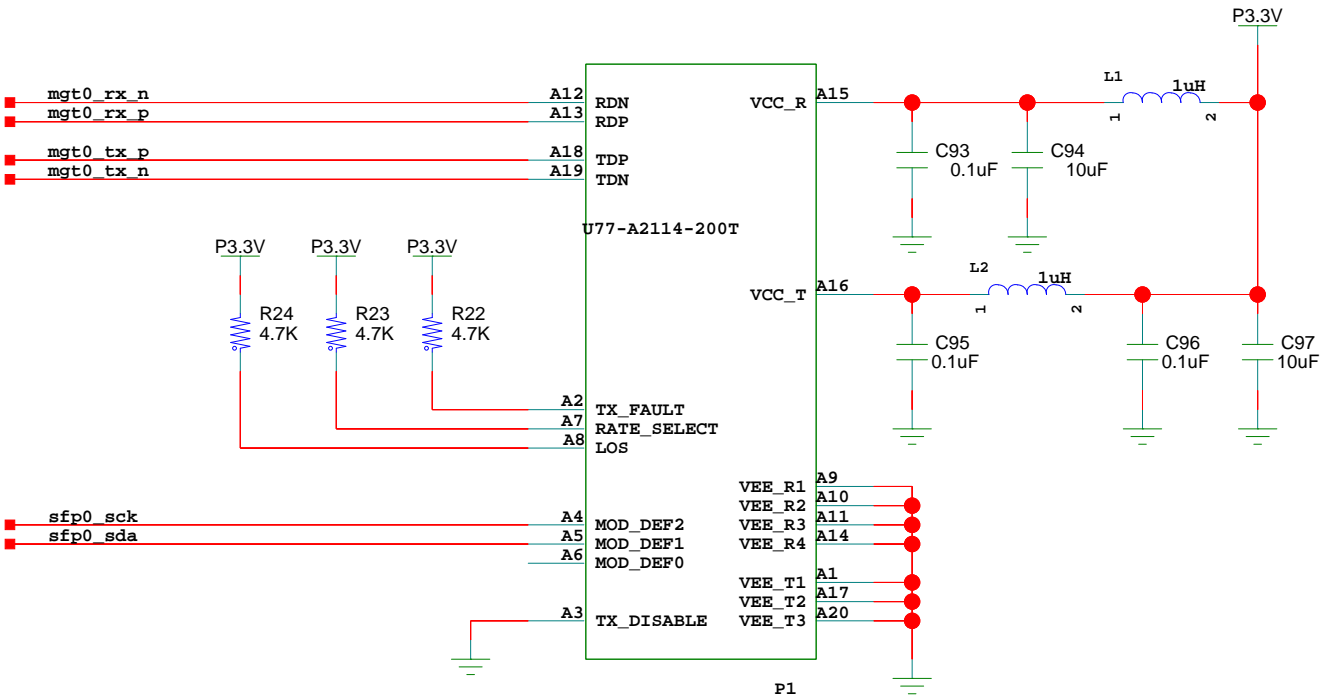
Temp Sensors



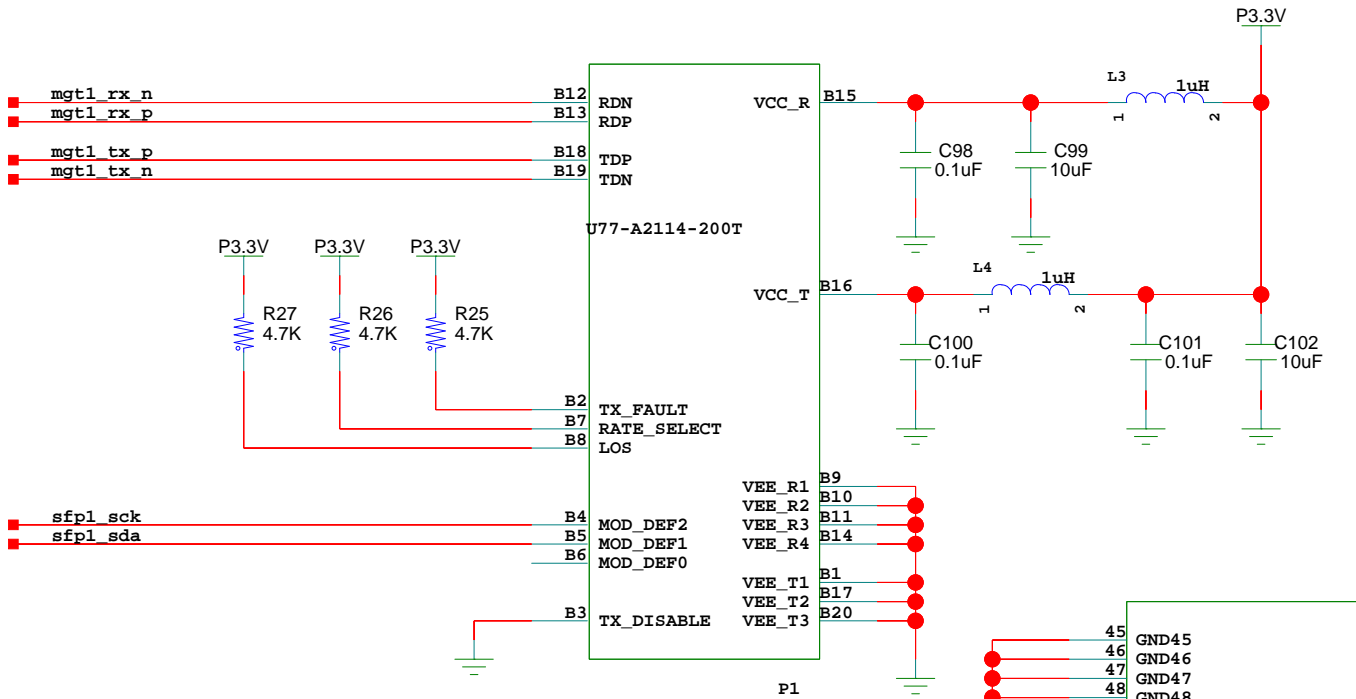
Title:		APS BESOCM FPGA BOARD	
Date:	8-22-22	Ver:	
Sheet Size:	B	Rev:	B
Sheet	19	of	23
Drawn By		J. Mead	

SFP Connecters

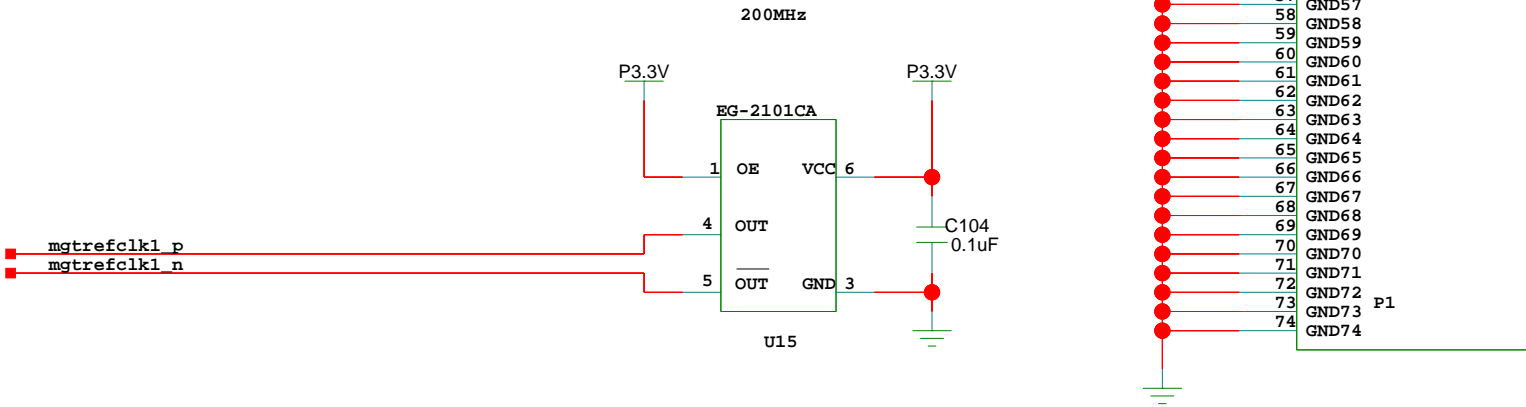
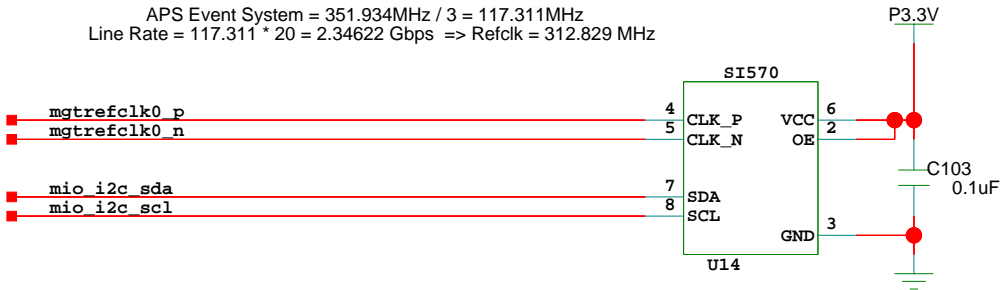
Event Receiver



Data Transceiver

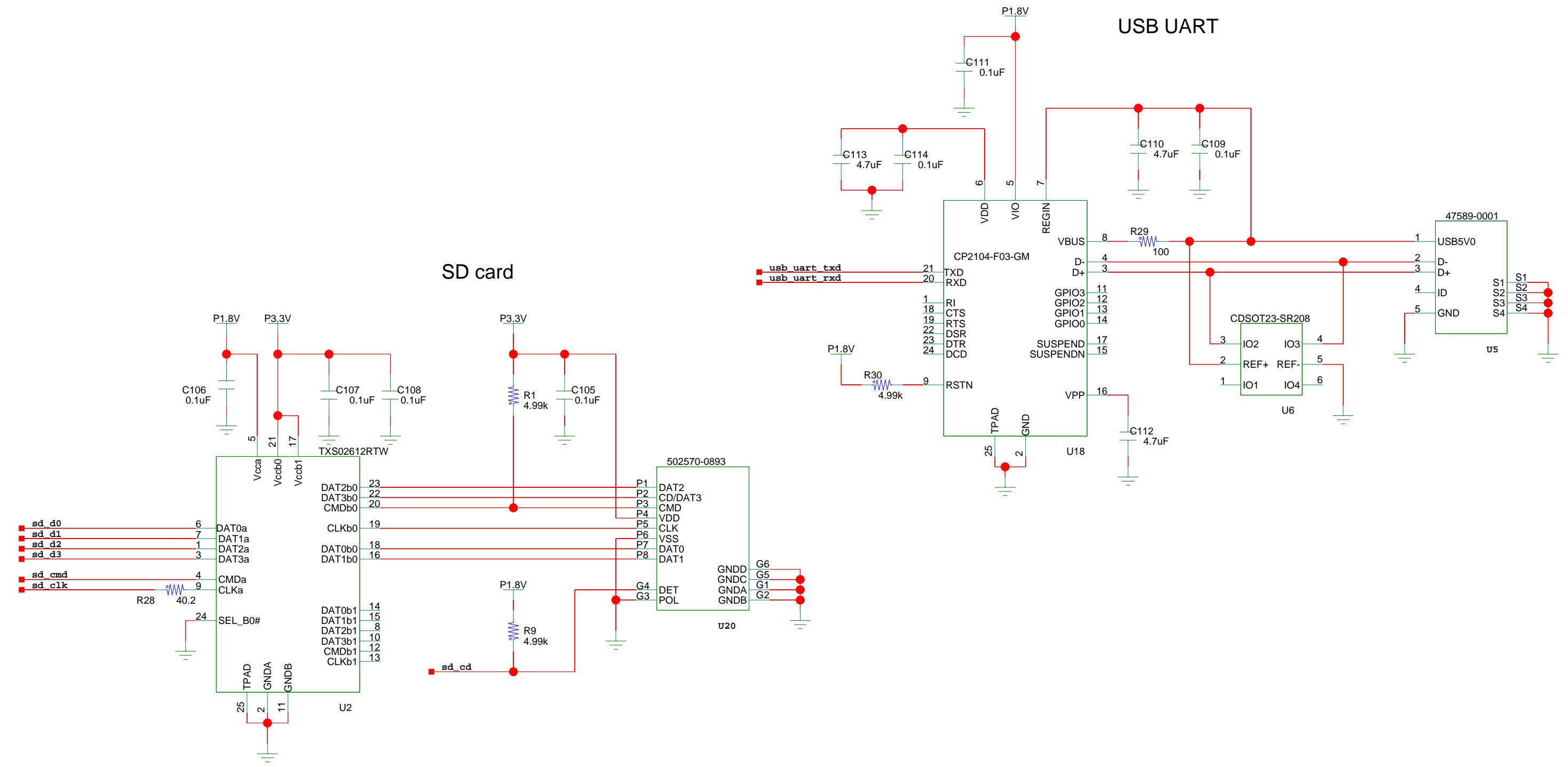


APS Event System = 351.934MHz / 3 = 117.311MHz
Line Rate = 117.311 * 20 = 2.34622 Gbps => Refclk = 312.829 MHz



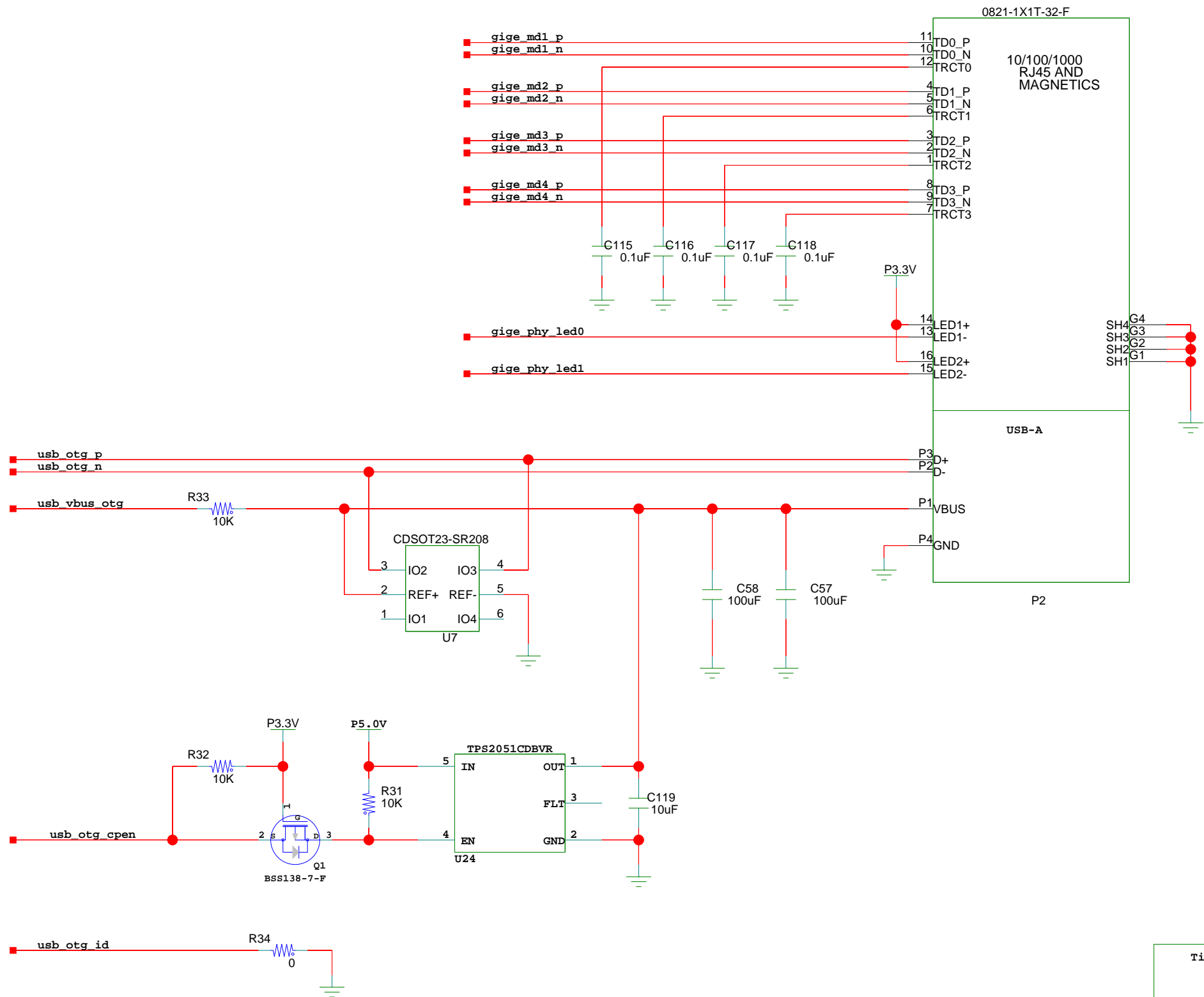
Title: APS BESOCM FPGA BOARD			
Date: 8-22-22	Ver:		
Sheet Size: B	Rev: B		
Sheet 20 of 23	Drawn By J. Mead		

Zynq Peripherals : SDCARD / UART



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Date:	8-22-22	Ver:	
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Sheet	21	of	23
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Zynq Peripherals : Gigabit Ethernet / USB

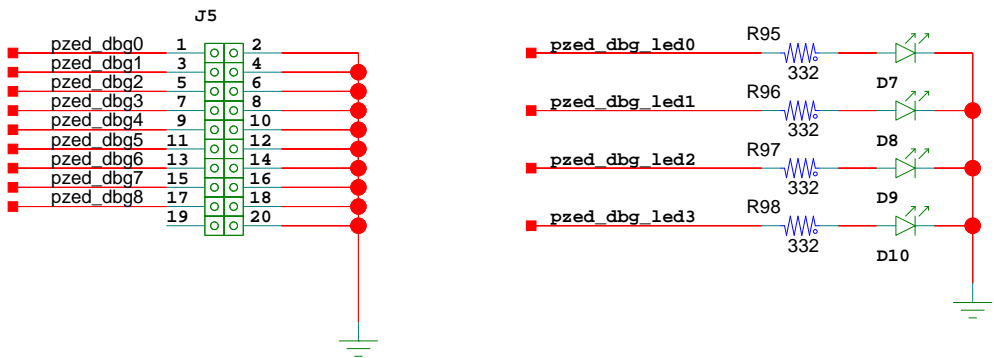


Do Not Install, selects
host mode vs device mode

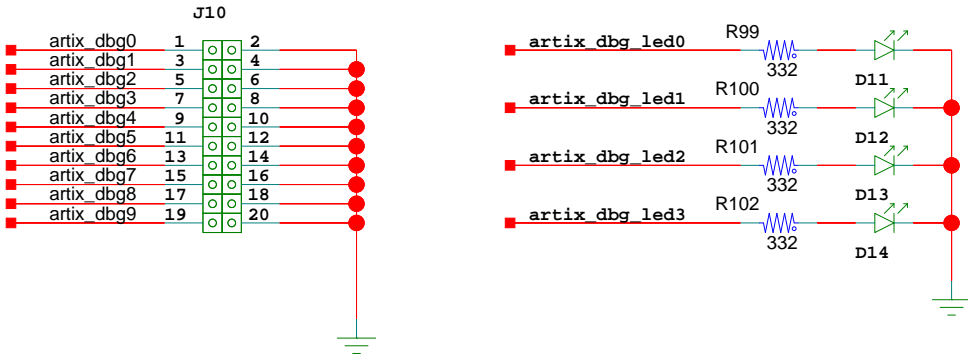
Title:		APS BESOCM FPGA BOARD	
Date:	8-22-22	Ver:	
Sheet Size:	B	Rev:	B
Sheet	22	of	23
Drawn By		J. Mead	

Miscellaneous

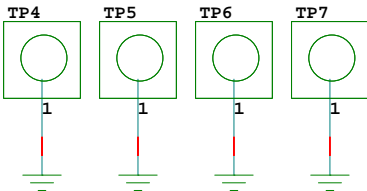
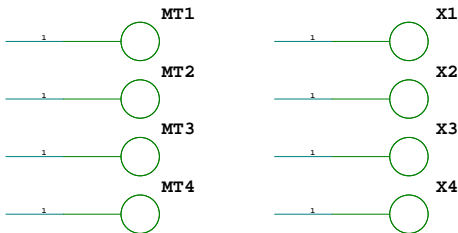
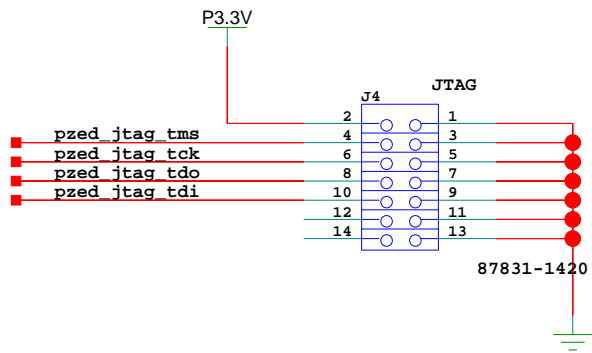
picoZed Debug Header



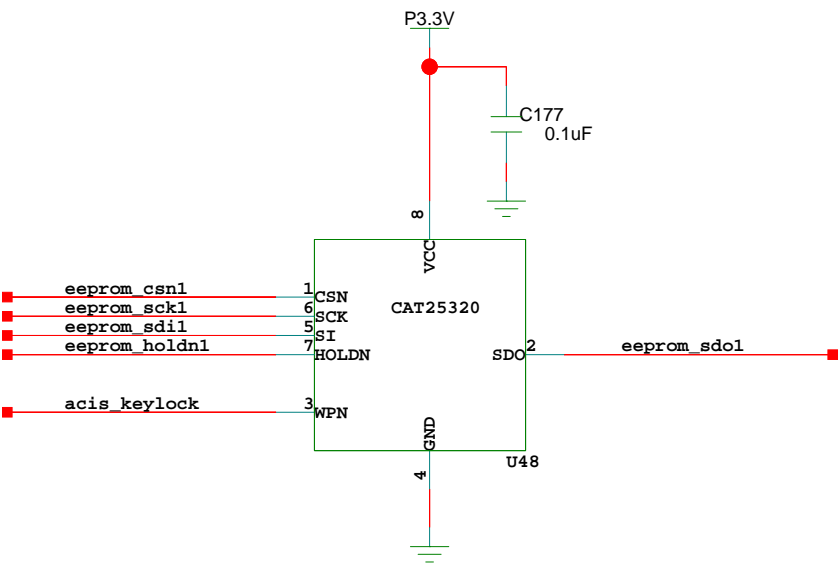
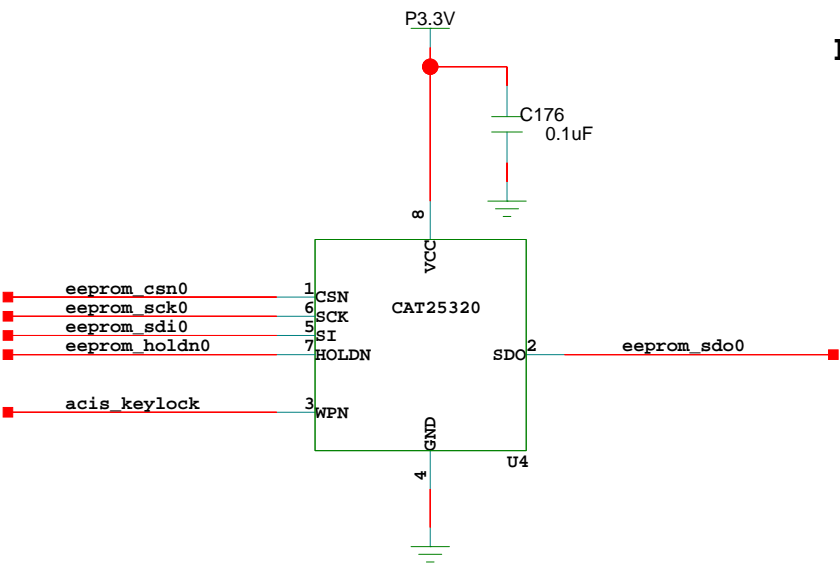
Artix Debug Header



picZed JTAG Header



EEPROM's



Title: APS BESOCM FPGA BOARD			
Date: 8-22-22	Ver:		
Sheet Size: B	Rev: B		
Sheet 23 of 23	Drawn By J. Mead		