Bipolar Power Converter User's Guide
10/11/25
Version 1.3

1. Introduction

The bipolar power converter (BPC) developed for the Advanced Light Source Upgrade project (ALS-U) is a family of 4-quadrant power converters with rated power ranging from 720 W to 3.2 kW. BPCs are switch-mode type, voltage-mode power amplifiers conceived, designed, and built by Brookhaven National Laboratory (BNL) to meet the tight physical space requirements of the ALS-U accelerator complex.

BPCs fall under drawing numbers LT-EL-SR-PS-CRR-6*x*0*y* where *x* is number of channels, and *y* is model type within the 6*x*0 group. Odd *y* is for slow models. Even *y* is for fast models. BPCs work in conjunction with newly developed power supply controllers (PSCs) in an EPICS controls environment. Consequently, BPCs have no front panel knob adjustments or displays. The PSC provides the high precision setpoint, current regulation, diagnostic readbacks, and ON/OFF control for the BPC. All control and status readbacks for the BPC are handled through a rear panel cable connection between the BPC and PSC. Table 1 summarizes BPC model names, number of channels, bandwidth class, and power ratings.

Model Name	Drawing Package	Number of Channels	Speed	Total Rated Power (W)
BPC-4CH-S-18V-10A	LT-EL-SR-PS-CRR-6401	4	Slow	720
BPC-2CH-S-18V-24A	LT-EL-SR-PS-CRR-6201	2	Fast	864
BPC-2CH-F-18V-24A	LT-EL-SR-PS-CRR-6202	2	Slow	864
BPC-2CH-S-16V-35A	LT-EL-SR-PS-CRR-6203	2	Slow	1120
BPC-1CH-S-18V-90A	LT-EL-SR-PS-CRR-6101	1	Slow	1620
BPC-1CH-F-16V-70A	LT-EL-SR-PS-CRR-6102	1	Fast	1120
BPC-1CH-S-16V-200A	LT-EL-SR-PS-CRR-6103	1	Slow	3200

Table 1. BPC Models

2. Chassis Mechanical Design

BPCs come in standard 19 inch rack-mountable chassis that occupy either 1U or 2U of vertical rack space. The top and bottom covers of the chassis are secured to the side panels with screws. The top and bottom covers also have welded z-bars at the front and rear edges of the cover panel. The z-bars interlock with mating flat plates welded to the top and bottom bends in the front and rear panels.

Figure 1 illustrates the underside of the top cover with its welded z-bars and the front panel with its welded flat plate. To remove the top cover, remove all the side screws on both top left and top right sides of the chassis except for the two screws in the back that secure the rear panel. Carefully rotate the front panel outward to separate the interlocking z-plate and front panel flat plate. Slowly lift the front edge of the top cover upward to clear the front panel while pulling the front panel forward to separate the interlocking plates between the top cover and the rear panel. Be careful not to lift the front edge of the cover too much when separating from the front panel to avoid putting stress on the interlocking plates in the rear.

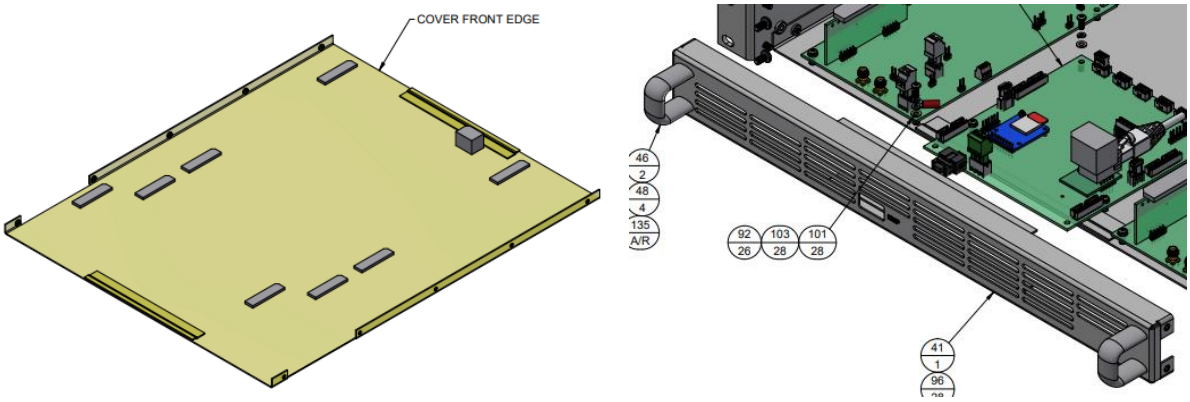

Figure 1. Top cover and front panel of 1U chassis.

2.1 Rear Panel

Figures 2a through 2e illustrate the rear panel layout of the seven BPC models. The rear panel of all seven BPC models includes the following components:

1. One or more screw terminal blocks for power output connections to the load. The 3200 W model uses bus bar bolted terminals instead of a terminal block.
2. DB25M or HD44M (4CH model only) connector(s) for channel control, analog readbacks, and digital I/O.
3. UL Recognized AC power entry module with C14/C20 cord inlet, ON/OFF switch, line filter, and circuit protection. The 3200 W model uses a UL Recognized 3-phase AC circuit breaker and separate AC line filter.
4. Ethernet RJ45 connector.
5. 2-position or 4-position (4CH model only) terminal connector into which a jumper block may be inserted. When inserted, the jumper block completes the connection to chassis of an internal 100 Ω resistor the other end of which is connected to the negative output terminal.

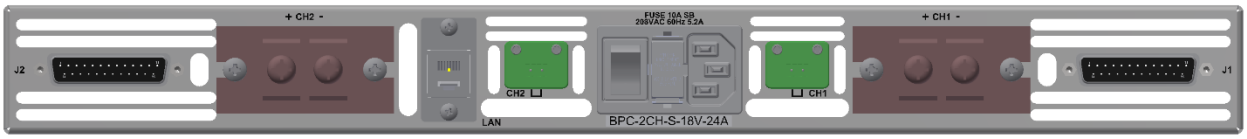

Figure 2a. Rear panel for BPC-2CH-S-18V-24A, BPC-2CH-F-18V-24A, and BPC-2CH-S-16V-35A

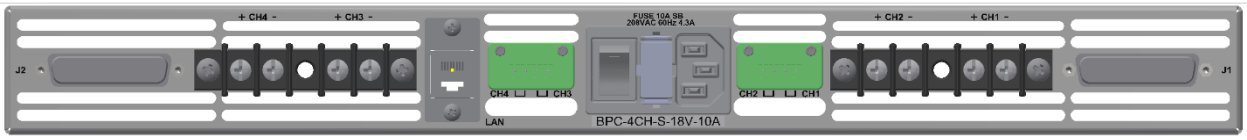

Figure 2b. Rear panel for BPC-4CH-S-18V-10A

Figure 2c. Rear panel for BPC-1CH-F-16V-70A

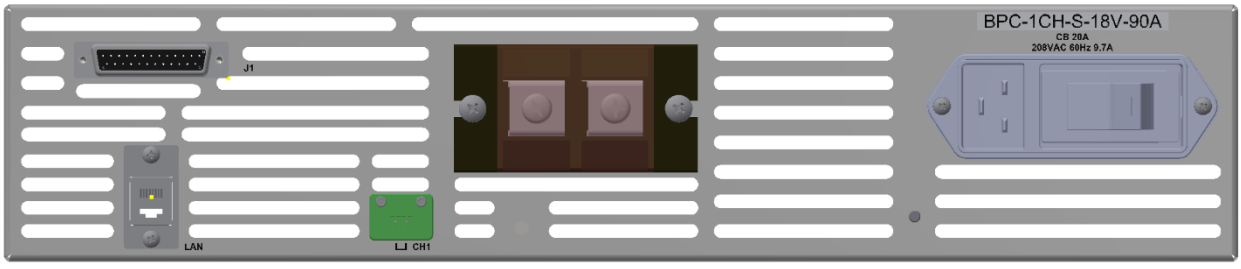

Figure 2d. Rear panel for BPC-1CH-S-18V-90A

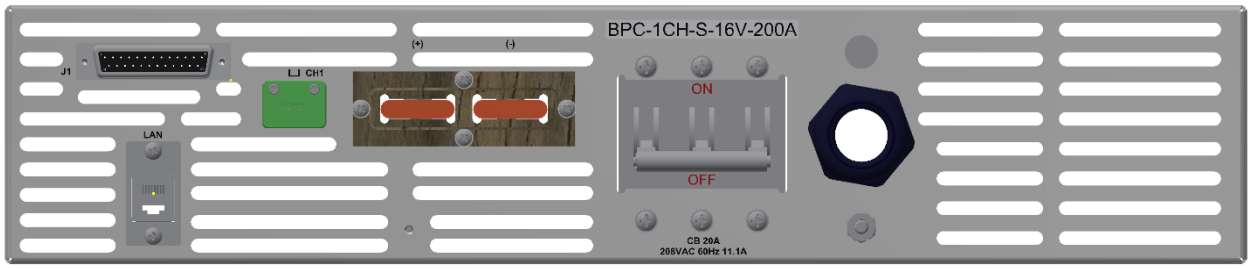

Figure 2e. Rear panel for BPC-1CH-S-16V-200A

2.2 Front Panel

Green LEDs visible through the vent slots in the front panel indicate which of the internal DC power supply modules are turned on. Since channels in some BPC models use more than one DC power supply module, these LEDs provide an indication of both channel ON/OFF status as well as diagnostic information about internal module operability.

A single amber LED provides a heartbeat indication from the microcontroller. This heartbeat is the same signal that appears as a digital output at the rear-panel Dsub connectors. Behavior of the amber LED is described in Table 4.

Blinking on for 1 s, off for 1 s	Normal Operation with AC on
Blinking Fast	SD card read failure at boot
Steady off	Hardware failure or AC power is off
Steady on	Hardware failure

Table 4. Front panel amber LED indications

The amber heartbeat LED is not affected by channels being on or off.

The front panel of a BPC has a 6-pin (3x2) header that can be used for In-Circuit Serial Programming (ICSP) of the Atmega microcontroller on the controller board.

3. Control Interface

All BPC models except the BPC-4CH-S-18V-10A model use a standard DB25M connector for controlling the power converter. The pinout for the DB25M connector is shown in Table 2.

DB25M Pin	Signal	Description
1	Vin+	Positive analog input control signal, ±10 V between Vin+ and Vin- gives ±19 V (±17 V)
14	Vin-	Negative analog input control signal
3	Vout_Readback	PS Vout analog readback
16	COM	
4	Ignd_Readback	PS Ignd analog readback
17	COM	
5	Vbus_Readback	Power amplifier DC Bus analog readback
18	COM	
7	ON1_cmd	Channel ON/OFF digital input. 100 Hz pulse train
8	ON2_cmd	Channel Enable digital input
9	RESET_cmd	Channel Fault Reset digital input
10	Spare_cmd	Channel Spare digital input
11	Cmd_RTN	Isolated return for digital inputs
12	Cmd_RTN	Isolated return for digital inputs
20	ON_Sts	Channel ON Status digital output
21	Fault1(SumFault)_Sts	Channel Fault digital output
22	Heartbeat_Sts	Processor Heartbeat digital output
23	Spare_Sts	Channel Spare digital output
24	Sts_RTN	Isolated return for digital outputs
25	Sts_RTN	Isolated return for digital outputs

Table 2. DB25M Pinout

The BPC-4CH-S-18V-10A model uses one high density HD44M connector for channel control, digital I/O, and analog readbacks for channels 1 and 2, and another HD44M connector for channels 3 and 4. The pinout for the HD44M connector is shown in Table 3.

HD44M Pin	Signal	Description
1	Vin+	CH1/CH3 Positive analog input control signal, ±10 V between Vin+ and Vin- gives ±19 V (±17 V)
17	Vin-	CH1/CH3 Negative analog input control signal
2	Vout_Readback	CH1/CH3 PS Vout analog readback
18	COM	
3	Ignd_Readback	CH1/CH3 PS Ignd analog readback

19	COM	
4	Vbus_Readback	CH1/CH3 Power amplifier DC Bus analog readback
20	COM	
5	ON1_cmd	CH1/CH3 ON/OFF digital input. 100 Hz pulse train
6	ON2_cmd	CH1/CH3 Enable digital input
7	RESET_cmd	CH1/CH3 Fault Reset digital input
8	Spare_cmd	CH1/CH3 Spare digital input
9	Cmd_RTN	Isolated return for CH1/CH3 digital inputs
10	Cmd_RTN	Isolated return for CH1/CH3 digital inputs
31	ON_Sts	CH1/CH3 ON Status digital output
32	Fault1(SumFault)_Sts	CH1/CH3 Fault digital output
33	Heartbeat_Sts	CH1/CH3 Processor Heartbeat digital output
34	Spare_Sts	CH1/CH3 Spare digital output
35	Sts_RTN	Isolated return for CH1/CH3 digital outputs
36	Sts_RTN	Isolated return for CH1/CH3 digital outputs
15	Vin+	CH2/CH4 Positive analog input control signal, ±10 V between Vin+ and Vin- gives ±19 V (±17 V)
30	Vin-	CH2/CH4 Negative analog input control signal
14	Vout_Readback	CH2/CH4 PS Vout analog readback
29	COM	
13	Ignd_Readback	CH2/CH4 PS Ignd analog readback
28	COM	
12	Vbus_Readback	CH2/CH4 Power amplifier DC Bus analog readback
27	COM	
26	ON1_cmd	CH2/CH4 ON/OFF digital input. 100 Hz pulse train
25	ON2_cmd	CH2/CH4 Enable digital input
24	RESET_cmd	CH2/CH4 Fault Reset digital input
23	Spare_cmd	CH2/CH4 Spare digital input
22	Cmd_RTN	Isolated return for CH2/CH4 digital inputs
21	Cmd_RTN	Isolated return for CH2/CH4 digital inputs
44	ON_Sts	CH2/CH4 ON Status digital output
43	Fault1(SumFault)_Sts	CH2/CH4 Fault digital output
42	Heartbeat_Sts	CH2/CH4 Processor Heartbeat digital output
41	Spare_Sts	CH2/CH4 Spare digital output
40	Sts_RTN	Isolated return for CH2/CH4 digital outputs
39	Sts_RTN	Isolated return for CH2/CH4 digital outputs

Table 3. HD44M Pinout

Note: The ON1 command signal must be a TTL level 100 Hz continuous pulse train to maintain a BPC channel in the ON state. This design is a safeguard against a hardware failure in the PSC that might leave the ON1 signal stuck in the ON state were only digital level detection to be used.

Caution: Do not apply more than ±10 V to the Vin+, Vin- control inputs of the BPC. When operating the BPC with a PSC, ensure that the magnet load designated for the BPC is connected to the BPC's output terminals.

4. AC Power

All BPC models except the BPC-1CH-S-16V-200A model are powered from single phase 208 VAC service (2 hot conductors). For testing the BPC at low power, 120 VAC power is acceptable.

The BPC-1CH-S-16V-200A model is powered from three phase 208 VAC 20 A service.

5. SD Card

The controller board uses an SD card to configure the BPC. The SD card is located on the controller board near the front of the chassis. Physical access to the SD card requires removing the top cover. The SD card does not need to be physically accessed to upgrade the firmware.

The SD card does not contain any firmware code, only configuration data in a file called config.txt. The config.txt file is read once at startup. The contents of the config.txt file look something like this:

Static IP Address: 192.168.0.15
MAC Address: 02,00,00,62,02,0F
1-Wire Sensor Left: 28,00,00,00,00,00,00,00
1-Wire Sensor Right: 28,00,00,00,00,00,00,00
HALL sensor gain: 1.02,1.02
Model.Serial Number: 6202015
IP Address static(0)/dhcp(1): 0

As shipped from BNL, the static IP address of a BPC is 192.168.0.*y* where *y* is the serial number of the unit.

The MAC address is 02,00,00,6*x*,0*y*,*z* where *x* and *y* complete the model number of the unit, and *z* is the serial number of the unit in hexadecimal.

If the last line of the config.txt file is set to a value of 1 for DHCP IP addressing, the BPC will wait for a response from a DHCP server when AC power is turned on. The BPC will time out from no DHCP

server response after 30 seconds. Following a DHCP request timeout, the BPC will use the static IP address given in the first line of the config.txt file.

6. Interlock Protection

The BPC is self protecting from the following fault conditions:

1. Over Current (OVC) fault. The internal OVC limit is model specific.
2. Over Temperature (OVT) fault.
3. Current sharing fault between internal power amplifier stages.
4. ON fault. The BPC will latch a fault if it is commanded on but the internal DC power converter does not turn on.
5. SD card fault.

These interlocks are active interlocks handled by microcontroller firmware. The BPC also has passive over-voltage protection in the form of energy extraction transient voltage suppressor diodes (TVSs) connected across the outputs of the power amplifier and the output EMI filter. The TVS diodes are bidirectional and extract energy from an inductive load, limiting what could otherwise be a large voltage transient across the output if the BPC is turned off while powering a magnet.

Note: The TVS diodes are not designed to withstand a steady state over voltage condition.

The BPC also incorporates an external interlock feature through the ON2 command signals. The ON2 inputs have a direct logic path to the inhibit input of the internal DC power supply. The ON2 input serves as a PSC Direct Inhibit control that can turn off the DC power supply even if the microcontroller program stops running.

Note: For 2CH and 4CH models, the ON2 inputs from all channels are logically ANDed together. All ON2 inputs for all channels must be in the logic high state for any BPC channel to be turned on.

7. Ethernet Interface

The ethernet interface can connect directly to PSC SFP port 4 or to an IOC on the controls network. The interface provides detailed diagnostic data for the BPC in the form of a 60-word housekeeping data packet using the UDP protocol. The interface can also be used for reading and modifying the contents of the SD card.

7.1 The UDP housekeeping data packet includes all the data listed in Table 5.

Word	Peripheral	Value	Description
0	-	1000.0	Frame start
1	ADC0	PC Dependent	HALL Current Sensor
2	ADC1	PC Dependent	HALL Current Sensor
3	ADC2	PC Dependent	HALL Current Sensor
4	ADC3	PC Dependent	HALL Current Sensor
5	ADC4	PC Dependent	HALL Current Sensor
6	ADC5	PC Dependent	HALL Current Sensor
7	ADC6	PC Dependent	HALL Current Sensor
8	ADC7	PC Dependent	HALL Current Sensor
9	ADC8	PC Dependent	HALL Current Sensor
10	ADC9	PC Dependent	HALL Current Sensor
11	ADC10	PC Dependent	HALL Current Sensor
12	ADC11	PC Dependent	HALL Current Sensor
13	ADC12	-	Reserved
14	ADC13	-	Reserved
15	ADC14	-	Reserved
16	ADC15	-	Reserved
17	-	-	Reserved
18	PMBus	PC Dependent	Delta PS Mod Vout
19	PMBus	PC Dependent	Delta PS Mod Iout
20	PMBus	PC Dependent	Delta PS Mod Vout
21	PMBus	PC Dependent	Delta PS Mod Iout
22	PMBus	PC Dependent	Delta PS Mod Vout
23	PMBus	PC Dependent	Delta PS Mod Iout
24	PMBus	PC Dependent	Delta PS Mod Vout
25	PMBus	PC Dependent	Delta PS Mod Iout
26	PMBus	PC Dependent	Delta PS Mod Vout
27	PMBus	PC Dependent	Delta PS Mod Iout
28	PMBus	PC Dependent	Delta PS Mod Vout

29	PMBus	PC Dependent	Delta PS Mod Iout
30	PMBus	PC Dependent	Delta PS Mod Vout
31	PMBus	PC Dependent	Delta PS Mod Iout
32	PMBus	PC Dependent	Delta PS Mod Vout
33	PMBus	PC Dependent	Delta PS Mod Iout
34	PMBus	-	Reserved
35	PMBus	20-	Delta PS Temperature
36	PMBus	20-	Delta PS Temperature
37	PMBus	20-	Delta PS Temperature
38	PMBus	0-17000	Delta PS Fan Speed
39	PMBus	0-17000	Delta PS Fan Speed
40	PMBus	0-17000	Delta PS Fan Speed
41	PMBus	0-17000	Delta PS Fan Speed
42	PMBus	0-17000	Delta PS Fan Speed
43	PMBus	0-17000	Delta PS Fan Speed
44	1-Wire	0-100	Temp Sens 1
45	1-Wire	0-100	Temp Sens 2
46	1-Wire	0-100	Temp Sens 3
47	-	-	Reserved
48	µP	0-100	Heatsink Fan % PWM 1
49	µP	0-100	Heatsink Fan % PWM 2
50	µP	0-100	Heatsink Fan % PWM 3
51	-	-	Reserved
52	Delta PS DIO	32 bits	PSMODSTAT
53	µP Logic	32 bits	PSFLTSTAT
54	-	6201.001	PS Model/SN
55	-	1.01	F/W Version
56	µP Logic	0-1000	Loop rate (loops/s)
57	µP Logic	0-65535	Packet counter
58		$0 – 2.815x10^8$	Uptime (s)
59	-	1001.0	Frame end

Table 5. UDP Housekeeping data packet

To receive the UDP housekeeping data packet, send the UDP message “Loop” to the BPC. The BPC responds with a 240-byte data packet packed as 60 4-byte IEEE 754 floats. The “Loop” message can be sent to the BPC at a maximum rate of 10 messages/second or 10 Hz.

7.2 The PSMODSTAT register in the housekeeping data packet shows the ON/OFF status of the internal DC power supply modules in the BPC chassis.

Delta PS Module Status (PSMODSTAT) Register

MSB

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	Mod8	Mod7	Mod6	Mod5	Mod4	Mod3	Mod2	Mod1

LSB

Mod*x* = 0 or 1 (Off or On)

7.3 The PSFLTSTAT register in the housekeeping data packet shows fault status for the BPC.

PS Fault Status (PSFLTSTAT) Register

MSB

-	-	-	-	-	-	-	-	-	-	v	u	t	s	r	q
-	o	n	m	-	k	j	i	h	g	f	e	d	c	b	a

LSB

a = Sum Fault CH1
b = Sum Fault CH2
c = Sum Fault CH3
d = Sum Fault CH4
e = OVC Fault PA1
f = OVC Fault PA2
g = OVC Fault PA3
h = OVC Fault PA4
i = Hall Sensor Mismatch PA1
j = Hall Sensor Mismatch PA2
k = Hall Sensor Mismatch PA3
m = OVT PA1
n = OVT PA2
o = OVT PA3
q = heartbeat
r = processor reset flag
s = ON1faultCH1
t = ON1faultCH2
u = ON1faultCH3
v = ON1faultCH4

Bit ‘r’ in the PSFLTSTAT register is an indication of processor reset. The bit goes high for 5 seconds when the firmware restarts then goes low forever.

7.4 To read out the contents of the SD card, send the UDP message “SDrd” to the BPC. The BPC responds with a multi-line string containing the contents of the SD card. A simple python app is available from BNL that can read the SD card and write the contents to file.

7.5 To change the contents of the SD card, send the UDP message “SDwr” to the BPC, then send another UDP message with a multi-line string containing the contents of the SD card. A simple interactive python app is available from BNL for updating the IP and MAC addresses and selecting static or DHCP IP addressing.

8. Performance Specifications

BPC Performance Specifications are summarized in Table 6.

Specification	Value	Comments
Output voltage range	±18 V (5 models) ±16 V (2 models)	
Bandwidth slow	1 kHz	
Bandwidth fast	25 kHz	
RMS noise (slow models)	<2 mV	Measurement BW=10 kHz
RMS noise (fast models)	<1 mV	Measurement BW=10 kHz
RMS ripple (slow models)	<5 mV	Measurement BW=20 MHz
RMS ripple (fast models)	<15 mV	Measurement BW=20 MHz
Output isolation	±20 V	Rear panel jumper block disconnected
AC Current:		
720 W Model	4.3 A	Single phase 208 VAC (2 hot conductors)
864 W Models	5.2 A	Single phase 208 VAC (2 hot conductors)
1120 W Models	6.7 A	Single phase 208 VAC (2 hot conductors)
1620 W Model	9.7 A	Single phase 208 VAC (2 hot conductors)
3200 W Model	11.1 A	3-phase 208 VAC

Table 6. Performance specifications

9. Theory of Operation

The BPC uses one or more commercial off the shelf DC power supplies as a power source combined with custom designed printed circuit board (PCB) assemblies to achieve high precision 4-quadrant operation. A block diagram of a single BPC channel is shown in Figure 3. As listed in Tables 2 and 3, the standard BPC/PSC channel interface consists of eight isolated digital I/O signals to/from the controller board, three analog signals to/from the PWM-Regulator board, and one analog signal for ground current.

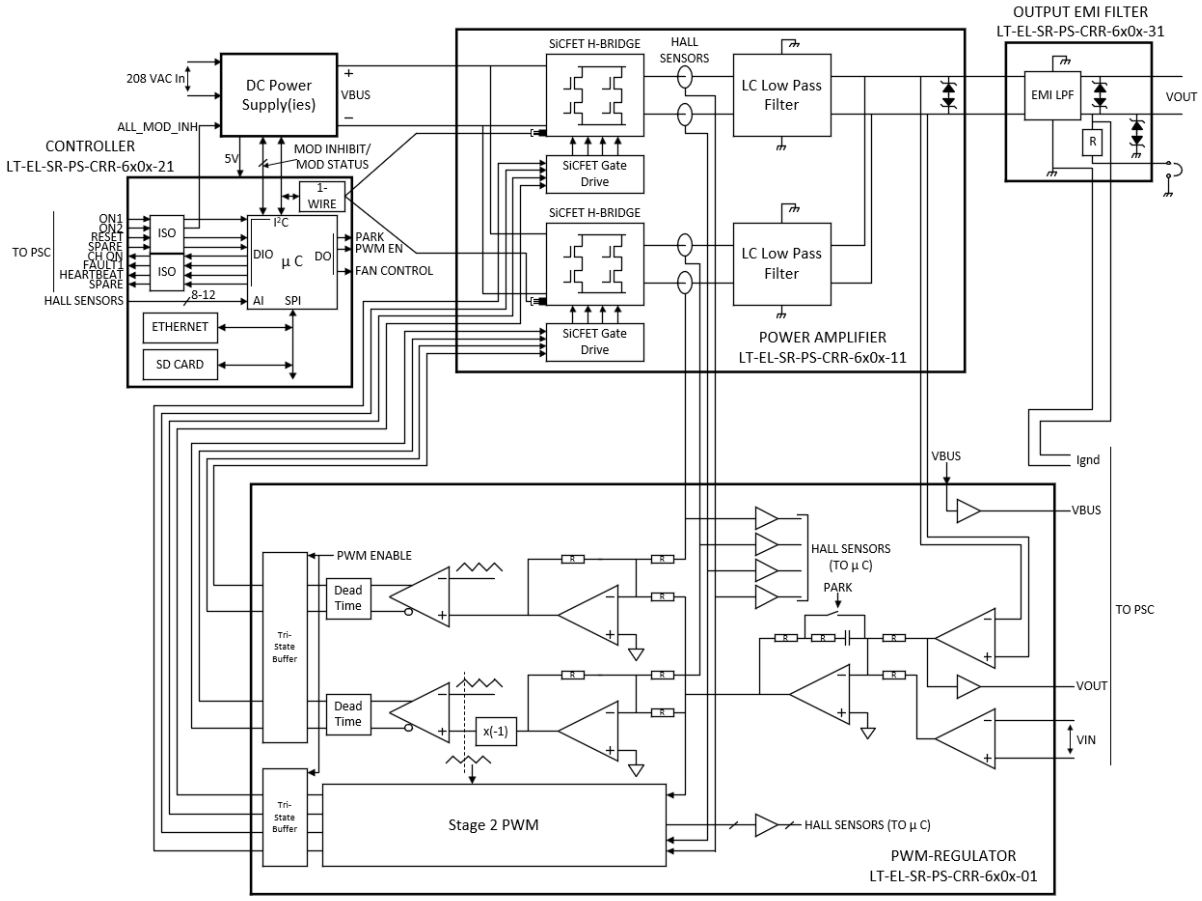

Figure 3. BPC single channel simplified block diagram.

9.1 PWM-Regulator Board

The PWM-Regulator board includes a proportional plus integral (P+I) controller circuit and two PWM channels. The controller circuit compares BPC output voltage feedback to the analog input control signal coming from the PSC. PWM generation is accomplished by comparing a reference triangle wave to the output of the P+I controller with high-speed comparators. The triangle wave

frequency is 250 kHz for all models except the 1620 W and 3200 W models. In these models the triangle wave frequency is 125 kHz.

The two triangle wave generators are phase staggered by 90 degrees so the resulting PWM outputs from each generator can be interleaved to produce composite PWM control at effectively twice the frequency of each individual PWM. A high effective switching frequency is necessary for achieving both high bandwidth in the fast models and low switch-mode output voltage ripple.

A “park” switch is placed across the integrating capacitor in the P+I controller. When the channel is turned on, PWM is disabled, and the park switch is in the closed position. Two seconds after a channel is turned on, PWM is enabled with the control loop still parked. Two seconds after PWM is enabled, the control loop is unparked, and voltage regulation is established.

9.2 Power Amplifier Board

The Power Amplifier board is a class-D amplifier built with two SiCFET H-bridge type power amplifier stages which can be used individually as two channels or paralleled together into one channel with twice the current capability. To ensure equal current sharing among paralleled bridges, every SiCFET bridge includes Hall current sensors whose output is sent to the PWM-Regulator board as current feedback. The current feedback corrects the PWM duty cycle control signal from the P+I controller to each bridge, forcing current from each bridge to match the control signal. The current feedback signals are also used by the controller board for the over-current and current mismatch protection interlocks.

The power amplifier boards are assembled to different printed circuit board (PCB) assembly drawing numbers depending on which model BPC they go into. The different component assemblies also use three different bare PCBs depending on which off-the-shelf DC power supply is used in the BPC. The off-the-shelf DC power supplies are factory configurable to accommodate a wide range of channels and power ratings. Figures 4a through 4e illustrate the different DC power supply and power amplifier topologies used in the BPCs.

The BPC-2CH models use the LT-EL-SR-PS-CRR-6201-12 power amplifier PCB which parallels the two H-Bridges. The board has a single DC bus input and a single output. The 18V/24A models use a 1.2 kW DC power supply, and the 16V/35A model uses a 2 kW DC power supply.

The BPC-1CH-F-16V-70A model also uses the LT-EL-SR-PS-CRR-6201-12 power amplifier PCB, but the outputs of two power amplifier boards are paralleled together in the chassis. This BPC uses a 2 kW DC power supply.

The BPC-1CH-S-18V-90A model uses the LT-EL-SR-PS-CRR-6101-12 power amplifier PCB, which parallels the outputs of the two H-bridges but keeps the DC bus inputs separate. This BPC uses

two power amplifier boards whose outputs are paralleled together in the chassis and two 1.2 kW DC power supplies.

The BPC-1CH-S-16V-200A model also uses the LT-EL-SR-PS-CRR-6101-12 power amplifier PCB, but there are three power amplifier boards whose outputs are paralleled together in the chassis. This BPC uses three 2 kW DC power supplies.
The BPC-4CH model uses the LT-EL-SR-PS-CRR-6401-12 power amplifier PCB which keeps the two H-Bridges as separate channels with separate DC buses and separate outputs. This BPC uses a single 1.2 kW DC power supply.

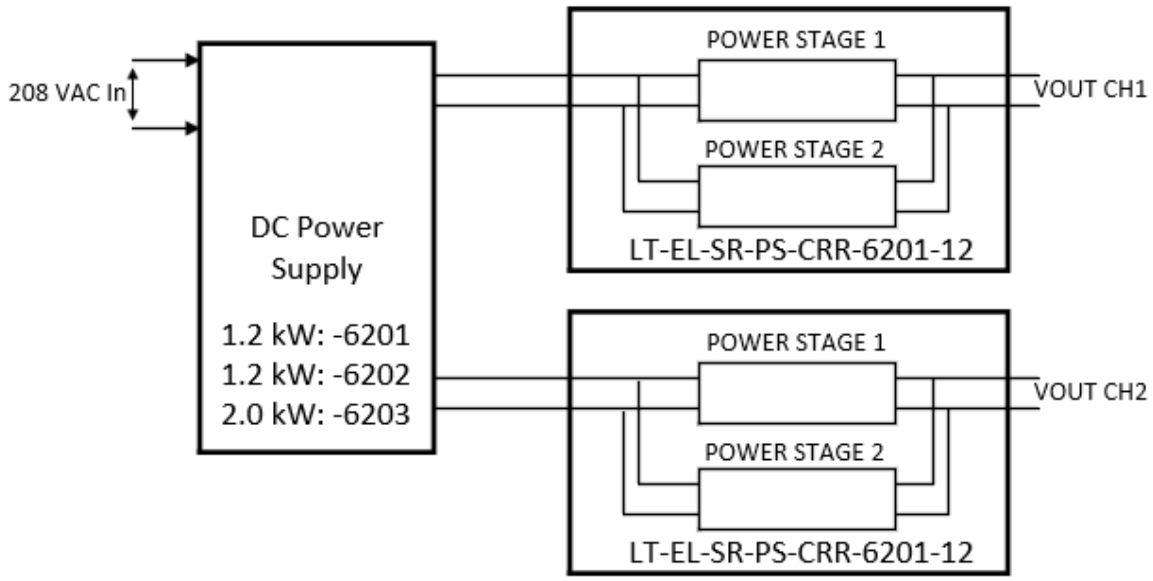

Figure 4a. Topology of DC power supply and power amplifier boards for BPC-2CH models.

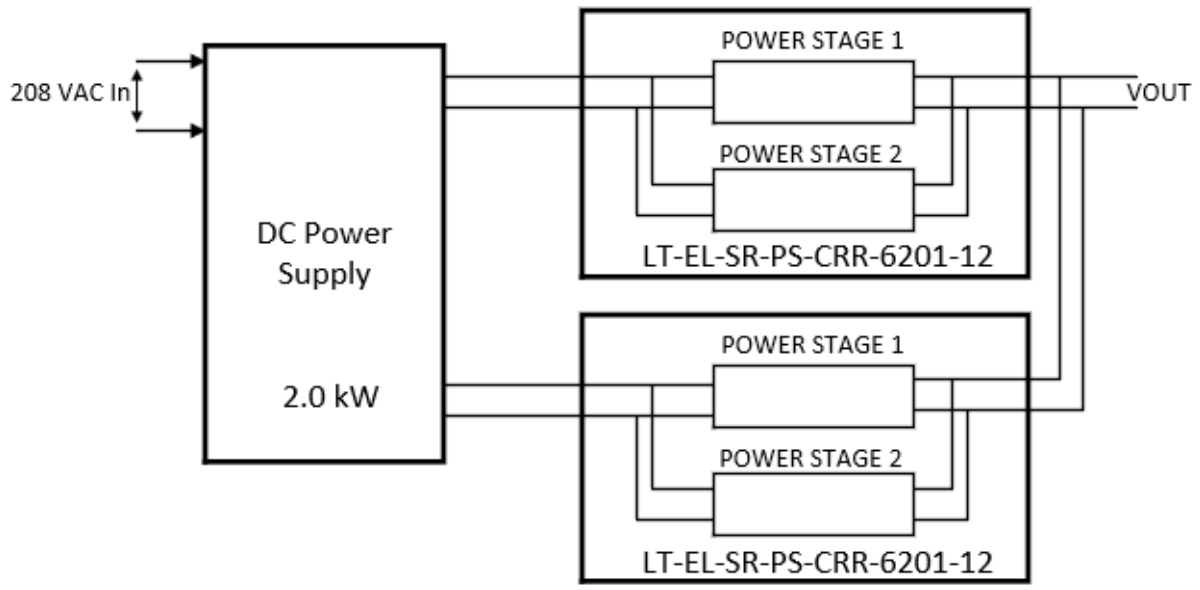

Figure 4b. Topology of DC power supply and power amplifier boards for BPC-1CH-F-16V-70A model.

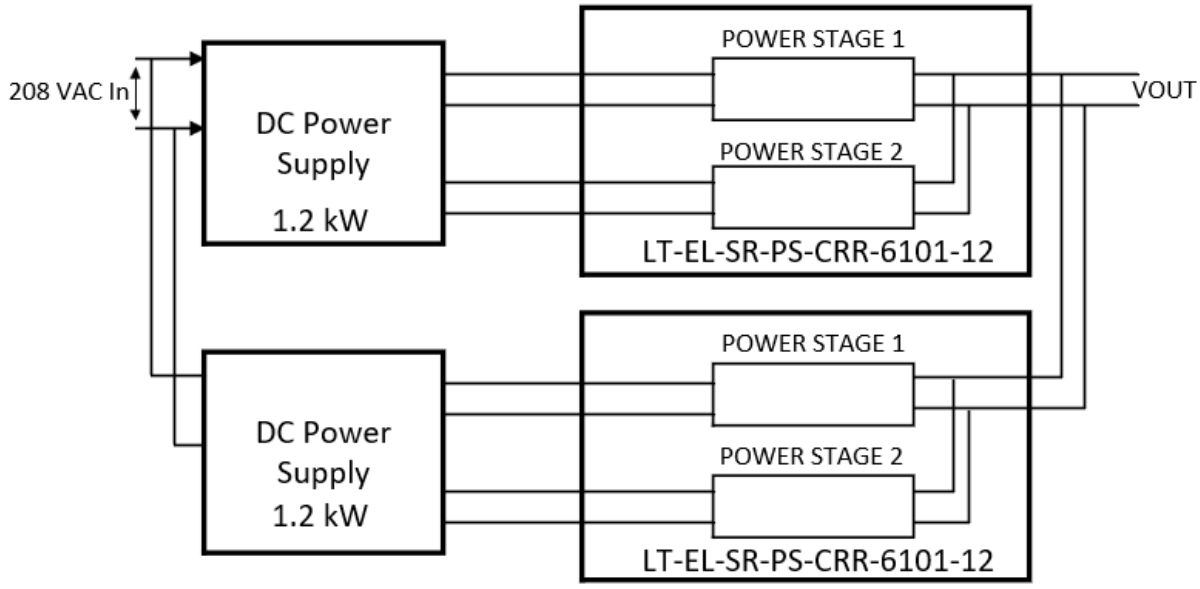

Figure 4c. Topology of DC power supplies and power amplifier boards for BPC-1CH-S-18V-90A model.

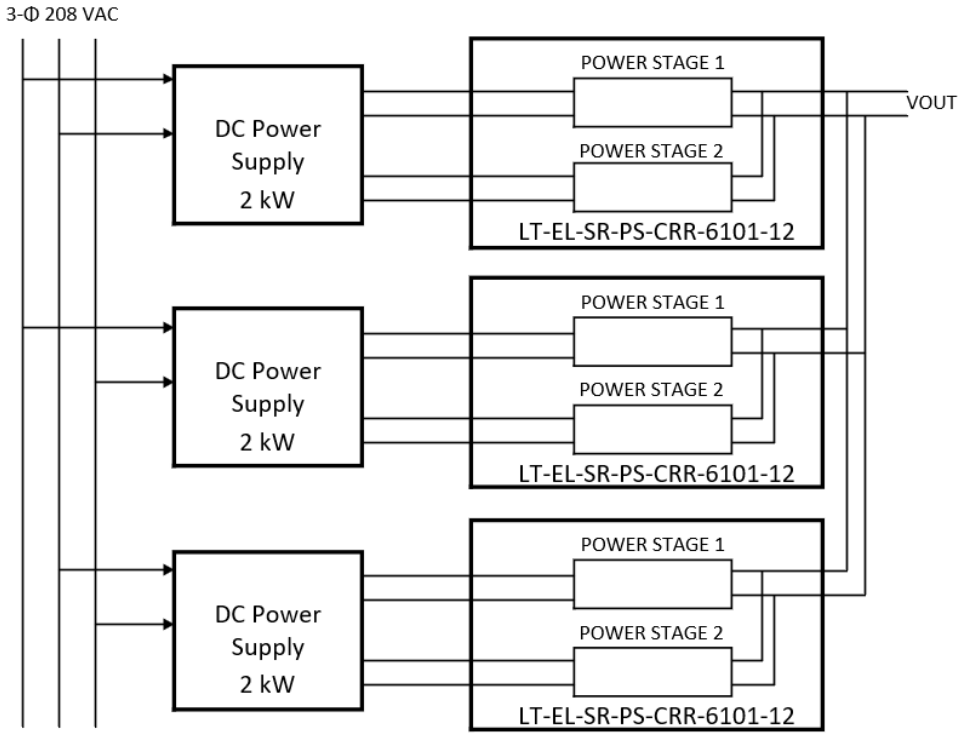

Figure 4d. Topology of DC power supplies and power amplifier boards for BPC-1CH-S-16V-200A model.

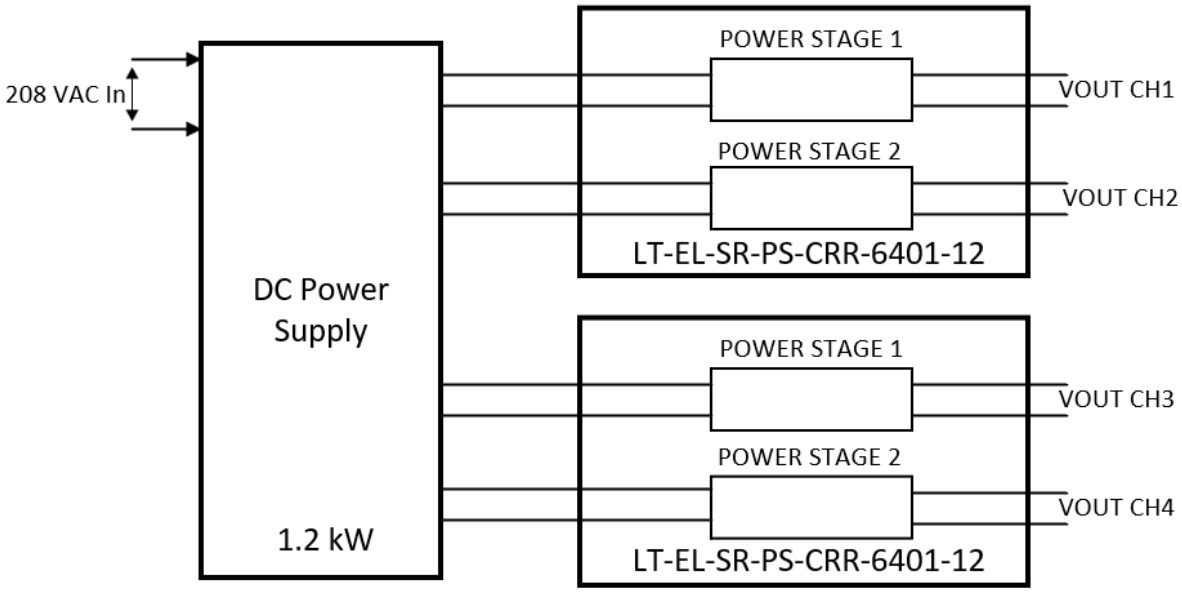

Figure 4e. Topology of DC power supply and power amplifier boards for BPC-4CH-S-18V-10A model.

9.3 Output EMI Filter Board

The Output EMI Filter board connects directly across the output terminals inside the chassis. The filter's purpose is to limit radiated emission of high frequency harmonics of the power amplifier's switching frequency. The filter includes both differential and common mode filtering through low inductance connections across the output terminals and between the output terminals and chassis.

The board also includes:

1. A TVS diode across the output terminals
2. A TVS diode between the output minus terminal and chassis.
3. A 100 Ω 2 W resistor connected between the minus output terminal and the rear panel jumper block.