Description of ALS-U zPSC Calibration

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11/12/25

Introduction

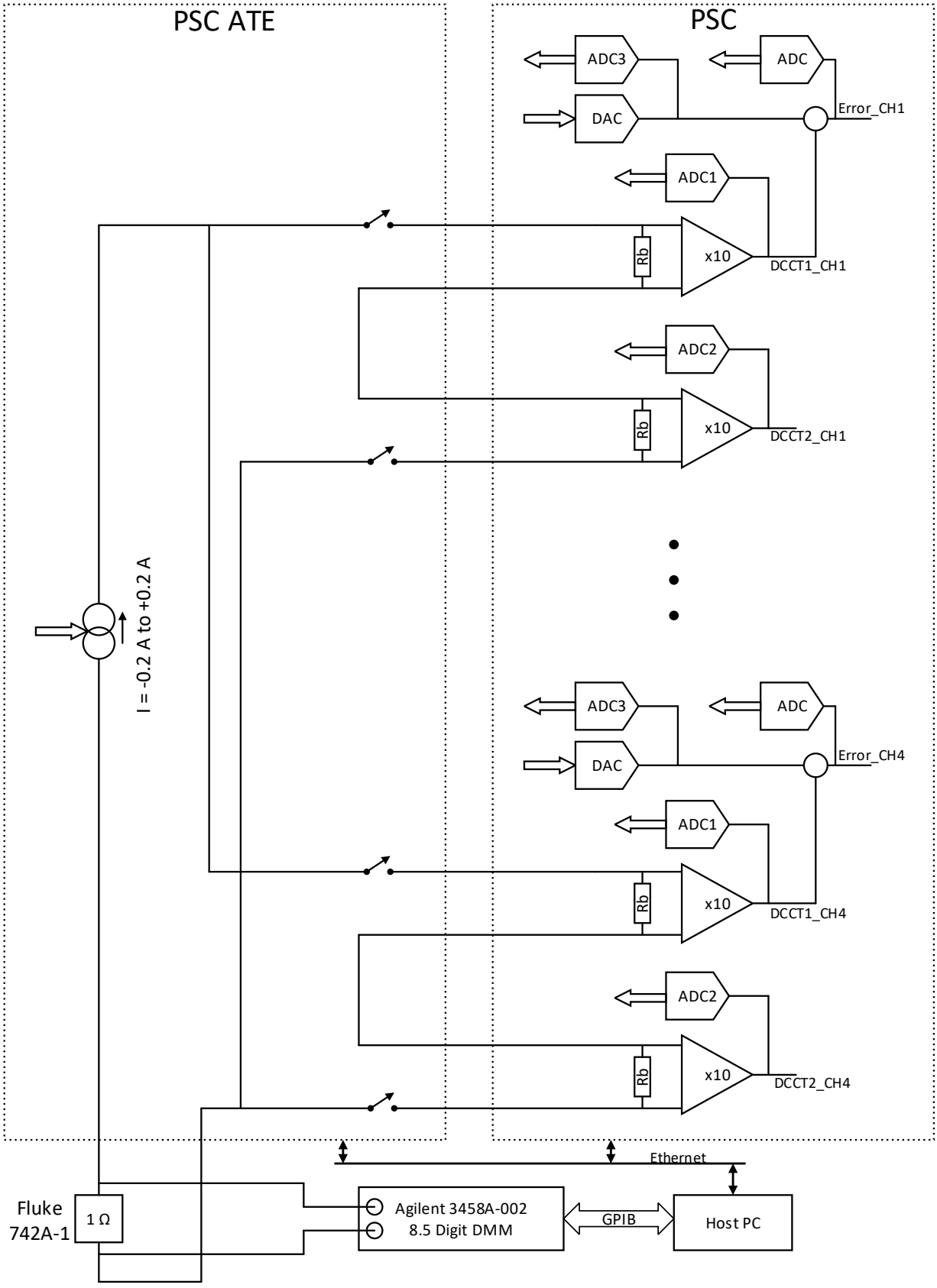
ALS-U PSCs, a.k.a. zPSCs, use either 18-bit or 20-bit digital to analog converters (DACs) for the power supply current setpoint reference and 18-bit or 20-bit analog to digital converters (ADCs) for readback of DCCT current measurements. Uncalibrated accuracy of PSCs is at the level of 0.5 %, so calibrations of PSC DACs and ADCs are performed to improve regulation and readback accuracy to the level of 20 ppm. Selectable averaging modes in the PSC further reduce measurement variation in DCCT readback data. Taken altogether, calibrated accuracy, engineered stability, traceability to accredited electrical standards, selectable integration times, and waveform capture functions confer measurement capability to the PSC approaching that of a laboratory grade 7.5 digit digital multimeter (DMM).

PSC ATE

An Automated Test Equipment (ATE) system has been built at Brookhaven National Laboratory (BNL) to carry out automated test and calibration of ALS-U PSCs. For the calibration part of testing, the ATE includes a precision bipolar current source adjustable from -0.2 A to 0.2 A and laboratory electrical standards representing the Volt and the Ohm. The calibration current source has control resolution of 20 bits. The standard for the Volt is an Agilent 3458A-002 8.5 digit digital multimeter (DMM) with high stability option (4 ppm, 1 year uncertainty). The standard for the Ohm is a Fluke 742A-1 1 Ω Standard Air Resistor. Both standards are sent out for calibration annually to accredited providers of calibration services.

In test mode, where PSC PID control loop behavior is tested, the selector switches connect the PSC's burden resistors to the part of the ATE that emulates power supply and magnet system dynamic response and corresponding DCCT secondary current. In calibration mode, ATE selector switches connect the burden resistors of the PSC under test to the calibration current source.

A block diagram of the ATE's calibration part is shown below.


PSC ATE
PSC
ADC3
ADC
DAC
Error_CH1
ADC1
Rb
x10
DCCT1_CH1
ADC2
Rb
x10
DCCT2_CH1
I = -0.2 A to +0.2 A
ADC3
ADC
DAC
Error_CH4
ADC1
Rb
x10
DCCT1_CH4
ADC2
Rb
x10
DCCT2_CH4
Ethernet
Fluke
742A-1
1 Ω
Agilent 3458A-002
8.5 Digit DMM
GPIB
Host PC

Calibration Procedure

The standard against which the PSC is calibrated is the standard reference current generated by the ATE. The current source is controlled by a host computer running a calibration program, and the circuit includes the two burden resistors of the PSC channel being calibrated and the 1 Ω standard resistor. Voltage readings across the 1 Ω standard resistor acquired by the 8.5 digit DMM provide precise measurement of the test current at each test step.

Gain and offset correction parameters are stored in PSC nonvolatile QSPI memory and can be updated either through EPICS PVs or directly through a PSC front panel USB connection.

PSC channels are calibrated one at a time. The calibration procedure goes as follows.

1. Set offset parameters for ADC1, ADC2, and ADC3 to zero, where ADC1 and ADC2 are the digitizers for DCCT1 and DCCT2 respectively, and ADC3 is the digitizer for the DAC readback.
2. Set offset parameter for DAC setpoint to zero.
3. Set gain parameters for ADC1, ADC2, and ADC3 to a value of 1.000000.
4. Set gain parameter for DAC setpoint gain to 1.000000.
5. Set the current standard to value of 10 % of full scale current for the power supply the PSC is intended for.
6. Iteratively adjust the DAC setpoint to produce a value of zero (null) from the PID error ADC.
7. Record reference current value (DMM reading), ADC1 and ADC2 readings, and the DAC setpoint value needed to null the error.
8. Repeat steps 5 through 7 but with the current standard set to a value of 90 % of full scale current.
9. Compute gain and offset corrections from the recorded data.
10. Apply gain and offset corrections for ADC1, ADC2, and DAC setpoint to PSC QSPI nonvolatile memory.
11. Set the DAC setpoint to values of 10 % and 90 % of full scale, and record DAC setpoint and ADC3 (DAC readback) values.
12. Compute gain and offset corrections for ADC3 from the recorded data.
13. Apply gain and offset corrections for ADC3 to PSC QSPI nonvolatile memory.
14. Perform verification. Repeat steps 5 through 7 at 10 % and 90 % reference current levels. Also record DAC readback data.

15. Compute gains and offsets of the measured data, and verify that calibrated readbacks have slope of 1.00000 ± allowable gain error and that calibrated offset corrections are less than allowable offset error.
16. Repeat steps 1-15 five times and compute mean and standard deviation of computed gain and offset corrections.
17. Verify that standard deviation results are consistent with allowable uncertainties.

Since PSC calibration does not include the DCCTs, it may be necessary to perform an auto-zero calibration in situ once PSCs are installed in the power supply racks.

An in-rack auto-zero procedure needs to perform the following steps.

1. Turn the power supply off.
2. Set ADC1, ADC2, ADC3, and DAC setpoint offset corrections to zero.
3. Apply measured readbacks for ADC1 and ADC2 as offset corrections for ADC1 and ADC2 to PSC QSPI nonvolatile memory.
4. Iteratively adjust DAC setpoint to give zero from the PID error ADC.
5. Apply negative value of DAC setpoint needed to null the error readback as offset correction for DAC setpoint to PSC QSPI nonvolatile memory.
6. Set DAC setpoint to zero. Apply measured readback for ADC3 as offset correction for ADC3 to PSC QSPI nonvolatile memory.