Briefs

Simple Formulas for Two- and Three-Dimensional Capacitances

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Abstract—**This paper proposes simple formulas for wiring capacitances in VLSI, including two- and/or three-dimensional effects. The accuracy of these formulas are practically sufficient for a wide range of wire thickness, wire width, and interwire spacing.**

INTRODUCTION

Two- or three-dimensional effects must be taken into account to estimate wiring capacitances in VLSI. Much effort has been made to accurately calculate this wiring capacitance by rigorous numerical analysis [1]-[3]. This type of calculation is too time-consuming, when implemented in CAD circuit programs. To overcome this situation, simple formulas which give approximate results have been proposed by Chang [4] and Elmasry [5]. However, Chang's closed form two-dimensional formula is still complicated and time-consuming, and the dependence on the parameters is not clear, though the accuracy is sufficient. On the other hand, Elmasry's empirical formula, while being simple, is not satisfactory in accuracy, although the formula can easily be physically interpreted and correctly reproduces the asymptotic behavior of the capacitances for infinitely small line thickness and large line width. In this letter, a very simple empirical formula which describes two-dimensional line capacitance is presented. Formulas which include three-dimensional effects and interline effects are also discussed.

FORMULAS

In order to develop empirical formulas for a two-dimensional case, numerical calculation has been carried out. This calculation is based on the "sub-area" method [6], [7]. The calculation errors are eliminated by dividing the system into sub-area to the extent where less than a 1-percent improvement is observed when the number of the sub-areas is doubled. The calculated results coincide with those published previously [1], [3], within a reading error.

A. Single Line on Ground Plane

The capacitance C_1 per unit length of a single line placed on bulk silicon (Fig. 1(a)) is given by

$$\frac{C_1}{E_{ox}} = 1.15\left(\frac{W}{H}\right) + 2.80\left(\frac{T}{H}\right)^{0.222} \tag{1}$$

where E_{ox} is a dielectric constant of an insulator (for SiO_2, $E_{ox} \approx (3.9) \times (8.855E\text{-}14)$ [F/cm]). The relative error of this formula is within 6 percent for $0.3 < W/H < 30$ and $0.3 < T/H < 30$, as is shown in Table I. In this formula, the first term can be considered as contributions from lower and upper surfaces of the line, and the second term represents the side wall contribution. Fig. 2 shows a comparison of the calculated results of the numerical analyses; Chang's formula [4], Elmasry's formula [5], and the present formula (1).

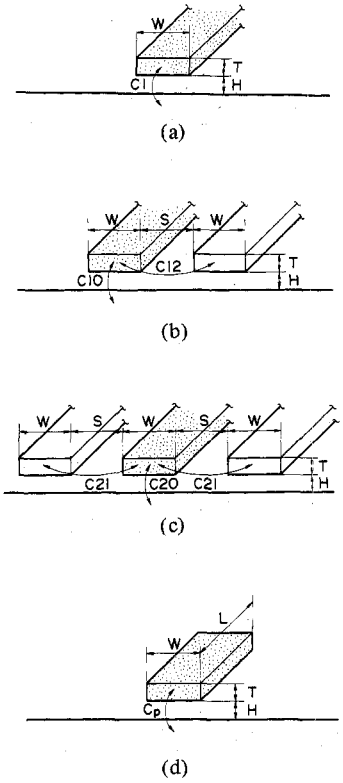

Fig. 1. Geometry of wiring. (a) Single line on ground plane. (b) Two lines on ground plane. (c) Three lines on ground plane. (d) Single plate on ground plane.

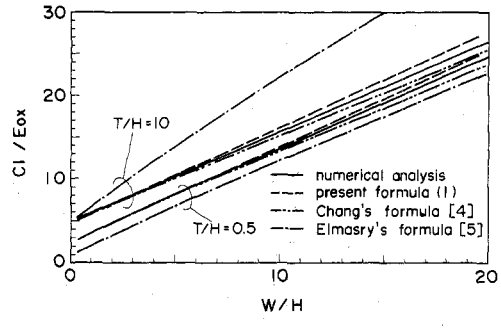

Fig. 2. Calculated wiring capacitance by various formulas.

B. Two or Three Lines on Ground Plane

When two or three lines are placed on bulk silicon, the total capacitance of one line includes the "coupling" capacitance between lines (C_{12} in Fig. 1(b) and C_{21} in Fig. 1(c)) and "ground" capacitance between the line and the ground (C_{10} in Fig. 1(b) and C_{20} in Fig. 1(c)). In the case of two lines, we designate the total capacitance of either line per unit length as

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TABLE I
RELATIVE ERROR OF SIMPLE FORMULA (1)
(Single line on ground plane.)

W/H	T/H .3	1.0	2.0	5.0	10.0	20.0	30.0
.3	1.2	2.4	-0.5	-2.5	-3.8	-3.6	-2.6
.5	1.5	1.0	-0.2	-2.6	-3.7	-3.6	-2.7
1.0	3.9	-0.5	-0.7	-2.2	-3.0	-2.8	-2.1
2.0	4.3	-0.8	-0.4	-1.1	-1.6	-1.3	-0.6
3.0	3.5	-0.3	0.3	-0.0	-0.5	-0.3	0.3
5.0	1.7	0.9	1.5	1.6	1.2	1.1	1.1
10.0	1.2	3.0	3.5	3.7	3.6	2.6	2.3
20.0	5.3	4.2	4.7	5.0	4.6	3.6	2.0
30.0	6.0	3.2	4.1	4.6	4.1	2.3	-0.2

(Errors are in %)

TABLE II
RELATIVE ERROR OF SIMPLE FORMULA (2a)
(Two lines on ground plane.)

T/H	W/H	S/H .5	1.0	5.0	10.0	20.0
.3	.3	-3.1	.6	2.0	1.6	1.3
.3	1.0	-7.7	-5.0	-3.3	-3.6	-3.8
.3	5.0	-1.7	-1.9	-1.4	-1.5	-1.6
.3	10.0	3.4	1.8	1.4	1.3	1.2
1.0	.3	4.7	5.0	4.8	3.5	2.8
1.0	1.0	.8	.7	1.3	.4	-.1
1.0	5.0	2.4	1.2	1.7	1.3	1.1
1.0	10.0	5.7	3.8	3.5	3.3	3.1
5.0	.3	4.4	-2.1	1.4	.6	-1.0
5.0	1.0	3.5	-2.9	.7	.3	-.9
5.0	5.0	2.9	-.9	2.6	2.8	2.3
5.0	10.0	3.0	1.4	4.1	4.4	4.1
10.0	.3	-1.5	-7.9	-3.3	-1.1	-1.7
10.0	1.0	-.5	-7.6	-3.1	-.8	-1.1
10.0	5.0	-1.3	-5.1	-.0	2.0	2.1
10.0	10.0	-6.1	-2.9	2.3	3.8	4.1

(Errors are in %)

TABLE III
RELATIVE ERROR OF SIMPLE FORMULA (2b)
(Three lines on ground plane.)

T/H	W/H	S/H .5	1.0	5.0	10.0	20.0
.3	.3	-4.2	.8	2.9	2.0	1.5
.3	1.0	-9.7	-5.6	-2.7	-3.3	-3.7
.3	5.0	-1.6	-2.0	-1.0	-1.4	-1.5
.3	10.0	5.4	2.6	1.8	1.5	1.3
1.0	.3	8.1	8.2	7.3	4.6	3.3
1.0	1.0	2.6	2.3	3.1	1.2	.2
1.0	5.0	3.6	1.8	2.5	1.7	1.3
1.0	10.0	7.8	4.5	4.0	3.6	3.3
5.0	.3	7.6	-.1	5.4	3.6	.5
5.0	1.0	5.9	-1.8	3.8	2.8	.4
5.0	5.0	3.7	-1.7	3.7	3.9	3.0
5.0	10.0	2.8	.3	4.6	5.1	4.6
10.0	.3	2.7	-6.3	-1.8	1.7	.5
10.0	1.0	.8	-7.6	-2.3	1.4	.7
10.0	5.0	-1.4	-6.9	-.6	2.9	3.2
10.0	10.0	-8.2	-5.5	1.5	4.3	4.7

(Errors are in %)

C_2 ($=C_{10}+C_{12}$). In the case of three lines, we designate the total capacitance of the middle line per unit length as C_3 ($=C_{20}+2*C_{21}$). Then the empirical formulas for C_2 and C_3 are expressed as follows:

$$\frac{C_2}{E_{ox}}=\frac{C_1}{E_{ox}}+\left[0.03\left(\frac{W}{H}\right)+0.83\left(\frac{T}{H}\right)-0.07\left(\frac{T}{H}\right)^{0.222}\right]\left(\frac{S}{H}\right)^{-1.34} \tag{2a}$$

and

$$\frac{C_3}{E_{ox}}=\frac{C_1}{E_{ox}}+2\left[0.03\left(\frac{W}{H}\right)+0.83\left(\frac{T}{H}\right)-0.07\left(\frac{T}{H}\right)^{0.222}\right]\left(\frac{S}{H}\right)^{-1.34}. \tag{2b}$$

The relative error of both (2a) and (2b) is less than 10 percent for $0.3<W/H<10$, $0.3<T/H<10$ and $0.5<S/H<10$, as shown in Tables II and III. It should be noted that although this formula is totally empirical, each term in (2a) and (2b) can be interpreted physically. The first term is the single line capacitance (1). The second term is to compensate the contribution related to the upper and lower surfaces of the line. The third term represents coupling effects between side walls of adjacent lines, and the last term is for the reduction in "ground" capacitance, due to the side wall. It is to be emphasized that both of (2a) and (2b) tend to be single line capacitance (1) when the line space S approaches infinity.

C. Single Plate with Finite Dimension on Ground Plane

When a single plate with finite length is put on a ground plane as shown in Fig. 1(d), the capacitance C_p between the plate and the ground includes three-dimensional effects. C_p is given by

$$\frac{C_p}{E_{ox}}=1.15\frac{(\text{area of the plate})}{H}+1.40\left(\frac{T}{H}\right)^{0.222}(\text{circumference of the plate})+4.12\left(\frac{T}{H}\right)^{0.728}H. \tag{3}$$

The calculated results of this formula coincide with the published data by Ruehli *et al.* [1] within the error of 10 percent for $0<W/L<1$, $0.5<W/H<40$, and $0.4<T/H<10$. The last term of (3) represents the contribution of the four corners of the plate. Again, it should be noted that (3) tends to (1), as the plate length approaches infinity.

In conclusion, these formulas (1)–(3) can be incorporated into CAD circuit programs with very little time consumption. Furthermore, they can be used as a VLSI design aid since the dependency of the capacitances on the line width, thickness, and space is relatively clear. This analytical transparency is useful in choosing the design rules of VLSI, together with the calculation method of the RC delays induced by the interconnection lines [8].

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Errata

In the article "Gate formation in GaAs MESFET's using ion-beam etching technology," by C.-L. Chen and K. D. Wise published in *IEEE Trans. Electron Devices*, vol. ED-29, no. 10, pp. 1522–1529, Oct. 1982, Fig. 3(a) and (b) on p. 1524 was rotated 90° clockwise inadvertently.

In the article "Investigation of polycrystalline silicon back surface field solar cells," by W. A. Orr and M. Arienzo, *IEEE Trans. Electron Devices*, vol. ED-29, no. 8, pp. 1151–1155, Aug. 1982, the caption of Fig. 2 on p. 1152 should read: "Photomicrograph of the boundary at higher magnification (132X). The (100) grain is on the left of the boundary."

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