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# Direct Formation of Wafer Scale Graphene Thin Layers on Insulating Substrates by Chemical Vapor Deposition

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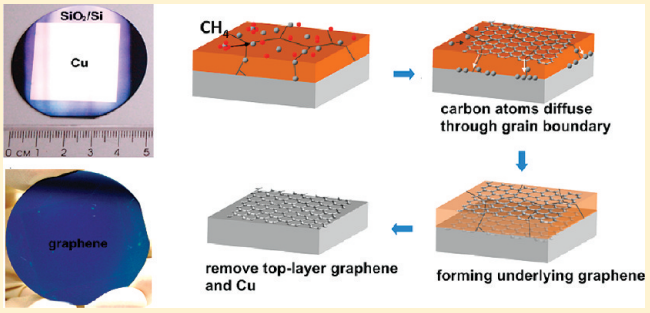
Supporting Information

**ABSTRACT:** Direct formation of high-quality and wafer scale graphene thin layers on insulating gate dielectrics such as $SiO_2$ is emergent for graphene electronics using Si-wafer compatible fabrication. Here, we report that in a chemical vapor deposition process the carbon species dissociated on Cu surfaces not only result in graphene layers on top of the catalytic Cu thin films but also diffuse through Cu grain boundaries to the interface between Cu and underlying dielectrics. Optimization of the process parameters leads to a continuous and large-area graphene thin layers directly formed on top of the dielectrics. The bottom-gated transistor characteristics for the graphene films have shown quite comparable carrier mobility compared to the top-layer graphene. The proposed method allows us to achieve wafer-sized graphene on versatile insulating substrates without the need of graphene transfer.




**KEYWORDS:** Graphene, chemical vapor deposition, Raman spectroscopy, transparent conductive film, graphitization

Single- and few-layer graphene films[1−4] are promising materials for post-silicon electronics because of their high carrier mobility and great potential of integrating bottom-up nanomaterial synthesis with top-down lithographic fabrication at wafer scale.[5] Many approaches have been used to obtain graphene layers, including mechanical and liquid phase exfoliation from graphite,[1,6,7] epitaxial growth on crystalline substrate,[8−11] and reduction from graphene oxides.[12−17] Recent developments in chemical vapor deposition (CVD) have allowed successful production of large scale graphene layers on catalytic metal substrates,[18−25] greatly encouraging the utilizing of graphene in practical fabrications. To date, large area CVD graphene has all been produced on metal substrates and it is necessary to transfer the as-grown graphene onto desired substrates. In such a wet-transfer process, for example, graphene films are capped with a supporting polymer layer, followed by metal substrate etching and polymer/graphene transfer to receiving substrates. The wet-transfer process is perhaps unfavorable in current Si-wafer fabrication processes. Hence, many efforts have been made to avoid the wet-transfer processes. Ismach et al. reported that the chemical vapor deposited graphene on Cu layer can be directly transferred onto underlying dielectrics surfaces by dewetting and evaporating the Cu layers with an extended period of thermal annealing.[26] Levendorf et al. developed a method to allow the patterned graphene on Cu to directly settle on dielectrics after etching the metal layers underneath graphene.[27] However, these transfer processes may be only feasible for the graphene with small lateral sizes. Also, some additional mechanical stress on graphene is anticipated during the transfer process. Recently, organic polymers coated on insulators have been thermally converted to few-layer graphene by a Ni capping layer.[28] Lee et al. have observed that graphene layers can be formed at the Ni and $SiO_2$ interface using plasma-enhanced CVD although the interface graphene is thick and defective.[29] It has been shown that the formation of graphene on Ni is due to the segregation or precipitation process of the carbon species dissolved in Ni.[30] Due to this effect, the carbon precipitation is a nonequilibrium process and it may be challenging to get uniform graphene films by using Ni as a catalytic metal.[21,30] Here we report that high-quality and uniform wafer scale graphene thin layers can be directly formed at the interface between Cu and insulators using a CVD method. The key idea is to deposit a thin Cu catalytic layer (~300 nm thick) on the target insulating substrates such as $SiO_2$ and quartz. By controlling the synthetic parameters, the carbon species dissociated from methane diffuse through the Cu grain boundaries to the Cu−substrate interface. Moreover, to avoid the dewetting or evaporation of Cu, our CVD process temperature is set at 900 °C, significantly lower than the 1000 °C used in other reports.[22,26] Most importantly, in addition to the structural characterization data such as Raman spectra and STM images, we have also reported the electrical characteristics for the bottom-layer graphene.

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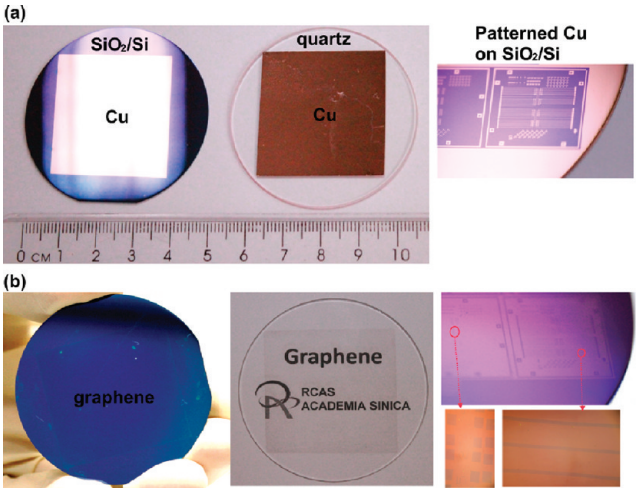


**Figure 1.** (a) Photos of 2 in. insulating substrates: Cu on $SiO_2$ (300 nm)/Si, Cu on quartz, and patterned Cu on $SiO_2$ (300 nm)/Si. (b) Photos of the as-grown bottom layer graphene on the corresponding substrates shown in (a).

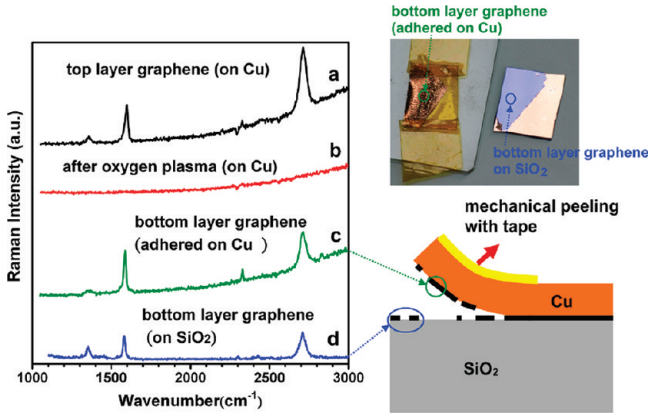


**Figure 2.** The Raman spectra for (a) as-grown top layer graphene on Cu and (b) the sample after oxygen plasma stripping, where all the top layer graphene is removed. After mechanical peeling of the Cu layer, some bottom layer graphene can be found on Cu as shown in (c), and the rest of the film stays on $SiO_2$ surfaces as evidenced by Raman curve (d).

This work may stimulate further developments in utilizing graphene for silicon-wafer compatible production.

**Results and Discussion.** It is known that the methane molecules dissociate on Cu surfaces at high temperature.[22,30,31] In this report, we observe that the carbon species not only result in graphene layers on top of the catalytic Cu thin films (top layer graphene) but also diffuse though Cu grain boundaries and directly form a graphene layer at the Cu−dielectric interface (bottom layer graphene). A conventional quartz tubular furnace was adopted to synthesize the bottom layer graphene films. To be able to directly form a graphene layer on an insulating substrate ($SiO_2$/Si, quartz or sapphire), a 300 nm Cu thin film layer was deposited on the insulating substrate and methane was used as the carbon source. After the substrate was loaded into the furnace, it was heated to 750 °C in a hydrogen atmosphere ($H_2$, 415 sccm; Ar, 400 sccm) at 500 Torr followed by thermal annealing at the same temperature for 25 min to remove native oxides on Cu. The furnace was then heated to the process temperature 900 °C in a pure $H_2$ gas environment ($H_2$, 15 sccm; pressure, 800 mTorr). After the temperature reached 900 °C, the gas condition was switched to a methane/hydrogen gas mixture ($CH_4$ = 75 sccm and $H_2$ = 15 sccm) for 5 min at 800 mTorr to grow graphene layers. During the cooling stage, the furnace was cooled to room temperature with a cooling rate ~20 °C/min, where the gas condition was maintained as the same from the beginning of growth stage to the end of cooling stage. By contrast to the conventional graphene growth temperature 1000 °C on top of Cu foils,[22] we used a relatively lower process temperature (900 °C) to avoid the evaporation and dewetting of Cu film as observed by Ismach et al.[26] Note that growth pressure is preferably not lower than 800 mTorr. Otherwise, Cu dewetting becomes pronounced due to the fast evaporation of Cu. Meanwhile, the high-temperature process 1000 °C in a $H_2$ environment shall largely degrade the quality of underlying $SiO_2$, leading to large gate leakage current if the $SiO_2$ is used directly as a gate dielectric material. With the optimized CVD synthetic condition, the bottom layer graphene can be continuous in a wafer scale.

Figure 1a shows the photos of several 2 in. substrates prepared for bottom layer graphene growth, including Cu on $SiO_2$ (300 nm)/Si, Cu on quartz, and patterned Cu on $SiO_2$ (300 nm)/Si. All these wafers were subjected to the synthetic condition mentioned above for growing bottom layer graphene. Figure 1b demonstrates the photos of the as-grown bottom layer graphene after removing the top layer graphene by oxygen plasma (power, 60 W for 6 min) and the Cu layers by $Fe(NO_3)_3$ wet etching. These photos in Figure 1 demonstrate that our growth process is able to directly form a large area and continuous thin graphene layers on top of arbitrary insulating substrates. Figure 1 shows that patterned graphene is also obtainable if patterned Cu films are used for bottom layer graphene growth. Raman measurement has been performed to further confirm that the bottom layer graphene we observed in Figure 1 was not unintentionally transferred (or settled down) from the top layer graphene. The Raman curve a in Figure 2 was taken from the as-grown top layer graphene on Cu, where G (~1598 $cm^{-1}$) and 2D (~ 2712 $cm^{-1}$) bands were clearly observed. After oxygen plasma treatment, all the Raman features for graphene vanished (curve b), demonstrating that top layer graphene was totally removed. The presence of bottom layer graphene actually weakens the interfacial adhesion between Cu and underlying $SiO_2$; hence, mechanical peeling of the Cu layer can be done using adhesive tapes. We observe that part of the bottom layer graphene is lifted by Cu film (Raman curve c) and the rest of graphene stays on $SiO_2$ substrates (Raman curve d) as shown in the photo and schematic illustration in Figure 2. These results confirm the formation of graphene layer at the Cu−insulator interface. Figure S1 in the Supporting Information further shows that the growth of graphene on several other insulators such as sapphire and ST-cut quartz is feasible.

Figure 3 schematically illustrates the growth mechanism of the graphene layers in between the catalytic Cu thin film and underlying insulating substrates. The methane molecules are dissociated into carbon species on the Cu surface. It is known that the carbon atoms possess a very low solubility in Cu; hence, they migrate on Cu surfaces to form large-area and continuous thin graphene films.[22] Meanwhile, some of these carbon species can better diffuse through the Cu grain boundaries and reach the interface between the Cu and underlying insulators. We note that there is no graphene growth underlying Cu film if methane is absent during the growth process, suggesting the bottom layer graphene formation is related to the methane precursors rather than other possible carbon impurities. Also, 300 nm of Cu thin film is close to the optimized condition for bottom layer graphene growth. Decrease in Cu thickness shall lead to pronounced dewetting of Cu from insulators as observed by Ismach et al.[26] even at 900 °C. Further increase in Cu film thickness


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results in poor continuity of the bottom layer graphene or even no graphene formation at the Cu−insulator interface, which is expected due to the length increase of carbon diffusion path from top Cu surface to the bottom interface. This observation also suggests that the formation mechanism of the bottom layer graphene underlying Cu metals is likely different from the carbon dissolution−surface segregation mechanism proposed for graphene growth on Ni surfaces.[21,30]

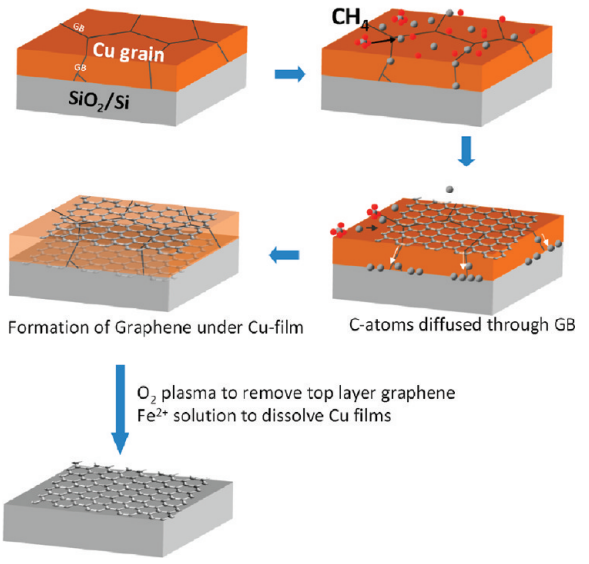


**Figure 3.** The schematic illustration of the growth. Step 1: Formation of Cu grains after thermal annealing. Step2: The $CH_4$ precursors dissociate into carbon species and migrate on Cu surfaces, where some of the carbon species diffuse downward through Cu grain boundary (GB). Step 3: The graphene layer formed on the Cu surface; meanwhile, the carbon atoms continue to diffuse through Cu GB and segregate at the Cu−insulator interface. Step 4: The graphitization of carbon atoms underlying Cu film leads to the formation of bottom layer graphene. Step 5: The large-area and continues graphene layers can be obtained directly on substrate after removing the top layer graphene, followed by wet-etching of Cu thin film.

Figure 4a shows the typical atomic force microscope (AFM) image for the bottom layer graphene grown on a $SiO_2$/Si substrate. It is clearly seen that the $SiO_2$ substrate is fully covered with the graphene layers. We show in Figure S2 (Supporting Information) the effect of growth time on the size of the obtained bottom layer graphene, where the nucleation process occurs in the beginning, followed by the graphene domain growth. We find that once our process parameters are adjusted to get large-area continuous bottom layer graphene, the film is always few-layered. The growth of bottom layer graphene seems to be not self-limited at the monolayer. Actually Yan et al. have also observed the breaking of self-limit growth on Cu surfaces, where the graphene domain boundaries and impurities in the first grown graphene layer could serve as nucleation sites for growth of additional graphene layers on top of the first layer.[24] We believe this is the main reason that we can grow wafer scale few-layer bottom graphene. Figure S3 in the Supporting Information shows that the film thickness obtained from the AFM cross-section measurements is around 1.34 nm, suggesting that the bottom layer graphene is thin (about 2 to 3 layered). It is also noted that a wrinkle-like structure exists in the AFM image (Figure 4a), where the domain size surrounded by the wrinkles is similar to the Cu grain size as revealed in the optical micrograph (Figure 4a inset). Figure 4c displays the low magnification TEM cross section of the Cu/$SiO_2$ after graphene growth, where we clearly observe the void formed between two Cu grains. The graphene and excess carbon materials may accumulate at the

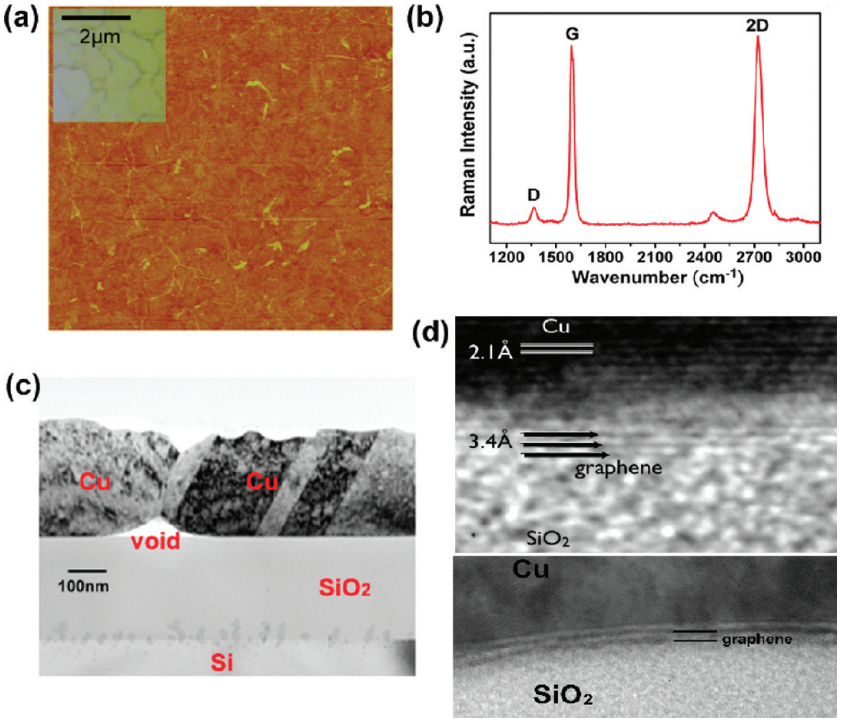


**Figure 4.** (a) Typical AFM image for the bottom layer graphene grown on a $SiO_2$/Si. (Insert) Optical micrograph of the Cu layer after graphene growth. Note that graphene is not visible but Cu grains can be identified. (b) Raman spectrum (excited by 473 nm laser) for the bottom layer graphene, where D, G, and 2D bands are indicated in the figure. (c) Low-magnification and (d) high-magnification TEM for the Cu−graphene−$SiO_2$ cross section.


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void area during the growth and Cu etching process. Meanwhile, the channels between Cu grains, which may be the major C diffusion routes, are also observed in Figure 4c. Figure 4d shows the high magnification TEM image for the Cu−graphene−$SiO_2$ interface, where we can identify the presence of trilayer and bilayer graphene. This is the direct evidence for bottom layer graphene at the interface between copper and silicon dioxide. Figure S4 in the Supporting Information displays the scanning tunneling microscopy (STM) image for the bottom layer graphene on $SiO_2$/Si. The STM measurement was carried out in a Veeco STM base operated with the constant current mode in ambient condition. We can see hexagonal carbon lattice in most of the area. Occasionally, the A−B stacked (i.e., Bernal stacked) bilayer graphene can be observed as indicated by a circle, where the atomic configuration was schematically shown in the inset.[32] It is noteworthy that not all the area shows a clear A−B stacking feature in STM, suggesting other stacking configurations also exist. Figure 4b displays the typical Raman spectrum (excited by 473 nm laser) for the bottom layer graphene. The graphene sheet exhibits an intense G band at around 1590 $cm^{-1}$ and a sharp 2D band at around 2720 $cm^{-1}$, suggesting that the bottom layer graphene is highly graphitized, which is consistent with the STM observation in Figure S4, Supporting Information. Note that there is still a weak D band observed in the Raman spectrum. Figure S5a in the Supporting Information shows the Raman map constructed by plotting the intensity ratio of 2D and G band, $I(2D)/I(G)$, which has been used to indicate the number of layers for CVD graphene.[21] The Raman $I(2D)/I(G)$ mapping consistently suggests that the bottom layer graphene is thin and continuous, likely ranging from two to three layers. One may be interested in comparing the top and bottom layer graphene, and we show in Figure S5b (Supporting Information) the Raman spectra for both the top and the bottom layer graphene obtained from our optimized reaction process (for bottom layer graphene). In brief, both layers similarly exhibit a small D band, which is likely unavoidable due to the high $CH_4/H_2$ gas ratio and lower growth temperature (900 °C) optimized for obtaining large-area bottom graphene. To understand more about the growth behaviors of bottom layer graphene, some systematic investigations on growth parameters, such as the growth temperature and the thickness of Cu thin film, have been performed (see Figure S6, Supporting Information, for the Raman results). In brief, lower growth temperature (e.g., 850 °C) was not able to form a continuous film underlying Cu and the Raman D band of the film is high, likely due to the poor graphitization at low temperature. When the temperature is higher than 950 °C, the defect level of the film is also high. This could be due to the segregation of carbon species to the Cu−insulator interface being faster than the graphitization.

Figure 5 shows the optical measurement results for the bottom layer graphene directly grown on quartz. It has been reported that one layer graphene absorbs ~2.3% of light.[33] The bottom layer graphene absorbs about 5.2% of light, which consistently suggests that the graphene layer we obtained is on average about two layered. The sheet resistance ($R_s$) data obtained in a four-point probe system for our bottom-layer graphene is ~2 kΩ/sq. To evaluate the electrical performance of these graphene sheets, the bottom layer graphene on $SiO_2$/Si was patterned into a strip with the width around 10 $\mu$m using conventional photolithography. The bottom-gate operated transistors were fabricated by evaporating Au electrodes directly on top of the patterned graphene. Figure 6a demonstrates the transfer curve (drain current $I_d$ vs gate voltage $V_g$) for the device prepared.

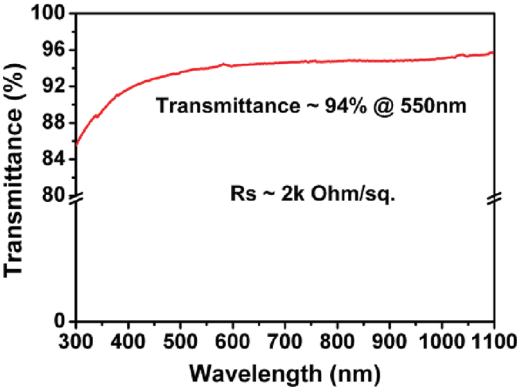


**Figure 5.** The optical transmittance for a bottom layer graphene grown on a 2 in. quartz substrate. The sheet resistance of as-grown bottom layer graphene is ~2 kΩ/sq (with ~94% transmittance). The inset shows that the as-grown wafer scale graphene film is conductive.

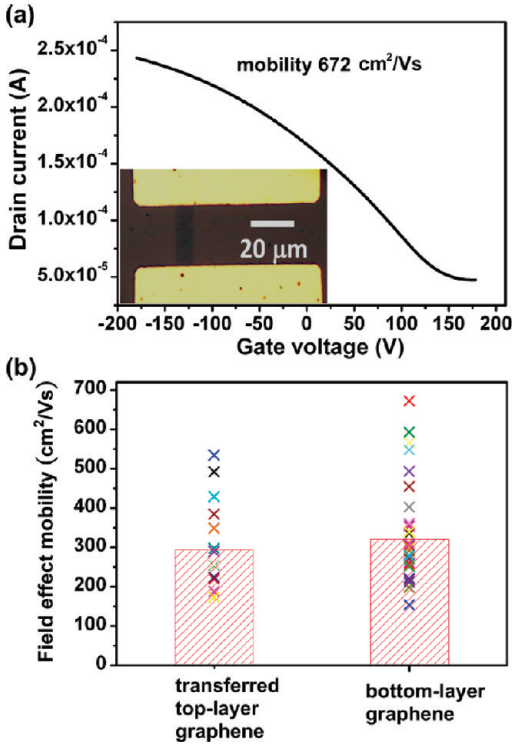


**Figure 6.** (a) Transfer curve (drain current $I_d$ vs gate voltage $V_g$) for a device prepared from a patterned bottom layer graphene film. Inset shows the photograph of the device. (b) Statistical field-effect mobility data for the devices made from top layer graphene (process condition was separately optimized for single-layer graphene on Cu and then transferred onto $SiO_2$/Si for device fabrication) and bottom layer graphene (as discussed in text). The bar chart with red-shaded box shows the average value of mobility for transferred top-layer graphene (17 devices tested) and bottom-layer graphene (35 devices tested).

Inset shows the top view of the device. The field-effect mobility of holes was extracted based on the slope $\Delta I_d/\Delta V_g$ fitted to the linear regime of the transfer curves using the equation $\mu = (L/WC_{ox}V_d)\cdot(\Delta I_d/\Delta V_g)$, where $L$ and $W$ are the channel length and width and $C_{ox}$ is the gate capacitance.[34] The effective field effect mobility for the graphene device can be up to 670 $cm^2/(V\cdot s)$ in ambient. We note that the neutrality point (valley point of the transfer curve) for most


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of our devices is beyond 100 V (the maxima $V_g$ we applied), suggesting that the graphene sheets are heavily p-doped. It is known that p-doping of graphene in ambient has been well explained by intrinsic graphene screening of charge at the graphene/$SiO_2$ substrate interface.[35,36] Ryu et al. have demonstrated that thermal annealing induces a pronounced distortion in the graphene sheet on $SiO_2$.[37] This structural deformation closely coupled to silicon dioxide at room temperature. When exposed to atmosphere, it greatly promotes hole doping caused by ambient $O_2$ and moisture. It is noted that our graphene was directly grown on $SiO_2$ at 900 °C; therefore, the heavy p-doping in our case is anticipated. Figure 6b compares the statistical results of field effect mobility for the devices prepared from the bottom layer graphene and those from the top layer graphene (process condition was separately optimized for single-layer graphene on Cu and typical transfer processes[22] were adopted to transfer top layer graphene onto $SiO_2$/Si for device fabrication). These results show that the field effect mobility for these two types of film, i.e. single-layered top graphene and few-layered bottom graphene, are roughly comparable in our device structure. The mobility value reported here is likely limited by other factors such as photoresist residues, metal contact, or etching process.

**Conclusions.** In conclusion, we report the first direct synthesis of wafer scale graphene thin layers on arbitrary insulating substrates using a CVD method with the assistance of Cu thin film. The growth mechanism of bottom layer graphene underlying Cu has also been proposed. The sheet resistance values are obtained directly on the substrate used in CVD growth without the need of performing graphene transfer. Most importantly we have also obtained the field effect mobility for the bottom layer graphene directly using the $SiO_2$/Si as the bottom gate. We hope this work shall stimulate more research efforts in direct formation of graphene films on insulators for Si-wafer compatible device fabrications.

## ■ ASSOCIATED CONTENT

**Supporting Information.** Raman spectra and AFM images. This material is available free of charge via the Internet at http://pubs.acs.org

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## ■ ACKNOWLEDGMENT

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