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Wafer-scale synthesis of multi-layer graphene by high-temperature carbon ion implantation

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We report on the synthesis of wafer-scale (4 in. in diameter) high-quality multi-layer graphene using high-temperature carbon ion implantation on thin Ni films on a substrate of SiO_2/Si. Carbon ions were bombarded at 20 keV and a dose of 1×10^{15} cm^{-2} onto the surface of the Ni/SiO_2/Si substrate at a temperature of 500 °C. This was followed by high-temperature activation annealing (600–900 °C) to form a sp^2-bonded honeycomb structure. The effects of post-implantation activation annealing conditions were systematically investigated by micro-Raman spectroscopy and transmission electron microscopy. Carbon ion implantation at elevated temperatures allowed a lower activation annealing temperature for fabricating large-area graphene. Our results indicate that carbon-ion implantation provides a facile and direct route for integrating graphene with Si microelectronics. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4926605]

In the last decade, graphene has been intensively studied for its unique optical, mechanical, electrical, and structural properties, including its high optical transmittance, superior thermal and electrical conductivities, capacity for ballistic transport, and high failure strain.[1–5] Many fabrication techniques, including mechanical cleavage of highly oriented pyrolytic graphite, Hummer's method, high-temperature annealing of silicon carbide, ion implantation, and chemical vapor deposition (CVD), have been investigated for their capacities to obtain high-quality graphene with good uniformity and size.[1,2,5] Although CVD is widely used for the large-area synthesis of graphene using Cu or Ni films, the CVD method requires a high growth temperature above 1000 °C and a subsequent transfer process of the graphene from the metallic film to a target substrate by using poly(methyl methacrylate) (PMMA).[6,7] Neither the high growth temperature nor this transfer process is compatible with Si microelectronics, which limits the implementation of graphene. In Si microelectronics, graphene is a potential contact electrode and interconnection material. This renders high processing temperatures undesirable, especially for back-end-of-line (BEOL) fabrication, as temperature-induced damage, strains, metal spiking, and unintentional diffusion of dopants may occur.[8]

Ion implantation, which is compatible with Si microelectronics, can mechanically damage the substrate, but this is limited by controlling the kinetic energy of the incident ions and curing the damage by post-implantation annealing. Although high-temperature annealing is essential for synthesis or activation after ion implantation, the necessary activation annealing temperature can be lowered by performing the implantation itself at an elevated temperature.[8] In other words, the mounting stage where the samples are subject to ion implantation can be heated during the implantation process. With this knowledge, the well-matured and microelectronics-compatible carbon ion implantation method has been proposed as a scalable, low-temperature route to directly synthesize graphene on Si substrates;[9–11] commercial ion implanters can support wafer substrates with diameters up to 300 mm. Baraton *et al.* and Gutierrez *et al.* reported the fabrication of graphene structures by the high-temperature annealing of Ni thin films implanted with carbon ions, as the solubility of carbon in Ni is temperature-dependent.[9,10] Bangert *et al.* reported the doping of graphene with boron by low energy ion implantation, which may solve graphene's chemical doping issues such as contamination and long-term instability.[11] The ion implantation technique also offers finer control on the final structure of the product than other methods, as the graphene layer thickness can be precisely determined by controlling the dose of carbon ion implantation.

In this paper, we demonstrate the direct synthesis of wafer-scale graphene by carbon ion implantation at a high implantation temperature (500 °C) and investigate the effects of both post-implantation annealing conditions and the presence of a capping layer on the fabrication of high-quality multi-layer graphene.

Figures 1(a)–1(d) depict the fabrication procedure. A 200-nm-thick Ni film is deposited onto a 4-inch SiO_2/Si (300 nm/500 μm layer thickness) wafer using an electron-beam evaporator (UEE, ULTECH) as shown in Fig. 1(a). The Ni layer, with high carbon solubility, acts as a catalyst for graphene synthesis. The Ni/SiO_2/Si wafer is pre-annealed at 500 °C for 90 s by rapid thermal processing technique to increase the average Ni grain size. Figure 1(b) illustrates the Ni films being subjected to carbon ion implantation at an energy of 20 KeV with a dose of 1×10^{15} ions/cm^2 at a tilt angle of 7° (Impheat, Nissin). The projected range-of-penetration depth by ions implanted at 20 keV was approximately 24 nm, according to the calculation by Stopping and Range of Ions in Matter (SRIM) program; this was intentionally close to the top surface of the Ni film to minimize possible damage to the SiO_2/Si substrate. The implantation process was performed at 500 °C to reduce implantation-induced

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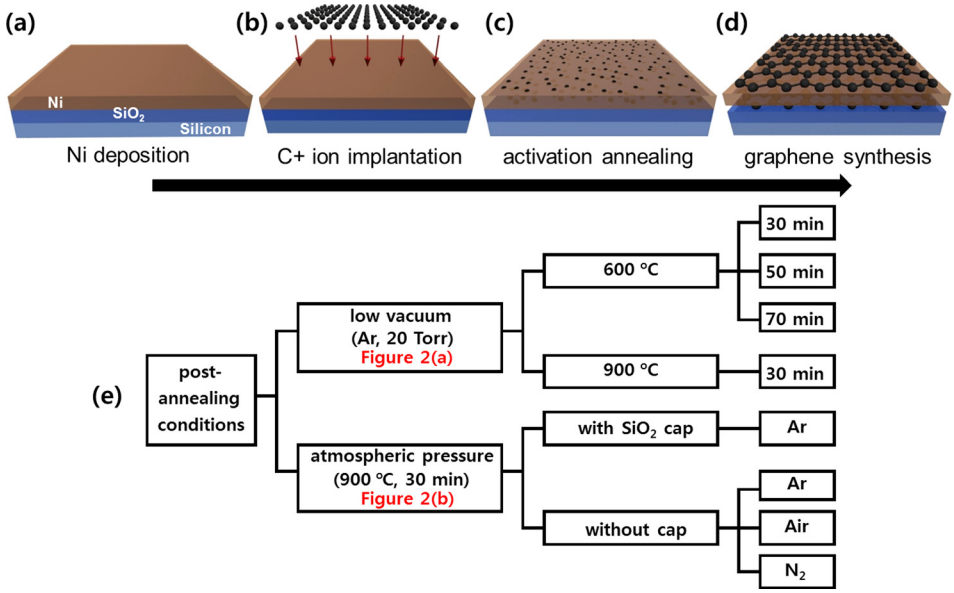

FIG. 1. Schematics of (a) E-beam evaporation of Ni on SiO_2/Si substrate, (b) carbon ion implantation into Ni, (c) post-implantation activation annealing at various conditions, and (d) graphene synthesized on both sides of Ni layer. (e) Diagram of the post-implantation activation annealing conditions.

damage and lower the required activation annealing temperature. Figures 1(c) and 1(e) show the annealing conditions, including the ambient gas, annealing time, pressure, and temperature, for each sample, heated using a horizontal tube furnace (TF55035A, Lindberg/Blue M). The furnace was cooled rapidly at a rate of 15 °C/s for quenching. Graphene grew on both faces of the Ni film, as shown in Fig. 1(d).

The graphene grown on top of the Ni films was characterized by Raman scattering; afterwards, the graphene was transferred onto another SiO_2/Si substrate by the PMMA-based transfer method. Graphene found to have grown beneath the Ni films was also characterized by Raman scattering, using the procedure described. After the graphene synthesized on top of the Ni film was etched using reactive-ion etching (RIE5000, SNTEK) with O_2 plasma for 5 s (O_2 flowing at 20 sccm, plasma power of 100 W), the samples were immersed in a solution of $FeCl_3$ (Sigma-Aldrich) to remove Ni. Micro-Raman spectroscopy was performed in back-scattering mode, using the 532 nm line of a diode-pumped solid-state laser (Omicron) at room temperature with a beam size at the sample surface of approximately 3 μm. The graphene/Ni/SiO_2/Si substrate was cut using a focused-ion beam technique (Quanta 3D 200, FEI) to prepare the specimen for examination by transmission electron microscopy (TEM, Tecnai F30 G2ST, FEI). The SiO_2 cap was deposited by plasma-enhanced chemical vapor deposition (PECVD, High-DEP, BMR).

The effects of the post-implantation annealing temperature and time on the graphene synthesis are characterized as shown in Fig. 2(a). Three characteristic phonon peaks are observed by Raman scattering at approximately 1350 cm^{-1} (D peak), 1580 cm^{-1} (G peak), and 2700 cm^{-1} (2D peak), confirming the synthesis of multi-layer graphene at an activation temperature of 600 °C on the wafer, based on the intensity ratio of G to 2D peaks (I_G/I_{2D}) and the position of the 2D peak.[4,6,9] This is very promising for the integration of graphene with Si microelectronics, showing that graphene can be directly synthesized on Si substrate at the temperatures as low as 600 °C. The intensity ratio of D to G peaks (I_D/I_G) of our graphene synthesized at 600 °C is lower than those reported by other groups in which graphene was obtained by carbon ion implantation at the same temperature (600 °C),[12] which we attribute to the higher temperature during implantation in our experiment. High temperature ion implantation is known to reduce the necessary post-implantation activation temperature and decrease the concentration of defects in the lattice.[8,13] The graphene grown at an annealing temperature of 600 °C under low vacuum

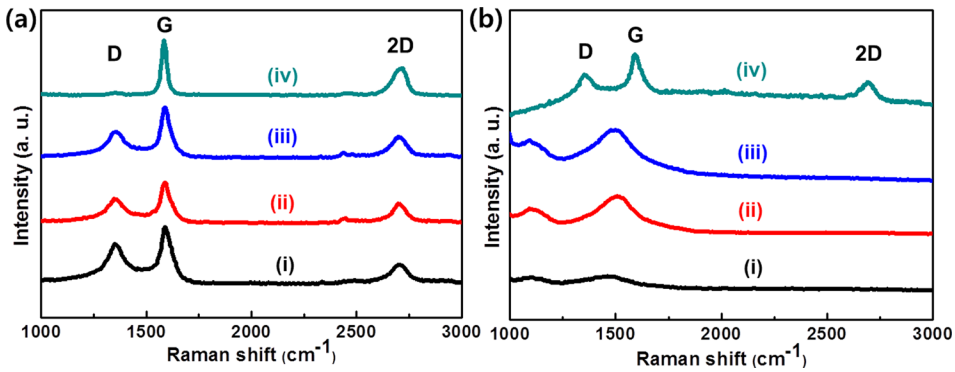

FIG. 2. (a) Thermal annealing of implanted samples under low vacuum (Ar ambient, 20 torr) at temperatures of (i) 600 °C for 30 min, (ii) 600 °C for 50 min, (iii) 600 °C for 70 min, and (iv) 900 °C for 30 min. (b) Thermal annealing of implanted samples at a temperature of 900 °C for 30 min under atmospheric pressure: (i) Ar ambient without cap, (ii) N_2 ambient without cap, (iii) dry air ambient without cap, and (iv) Ar ambient with SiO_2 cap.

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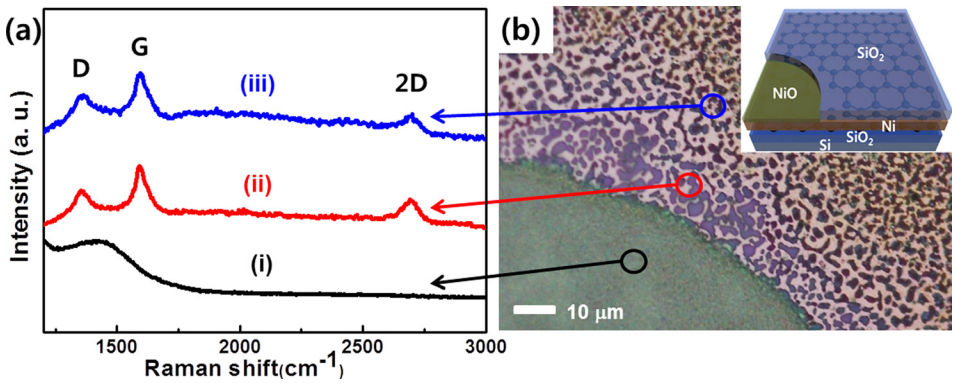

FIG. 3. (a) Raman spectra from different positions after thermal annealing at a temperature of 900 °C for 30 min under atmospheric pressure (Ar ambient with SiO_2 cap): (i) Ni exposed during thermal annealing; (ii and iii) Ni protected during thermal annealing. (b) Microscope image showing the protected and exposed areas. Inset provides schematic of the microscope image.

conditions (Ar, 250 sccm) contained a high density of defects. The average distance between the defects, L_D, can be estimated using the equation[14]

$$L_D^2(\mathrm{nm}^2) = \frac{4.3 \times 10^3}{E_L^4(\mathrm{eV}^4)} \left[\frac{I(D)}{I(G)}\right]^{-1}, \quad \text{valid for } L_D > 10\,\mathrm{nm},$$

in which E_L is the laser excitation energy, here equal to 2.33 eV. The average distances between the defects, L_D, of the graphene grown at an annealing temperature of 600 °C was ~15 nm (Fig. 2(a)(i)), ~16 nm (Fig. 2(a)(ii)), and ~17 nm (Fig. 2(a)(iii)). However, we obtained better-quality graphene at the higher annealing temperature of 900 °C (see Fig. 2(a)(iv)). The full-width-at-half-maximum (FWHM) of the sample annealed at 900 °C (Fig. 2(a)(iv)) is equal to 28.5 cm^{-1}, which is much smaller than those (51.8–61.0 cm^{-1}) of the samples annealed at 600 °C (Fig. 2(a)(i, ii, and iii)). In addition, the D peak of the sample annealed at 900 °C is minimal, with a low I_D/I_G ratio (0.037) compared with the high I_D/I_G ratios (0.49–0.66) of the samples activated at 600 °C, regardless of the annealing time duration. L_D of the graphene annealed at 900 °C was approximately 63 nm, which is longer than the samples annealed at 600 °C. This shows that the annealing temperature is more critical for producing high-quality graphene than the annealing time for synthesis by carbon ion implantation.

Although graphene was manufactured under reduced pressures, the effects of changing the ambient gas species and pressure remained of interest. The results in Fig. 2(b) indicate the negative effects of oxygen molecules during activation annealing. In our experiments, graphene was not obtained by activation annealing under atmospheric pressure, which can be explained by the presence of oxygen molecules,[15,16] although the tube furnace chamber was purged with the various ambients before each thermal annealing cycle. In our experiments, reduced pressure was more effective than atmospheric pressure in removing oxygen molecules from the annealing chamber, in combination with purging. The peak at 1490 cm^{-1} in plots (i), (ii), and (iii) of Fig. 2(b) is ascribed to NiO,[17] confirming that the carbon source was consumed by reactions with oxygen molecules, and Ni reacted with oxygen molecules to form the oxide. For this reason, we deposited a protective capping layer of SiO_2 on top of the Ni using

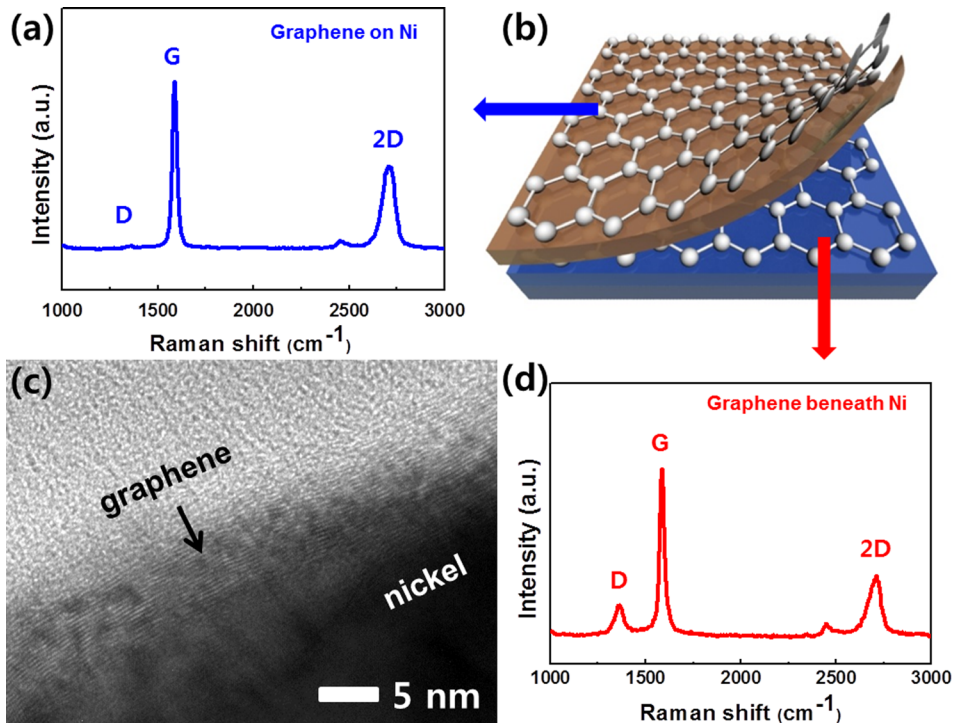

FIG. 4. (a) Raman spectrum from graphene synthesized on top of Ni. Note that Raman spectrum was obtained after graphene was transferred to SiO_2/Si substrate. (b) Schematic image of graphene synthesized on both sides of Ni by ion implantation. (c) Cross-sectional TEM image showing graphene synthesized on Ni. (d) Raman spectrum from graphene synthesized at bottom of Ni. Note that Raman spectrum was obtained after removal of top graphene and Ni.

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PECVD, followed by activation annealing at the same conditions as the samples shown in plots (i), (ii), and (iii) of Fig. 2(b). Spectrum (iv) in Fig. 2(b) shows the efficacy of the SiO_2 cap as an oxidation barrier. To understand the oxidation protection more clearly, spectra from three different positions were compared. Figures 3(a) and 3(b) confirm that the PECVD-grown SiO_2 layer can protect the carbon source from oxidation even at elevated temperatures. Our experiments indicate that the SiO_2 layer allows the synthesis of graphene without a low-pressure chamber. Additionally, graphene growth at selected areas is possible by a combination of photolithographic patterning, which can obviate the isolation process in the device fabrication procedure.

Using ion implantation, graphene can also be synthesized at the bottom of the Ni film, because some carbon atoms can diffuse through the Ni at elevated temperatures. We observed graphene at the bottom of the Ni layer, although its coverage was poor compared with that of the graphene synthesized on top of the Ni. We believe that the graphene coverage on either face of the Ni layer can be manipulated by controlling the carbon ion energy. Figures 4(a) and 4(d) present Raman spectra of the graphene synthesized on and beneath the Ni layer, respectively. Although graphene was observed on both faces (see Figure 4(b)), the graphene synthesized on top of the Ni layer showed better quality, based on the I_D/I_G ratio (0.015 and 0.18 above and beneath the Ni, respectively) and FWHM (25.5 and 27.6 cm^{-1} above and beneath Ni) of the G peak. This is likely because we intended the projected penetration depth to be closer to the top of the Ni layer in our experiments. A cross-sectional TEM image (Fig. 4(c)) confirms the presence of multi-layer graphene synthesized on top of the Ni layer. For the integration of graphene into advanced Si microelectronics, large-area graphene free of wrinkles, tears, and residues must be deposited on Si wafers at low temperatures; this cannot be achieved with CVD graphene and the PMMA-based transfer method. We believe that the ion implantation technique has great potential for the direct synthesis of wafer-scale (over 300 mm in diameter) graphene for integrated circuit technologies.

In conclusion, we demonstrated the direct growth of multi-layer graphene on 4-inch $Ni/SiO_2/Si$ wafers by high-temperature carbon ion implantation. We systematically investigated the effects of the post-implantation annealing conditions on the synthesis of high-quality multi-layer graphene by varying the ambient pressure, ambient gas, temperature, and time during the treatment. Carbon ion implantation at a temperature of 500 °C was helpful to enhance the quality of the graphene, which was synthesized on both faces of the Ni layer. The presence of oxygen molecules during the activation annealing resulted in the formation of NiO; a PECVD-grown SiO_2 cap provided an oxidation protection layer. Our results show that graphene fabricated via ion implantation can ease the implementation of graphene in advanced Si microelectronics.

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