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Electrical characterization of back-gated bi-layer MoS_2 field-effect transistors and the effect of ambient on their performances

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Two-dimensional transition-metal dichalcogenides such as MoS_2 are promising channel materials for transistor scaling. Here, we report the performance and environmental effects on back-gated bi-layer MoS_2 field-effect transistors. The devices exhibit Ohmic contacts with titanium at room temperature, on/off ratio higher than 10^7, and current saturation. Furthermore, we show that the devices are sensitive to oxygen and water in the ambient. Exposure to ambient dramatically reduces the on-state current by up to 2 orders of magnitude likely due to additional scattering centers from chemisorption on the defect sites of MoS_2. We demonstrate that vacuum annealing can effectively remove the absorbates and reversibly recover the device performances. This method significantly reduces the large variations in MoS_2 device caused by extrinsic factors. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3696045]

Two-dimensional materials have attracted a lot of interests to study interesting physics and electronic devices.[1] As an outstanding example, graphene devices have shown large carrier mobility up to $\sim 10^5$ cm^2/Vs and cut-off frequency higher than ~100 GHz.[2] However, the absence of bandgap inhibits its applications as logic devices. Although one could open a bandgap in graphene by making nanoribbons, the carrier mobility is much degraded due to edge scattering.[3] Alternatively, layered transition-metal dichalcogenides (TMDs) such as MoS_2 are semiconductors with a bandgap of ~1.1–2 eV, which makes them suitable for CMOS-like logic device applications.[4–7] The absence of dangling bonds and the low dimensionality make TMDs outperform Si transistors at the scaling limit.[7]

Recently, monolayer MoS_2 field-effect transistors (FETs) and inverters have been demonstrated,[5,6] with room-temperature on/off ratio of 10^8 and mobility higher than 200 cm^2/Vs. On the other hand, bi-layer MoS_2 devices are also interesting and could outperform single-layer devices because of the following reasons: (1) bi-layer MoS_2 has a smaller bandgap,[4,8] thus higher on-state current at a given gate bias; (2) bi-layer MoS_2 are less sensitive to ambient due to less specific surface area; (3) similar to graphene, the bandgap of bi-layer MoS_2 is tunable by vertical electric field, therefore, opening the possibility of bandgap engineering.[9] However, bi-layer MoS_2 devices have not been systematically studied so far.

In this work, we report the performance of the back-gated bi-layer MoS_2 FETs. At room temperature, the bi-layer MoS_2 FETs exhibited on/off ratio of 10^7, Ohmic contacts, and current saturation. Temperature-dependent measurements indicated a small Schottky barrier of ~65 meV at the titanium contacts. Furthermore, from electrical measurements and X-ray photoemission spectroscopy (XPS), we found that as-made MoS_2 devices showed much degraded on-state current and large variations[6] due to accumulative exposure to ambient oxygen and water in the fabrication process. We demonstrated that a simple vacuum annealing (VA) step could effectively remove the absorbed oxygen and water and recover the "intrinsic" device performances in a fully reversible manner.

We started the device fabrication by micro-cleavage of bi-layer MoS_2 on degenerately n-doped Si (100) substrates with 300 nm thermal oxide (Fig. 1(a)).[5,6] Atomic force microscopy (AFM) was used to confirm bi-layer MoS_2 samples (Fig. 1(b)).[10] We used photolithography to pattern source/drain contacts, followed by electron-beam evaporation of 40-nm-thick Ti electrodes and lift-off. The devices were further annealed at 400 °C in a mixture of hydrogen and argon to improve contacts. Electrical measurements were carried out with an Agilent 4156 C parameter analyzer in a close-cycle cryogenic probe station.

Fig. 2(a) shows the I_{ds}-V_{bg} characteristics of a representative bi-layer MoS_2 FET with channel length $L \sim 800$ nm and width $W \sim 800$ nm (Fig. 1(c) inset), showing n-type transistor behavior.[5,6] When probed in air, the device had a low on-state conductivity $\sigma_{on} = \frac{I_{ds}}{V_{ds}}\frac{L}{W} = 13$nS and a large hysteresis, typical for all the fabricated monolayer and bi-layer devices. The extrinsic field-effect mobility $\mu = \frac{dI_{ds}}{dV_{bg}}\frac{L}{WC_gV_{ds}} \sim 0.12$ cm^2/Vs at this stage, where C_g is the gate capacitance per unit area. The low conductivity was not likely due to contact resistance because of the high temperature annealing step and instead, was attributed to the absorbed oxygen and water molecules from the ambient as discussed later.[6] It is well known that vacancies in the basal plane and edges of MoS_2 have high catalytic activity for oxygen and water chemisorption at room temperature,[11,12] which could act as local Coulomb scatters for electrons. The absorbed species also caused large hysteresis, similar to carbon nanotube devices.[13]

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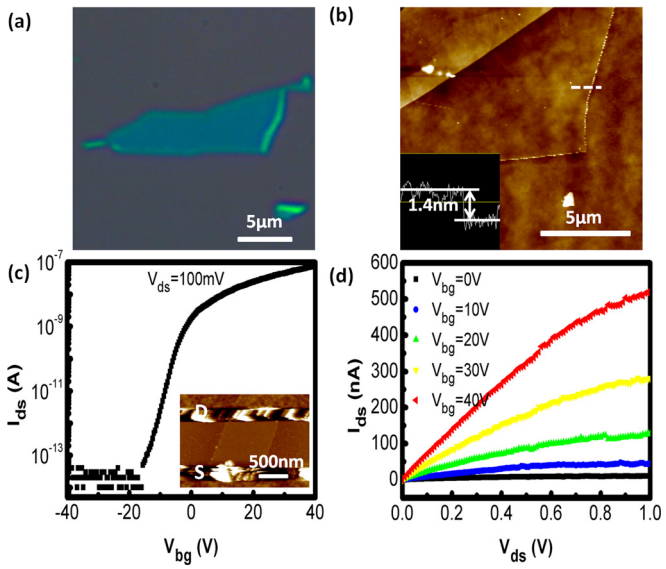

FIG. 1. (Color online) (a) Optical image of a bi-layer MoS_2 exfoliated on Si/SiO_2 substrate. (b) AFM image of a bi-layer MoS_2. (Inset) Cross-sectional profile along the white line showing the height of ~1.4 nm. (c) I_{ds}-V_{bg} curve for a back-gated bi-layer MoS_2 FET ($V_{ds} = 100$ mV). (Inset) AFM image of the device. (d) From bottom to top, I_{ds}-V_{ds} characteristics of the same device in (c) for $V_{bg} = 0$–40 V in steps of 10 V. (c) and (d) are measured at room temperature after vacuum annealing.

Next, we put the device under high vacuum (~10^{-6} Torr). As expected, we immediately observed an on-state current increase by ~10 times (at $V_{ds} = 100$ mV) and a reduced hysteresis (Fig. 2(a) and inset). Longer vacuum treatment at room temperature did not afford much more improvement. However, as we annealed the device *in-situ* to ~350 K (limited by our setup) under high vacuum, the on-state current gradually increased over the course of several hours, to a stable level which was ~5 times higher than the vacuum level (Fig. 2(a) and inset). Compared to the as-made device in air, the simple VA step increased the low-bias conductance by ~55 times. In other devices, we observed conductance change by more than 2 orders of magnitude after VA.

We used XPS to confirm the oxygen and water desorption by vacuum annealing. We compared MoS_2 samples cleaved and stored in air and samples undergone 350 K vacuum annealing in XPS chamber for 24 h (Fig. 2(b)). Both samples showed a broad peak near 532 eV, which could be partially assigned to absorbed oxygen or water molecules.[12,14] The oxygen signal reduction by 43% after vacuum annealing confirmed the partial oxygen and water desorption. The remaining oxygen after annealing was probably strongly bonded to the edges and defects, which required higher temperature to remove. However, our samples were not heavily oxidized as we did not observe any signatures of MoO_3 (as triplet in the Mo 3 d region) in the XPS (Fig. 2(b) inset).[15]

To further investigate the effect of environments on MoS_2 FETs, we measured the devices under a controlled oxygen pressure (Fig. 2(c)). We first did the vacuum annealing to recover the on-state current, followed by gradual increase of dry oxygen pressure (99.999% purity). After reaching each pressure set point, we waited for ~5 min for the absorption process to reach equilibrium before measuring the devices. We found that the on-state conductivity and mobility dropped dramatically as we increased the oxygen pressure and reached a plateau beyond ~500 Torr (Fig. 2(d)). The non-linear dependence of conductivity suggested a self-limiting absorption process, where most of the defect sites were already occupied by oxygen at high pressure. We stress that the vacuum annealing step can reversibly recover the on-state current of MoS_2 devices after repeated oxygen and air exposure (Fig. 2(c) inset). After vacuum annealing, a typical device (Fig. 1(c), d) showed $\sigma_{on} = 756$ nS, on/off ratio of

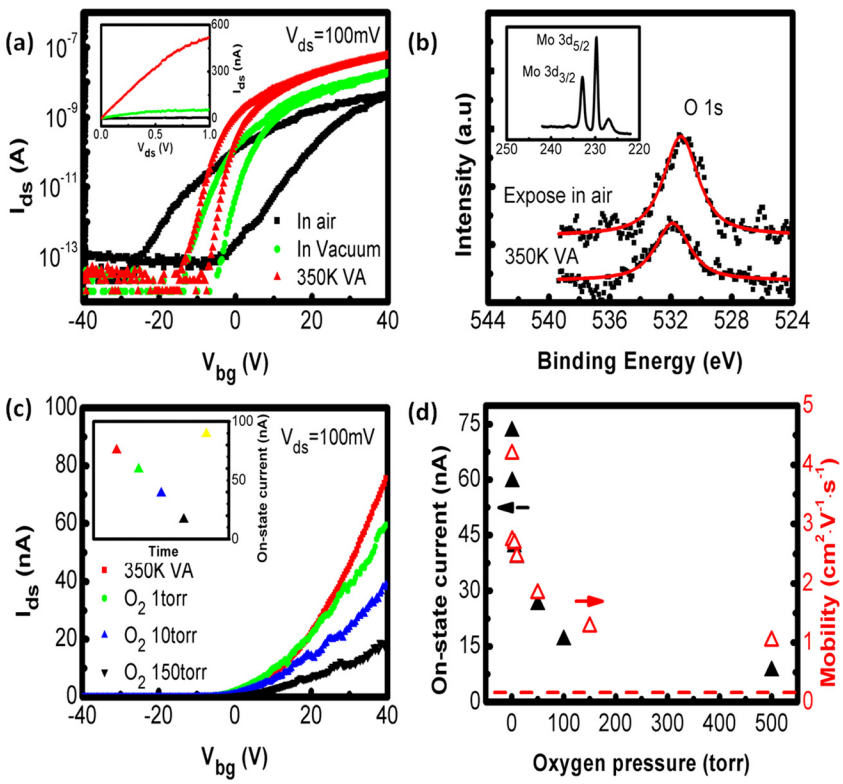

FIG. 2. (Color online) (a) Double sweep I_{ds}-V_{bg} characteristics of the bi-layer MoS_2 FET in Fig. 1, probed in air (square), in vacuum (circle), and after 350 K vacuum annealing for 24 h (350 K VA) (triangle). $V_{ds} = 100$ mV for all cases. (Inset) I_{ds}-V_{ds} characteristics for the three cases at $V_{bg} = 40$ V. (b) The XPS of MoS_2 in the O 1 s region after exposure in air and after 350 K vacuum annealing for 24 h (symbols). The solid lines are Lorentzian fittings with peak values at 531.7 eV and 532.2 eV, respectively. Inset shows typical Mo 3 d doublet in MoS_2. There is no obvious difference in Mo 3 d peaks for the two samples. (c) I_{ds}-V_{bg} characteristics of the bi-layer MoS_2 FET under O_2 pressure of 1 Torr (circle), 10 Torr (triangles pointing up), and 150 Torr (triangles pointing down) and after 350 K vacuum annealing (square). $V_{ds} = 100$ mV for all cases. (Inset) From left to right, on-state current at $V_{ds} = 100$ mV and $V_{bg} = 40$ V after vacuum annealing, under O_2 pressure of 1 Torr, 10 Torr, 150 Torr and after vacuum annealing following exposure in O_2, showing that the conductance can be recovered after exposure to oxygen. (d) On-state current (solid triangle, left axis) at $V_{ds} = 100$ mV and $V_{bg} = 40$ V and extrinsic field-effect mobility (open triangle, right axis) versus O_2 pressure for the bi-layer MoS_2 FET. The red dashed line shows extrinsic mobility of the same device in air.

10^7, and an extrinsic $\mu \sim 2.4\,cm^2/Vs$ (lower limit considering parasitics). These values are comparable to back-gated monolayer MoS_2 devices in Ref. 6 (~100 nS, 0.2 cm^2/Vs). Thick MoS_2 flakes showed a much higher conductivity (4900 nS) due to more conducting layers,[16] however, the conductivity per layer was much lower than our devices.

At room temperature, our devices exhibited Ohmic contacts as indicated by the linear I_{ds}-V_{ds} near at low bias (Fig. 1(d)). Furthermore, current saturation was observed beyond $V_{ds} \sim 0.6\,V$ in MoS_2 devices. In carbon nanotubes and graphene, current saturation can be ascribed to optical phonons or interfacial phonons of SiO_2 substrates.[17,18] However, due to different band structure and density of states, other mechanisms may be involved. Future theoretical and experimental works are needed to fully understand the origin of current saturation in MoS_2. We carried out variable temperature measurements to further investigate the carrier transport in bi-layer MoS_2 FETs. Compared to commonly used Au contacts, Ti has lower work function and, therefore, lower Schottky barrier for electrons. At low temperatures, however, we observed an exponential decrease in conductance and non-linearity in the I_{ds}-V_{ds} characteristics (Figs. 3(a) and 3(b)), which suggested finite Schottky barrier. The Arrhenius plot of current at strong electron accumulation region ($V_{bg} = 40\,V$) clearly showed the contributions from thermionic emission ($\sim \exp\left(-\frac{\phi_{SB}}{k_B T}\right)$, where ϕ_{SB} was the Schottky barrier height) and tunneling, separated by $T \sim 100\,K$ (Fig. 3(c)). From the Arrhenius plot, the effective barrier height was derived and zero-field barrier was extrapolated to be ~65 meV for electrons (Fig. 3(d)). The barrier is smaller than expected, considering that bi-layer MoS_2 has smaller electron affinity than that of bulk MoS_2 crystal (~4 eV)[19] and that the work function of Ti is 4.33 eV. At $V_{bg} = 40\,V$, the electrostatic field of the gate caused band bending at the contact, which might result in a lower effective barrier height.[20] Another possibility was that the Schottky barrier height could be pinned by charge neutrality requirement for filling the interface states. Further reduction of Schottky barrier height is possible by using lower work function metals such as Al.

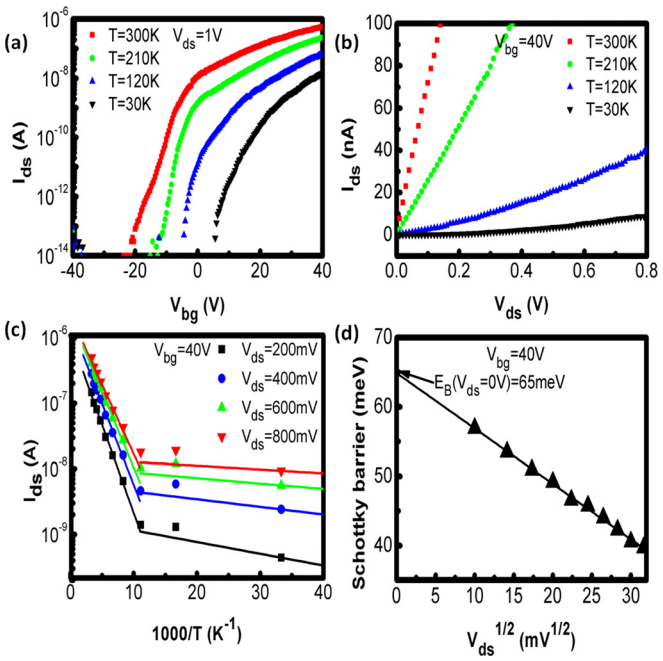

FIG. 3. (Color online) (a) From bottom to top, I_{ds}-V_{bg} characteristics of the bi-layer MoS_2 device taken at $V_{ds} = 1\,V$ at 30 K, 120 K, 210 K, and 300 K. (b) From bottom to top, I_{ds}-V_{ds} curves taken at $V_{bg} = 40\,V$ at 30 K, 120 K, 210 K, and 300 K. The low bias region becomes non-linear at low temperatures, indicating a positive Schottky barrier. (c) A set of Arrhenius plots for electron transport at $V_{bg} = 40\,V$ under different V_{ds}. The solid lines at high temperatures are exponential fittings to extract the Schottky barrier. (d) Plot of the Schottky barrier height for electron as the function of the square root of V_{ds}. The barrier height in the absence of the field is extrapolated to be 65 meV.

In summary, we have demonstrated the back-gated bi-layer MoS_2 FETs with high on/off ratio, Ohmic contacts, and current saturation. A small Schottky barrier still exists at the Ti contacts. In addition, we show that chemisorption of oxygen and water from the ambient causes degradation of device conductance by up to ~100 times, but could be reversibly recovered by a simple vacuum annealing process. The vacuum annealing can also significantly reduce the commonly observed variations in MoS_2 device performances.

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