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LETTERS

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Single-layer MoS_2 transistors

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Two-dimensional materials are attractive for use in next-generation nanoelectronic devices because, compared to one-dimensional materials, it is relatively easy to fabricate complex structures from them. The most widely studied two-dimensional material is graphene[1,2], both because of its rich physics[3–5] and its high mobility[6]. However, pristine graphene does not have a bandgap, a property that is essential for many applications, including transistors[7]. Engineering a graphene bandgap increases fabrication complexity and either reduces mobilities to the level of strained silicon films[8–13] or requires high voltages[14,15]. Although single layers of MoS_2 have a large intrinsic bandgap of 1.8 eV (ref. 16), previously reported mobilities in the 0.5–3 $cm^2 V^{-1} s^{-1}$ range[17] are too low for practical devices. Here, we use a halfnium oxide gate dielectric to demonstrate a room-temperature single-layer MoS_2 mobility of at least 200 $cm^2 V^{-1} s^{-1}$, similar to that of graphene nanoribbons, and demonstrate transistors with room-temperature current on/off ratios of 1×10^8 and ultralow standby power dissipation. Because monolayer MoS_2 has a direct bandgap[16,18], it can be used to construct interband tunnel FETs[19], which offer lower power consumption than classical transistors. Monolayer MoS_2 could also complement graphene in applications that require thin transparent semiconductors, such as optoelectronics and energy harvesting.

MoS_2 is a typical example from the layered transition-metal dichalcogenide family of materials. Crystals of MoS_2 are composed of vertically stacked, weakly interacting layers held together by van der Waals interactions (Fig. 1a). Single layers, 6.5 Å thick (Fig. 1b,c), can be extracted using scotch tape[17,20] or lithium-based intercalation[21,22]. Large-area thin films can also be prepared using MoS_2 suspensions. Bulk MoS_2 is semiconducting with an indirect bandgap of 1.2 eV (ref. 23), whereas single-layer MoS_2 is a direct gap semiconductor[16,18] with a bandgap of 1.8 eV (ref. 16). MoS_2 nanotubes[24] and nanowires[25] also show the influence of quantum-mechanical confinement in their electronic and optical properties. Other features that could make MoS_2 interesting for nanoelectronic applications include the absence of dangling bonds and thermal stability up to 1,100 °C.

Single-layer MoS_2 could also be interesting as a semiconducting analogue of graphene, which does not have a bandgap in its pristine form. Bandgaps up to 400 meV have been introduced by quantum-mechanical confinement in patterned[8] or exfoliated graphene nanoribbons[9], but always at the price of significant mobility reduction (200 $cm^2 V^{-1} s^{-1}$ for a 150 meV bandgap)[9,10], loss of coherence[11] or increased off-state currents due to edge roughness[12]. Bandgaps have also been induced by applying a perpendicular electric field in bilayer graphene[14,15], but the highest reported optical gap is 250 meV, requiring the application of a voltage exceeding 100 V (ref. 14). This makes it very difficult to build logic circuits based on graphene that would operate at room temperature with low standby power dissipation. In fact, for any potential replacement of silicon in CMOS-like digital logic devices, a current on/off ratio[7] I_{on}/I_{off} between 1×10^4 and 1×10^7 and a bandgap exceeding 400 meV (ref. 26) are desirable.

The starting point for the fabrication of our transistors was scotch tape-based micromechanical exfoliation[1,17] of single-layer MoS_2. MoS_2 monolayers were transferred to degenerately doped silicon substrates covered with 270-nm-thick SiO_2 (Fig. 2a). We have previously found that this oxide thickness is optimal for optical detection of single-layer MoS_2, and have established the correlation between contrast and thickness as measured by atomic force microscopy (AFM)[27]. Electrical contacts were fabricated using electron-beam lithography followed by deposition of 50-nm-thick gold electrodes. The device was then annealed at 200 °C to remove resist residue[28] and decrease contact resistance (for more details see Supplementary Information). At this point our single-layer devices show a typical mobility in the range 0.1–10 $cm^2 V^{-1} s^{-1}$, similar to previously reported values for single layers[17] and thin crystals containing more than 10 layers of MoS_2 (ref. 29). This is lower than the previously reported phonon-scattering-limited room-temperature mobility in the 200–500 $cm^2 V^{-1} s^{-1}$ range for bulk MoS_2 (ref. 30). Encouraged by recent theoretical predictions of mobility improvement by dielectric screening[31] and its successful application to graphene[32], we proceeded with atomic layer deposition (ALD) of 30 nm HfO_2 as a high-κ gate dielectric for the local top gate and mobility booster to realize the full potential of the single-layer MoS_2. We chose HfO_2 because of its high dielectric constant of 25, bandgap of 5.7 eV and the fact that it is commonly used as a gate dielectric both by the research community and major microprocessor manufacturers[33,34]. The resulting structure, composed of two field-effect transistors connected in series, is shown in Fig. 2b. A schematic depiction of the device is shown in Fig. 2c. The width of the top gate of our device was 4 μm and the top gate length, source–gate and gate–drain spacing were 500 nm.

We performed electrical characterization of our device at room temperature using a semiconductor parameter analyser and shielded probe station with voltage sources connected in the configuration depicted in Fig. 3a. We first characterized our MoS_2 transistors with 6.5-Å-thick conductive channels by applying a drain–source bias V_{ds} to a pair of gold electrodes and gate voltage V_{bg} to the degenerately doped silicon substrate while leaving the top gate electrically floating[35]. The gating characteristics of the left-most transistor shown in Fig 2b are presented in Fig. 3b; these are typical of FET devices with an n-type channel. We concentrate on this device in the remainder of this Letter. Characterization details for other devices and fabrication batches are available in the Supplementary Information. All the MoS_2 transistors we fabricated, regardless of the number of layers or contacting material, show behaviour typical of FET devices with n-type channels. Repeated V_{bg} sweeps on the same device do not show significant variation, while keeping all the voltages constant results in constant I_{ds}, indicating that the top gate is not likely to accumulate charge during measurements. We estimate that a constant surface charge of $n \approx 4.6 \times 10^{12}$ cm^{-2} trapped on the top gate would shift the threshold voltage by ~1 V but not change the

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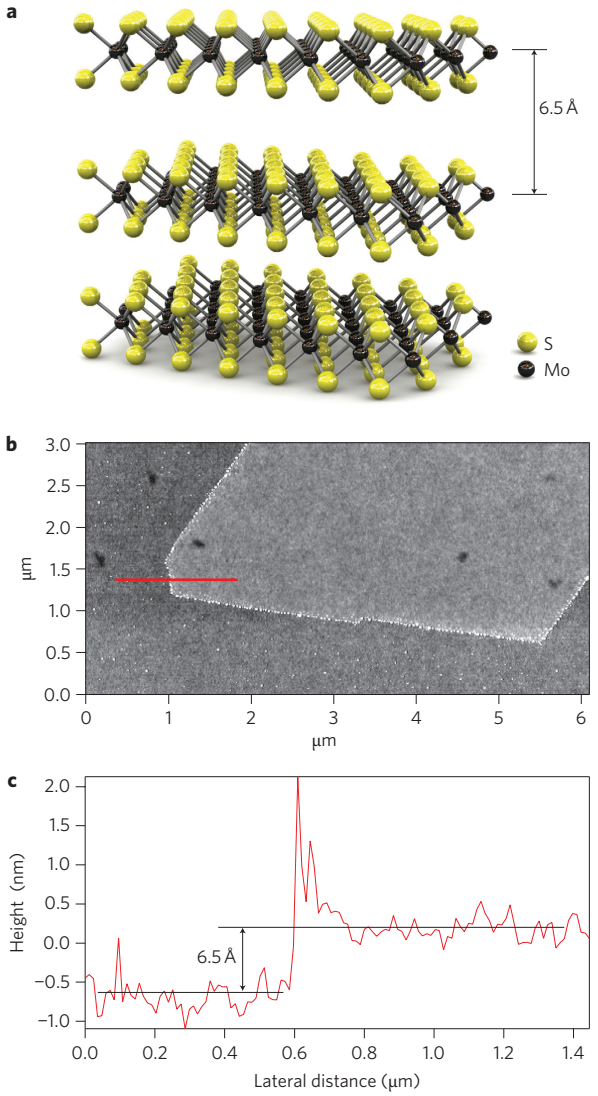

Figure 1 | Structure and AFM imaging of monolayer MoS_2. **a**, Three-dimensional representation of the structure of MoS_2. Single layers, 6.5 Å thick, can be extracted using scotch tape-based micromechanical cleavage. **b**, Atomic force microscope image of a single layer of MoS_2 deposited on a silicon substrate with a 270-nm-thick oxide layer. **c**, Cross-sectional plot along the red line in **b**.

slope of the $I_{ds} - V_{bg}$ curve in Fig. 3b used for estimating channel mobility. The source current versus source bias characteristics (Fig 3b, inset) is linear in the $\pm$50 mV range of voltages, indicating that our gold contacts are ohmic.

The on-resistance of our transistor was 27 kΩ for $V_{ds} = 10$ mV and $V_{bg} = 10$ V, with a gate width of 4 μm and bottom gate length of 1.5 μm. We have noticed that the device resistance can increase during storage at ambient conditions for a period of two months. This could be attributed to absorption of oxygen and/or water from the environment and could be mitigated by device encapsulation.

From the data presented in Fig. 3b we can extract the low-field field-effect mobility of $\sim 217\ cm^2\ V^{-1}\ s^{-1}$ using the expression $\mu = [dI_{ds}/dV_{bg}] \times [L/(WC_iV_{ds})]$, where $L = 1.5$ μm is the channel length, $W = 4$ μm is the channel width and $C_i = 1.3 \times 10^{-4}\ F\ m^{-2}$ is the capacitance between the channel and the back gate per unit area ($C_i = \varepsilon_0\varepsilon_r/d$; $\varepsilon_r = 3.9$; $d = 270$ nm). Note that this value represents the lower limit because of contact resistance. As our device displays ohmic I_{ds}–V_{ds} behaviour (Fig. 3b, inset), we exclude the possibility that our field-effect behaviour is dominated by Schottky barriers at the contacts.

Although the room-temperature value of phonon-scattering limited[30] mobility for bulk MoS_2 is in the 200–500 $cm^2\ V^{-1}\ s^{-1}$ range, exfoliation of single layers onto SiO_2 results in a decrease of mobility to 0.1–10 $cm^2\ V^{-1}\ s^{-1}$. The improvement in mobility with the deposition of a high-κ dielectric could be due to suppression of Coulomb scattering due to the high-κ dielectric environment[31] and modification of phonon dispersion[36] in MoS_2 monolayers. Extensive future theoretical work including the calculation of phonon dispersion relations in single-layer MoS_2, calculation of scattering rates on phonons and charge impurities would be needed to provide a complete picture.

Before we compare the value of mobility in our case with the mobility of graphene or thin-film silicon we should note that semiconductors such as carbon nanotubes or graphene nanoribbons mostly follow the general trend of decreasing mobility with increasing bandgap[26]. Even though graphene has a high room-temperature mobility of 120,000 $cm^2\ V^{-1}\ s^{-1}$, this value relates to large-area, gapless graphene[6]. On the other hand, measurements on 10-nm-wide graphene nanoribbons with $E_g \approx 400$ mV indicate mobilities lower than 200 $cm^2\ V^{-1}\ s^{-1}$ (ref. 9), in good agreement with theoretical models that predict decreased mobility in small-width graphene nanoribbons due to electron–phonon scattering[13]. This is comparable to the mobility of 250 $cm^2\ V^{-1}\ s^{-1}$ found in 2 nm thin strained silicon films[37]. Our MoS_2 monolayer has similar mobility but a higher bandgap than graphene nanoribbons[9], and a smaller thickness than the thinnest silicon films fabricated to date[37].

One of the crucial requirements for building integrated circuits based on single layers of MoS_2 is the ability to control charge density in a local manner, independently of a global back gate. We can do this by applying a voltage V_{tg} to the top gate, separated from the monolayer MoS_2 by 30 nm of HfO_2 (Fig. 3a), while keeping the substrate grounded. The corresponding transfer characteristic is shown in Fig. 4a. For a bias of 10 mV we observe an

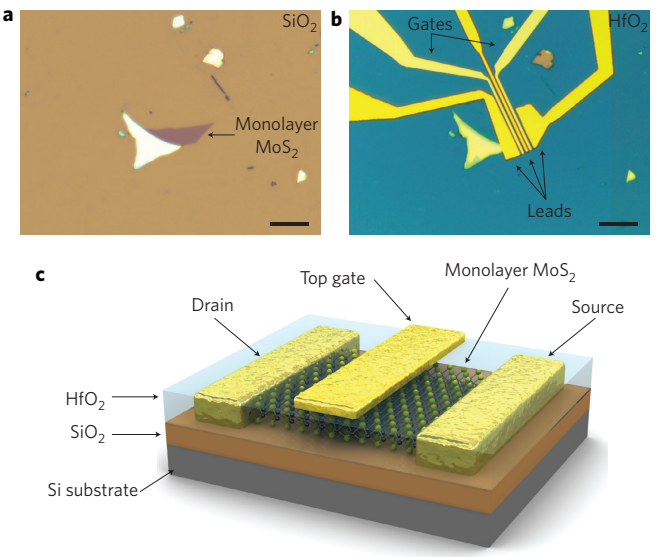

Figure 2 | Fabrication of MoS_2 monolayer transistors. **a**, Optical image of a single layer of MoS_2 (thickness, 6.5 Å) deposited on top of a silicon substrate with a 270-nm-thick SiO_2 layer. **b**, Optical image of a device based on the flake shown in **a**. The device consists of two field-effect transistors connected in series and defined by three gold leads that serve as source and drain electrodes for the two transistors. Monolayer MoS_2 is covered by 30 nm of ALD-deposited HfO_2 that acts both as a gate dielectric and a mobility booster. Scale bars (**a**,**b**), 10 μm. **c**, Three-dimensional schematic view of one of the transistors shown in **b**.

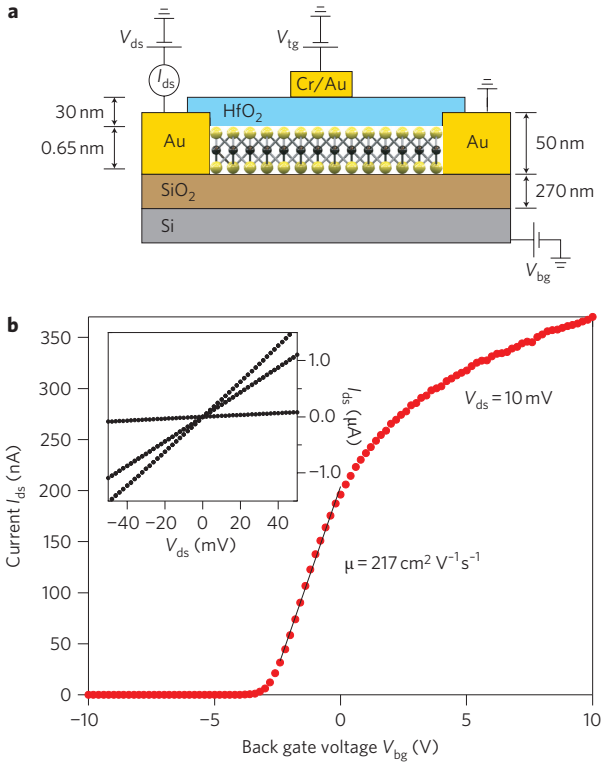

Figure 3 | Characterization of MoS_2 monolayer transistors. a, Cross-sectional view of the structure of a monolayer MoS_2 FET together with electrical connections used to characterize the device. A single layer of MoS_2 (thickness, 6.5 Å) is deposited on a degenerately doped silicon substrate with 270-nm-thick SiO_2. The substrate acts a back gate. One of the gold electrodes acts as drain and the other source electrode is grounded. The monolayer is separated from the top gate by 30 nm of ALD-grown HfO_2. The top gate width for the device is 4 μm and the top gate length, source–gate and gate–drain spacing are each 500 nm. **b**, Room-temperature transfer characteristic for the FET with 10 mV applied bias voltage V_{ds}. Back-gate voltage V_{bg} is applied to the substrate and the top gate is disconnected. Inset: I_{ds}–V_{ds} curve acquired for V_{bg} values of 0, 1 and 5 V.

on-current of 150 nA (37 nA μm^{-1}), current on/off ratio $I_{on}/I_{off} > 1 \times 10^6$ for the ±4 V range of V_{tg}, an off-state current that is smaller than 100 fA (25 fA μm^{-1}) and gate leakage lower than 2 pA μm^{-2}. The observed current variation for different values of V_{tg} indicates that the field-effect behaviour of our transistor is dominated by the MoS_2 channel and not the contacts.

At the bias voltage $V_{ds} = 500$ mV, the maximal measured on-current is 10 μA (2.5 μA μm^{-1}), with I_{on}/I_{off} higher than 1×10^8 for the ±4 V range of V_{tg}. The device transconductance, defined as $g_m = dI_{ds}/dV_{tg}$ at $V_{ds} = 500$ mV is ~4 μS (1 μS μm^{-1}), similar to values obtained for high-performance CdS nanoribbon array transistors (2.5 μS μm^{-1} at $V_{ds} = 1$ V)[38]. High-performance top-gated graphene transistors can have normalized transconductance values as high as 1.27 mS μm^{-1} (ref. 39). The large degree of current control in our device is also clearly illustrated in Fig. 4b, where we plot the drain–source current versus drain–source bias for different values of voltage applied to the local gate. From the channel current dependence on top-gate voltage, we deduce a subthreshold slope for the transition between the on and off states of 74 mV dec^{-1} for a bias $V_{ds} = 500$ mV. Being a direct gap semiconductor, single layers of MoS_2 offer the intriguing possibility for the realization of an interband tunnel FET, which is characterized by a turn-on sharper than the theoretical limit of 60 mV dec^{-1} for classical transistors and consequently smaller power dissipation. This feat has remained difficult in the case of silicon, an indirect gap semiconductor, because interband transitions there require phonons and recombination centres.

To summarize, we have realized a field-effect transistor with a single, two-dimensional layer of the semiconductor MoS_2 as a conductive channel and HfO_2 as a gate insulator. The conductive channel in our device is only 6.5 Å thick. Our transistor exhibits a room-temperature current on/off ratio exceeding 1×10^8 and mobility of ~200 cm^2 V^{-1} s^{-1}, comparable to the mobility achieved in thin silicon films[37] or graphene nanoribbons[9]. Such a transistor could form the backbone of future electronics based on layered materials in which MoS_2 transistors could be fabricated on insulating boron nitride substrates[40]. Our results provide an important step towards the realization of electronics and low-standby-power integrated circuits based on two-dimensional materials. Being a thin, transparent semiconducting material, MoS_2 monolayers also present a wealth of new opportunities in areas that include mesoscopic physics, optoelectronics and energy harvesting. With the possibility of fabricating large-area circuits using solution-based

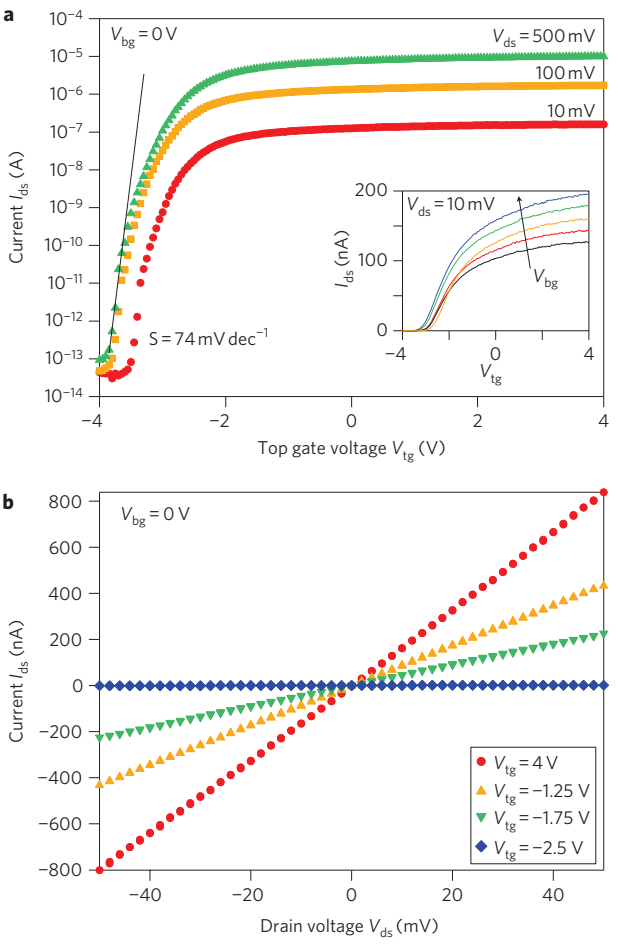

Figure 4 | Local gate control of the MoS_2 monolayer transistor. a, I_{ds}–V_{tg} curve recorded for a bias voltage ranging from 10 mV to 500 mV. Measurements are performed at room temperature with the back gate grounded. Top gate width, 4 μm; top gate length, 500 nm. The device can be completely turned off by changing the top gate bias from −2 to −4 V. For $V_{ds} = 10$ mV, the I_{on}/I_{off} ratio is $>1 \times 10^6$. For $V_{ds} = 500$ mV, the I_{on}/I_{off} ratio is $>1 \times 10^8$ in the measured range while the subthreshold swing $S =$ 74 mV dec^{-1}. Top and bottom gate leakage is negligible (Supplementary Fig. S3). Inset: I_{ds}–V_{tg} for values of $V_{bg} = -10$, −5, 0, 5 and 10 V. **b**, I_{ds}–V_{ds} curves recorded for different values of V_{tg}. The linear dependence of the current on bias voltage for small voltages indicates that the gold contacts are ohmic.

processing, our finding could be important for producing electronic devices that could combine the ease of processing associated with organic conductors with performance figures commonly associated with silicon-based electronics.

Methods

Single layers of MoS_2 were exfoliated from commercially available crystals of molybdenite (SPI Supplies Brand Moly Disulfide) using the scotch-tape micromechanical cleavage technique method pioneered for the production of graphene[1]. AFM imaging was performed using the Asylum Research Cypher AFM. After gold contact deposition, devices were annealed in 100 s.c.c.m. of argon and 10 s.c.c.m. H_2 flow at 200 °C for 2 h (ref. 28). ALD was performed in a home-built reactor using a reaction of H_2O with tetrakis(dimethylamido)hafnium (Sigma Aldrich). Electrical characterization was carried out using an Agilent E5270B parameter analyser and a home-built shielded probe station with micromanipulated probes.

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Author contributions

B.R., J.B., V.G. and A.K. worked on device fabrication and contact optimization. A.R. built the system for atomic layer deposition of HfO_2. B.R. and A.K. performed measurements and analysed the data presented in the paper and Supplementary Information. A.K. initiated the research and wrote the manuscript. All the authors read and commented on the manuscript.

Additional information

The authors declare no competing financial interests. Supplementary information accompanies this paper at www.nature.com/naturenanotechnology. Reprints and permission information is available online at http://npg.nature.com/reprintsandpermissions/. Correspondence and requests for materials should be addressed to A.K.

ERRATUM

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In the version of this Letter originally published online, the label 'V_{tg}' was missing from Fig. 3a and the expression '$\mu = 217\ cm^{-2}\ V_s$' should have read '$\mu = 217\ cm^2\ V^{-1}\ s^{-1}$' in Fig. 3b. These errors have now been corrected in all versions of the Letter.