Back-Gate Forward Bias Method for Low-Voltage CMOS Digital Circuits

Ming-Jer Chen, *Member, IEEE,* Jih-Shin Ho, Tzuen-Hsi Huang, *Member, IEEE,* Chuang-Hen Yang, Yeh-Ning Jou, and Terry Wu

Abstract— **The back-gate forward bias method suitable for present standard bulk CMOS processes has been promoted for low-voltage digital circuit application. A CMOS inverter employing the method has experimentally exhibited the ability of electrically adjusting the transition region of the dc voltage transfer characteristics. Transient measurement has further shown that the inverter with a back-gate forward bias of 0.4 V can operate at low supply voltages down to 0.6 V without significant loss in switching speed. Guidelines for ensuring proper implementation of the method in a bulk CMOS process has been set up against latch-up, parasitic bipolar, impact ionization, and stand-by current. Following these guidelines, a cost-effective low-power, low-voltage, high-density mixed-mode CMOS analog/digital integrated circuits chip with both reasonable speed and improved precision has been projected for the first time.**

I. Introduction

In CMOS digital circuits the power dissipated in the dynamic active mode is proportional to the square of power supply voltage and thus lowering the supply voltage can help achieve the objective of low power consumption for the battery-operated portable applications. Simultaneously, the threshold voltage of MOSFET's must be reduced in order to maintain the operating speed as high as possible. However, a reduction in threshold voltage can increase exponentially the stand-by subthreshold current. This problem can be overcome in the circuit level by using high threshold voltage MOSFET's from multi-threshold CMOS process [1] or inserting the switched impedance into the source [2], [3]. Very recently, a novel back-gate reverse or forward bias scheme [4]–[6] has been introduced as an efficient trade-off between switching speed and subthreshold power. In [4], a near-zero threshold voltage was obtained by modifying the threshold implant mask, which was then electrically increased by reverse biasing the back gate to the level suitable for operation in the active mode, and optionally in the stand-by mode can further be increased to another higher level such as to maintain a very low subthreshold current. In [5] and [6], the back-gate forward bias method was achieved by tying together the gate and body of MOSFET's, creating a three-terminal gated lateral bipolar transistor and thus constituting the so called dynamic threshold voltage characteristics; however, only SOI (Silicon-On-Insulator) or oxide isolation process is possible to realize since a common p- or n-type substrate is inhibited in this scheme. On the other hand, the back-gate forward bias method in terms of a four-terminal gated lateral bipolar transistor in a MOSFET structure as cited in [7] and [8] possesses two competitive abilities as compared with [4]–[6]: it is fully compatible with present low-cost, high-yield standard bulk CMOS processes; and the threshold voltage in the active mode can be electrically reduced, without any mask or process modification.

In this paper we promote the back-gate forward bias method suitable for present standard bulk CMOS processes to the circuit level for low-voltage digital application. Transient switching waveforms and dc transfer characteristics measured from a CMOS inverter employing the method at reduced supply voltages will be given. Guidelines for ensuring proper implementation of the method in a bulk CMOS process will be set up. A new low-voltage, low-power, high-density mixed-mode CMOS analog/digital integrated circuits chip will further be projected to highlight the potential of the method.

II. Method and Results

The method of forward biasing the back gate or bulk with respect to the source in the dynamic active mode is schematically shown in Fig. 1 for a bulk CMOS inverter. The CMOS inverter was fabricated by one of existing standard bulk CMOS processes. The gate width to length ratio W/L of p- and n-MOSFET's were 20 μm/0.8 μm and 20 μm/0.9 μm, respectively. The gate oxide thickness was about 163 Å. The corresponding drain current versus gate voltage characteristics measured with the back-gate forward bias as parameter are plotted in Fig. 2. From Fig. 2 we can observe that at high gate voltages a small back-gate forward bias produces a small increase in the drain current while this current increase is magnified with reducing the gate voltage. Here we define the threshold voltage V_{th} as the gate voltage delivering a fixed drain current of 1×10^{-5} A. The threshold voltage extracted from Fig. 2 as function of the back-gate forward bias for n- and p-MOSFET's is plotted in Fig. 3. From Fig. 3, it can be clearly seen that for each MOSFET an increase in the back-gate forward bias from 0 V to 0.4 V can lower the threshold voltage magnitude from 0.52 V down to 0.31 V for n-MOSFET and from 0.55 V down to 0.40 V for p-MOSFET. The measured dependencies on the back-gate forward bias in

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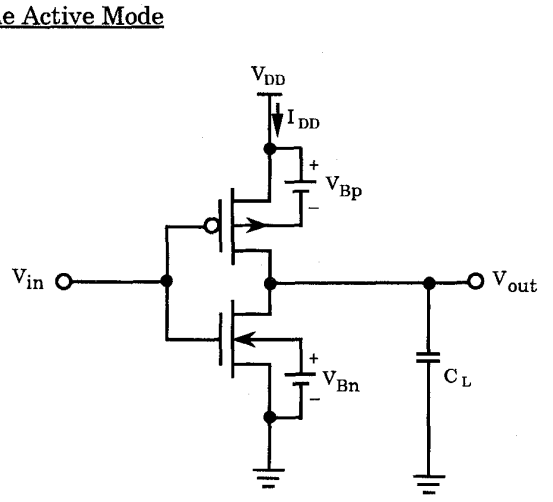

Fig. 1. The back-gate forward bias method employed for a bulk CMOS inverter.

Fig. 3 can be reasonably reproduced by [7], [8]

$$V_{th} = a_1 + a_2\sqrt{a_3 - V_{BS}} \tag{1}$$

where $V_{BS} = V_{Bn}$ or V_{Bp}; $V_{th} = V_{thn}$ and $|V_{thp}|$ for n- and p-MOSFET's, respectively; and a_1, a_2, and a_3 are three process-dependent parameters to be fitted. The fitting parameter values of $a_1 = 0.027$ V, $a_2 = 0.635$ $V^{1/2}$, and $a_3 = 0.603$ V for n-MOSFET as well as $a_1 = 0.220$ V, $a_2 = 0.446$ $V^{1/2}$, and $a_3 = 0.558$ V for p-MOSFET both lead to good agreement as demonstrated in Fig. 3.

A. DC Voltage Transfer Characteristics

The measured dc inverter characteristics for two different power supply voltages in terms of both the output voltage versus input voltage curves and the power supply current versus input voltage curves are plotted in Fig. 4 each with different combinations of back-gate forward biases. Intuitively, a decrease in the V_{thn} causes a decrease in the critical input voltage needed to turn on the n-MOSFET and pull down the output to the ground. On the other hand, a decrease in the magnitude of V_{thp} produces an increase in the critical input voltage needed to turn on the p-MOSFET and pull up the output to the supply voltage V_{DD}. This tendency agrees with Fig. 4(a): applying the back-gate forward bias V_{Bp} in p-MOSFET shifts the transition region along the input voltage axis toward the high voltage level while the back-gate forward bias V_{Bn} in n-MOSFET pushes the transition region to the low voltage level. Traditionally, the transition region adjustment to the midway between high and low levels was performed primarily through the channel width ratio. Thus, the back-gate forward bias method can provide an efficient alternative to adjust the transition region to around the midway between high and low levels. Further observation of the measured direct current characteristics in Fig. 4(b) reveals that: 1) the peak current occurring at the transition region decreases with decreasing the power supply voltage; and 2) application of a back-gate forward bias can raise significantly the current. Note

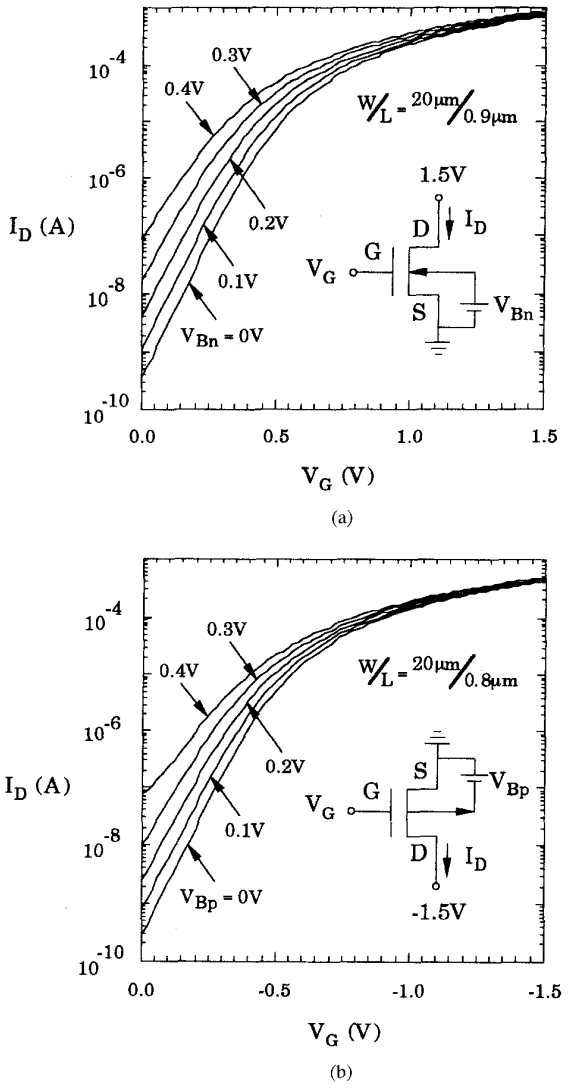

Fig. 2. The measured drain current versus gate voltage characteristics with the back-gate forward bias as parameter for both MOSFET's in a CMOS inverter.

that the direct current power dissipation in the active mode is usually negligible as compared with the dynamic one.

B. Transient Switching

Transient experiment was performed by means of the pulse generator HP 8110A and the storage digitizing oscilloscope Tektronix 11402A. The measurement conditions were: the input voltage waveform with high-level $V_H = V_{DD}$ and low-level $V_L = 0$ V as well as with the rise and fall times both fixed at 15 ns; and the power supply voltage V_{DD} ranging from 1.5 V down to 0.6 V. The reason for the minimum V_{DD} value of 0.6 V in our work is that for gate voltage less than this value, the amount of the drain current, as seen in Fig. 2, is comparable with the leakage current ($\approx 10^{-7}$ A) through the oscilloscope probe in the transient experiment. Fig. 5 demonstrates the measured voltage waveforms at the input and output with and without the back-gate forward bias

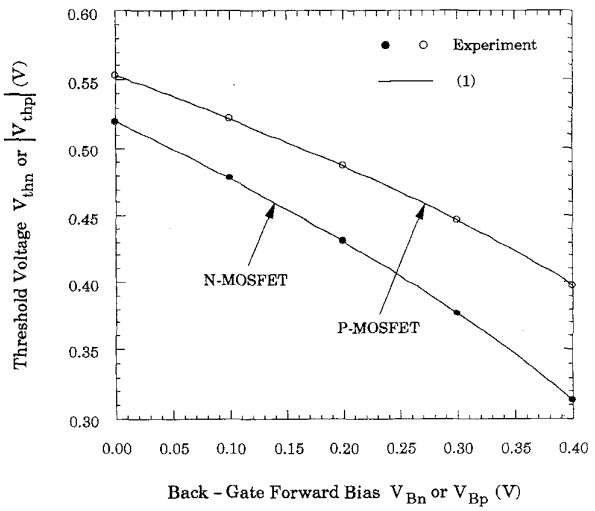

Fig. 3. The measured and calculated threshold voltage versus the back-gate forward bias for both MOSFET's.

method for three different power supply voltages of 0.6, 0.8, and 1.0 V. From Fig. 5 we can observe that not only the fall time in the output pull-down waveform but also the rise time in the output pull-up waveform are decreased with the method applied. Evaluation of improvement in the switching speed due to back-gate forward bias can further be obtained by plotting the measured delay time t_d versus the power supply voltage V_{DD} in Fig. 6. From Fig. 6 it can be seen that: 1) from $V_{DD} = 1.5$ V to about 1.0 V the change in the delay time is gradually slow while further reduction of V_{DD} can dramatically increase the delay time; and 2) the delay time can be substantially decreased by the back-gate forward bias especially at low power supply voltages, i.e., the delay time is reduced by a large factor of about 3.0 at $V_{DD} = 0.6$ V. Also plotted in Fig. 6 are the calculated results by a simple delay time formula [9]

$$t_d = \frac{C_L}{4} V_{DD} \left(\frac{1}{I_{dn}} + \frac{1}{I_{dp}} \right) \tag{2}$$

where C_L is the output capacitance; and I_{dn} and I_{dp} are the drain saturation currents of n- and p-MOSFET's, respectively. With the measured I-V characteristics of both MOSFET's in Fig. 2 as input parameters for the currents I_{dn} and I_{dp} in (2), the equivalent value of the output capacitance C_L in the measurement has been extracted to be 62 pF by fitting the eight data points in Fig. 6. The calculated delay times versus the power supply voltage are plotted in Fig. 6. From Fig. 6 we can observe that excellent agreements with the measured ones with and without the back-gate forward bias method are simultaneously achieved. Further calculation has been performed using (2) with the same I-V characteristics in Fig. 2 for a small $C_L = 100$ fF typically encountered in the internal circuitry, as plotted in Fig. 7. From Fig. 7 we can clearly observe that: 1) without the proposed method the delay time dramatically changes over the low power supply voltage range between 0.5 V and 1.0 V; and 2) a relatively slow change in the delay time less than 800 ps is obtained with back-gate

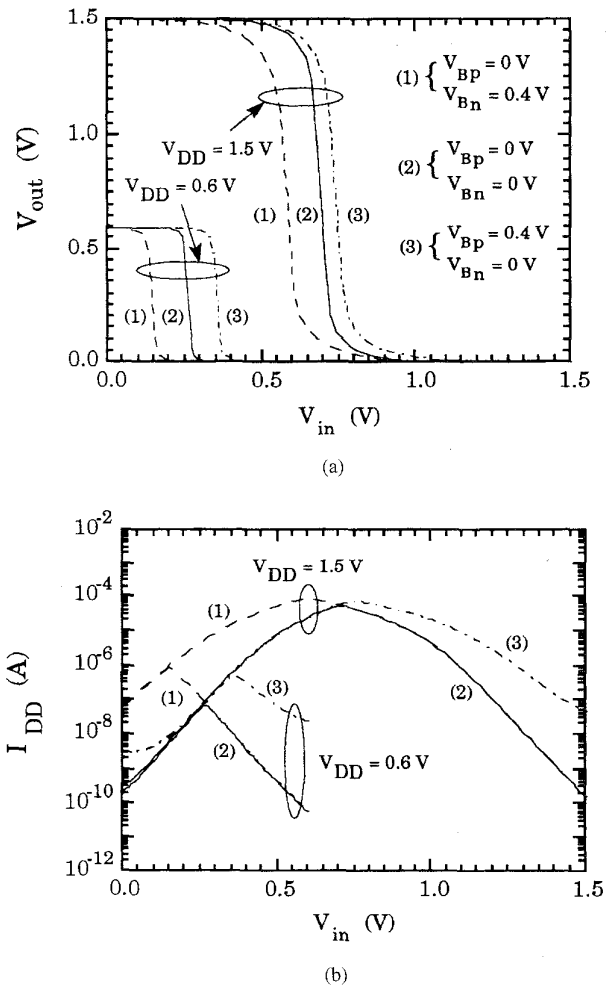

Fig. 4. (a) The measured voltage transfer characteristics for two different power supply voltages each with three different combinations of back-gate forward biases in a CMOS inverter; and (b) the corresponding measured power supply current versus the input voltage.

forward bias. Note that the supply voltage range in Fig. 7 is free from latch-up and impact ionization as explained later.

III. The Guidelines

Since the implementation of the method requires the bulk or substrate forward biased, guidelines must be carefully established in order to avoid malfunction or permanent damage caused by parasitic bipolar, impact ionization, latch-up, and stand-by current. This is achieved by constraining quantitatively the range of the supply voltage and forward bias as demonstrated below.

First, the range of $0 \leq V_{Bp} \leq 0.4$ V and $0 \leq V_{Bn} \leq 0.4$ V can guarantee the action of the gated lateral bipolar transistors in low-level injection; that is, the parasitic bipolar far away from the surface is essentially inactive. We have measured a considerable amount of the current disturbing the nearby circuitry only for $V_{Bp} > 0.5$ V or $V_{Bn} > 0.5$ V. Further, the power supply voltage V_{DD} is limited to below about 2 V for elimination of impact ionization at the drain. This can make the hot carrier effect due to impact ionization less of

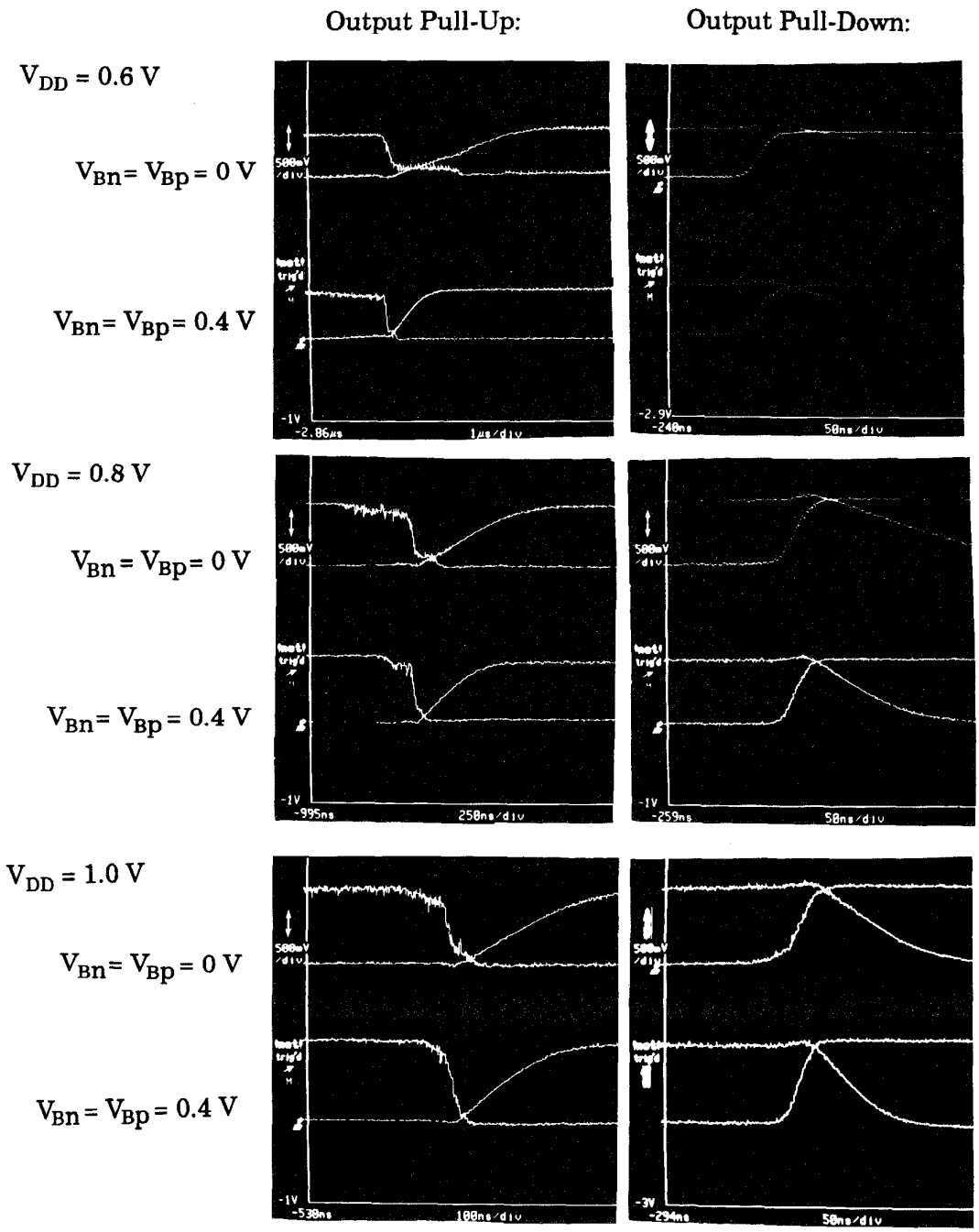

Fig. 5. The measured input and output voltage waveforms in a CMOS inverter for three different power supply voltages each with and without the back-gate forward bias.

the problem. Under this situation, the base current reversal [10], as an indicator of impact ionization, disappears. The latch-up test experiment has been performed on the long-stripe standard latch-up structure with the back-gate forward bias as parameter. Fig. 8 depicts the measured latch-up I-V characteristics for an n-p spacing of 6 μm with $V_{Bn} = V_{Bp} =$ 0.2 V and $V_{Bn} = V_{Bp} = 0.4$ V. From Fig. 8, we can observe that the holding voltage for sustaining the latch-up is about 1 V and thus a maximum supply voltage of 1 V can guarantee latch-up free operation. Therefore to ensure proper utilization of the back-gate forward bias method, in this work the supply voltage is limited to less than 1 V, which in turn automatically eliminates the impact ionization.

To overcome the increased subthreshold current due to the method, the source impedance switch as described in detail in [1]–[3] is suggested as a design guideline in the circuit level. By combining the back-gate forward bias method and the source impedance switch, we have measured a great reduction

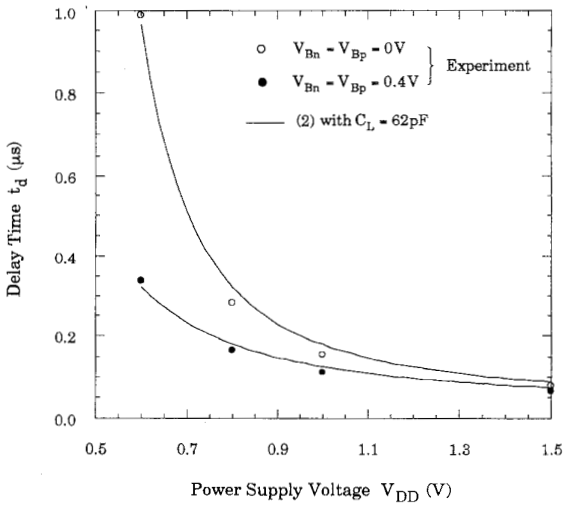

Fig. 6. The comparison of measured and calculated delay times versus power supply voltage with and without the back-gate forward bias.

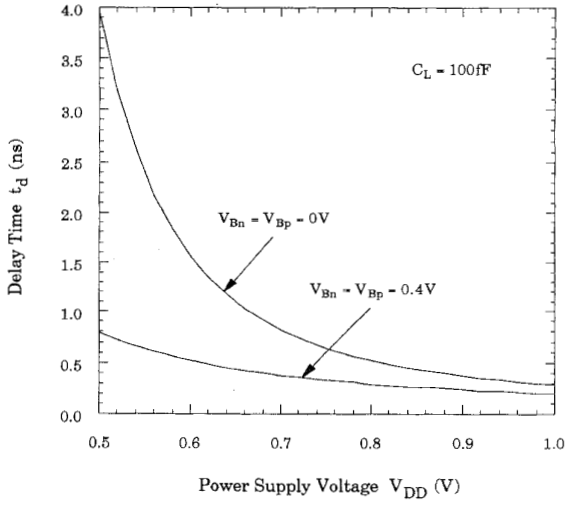

Fig. 7. The calculated delay times versus power supply voltage with and without the back-gate forward bias for $C_L = 100$ fF.

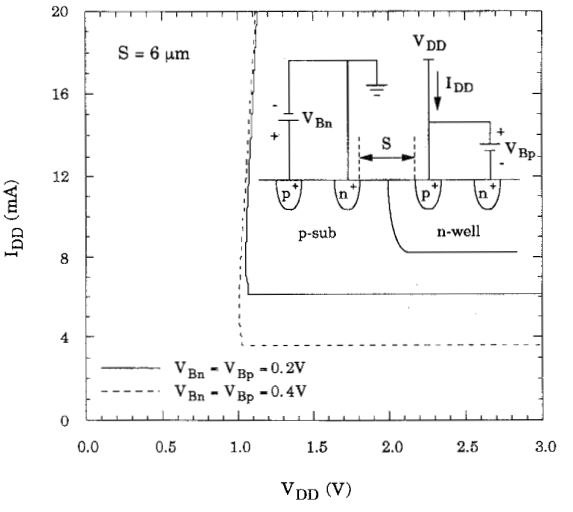

Fig. 8. The measured latch-up I-V characteristics with back-gate forward bias as parameter.

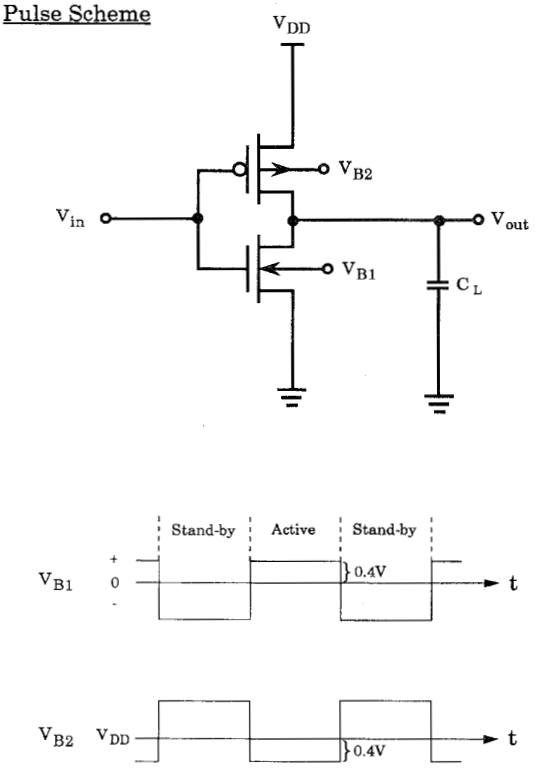

Fig. 9. The back-gate bias pulse scheme suggested for the bulk CMOS inverter.

in the subthreshold current by about three orders of magnitude, comparable with those reported in [1]–[3]. Another alternative choice is also suggested as schematically shown in Fig. 9. The back-gate bias pulse waveforms in Fig. 9 can be separated into two distinct components: the active mode and the stand-by mode. In the active mode the aforementioned back-gate forward bias method is employed while the back gate or substrate is reverse biased in the stand-by mode in order to maintain a very low subthreshold current. The back-gate bias pulse waveforms in Fig. 9 can be provided externally or generated on chip.

IV. The Impacts

Following the above guidelines, the method based on a four-terminal gated lateral bipolar transistor in low-level injection can produce several important features for low-voltage digital circuit application: 1) the transition region of the dc voltage transfer characteristics can be electrically adjusted to around the midway between high and low levels; and 2) the switching speed can be substantially improved. Further combining the source impedance switch [1]–[3] or the pulse waveforms in Fig. 9, low power demand can be achieved. It is noticeable that under the suggested range for V_{Bp} and V_{Bn}, the base or bulk current is negligible (i.e., an amount of about 10^{-10} A was measured in the bulk at $V_{Bn} = 0.4$ V or $V_{Bp} = 0.4$ V),

implying an inherent high-gain feature. This thereby significantly lowers the power consumed externally for provision of the back-gate forward bias or by on-chip back-gate forward bias generator circuitry (i.e., the band gap voltage references plus the comparators). Therefore, the present standard bulk CMOS processes can be readily utilized for realization of low-voltage, low-power digital circuits without any process or mask modification. Moreover, the original merit of low cost and high yield can be maintained along with the resultant comparable performances. For example, Fig. 3 shows a low-threshold voltage of 0.31 V at $V_{Bn} = 0.4$ V, which is comparable to that ($= 0.3$ V) obtained by multi-threshold CMOS process [1]; and Fig. 7 shows a three times reduction in delay time for $V_{DD} = 0.6$ V, which is also comparable to those obtained by using SOI process as cited in [5].

On the other hand, the same method has recently found new application in low-voltage, low-current, high-density CMOS analog integrated circuits [11]: a substantial improvement in match between the identically drawn small-size devices has been characterized over the weak inversion and moderate inversion region between weak and strong inversion. This is achieved by operating MOSFET's as four-terminal gated lateral bipolar transistors in low-level injection. The created better precision over the conventional MOSFET's is due to forward back-gate bias effect and has been successfully reproduced by a new mismatch model [11]. Apparently, by following the same guidelines, both reasonable digital speed and improved analog precision can be readily combined on the same chip. To highlight the potential of the back-gate forward bias method, a cost-effective mixed-mode low-voltage, low-power, high-density CMOS analog/digital integrated circuits chip is thus projected for the first time.

V. Conclusion

The back-gate forward bias method has been examined experimentally in the present standard bulk CMOS processes, exhibiting the abilities for low-voltage digital applications: electrically adjusting the transition region of the dc voltage transfer characteristics as well as substantially improving the switching speed. Guidelines for proper implementation of the method have been established. A new low-voltage, low-power, high-density mixed-mode CMOS analog/digital integrated circuits chip has been projected to highlight the potential of the method.

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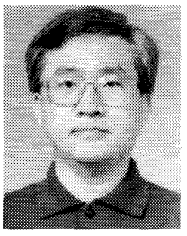

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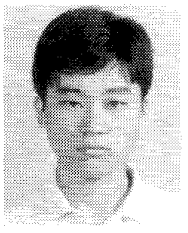

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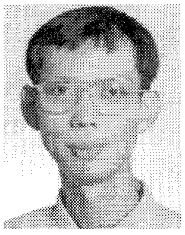

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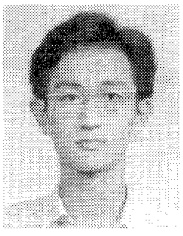

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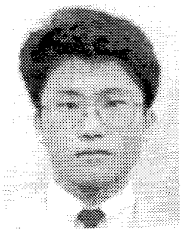

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