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Review Article

Chemical vapor deposited graphene: From synthesis to applications

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Graphene is a material with enormous potential for numerous applications. Therefore, significant efforts are dedicated to large-scale graphene production using a chemical vapor deposition (CVD) technique. In addition, research is directed at developing methods to incorporate graphene in established production technologies and process flows. In this paper, we present a brief review of available CVD methods for graphene synthesis. We also discuss scalable methods to transfer graphene onto desired substrates. Finally, we discuss potential applications that would benefit from a fully scaled, semiconductor technology compatible production process.

1 Introduction Graphene, the "first" of many two-dimensional materials, has received tremendous attention over the years since its discovery in 2004 [1]. Graphene is endowed with many extraordinary intrinsic properties that include high carrier mobility [2], broadband optical absorption [3], high current density [4], tensile strength in excess of 1 TPa [5], and high thermal conductivity [6]. Based on these properties, graphene is considered for numerous applications in various technological areas [7] covering microelectronics [8], optoelectronics [9], and nanoelectromechanical systems (NEMS) [10]. In addition, the fact that graphene is largely compatible with current complementary metal oxide semiconductor (CMOS) technology means that the material can be easily adopted for graphene co-integration with silicon devices [11]. Particular promise is seen for integration at the back-end-of-the-line, where graphene could provide added functionality to the existing CMOS platform [12]. With all this in mind, most or all of the potential applications require large-scale production of graphene layers with uniform thickness.

The highest quality graphene samples can be obtained by mechanical exfoliation of graphite [1]. However, this method yields only micron sized graphene flakes. While these are excellent for fundamental research, their thickness, size, and uniformity is not controllable. Epitaxial graphene can be grown on a large scale by thermal decomposition of silicon carbide (SiC) [13]. The graphene grown by this method exhibits good electronic properties and is suitable for large-scale processing of graphene field effect devices grown directly on SiC substrates. It is, however, difficult to transfer the graphene to other substrates. In addition, the high process temperatures, the high cost of SiC substrates, and their limited size scalability restrict its co-integration with silicon CMOS technology. Chemical vapor deposition (CVD) is a potential method for large-scale production of graphene. A comparison of different production methods, mentioned here, is shown in Table 1. After the first reports of CVD growth of graphene, the method has emerged as a potential pathway for graphene commercialization [14, 15]. The most commonly used growth substrate is copper (Cu), because graphene growth on Cu can be limited to monolayer thickness with excellent uniformity over a large area.

In this paper, we present an overview of different variants of CVD methods for graphene growth on Cu substrates. Most of the graphene applications require its deposition on dielectric substrates. For this, CVD graphene on Cu needs to be transferred to respective substrates. Therefore, we also present an overview of existing graphene transfer methods with their advantages and disadvantages.

Finally, some potential applications of CVD graphene are also discussed.

2 CVD growth of graphene

2.1 Thermal CVD In a typical CVD process, appropriate precursor species are fed into a reaction chamber. In the chamber, chemical reactions take place leading to the production of solid material on a substrate kept at elevated temperatures. In case of graphene growth, a hydrocarbon gas such as CH_4 is used as a precursor to yield graphitic material on a suitable catalytic material. The main steps of CVD graphene growth are the decomposition of hydrocarbon into carbon and then the formation of the graphitic structure, i.e., graphene on the catalytic surface. Therefore, the most important roles of a catalyst in graphene growth are to lower the energy barrier of reactions involving hydrocarbon pyrolysis and effective formation of graphene layers. This condition is mostly satisfied by transition metals like Ni, Cu, Pt, Pd, Rh, Fe, and Co. Their catalytic activity is argued to arise from partially filled d orbitals [18]. In the case of Ni, once the hydrocarbon is decomposed into carbon atoms, the carbon can diffuse into the bulk of the transition metal and

Table 1 Comparison of graphene production methods.

method	crystallite size	carrier mobility on SiO_2/SiC at RT ($cm^2 V^{-1} s^{-1}$)[a]	applications	remarks
mechanical exfoliation	100 μm	>10 000 [1]	fundamental research	no potential for industry scale
SiC decomposition	50 μm	>10 000[16]	high-frequency electronic devices and monolithic integration	scalable to SiC substrate size, non-transferrable
CVD	~5 mm [17]	~16 000 [17]	biosensing, nanoelectronics, photonics, transparent conducting layers	ultimately scalable, transferrable to desirable substrates

[a]The mobility values are for supported graphene at ambient conditions.

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Stefan Wagner is pursuing his PhD under the supervision of Prof. Max Lemme in the Department of Graphene-based Nanotechnology at the University of Siegen. He received his Dipl.-Ing. in Mechatronics at the University of Applied Sciences Ulm, Germany in 2007 and his MSc in Nanotechnology from the Royal Institute of Technology (KTH), Stockholm, Sweden in 2012. From 2007 to 2010, he worked as design and project engineer for the consultant companies YACHT-Teccon Engineering GmbH & Co. KG and MATIS Germany in Munich, respectively. His research interests include MEMS and NEMS devices and applications, in particular graphene-based sensors.

Max Lemme received the Dipl.-Ing. (MSc) and Dr.-Ing. (PhD) degree in Electrical Engineering from RWTH Aachen University in Germany. He became Heisenberg-Professor for Graphene-based Nanotechnology at the University of Siegen, Germany in 2012 and has been Affiliate- and Guest-Professor at KTH Royal Institute of Technology, Sweden since 2010. Before joining KTH, he was a research fellow at Harvard University from 2008 to 2010 and worked for 10 years at nanotechnology start-up AMO GmbH, Germany, as Head of Technology Department. His research interests include non-conventional nano-CMOS devices, novel high-*k* materials for gate stacks and the technology, devices, and circuits based on graphene and other 2D materials. He received a NanoFutur Award by the German Federal Ministry for Education and Research (BMBF) in 2006, a Humboldt-Fellowship in 2007 and an ERC Starting Grant in 2012. He is a senior member of the IEEE.

later precipitate to the surface during cooling. Similar processes take place for other carbide forming metals like Fe and Co. If the carbon solubility in the metal is limited or negligible, then graphene formation takes place as a surface process, e.g., in the case of Cu and Ru. It has been demonstrated experimentally that graphene growth on Ni is diffusion–precipitation dominated while it is a surface diffusion process on Cu surfaces [15]. Therefore, it is difficult to control uniformity and thickness of graphene layers on Ni and similar metals. In contrast, graphene growth is restricted mostly to monolayer thickness on Cu and similar surfaces, because once a monolayer is formed, the graphene film acts as a diffusion barrier for other carbon atoms. Therefore, and because of the wide availability and low cost, Cu is the mostly used catalyst for CVD graphene growth.

There are many ways through which hydrocarbons can be decomposed or pyrolysed into carbon atoms. One of the most commonly used methods is by high temperatures and the process is therefore termed as thermal CVD. For large area thermal CVD growth of graphene, CH_4 gas is decomposed at elevated temperatures of around 1000 °C. Figure 1a shows the schematic of a typical thermal CVD hot wall reactor. In our experiments, a rapid thermal processing cold wall reactor (Moorfield nanoCVD) has been used, where only the Cu foil is heated through a heating stage (Fig. 1b). Cu foil is heated to high temperatures in an atmosphere of Ar and H_2 gases. The substrate is first annealed for a certain length of time to reduce the oxides on the Cu surface and for grain growth. For graphene growth, an appropriate mixture of CH_4/H_2 gas is then used. During this time, CH_4 dissociates into radicals/atoms and surface reactions involving adsorption and surface diffusion take place at the Cu surface leading to graphene growth, as shown schematically in Fig. 1c.

Hydrogen helps to reduce the native surface oxides on the Cu surface, which passivates the growth of graphene. Recently, the role of surface oxygen on graphene growth has been investigated thoroughly and it has been found that surface oxygen is helpful in growing large grained graphene on Cu surface [19]. This happens because surface oxides reduce the nucleation density of graphene nuclei, thereby encouraging the large growth of single grains. The thermal CVD process can be carried out at pressures ranging from low pressures to atmospheric pressure. Figure 1d shows the photograph of a Cu foil after graphene growth. The quality of graphene is assessed by Raman area mapping after transfer to a SiO_2/Si substrate, as shown in Fig. 1e.

The main parameters that affect the growth of graphene on Cu are process pressure and CH_4 to H_2 ratio. The role of hydrogen during thermal CVD has been demonstrated and it was found that H_2 partial pressure has a significant effect on the graphene grain size and shape [20]. Generally, graphene growth is limited to monolayer on Cu but by changing the working pressure and H_2/CH_4 ratio, researchers are now able to control the number of graphene layers on Cu by thermal CVD [21]. The proposed growth mechanism involves formation of graphene seeds, which pre-define the thickness of graphene layers, by supersaturated surface carbon in Cu. These graphene seeds grow independently before forming continuous graphene film. The growth mechanism is proposed to be simultaneous-seeding and self-limiting process rather than a layer-by-layer growth. Direct growth of graphene

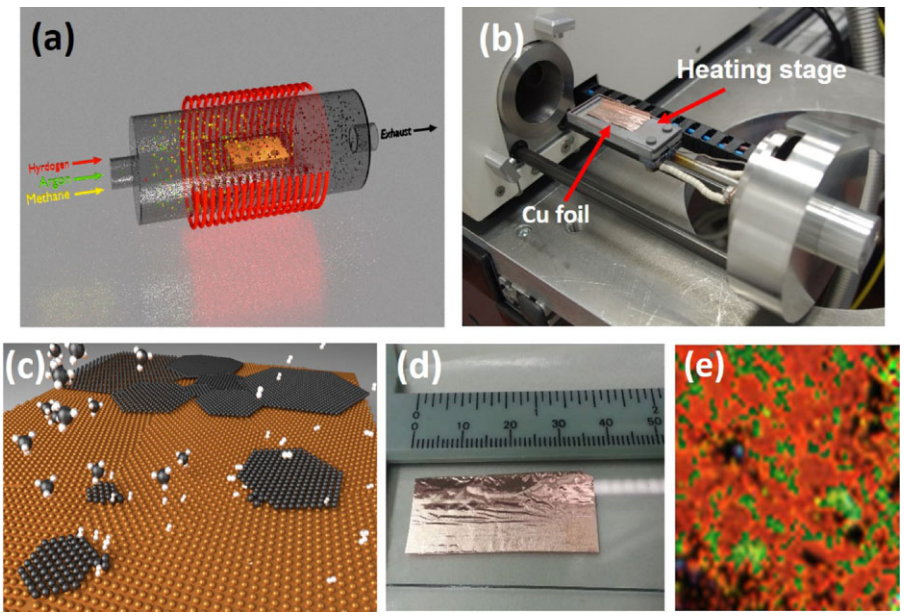

Figure 1 (a) Schematic of typical CVD of graphene using CH_4 gas as a precursor. (b) Photograph of a Cu foil kept on a heating stage before loading in a rapid thermal processing cold wall reactor. (c) Graphene growth on Cu as a surface reaction. (d) CVD graphene on Cu foil. (e) A Raman map of graphene film transferred on SiO_2/Si substrate. The area is $64 \times 64\ \mu m^2$. Red color in the image represents single layer coverage. Green color represents multilayer regions.

on dielectric substrates has been demonstrated using Cu thin films as catalysts. Recently, graphene has been grown using Cu vapors by placing a SiO_2 substrate directly underneath a Cu foil [22]. Roll-to-roll production of graphene films has been demonstrated using thermal CVD making it a promising technique for continuous large-area growth of graphene [23]. The processing time of thermal CVD is around 2–3 h including heating, annealing, growth, and cooling times. This can vary depending on the annealing time and CH_4 exposure time for graphene growth. In conventional thermal CVD, the substrate is heated to the desired temperature by convection or radiation heating and takes a longer time to reach the deposition temperature. However, the heating and cooling time can be reduced dramatically by using rapid thermal annealing (RTA) systems. This reduces the total processing time to about 30–40 min.

Generally, the graphene grown on Cu foils is polycrystalline in nature and contains grain boundaries that degrade their electronic properties. To circumvent the problem of polycrystallinity, efforts have been made to grow large-area single crystal graphene. For this, single crystal germanium (Ge) has been used as a catalytic substrate, utilizing the low solubility of C in Ge even at its melting point [24–26]. Wang et al. [24] have demonstrated thermal CVD growth of uniform and wafer scale graphene on Ge substrate. By depositing graphene at different temperatures, they found that graphene growth on Ge is self-limited and surface mediated as in case of Cu. However, graphene transfer from Ge substrate to desired substrates led to wrinkled and folded regions. Lippert et al. [25] have also reported direct uniform deposition of graphene on Ge (001) layers on Si (001) wafers. Their results indicate that graphene can be directly deposited at the active regions of Si transistors with a process compatible with Si technology. Lee et al. [26] have reported the growth of wafer scale growth of single crystal monolayer graphene on hydrogen terminated Ge substrates. Here, a controlled low-pressure thermal CVD process leads to wrinkle free growth on epitaxially grown single crystal Ge layers on Si (110) wafers. Weak adhesion between the graphene and an H terminated Ge buffer layers allowed mechanical exfoliation of graphene using Au thin films as a support layer. Using this transfer process, the authors demonstrated that Ge substrates can be reused several times for graphene growth. In addition to the potential quality and cost advantage, the growth of graphene on Ge substrates may solve contamination issues associated with the use of catalytic metals in conventional graphene CVD.

2.2 Alternative CVD methods A hot filament CVD (HF-CVD) technique has been used to grow diamond films and carbon nanotubes (CNT) on industrial scale. In this technique, the hydrocarbon gas like CH_4 is decomposed by thermal means using a hot filament, as shown in Fig. 2a. Recently, the technique has been used to grow high quality graphene on Cu foils [27, 28]. Figure 2b–e show the quality of graphene grown by HF-CVD technique analyzed by optical and Raman spectroscopy.

In this method, a tungsten or Mo filament is heated to temperatures as high as 2000 °C by passing current through it. A mixture of CH_4 and H_2 gas is showered on the hot filament through a gas shower and Cu foil is kept just below the filament. The hot temperature zone near the filament decomposes the CH_4 gas and heats the substrate to high temperatures of about 1000 °C. The substrate temperature depends on the position of substrate from the hot filament, i.e., the farther it is, the lower the temperature is. The advantage of this technique is that cooling rates can be very high and the Cu foil can be brought to room temperature in few minutes as it is being radiatively heated by the hot filament. This is already an industrial technique to grow large area diamond and CNT films, and it can therefore potentially be scaled up for graphene growth as well.

Thermal CVD techniques use high temperatures to decompose CH_4 gas into reactive radicals. However, the thermal budget (temperatures and process times) is

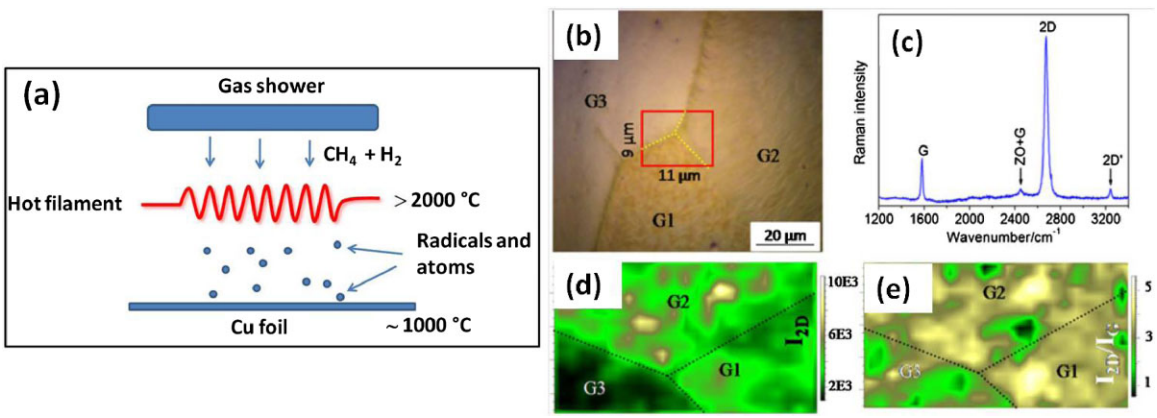

Figure 2 (a) Schematic depicting the CVD process in a hot-filament CVD set up. (b) Optical micrograph of a Cu foil after graphene growth depicting the three grains G1, G2, and G3. (c) A typical Raman spectrum of HF-CVD graphene on Cu foil. Raman map of (d) 2D band intensity and (e) intensity ratio of 2D and G band from the area enclosed in the red square in (b) (figures adapted from Ref. [27]).

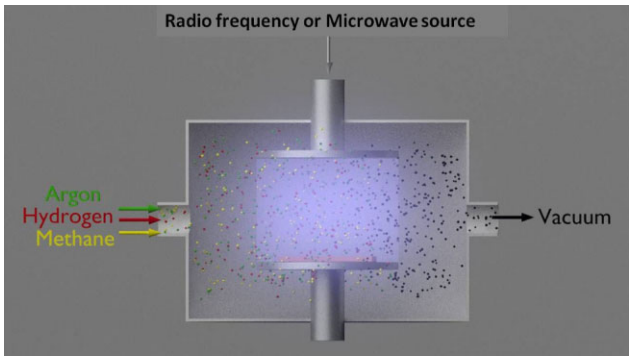

Figure 3 PECVD set up for graphene growth.

incompatible with CMOS technology. Hence, there is a need to grow graphene at low temperatures and ideally directly on dielectric substrates, which would make the process fully compatible with the present CMOS technology. To achieve this, plasma-enhanced CVD (PECVD) techniques have been proposed. Plasma assists in dissociating CH_4 gas into reactive radicals at low temperatures and the substrate temperatures can be kept as low as 600 °C. Figure 3 shows a typical PECVD set up where a radio-frequency (RF) or microwave source is used to generate the plasma. The main steps of graphene growth are similar to thermal CVD with the only difference that plasma is used instead of temperature to dissociate hydrocarbon into activated carbon radicals. As with thermal CVD, the carbon radicals reach the Cu surface and form graphene layers.

Microwave and RF plasma have been used to synthesize graphene at low temperatures [29, 30]. Researchers have also used remotely ignited RF plasma to grow large-area graphene on catalyst-coated dielectric substrates [31]. This was done in order to avoid damage to the growing graphene layer by ion bombardment. As a downside, this process requires high vacuum conditions to operate. Although graphene films can be grown at moderate temperatures using PECVD technique, the quality of the graphene is not as good as that of thermal CVD graphene: the low process temperatures result in reduced graphene grain sizes due to restricted surface diffusion of carbon atoms on the catalytic surface. Nevertheless, due to its enhanced process compatibility, PECVD grown graphene has great promise for electronic and optoelectronic applications where highly conducting and transparent layers are required.

3 Graphene transfer

As discussed above, there have been serious efforts in growing high quality graphene by different methods. However, an often underestimated yet crucial step for almost any envisioned application of graphene lies in its efficient large-area transfer from catalytic substrates to the desired substrates, which vary according to the applications. For example, for transistor applications, graphene should be placed on a dielectric substrate. For touch screen displays and flexible devices, graphene needs to be transferred to flexible substrates like PTFE, etc. The most commonly employed methods for graphene transfer are discussed below with their pros and cons.

The method proposed first for graphene transfer involves etching of the metal substrate and is a widely used wet transfer method [18]. Figure 4a shows the schematic of the steps involved. First, a polymer is spin coated onto the as-grown graphene on Cu and is then hot-baked to evaporate the solvent. Cu foil is then placed in an etchant solution to etch away the Cu. Most common Cu etchants are iron chloride, sodium persulfate, ammonium persulfate, and HCl solution. After the Cu is etched, the polymer/graphene stack is fished out using a glass substrate or silicon wafer and placed in a water bath several times until the etchant is removed. The polymer/graphene stack is then transferred onto the desired substrate before the polymer is removed using an appropriate solvent. Figure 4b shows an optical micrograph of graphene transferred onto a SiO_2 substrate using the wet etching transfer method. Different recipes are being used to remove polymers. PMMA is the most commonly used polymer and is generally removed using acetone. However, since it has been demonstrated that PMMA is typically not removed entirely even after long exposures to acetone, a thermal annealing step is often used to completely remove PMMA, with temperatures between 300 and 500 °C in the presence of forming gas. Considering the difficult in completely removing the PMMA residues, polycarbonate is used as an alternative that leaves less residue than PMMA [32].

A thermal release tape method is often used to transfer graphene on flexible substrates [33]. In this method, a thermal release tape is laminated on the graphene/Cu stack. After laminating, Cu is etched using a wet etching method as described above and the remaining tape/graphene stack is transferred to a flexible substrate like PTFE or PET. A pressure is applied to the tape/graphene/PET stack and then the thermal tape is released under heat. This method has been adopted for demonstrating roll-to-roll production of 30 inch graphene films for transparent electrodes [33]. The main disadvantage of this method is the problem of unwanted tape residues, which can degrade the quality of graphene. To avoid such problems, the method has been modified for direct transfer of CVD graphene onto flexible substrates [34]. In this method, the target flexible substrate is directly pressed against graphene/Cu/graphene stack and a protective sheet of weighing paper is put on top of this stack. Then the stack is sandwiched between two polyethylene terephthalate films instead of using thermal release tape.

Another recent graphene transfer method is the "soak and peel" method [35]. This method does not use corrosive etchants and hence reduces the unintentional doping of graphene by etchant ions, as well as reduces the environmental concerns. A polymer support layer is first spin coated on a graphene/Cu stack. For handling purposes, Kapton tape is then applied with pressure on the polymer support. The Cu foil is then immersed in hot de-ionized water at 90 °C for 2 h, as shown in Fig. 4c. In this process, water slowly seeps through the weak graphene–Cu interface and thereby slowly removes the Kapton tape/polymer/

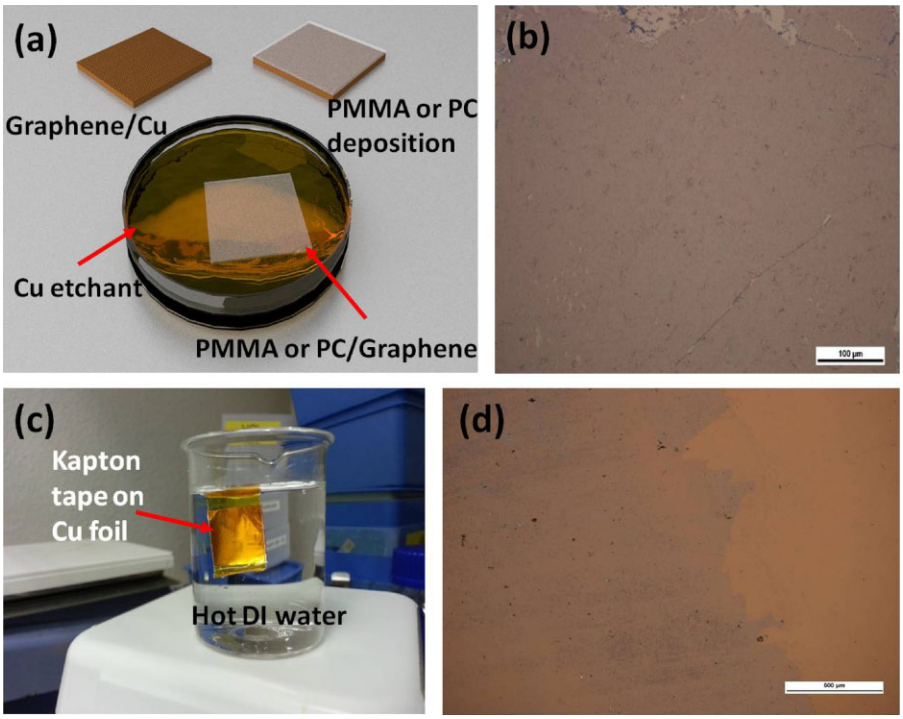

Figure 4 (a) Schematic representation of wet etching process steps. (b) Optical micrograph of graphene transferred onto a SiO_2 substrate using a wet etching process. (c) Photograph of a "soak and peel" process with Kapton tape. (d) Optical micrograph of "soak and peel" transferred graphene.

graphene stack. The Kapton tape is then pressed gently onto dielectric substrates like SiO_2 and is heated to around 140 °C for about 40 min, after which it can be carefully removed. Then, the polymer is removed using acetone. However, this process also leaves residues on the substrate, requiring annealing steps as described above. This process, though it avoids the use of etchant solution, produces more cracks, ripples, and folding and results in a non-uniform transfer, as shown by the optical micrograph in Fig. 4d.

All the above-mentioned transfer methods take from 30 min to few hours in removing graphene from the Cu surface. Electrochemical delamination or more commonly known as "bubble transfer method" is a very fast and efficient method to remove graphene from a metal catalyst surface [36, 37]. Like other methods, a polymer supporting layer is spin coated on the Cu surface after graphene growth. In the delamination process, a direct current (DC) voltage is applied to the polymer/Cu electrode and another electrode like platinum and glassy carbon in an electrolyte cell arrangement, as shown in Fig. 5a. The electrolyte solutions includes Na or K salts like NaOH, KOH, NaCl, KCl, etc. A negative voltage is then applied to the Cu foil, which causes the generation of H_2 bubbles at the graphene–Cu interface due to the water-splitting process:

$$2H_2O(l) \rightarrow H_2(g) + 2OH^-(aq.)$$

H_2 bubbles assist in removing graphene from the Cu surface, and hence the process is called bubble transfer process. Figure 5b and c shows optical and scanning electron micrographs of a bubble transferred CVD graphene on SiO_2 substrate. Raman analysis shows that the quality of the graphene is maintained by this transfer method (Fig. 5d). The presence of graphene adlayers and grain boundaries, which act as defects are formed during graphene growth, resulted in a small D peak in the Raman spectrum. This process takes only a few seconds to completely remove the graphene layer from Cu surface. It is further non-destructive in nature as the metal catalyst can be reused for graphene growth many times. The method thus has potential for industrial scaling for large-area graphene transfer.

4 Applications Technologically, the CVD method with its metallic catalysts and transfer processes are not (yet) compatible with semiconductor process lines. This is particularly true for the front-end-of-the-line, where stringent requirements exist regarding organic, metallic, and particle contamination levels. Nevertheless, many potential applications of graphene are envisioned in microelectronics [8], optoelectronics [9], and NEMS [10]. These applications potentially make use of the exceptional material properties of graphene, and could be integrated in the back-end-of-the-line on top of existing CMOS circuits to add "more than Moore" functionalities.

One of the first suggested applications of graphene was as a replacement channel material in field effect transistors (GFETs) to exploit the material's high carrier mobility [38]. However, the absence of an electronic band gap results in

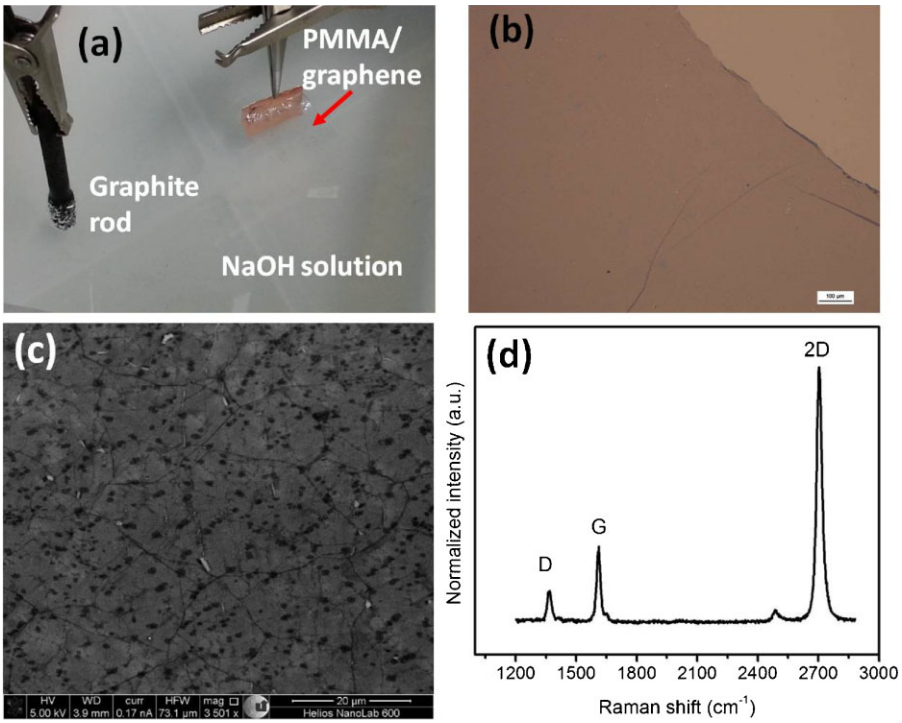

Figure 5 (a) Photograph of a typical graphene bubble transfer set up. (b) Optical micrograph of transferred graphene on SiO_2 substrate. (c) Scanning electron micrograph of transferred graphene. Dark spots are the graphene adlayers. (d) Raman spectra of bubble transferred graphene.

ambipolar switching characteristics and limits the current modulation in GFETs. Gapless graphene is therefore unsuitable for logic circuits, where transistors are required to display a high ratio between currents in the ON-state versus the OFF-state, i.e., they need to be switched off. Transistors for RF applications, in contrast, do not require such high ON/OFF ratios [39]. As a consequence, cut-off frequencies f_T (where the unilateral power gain equals unity) of up to several hundred GHz have been reported (after de-embedding) [40], rivaling those of state-of-the-art semiconductor devices. The message becomes mixed, however, once the other figure of merit for RF transistors is considered, i.e., the maximum frequency of oscillation f_{max}. Similar to the case of logic operation, Physics strikes again. Here, the ambipolar nature of graphene leads to limited saturation in the output characteristics (I_d vs. V_d) of GFETs, which in turn limits f_{max}. Therefore, bandgap engineering in graphene may be an option, either through confining the channel in one-dimension with graphene nanoribbons (GNRs) [41], using electrically biased bilayer graphene [42] or by doping graphene with boron and nitrogen [43]. All of these methods would improve some of the discussed issues, but at the same time introduce new challenges to devices engineers such as random GNR orientations, GNR width fluctuations, or increased design complexity due to double-gate operation or decrease in mobility after doping. Nevertheless, GFET applications remain a topic of intense research. Electronic device options beyond conventional field effect transistors include the barristor based on a graphene–silicon Schottky barrier [44], the theoretically proposed bilayer pseudospin FET (BISFET) based on an electron–hole-pair condensate [45] and lateral [46] and vertical tunnel transistors [47, 48]. One such implementation, a vertical hot electron transistor, is described in more detail in Section 4.1.

A variety of optoelectronic devices based on graphene have been demonstrated to date, building on the broadband universal absorption of 2.3% of incoming light and the high carrier mobility. While the former provides easy access to the commercially highly attractive infrared (IR) range, the latter adds potential for very high operating speeds. Graphene photodetectors typically rely on a graphene pn-junction in a diode [49] or transistor configuration [50]. They are generally extremely broadband due to the absence of a bandgap, covering a range from ultraviolet (UV) to far IR and THz, but suffer from limited responsivity due to the thinness of the material. There are several options to increase the responsivity, such as the co-integration of graphene with metallic plasmonic nanostructures [51], photon absorbing nanoparticles [52], or microcavities with built-in reflectors for specific wavelengths. All approaches are capable of enhancing the photoresponse considerably, but only for specific wavelengths. When integrated into photonic waveguides, graphene photodetectors can be quite efficient [53, 54], because the light is detected in-plane with the graphene, and the graphene detector can be scaled up in size.

Obviously, the RC delay of such a detector may limit the ultimate detector speed. Graphene can further act as a modulator for photonic waveguides. When gated, the Fermi level in a graphene modulator can be tuned to suppress absorption through Pauli blocking [55]. This effectively quenches absorption and results in the possibility of modulating the light passing through a (silicon) waveguide.

Micro- and NEMS often employ thin membranes of various materials to form mass or pressure sensors or accelerometers and actuators. Graphene is the ultimate membrane with its ultimate thinness, record high Young's modulus of over 1 TPa [5, 56], and stretchability of over 20% [57]. As a consequence, graphene-based resonators can operate at very high frequencies [58]. Extrapolated values for nm-scale graphene nanomembranes are of the order of 400 GHz [59], with q-factors sufficient for the detection of single hydrogen atoms. The field of graphene NEMS is probably the least developed compared with electronics and optoelectronics, but nevertheless has high potential for applications. A discussion of an integrated graphene pressure sensor based on the piezoresistive effect is described in detail in Section 4.2.

4.1 Vertical graphene base hot electron transistors Electronic devices with vertical carrier transport including 2D-materials have received considerable attention lately. One such candidate, a graphene-based hot electron transistor has been proposed conceptually [48] and later demonstrated in experiments [60]. In this device, a graphene sheet is sandwiched between two insulators, with metals or doped semiconductors on both sides (Fig. 6a). Carrier transport is vertical and happens by way of quantum mechanical tunneling. In such a device, the base contact is made up of graphene (hence, graphene base transistor (GBT)), because the combination of high electrical conductivity and extreme thinness of the material lead to high transmission of charge carriers. Consequently, the graphene transition time is expected to be much lower than for metals, which need to be at least ten times thicker in order to provide the same functionality. When a voltage is applied to the graphene base, the current can be modulated by several orders of magnitude (Fig. 6b). This is because the graphene base potential modulates the tunneling barrier between the emitter and the base. Above a certain threshold, charge carriers may tunnel via the Fowler–Nordheim mechanism and reach the collector by ballistic transport (Fig. 6c).

4.2 Graphene NEMS pressure sensor Pressure sensors based on the piezoresistive effect in graphene membranes have been demonstrated for uniaxial strain [61] and for biaxial strain [62]. In these devices, a layer of graphene is suspended over an air-filled cavity like a drum. The device is then placed inside a vacuum chamber and air is pumped out of the chamber. As the pressure of the chamber is reduced, the pressure of the trapped air presses against the suspended graphene membrane and strains it (Fig. 7a). This strain changes the electronic properties of the graphene, which is measured as a change in the resistance of the graphene membrane. The device structure is shown in Fig. 7b. Figure 7c shows the voltage output of one of the pressure sensors compared with the voltage output of a control device, which does not have an air-filled cavity. SEM images illustrate the difference between the pressure sensor and control device. Figure 7d shows the area-normalized sensitivity of a graphene pressure sensor in comparison to silicon and CNT sensors. When normalized by unit area, the graphene sensor has a sensitivity, which is 100 s of times higher than the conventional sensors. This potentially allows for aggressive device scaling and in connection with CVD graphene growth and transfer allows future on chip integration with essential cost advantages over existing technologies.

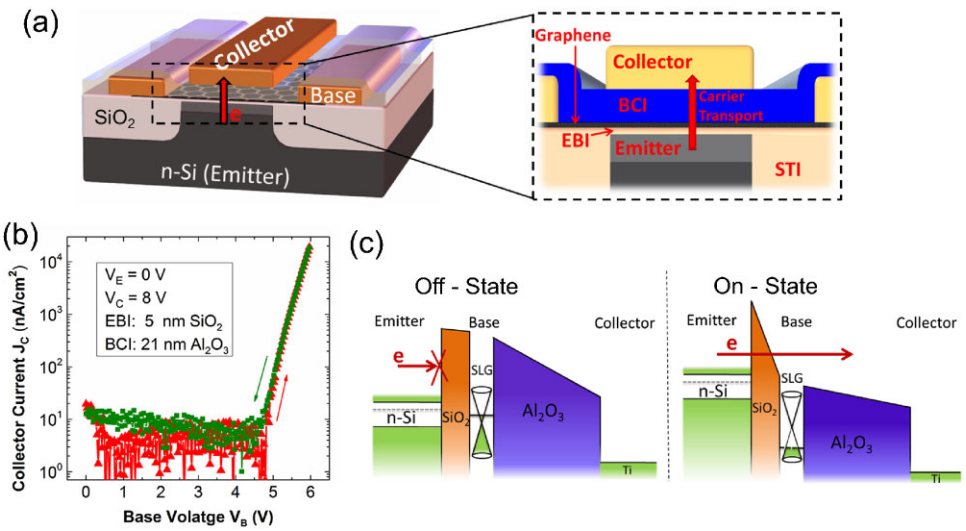

Figure 6 (a) Schematic of a vertical hot electron transistor with a base made of graphene (graphene base transistor (GBT)). (b) Transfer characteristics of a GBT. (c) Electronic band structure of a GBT in the off- and the on-state.

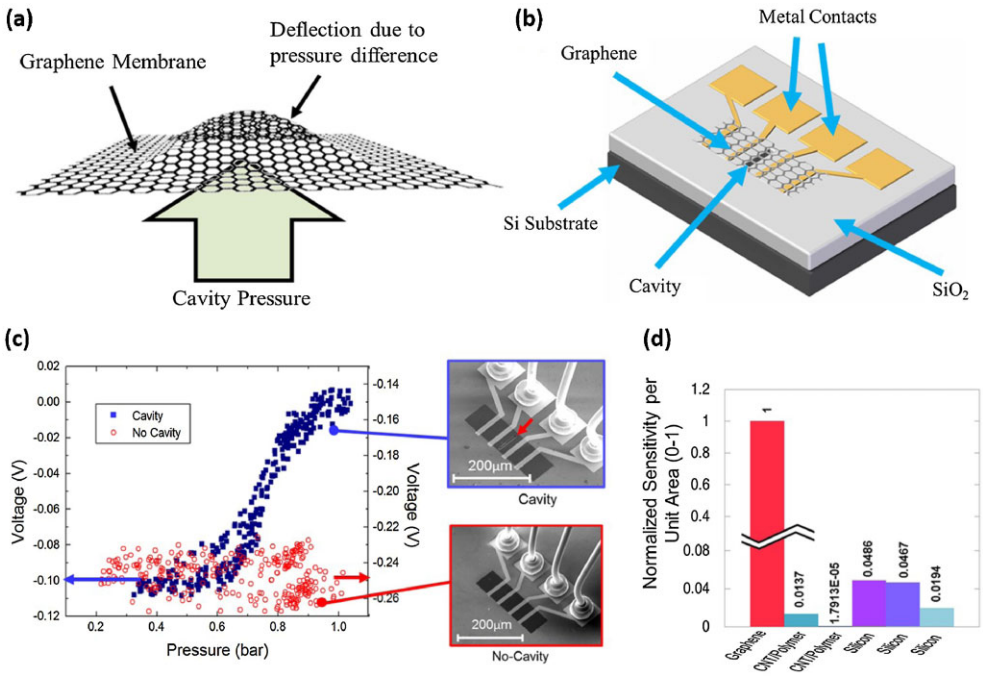

Figure 7 (a) Deflection of a graphene membrane as a result of a pressure differential between cavity pressure and the pressure of the vacuum chamber. (b) Schematic of a pressure sensor. (c) Comparison of the voltage signal output of a graphene sensor compared with a graphene device, which is not suspended over an air filled cavity. SEM images illustrating the difference between devices containing a cavity (indicated by red arrow) and devices without cavities. (d) Comparison of the area-normalized sensitivities of a graphene sensor and conventional silicon and carbon nanotube sensors.

5 Conclusions Graphene growth on a large-scale by CVD methods has been a key achievement on the road toward its commercialization. We discussed various CVD methods for growing graphene on different metallic substrates, especially on Cu as well as very recent reports of graphene growth on Ge. Thermal CVD methods provide reasonable quality graphene but are difficult to integrate with nanoscale semiconductor processes, as high thermal budgets are needed for graphene growth. PECVD methods use low temperatures as compared to thermal CVD, but yield poor quality graphene layers. For application purposes, CVD grown graphene needs transfer to desired substrates. A number of transfer methods have, therefore, been discussed. While applications can be demonstrated with current graphene CVD technology, we conclude that further developments in graphene growth at low temperatures and direct growth on insulating substrates are still highly desired.

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