1/2.7 Inch 2 Mega Pixel CMOS Image Sensor SP2305-2A

Specification

Version Commercial 1.0

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SuperPix Micro Technology Co., Ltd

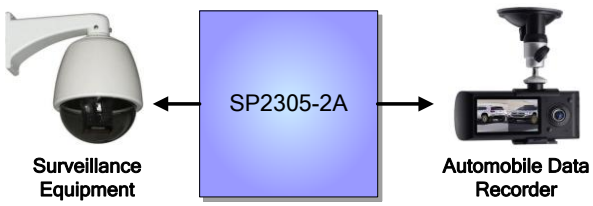
High performance SP2305-2A is a 1/2.7 inch 1080P format CMOS image sensor. It provides high quality digital images and high-definition (HD) video. SP2305-2A focuses on products including Security Surveillance systems and Automobile Data Recorder. By introducing advanced 3.0μm pixel architecture, SP2305-2A achieves low-light sensitivity, signal-to-noise ratio, full-well capacity, quantum efficiency and low-power consumption. The default mode and programmable mode of it allow a more convenient way for controlling the parameters of frame size, exposure time, gain value, and so on. The SP2305-2A is able to provide stable performance between 0℃ and 60℃. It also offers the following image control functions: mirror and flip, windowing, offset, auto black level calibration, defect pixel correction, black sun cancellation, and so forth. The SP2305-2A provides 2k-bit of OTP. It supports high frame rate up to 30fps@1920x1080 and 60fps@1280x720 format through the DVP interface and MIPI 2 lane interface. These prominent features integrated in SP2305-2A make it become the best-in-class image sensor, and will bring users vivid pictures and excellent experience.

Function list

- CMOS Image Sensor

Applications

- Security Surveillance
- Automobile data recorder



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Overview

General Description

High performance SP2305-2A is a 1/2.7 inch 1080P format CMOS image sensor. It provides high quality digital images and high-definition (HD) video. SP2305-2A focuses on products including Security Surveillance systems and Automobile Data Recorder.

By introducing advanced 3.0μm pixel architecture, SP2305-2A achieves low-light sensitivity, signal-to-noise ratio, full-well capacity, quantum efficiency and low-power consumption. The default mode and programmable mode of it allow a more convenient way for controlling the parameters of frame size, exposure time, gain value, and so on. The SP2305-2A is able to provide stable performance between 0℃ and 60℃.

SP2305-2A offers the following image control functions: mirror and flip, windowing, offset, automatic black level calibration, defect pixel correction, black sun cancellation, and so forth. The SP2305-2A provides 2k-bit of OTP. It supports high frame rate up to 30fps@1920x1080 and 60fps@1280x720 format through the DVP interface and MIPI 2 lane interface with transfer rate of typical 420 Mbps per lane.

These prominent features integrated in SP2305-2A make it become the best-in-class image sensor, and will bring users vivid pictures and excellent experience.

An overview of the SP2305-2A Image Sensor features and functions will be given below.

Function Diagram

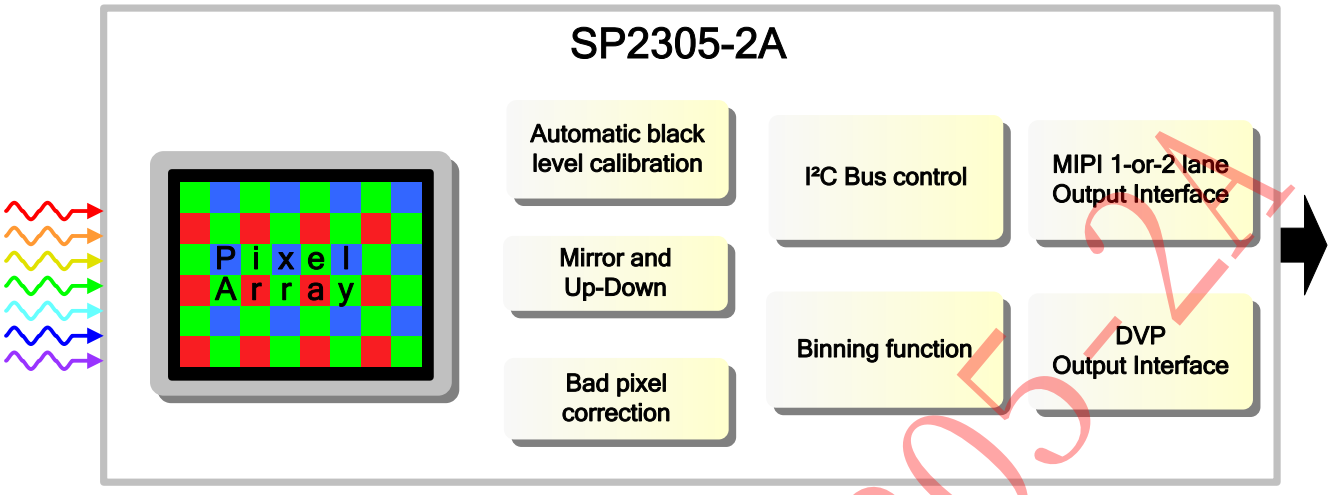


Figure 1 Function Diagram

Typical Application List

- Security Surveillance
- Automobile data recorder

Typical Application Diagram

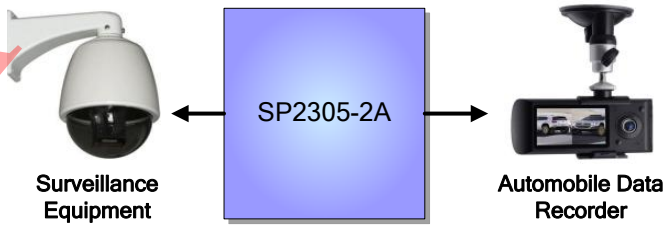


Figure 2 Typical Application

Key Performance Parameters

Parameter	Value	
Active Pixel Array	1920x1080	
Pixel Size	3.0μm x 3.0μm Square Pixel	
Lens Size	1/2.7 inch	
Color Filter	Primary Color Filter Bayer arrangement	
Power Supply	I/O	1.7V - 3.0V (1.8V typical)
	Analog	2.6V - 3.0V (2.8V typical)
	Core	1.7V - 1.9V (1.8V typical)
Power Consumption	Active	176 mW
	Standby	< 30μW
Data Format	Raw10	
Output Formats	DVP 10-bit	
	MIPI 2 lane	
Input Clock	6 – 27MHz	
Max. Frame Rate	30fps@1920x1080 Mode	
	60fps@1280x720 Mode	
Operating Temperature	-30 ℃ ~ 85 ℃	
Stable Temperature	0 ℃ ~ 60 ℃	
Package	CSP	

Table 1 Key Performance Parameters

Features List

- Supports 1080P (2Mega pixel, 1920x1080) resolution
- Supports 720P (0.9Mega pixel, 1280x720) resolution
- Supports 3.0µm x 3.0µm FSI pixel architecture
- Supports windowing
- Supports mirror and flip
- Supports automatic black level calibration
- Supports defect pixel correction
- Supports black sun cancellation
- Supports 2k-bit of OTP;
- I^2C control interface for register programming
- Supports binning function
- Supports on-chip phase lock loop(PLL)
- Supports 10-bit RAW image data output
- Supports MIPI 2 lane serial output interface
- Supports DVP 10-bit output interface
- Supports low power mode

Function Description

Pixel Array Structure

The SP2305-2A pixel array is configured as of 2012 columns by 1126 rows, and the active array size is 1920x1080. The details of pixel array are shown below.

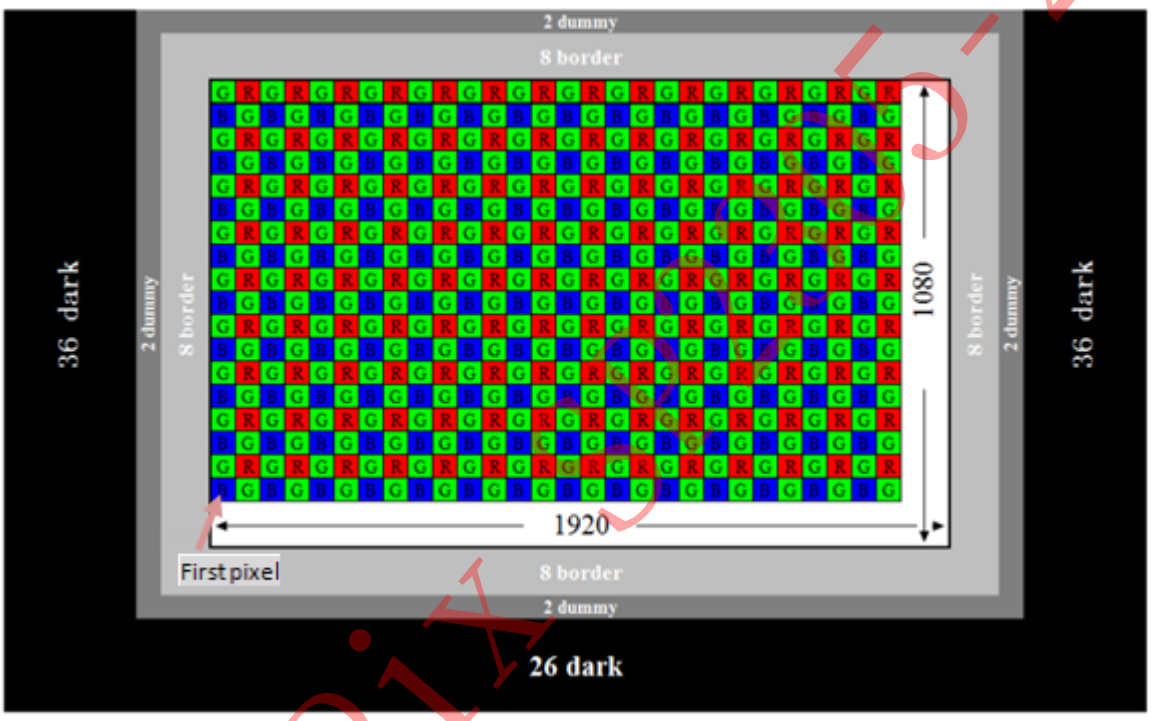


Figure 3 Pixel Floor Plan

Note:

The color filter of the first pixel at left bottom is blue.

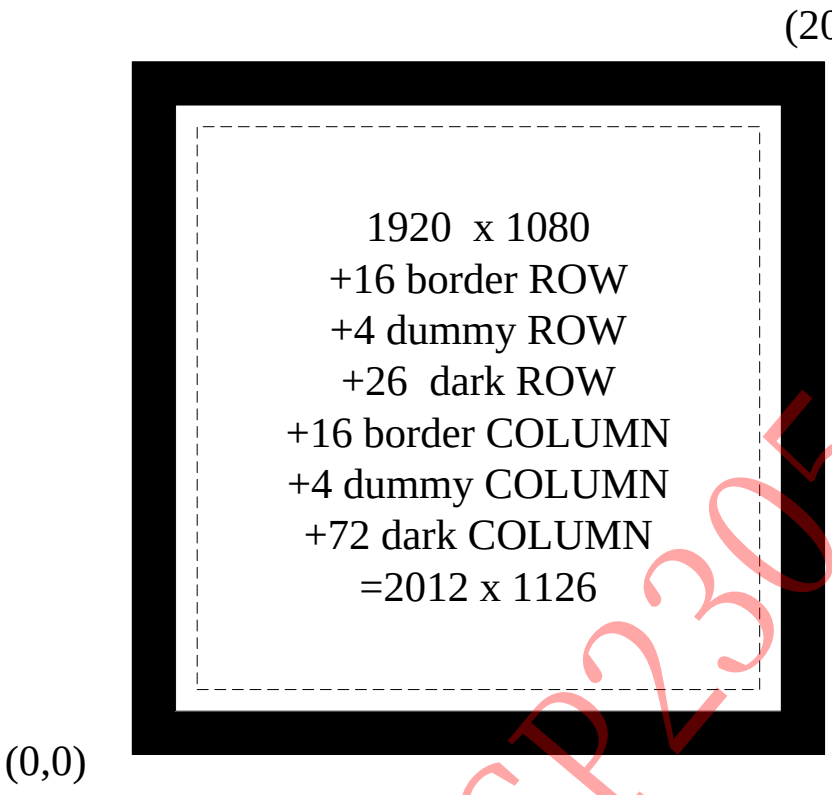


Figure 4 Sensor Pixel Description

Sensor Image Signal Processor Functionality

- Mirror and Flip
- Windowing
- Binning function
- Test Pattern
- Auto Black Level Calibration
- Defect Pixel Correction
- Gain

Mirror and UP-Down

Mirror and Flip read out modes are provided, and can reverse the sensor data read out order horizontally and vertically respectively.

Original Mirrored Flip Mirrored and Flip

Windowing

The embedded windowing function extracts an image windowing area by defining 4 parameters, including horizontal start, horizontal width, vertical start, and vertical height. By properly setting the parameters, the portions within the sensor array size can be cropped as a visible area. Windowing function will not conflict with the mirror and flip function.

Binning function

The SP2305-2A supports a binning mode to provide a lower resolution output while maintaining the field of view. The SP2305-2A support 2x2 binning by averaged the same color of adjacent pixels.

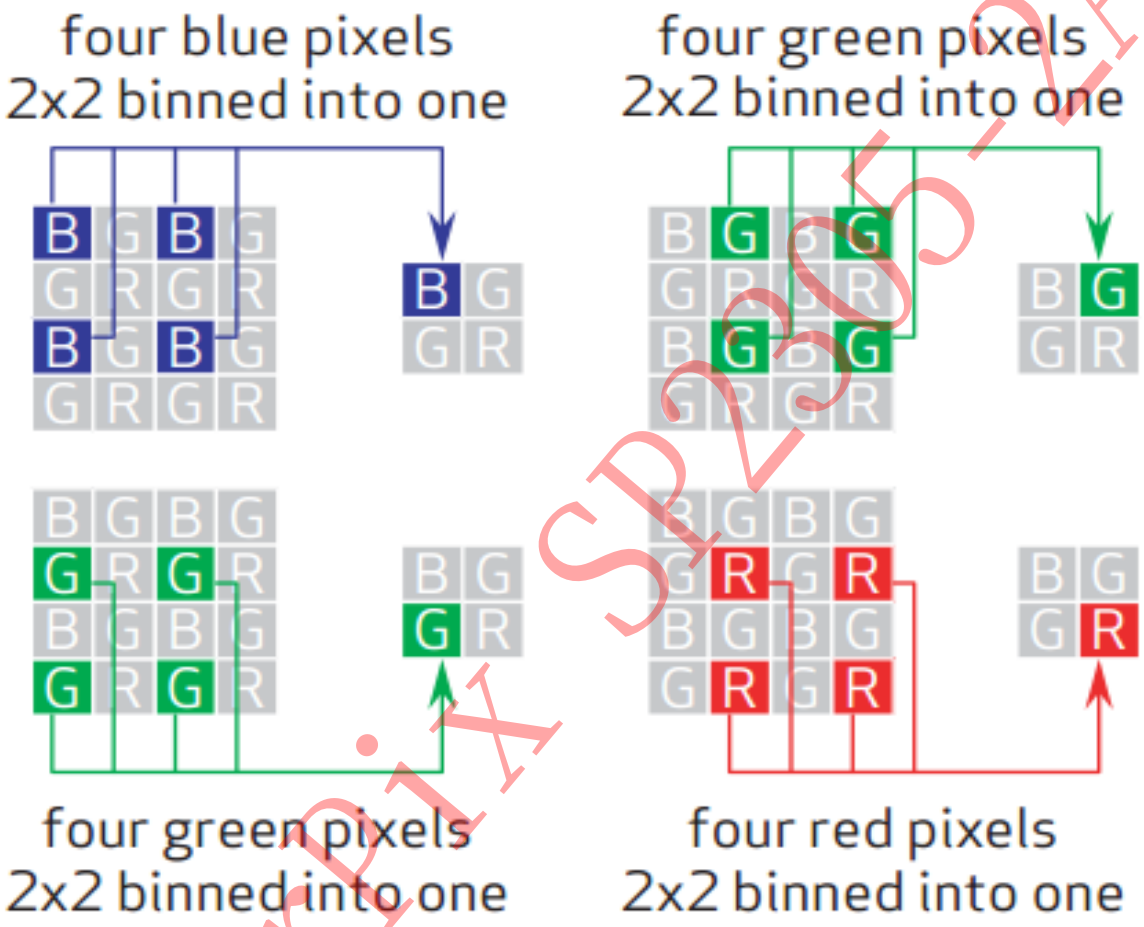


Figure 5 Binning function

Test Pattern

Test pattern, color bar, is offered for testing purpose.

Format and Frame Rate Control

Format	Resolution	Max. Frame Rate	Methodology	10-bit output MIPI data rate	DVP clock frequency
1080P	1920x1080	30fps	full resolution Qualified pixel (8+1920+8)x(8+1080+8)	2 lane@420Mbps/lane 10-bit MIPI	84MHz
binning	960x540	60fps	2x2binning Qualified pixel (4+960+4)x(4+540+4)	2 lane@200Mbps/lane 10-bit MIPI	40MHz
720P	1280x720	60fps	Crop from full resolution	2 lane@375Mbps/lane 10-bit MIPI	75MHz
VGA	640x480	60fps	Crop and binning	2 lane@200Mbps/lane 10-bit MIPI	40MHz

Auto Black Level Calibration

The SP2305-2A black level calibration function compensates for dark current to ensure constant output black level regardless of change in exposure time, gain and temperature.

Defect pixel Correction

Defect pixels will be detected and be replaced by a value calculated from the neighbor pixel during the Bad Pixel Correction unit.

A defect pixel is a pixel which is black, and is not charged when light hits it, a zero value is read. Such bad pixels will be detected and corrected.

Gain

Digital gain can be controlled by DG_Gr, DG_Gb, DG_R, DG_B.Each digital gain can be configured from a gain of 0 to 2. The format of each digital gain register is “x.yyyyyyy”, where “x” refers an integer gain of 0 to 1 and “yyyyyyy” is a fractional gain ranging from 0/128 to 1/128.

Analog gain can be obtained by adjusting the ramp’s slope, using pga_gain_ctl, register.

Output Interface

Both MIPI and DVP data output interface are integrated inside SP2305-2A.

DVP Interface

DVP interface defines an interface between a peripheral device and a host processor. The traditional DVP interface is imbedded in SP2305-2A. As a result, SP2305-2A can be compatible with most existing mainstream platform.

MIPI Interface

MIPI Interface is a serial interface which can support high-speed, high-precision and large-array transmission. So, it plays an important role in Security Surveillance, Video Conferencing, Traffic Sign Recognition, etc. With it SP2305-2A can provide more high definition images to the applications.

MIPI inside SP2305-2A provides one single uni-directional clock lane and two data lane solutions for communication links between components inside the application device. This MIPI can support some kinds of operating mode, such as burst mode, switch mode, ULPs mode and line sync mode. Users can select appropriate mode according to the requirement.

D-PHY Function

The D-PHY converts the DVP data from CSI_TOP to serial data that are compatible with MIPI protocol. The detail time sequences are below.

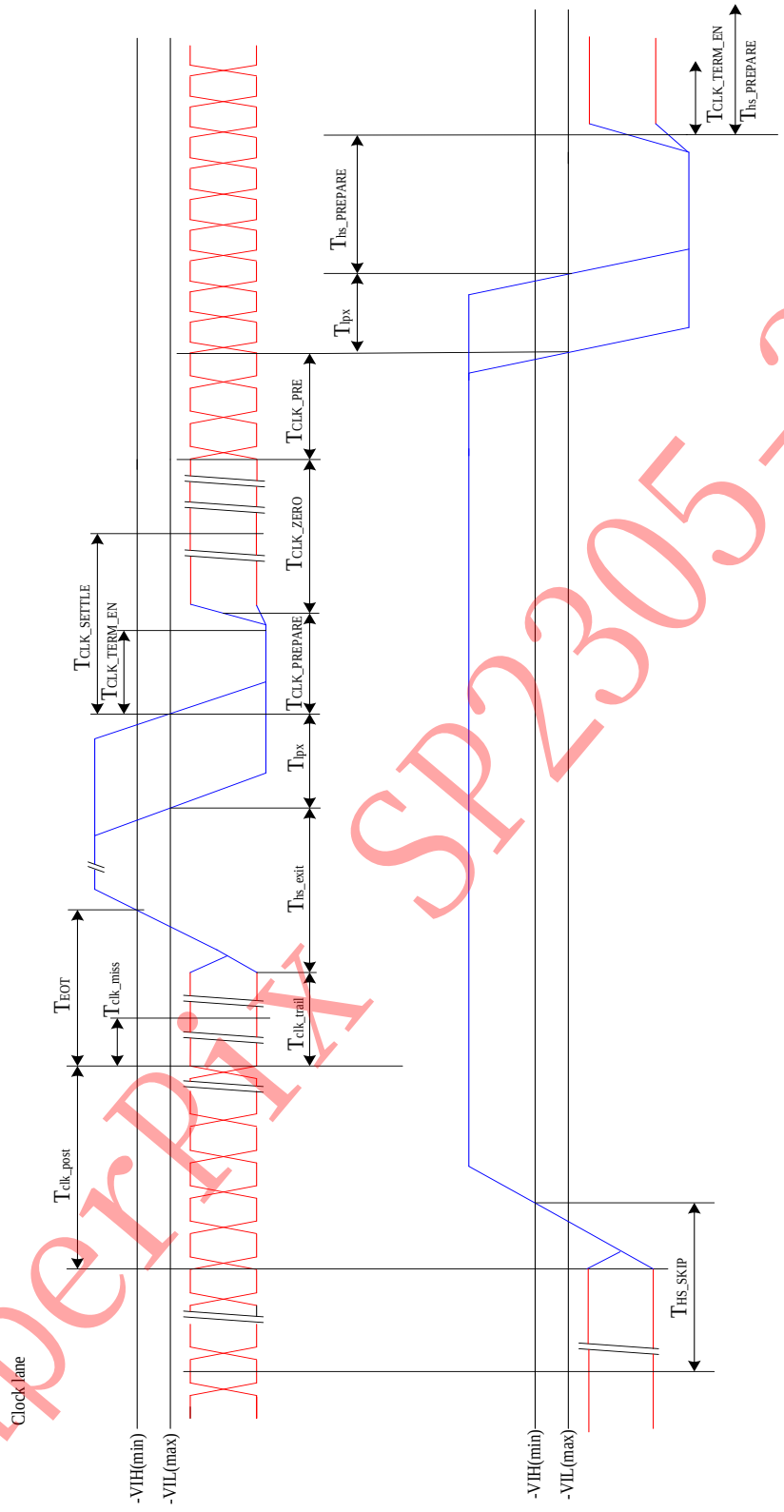


Figure 6 Switching the Clock Lane between Clock Transmission and Low-Power Mode

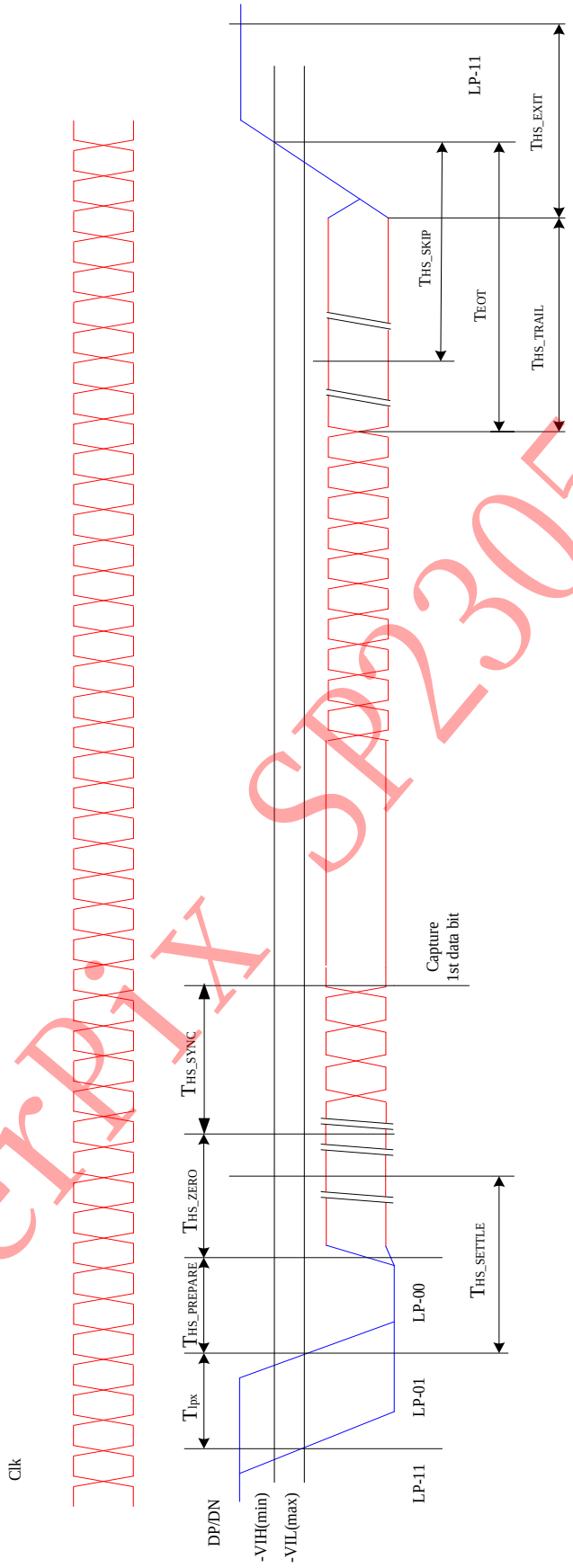


Figure 7 High-speed Data Transmission Bursts

Data Lane Parameter

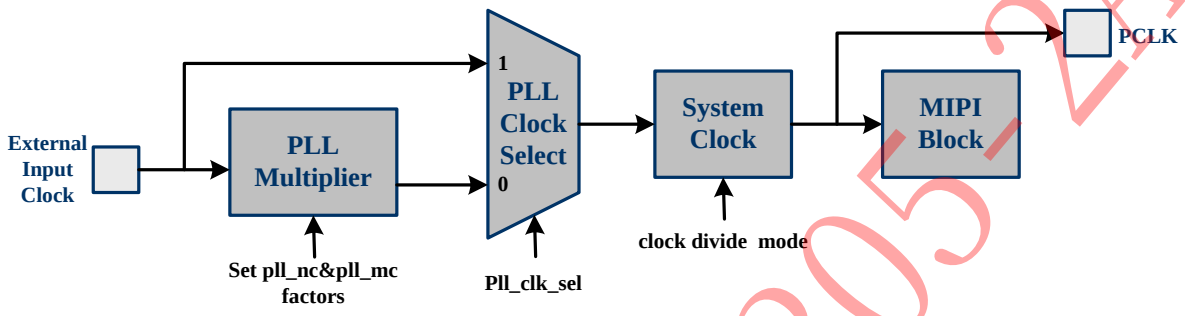
Parameter	Target	Min	Max
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	40ns+4*UI	85ns+6*UI
THS-PREPARE +THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns+10*UI	
THS-SETTLE	Time interval during which the HS receive shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE	85ns+6*UI	145ns+10*UI
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, follow a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40	55ns+4*UI
THS-TRAIL	Time that the transmitter drivers the HS-0 state after the last payload clock bit of a HS transmission burst.	Max(n*8*UI，60ns + n*4*UI)	
Tlpx	Transmitted length of any Low-Power state period	50ns	
TWAKEUP	Time that a transmitter drives a Mark-1 state prior to a stop state in order to initiate an exit from ULPS.	1ms	

Clock Lane Parameter

Parameter	Target	Min	Max
TCLK-MISS	Timeout for receive to detect absence of clock transmission and disable the clock lane HS-RX.	60ns	
TCLK-POST	Time that the transmitter continue to send HS clock after the last associated Data Lane has transitioned to LP MODE. Interval is define as the period from the end of Ths-trail to the beginning Tclk-trail.	60ns+52*UI	
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associate Data Lane beginning transition from LP to HS mode.	8*UI	
TCLK-PREPARE	Time that the transmitter driver the clock Lane LP-00 line state immediately before the HS-0 line state starting the HS transmission.	38ns	95ns
TCLK-SETTLE	Time interval during which the HS receive shall ignore any Clock Lane HS transmissions, starting from the beginning of TCLK-PREPARE	95ns	300ns
TCLK-TRAIL	Time that the transmitter driver the HS-0 state after the last payload clock bit of a HS transmission burst.	60ns	
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drivers the HS-0 state prior of starting the clock	300ns	
TEOT	Transmitted time interval from the start of TCLK-TRAIL or THS-TRAIL, to the start of the LP-11 state following a HS burst.		105ns+n*12*UI

PLL and Clock Generator

The sensor contains a Phase Locked Loop (PLL) block, which generates all the necessary internal clocks from the external clock input.
The internal function blocks of the PLL are shown below.



$$F_{out} = F_{in} * \frac{pll\_nc[4:0]+3}{pll\_mc[1:0]+1} \div 2^{pll\_outdiv[1:0]}$$

Note: $F_{in} * \frac{pll\_nc[4:0]+3}{pll\_mc[1:0]+1}$ is in the range of 120MHz to 300MHz.

I²C Bus

Single READ and Single WRITE

The SP2305-2A I²C write address and read address can be chosen by I²C ID pad. When the pad is set high, the write address is 0x7A and the read address is 0x7B, while the pad is set low, the write address is 0x78 and the read address is 0x79.

A typical READ or WRITE sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a WRITE and a '1' indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a WRITE, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

The figure shown below will illustrate SP2305-2A single READ sequence and single WRITE sequence.

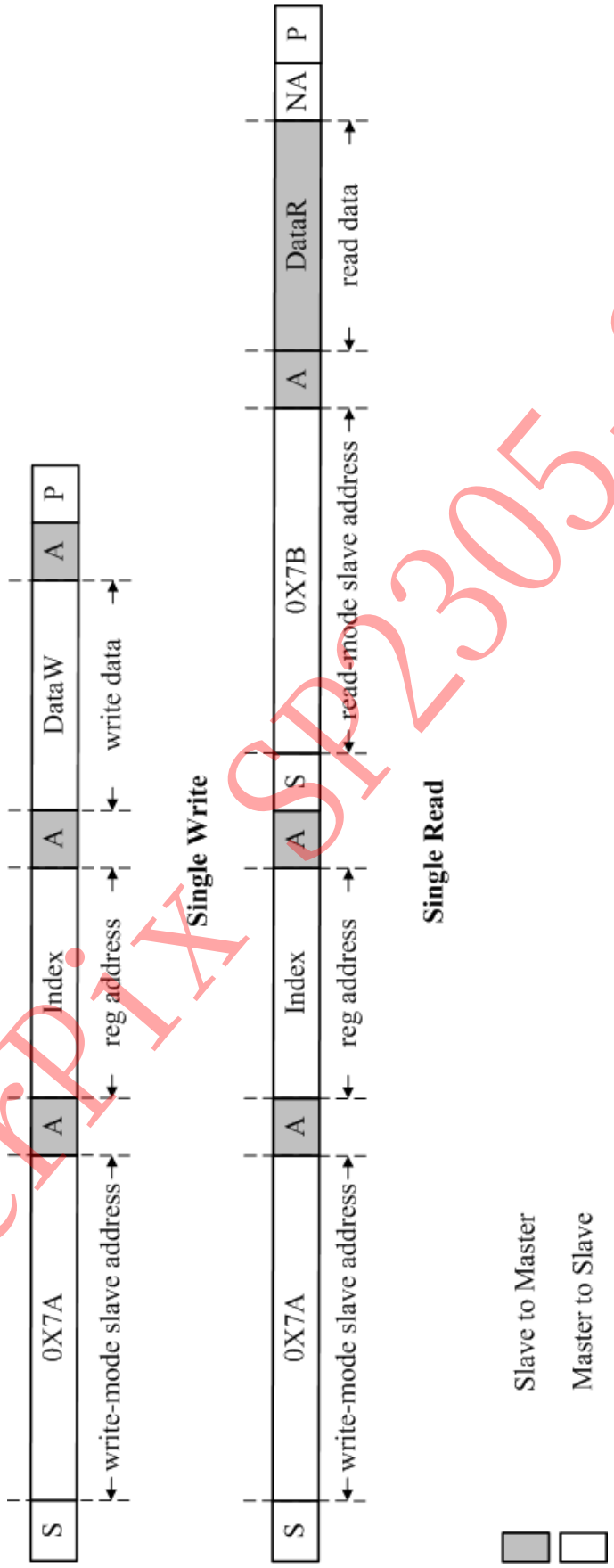


Figure 8 I²C Read & Write Message Description – I²C ID PAD set high

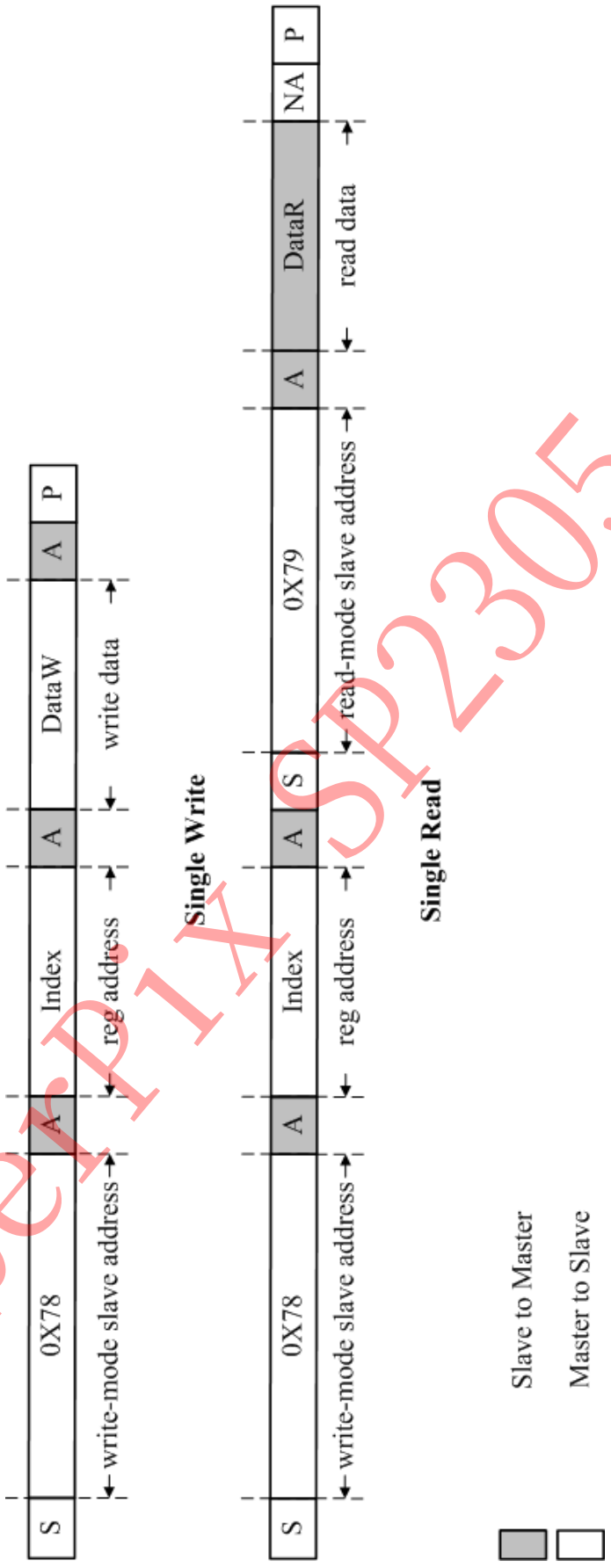


Figure 9 I²C Read & Write Message Description – I²C ID PAD set low

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock – it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The SP2305-2A will hold the value of the SBDA pin to logic ‘0’ during the logic ‘1’ state of the Acknowledge clock pulse on SBCL.

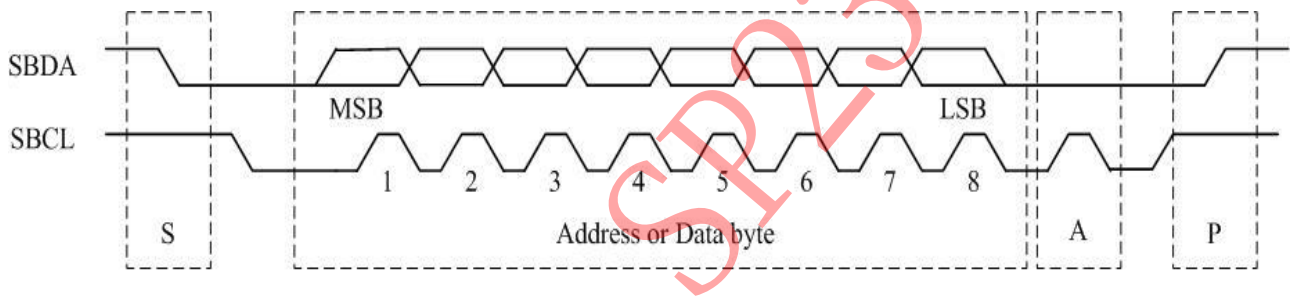


Figure 10 I²C Acknowledge Bit Description

Data Valid

The master must ensure that data is stable during the logic 1 state of the SBCL pin. All transitions on the SBDA pin can only occur when the logic level on the SBCL pin is ‘0’.

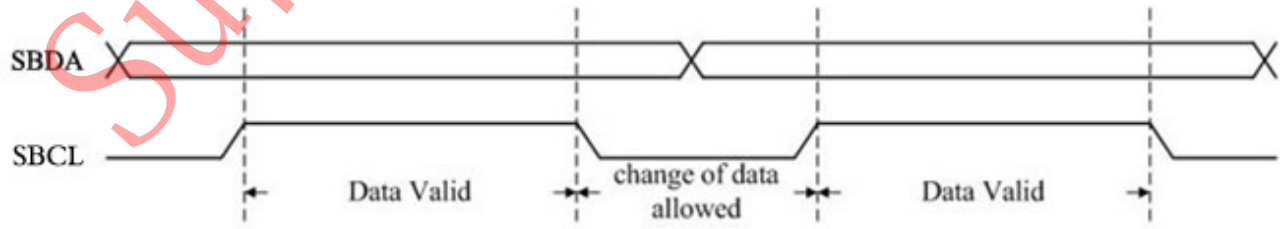


Figure 11 I²C Data Transport Description

Timing Parameter

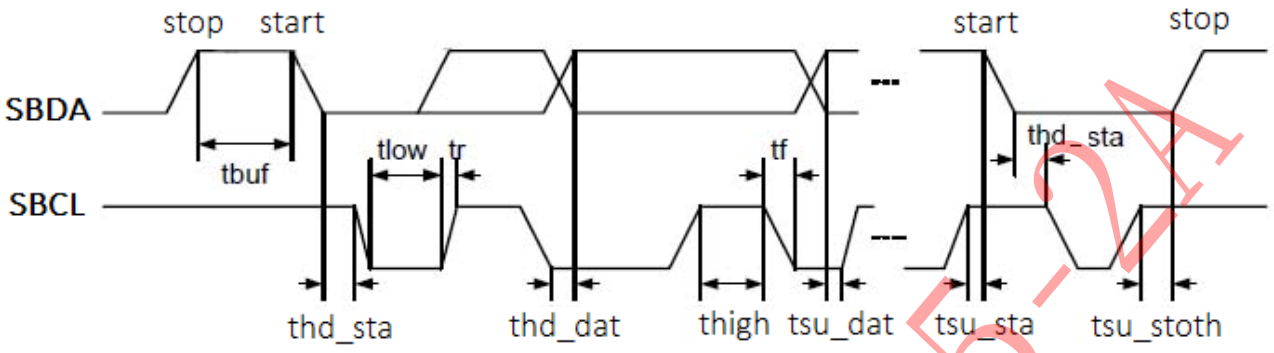


Figure 12 I²C Bus Timing Parameter Illustration

Symbol	Description	Min	Max	Unit
fscl	SBCL clock frequency	10	400	KHz
tbuf	Bus free time between a stop and a start	1.3	-	us
thd_sta	Hold time for a repeated start	0.6	-	us
tlow	LOW period of SBCL	1.3	-	us
thigh	HIGH period of SBCL	0.6	-	us
tsu_sta	Setup time for a repeated start	0.6	-	us
thd_dat	Data hold time	0	-	us
tsu_dat	Data Setup time	250	-	ns
tr	Rise time of SBCL, SBDA	-	300	ns
tf	Fall time of SBCL, SBDA	-	300	ns
tsu_sto	Setup time for a stop	0.6	-	us
Cb	Capacitive load of bus line (SBCL, SBDA)	-	-	pf

Electric Characteristics

DC Specifications

Symbol	Description	Min	Typ	Max	Unit
DOVDD	supply voltage (digital I/O)	1.7	1.8	3.0	V
		3.15	3.3	3.45	V
DVDD18	supply voltage (digital core)	1.62	1.8	1.98	V
AVDD	supply voltage (analog)	2.6	2.8	3.0	V
DOVDD	Active (operating) current		0.13	1	mA
DVDD18			40.8	55	mA
AVDD			36.5	45	mA
Digital inputs (typical conditions: DOVDD = 1.8V)					
VIL	Input voltage LOW			0.54	V
VIH	Input voltage HIGH	1.26			V
CIN	Input capacitor			10	pF
Digital outputs (standard loading 25 pF)					
VOH	Output voltage HIGH	1.62			V
VOL	Output voltage LOW			0.18	V
Serial interface inputs					
VIL[c]	SBCL and SBDA			0.54	V
VIH[c]	SBCL and SBDA	1.26			V

a. External clock is stooped during measurement

b. Standby current is based on room temperature

c. Based on DOVDD = 1.8V

Absolute Maximum Ratings

Supply Voltage (with respect to Ground)	DOVDD	4.5V
	DVDD18	3V
	AVDD	4.5V
All Input/Output Voltages (with respect to Ground)	-0.3V to DOVDD+1V	
Ambient Storage Temperature	High	125℃
	Low	-40℃
I/O current on any input or output pin	±200mA	
Peak solder temperature (10 second dwell time)	245℃	
Electro Static Discharge (ESD)	Human body model	2000V
	Machine model	200V

Note:

Exceeding the absolute maximum rating shown above can invalidate all AC and DC electrical specifications and may result in permanent device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Timing Characteristics

ymbol	parameter	Min.	Typ.	Max.	Unit
Oscillator and clock input					
f_{osc}	Frequency(MCLK)	6	24	27	MHz
t_r, t_f	Clock input rise/fall time			5	ns
	Clock input duty cycle	45	50	55	%

Power Up/Off Sequence

Power Up Sequence

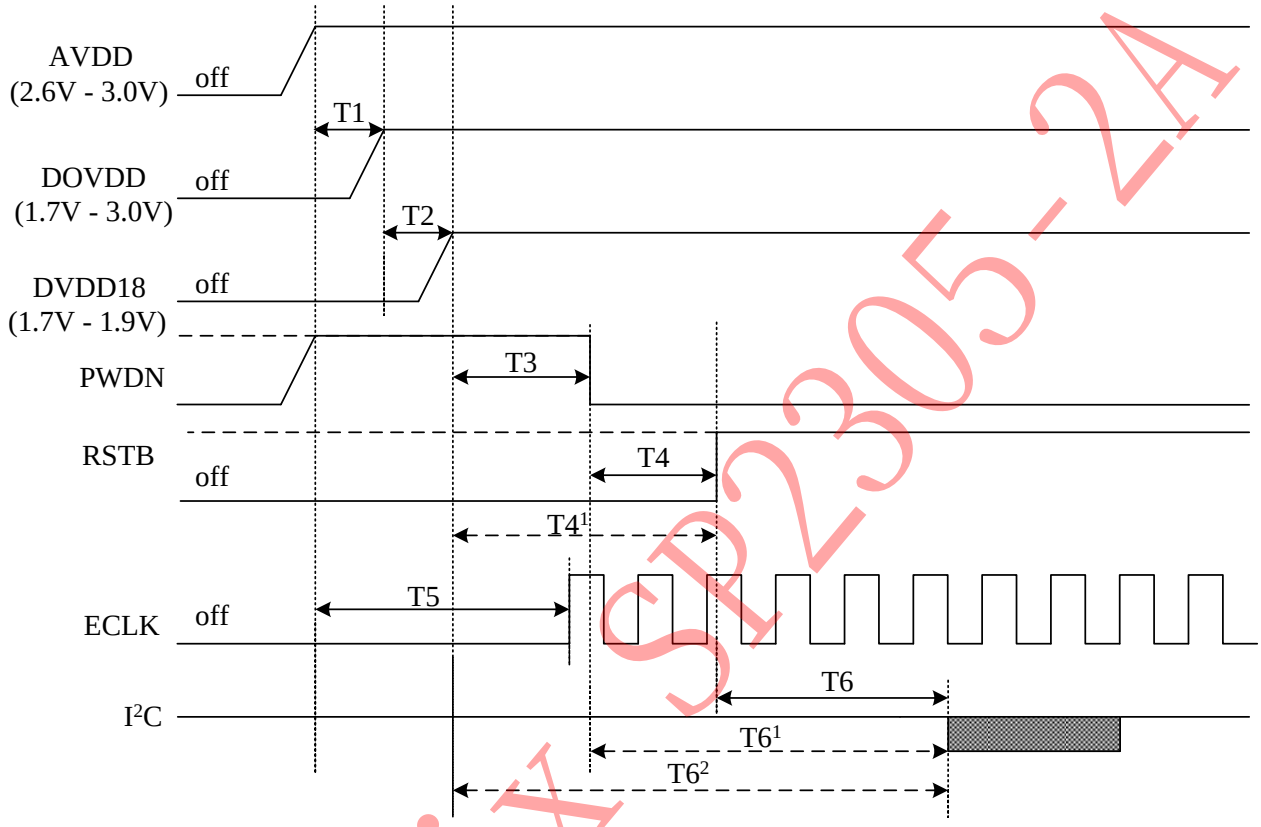


Figure 13 Power Up Sequence

Symbol	Description	Min.	Unit
T1	Delay from AVDD to DOVDD	0	ms
T2	Delay from DOVDD to DVDD18	0	ms
T3	Delay from DVDD18 stable to sensor power up stable	5	ms
T4	Delay from sensor power up stable to RSTB pull up	4	ms
$T4^1$	Attention-1：PWDN signal remains low at any time $T4^1$=T3+T4，$T4^1$ start at DVDD18 power up stable	9	ms
T5	Delay from AVDD stable to MCLK on	0	ms
T6	Delay from sensor power up stable to I2C initialization	5	ms
$T6^1$	Attention-2：RSTB signal remains high at any time $T6^1$=T4+T6，$T6^1$ start at sensor power up stable	9	ms
$T6^2$	Attention-3：PWDN=0 & RSTB=1 $T6^2$=T3+T4+T6，$T6^2$ starts at DVDD18 power up stable	14	ms

Power Off Sequence

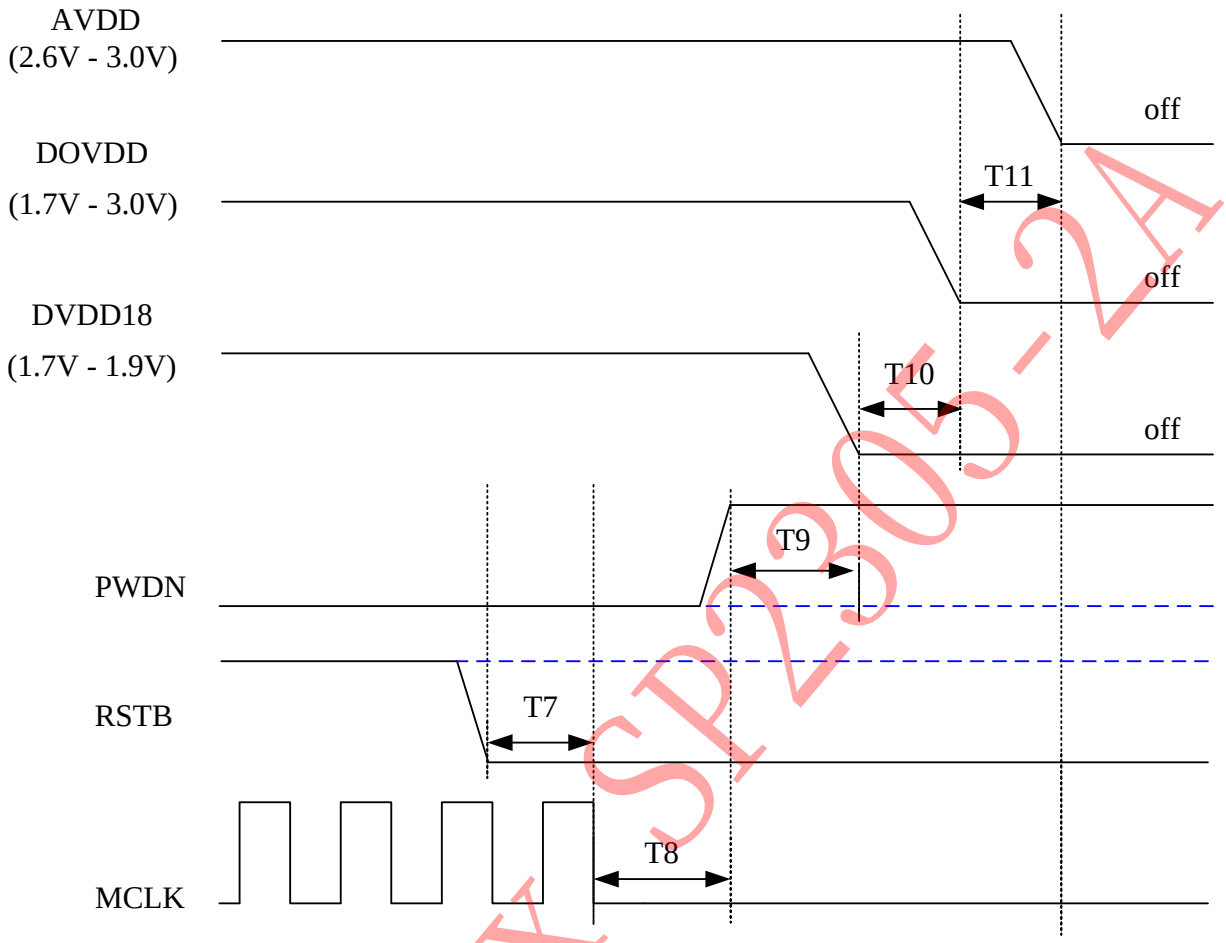


Figure 14 Power Off Sequence

Symbol	Description	Min.	Unit
T7	Delay from RSTB pull low stable to MCLK off	0	ms
T8	Delay from MCLK off to sensor power down	0	ms
T9	Delay from sensor power down to DVDD18 off	0	ms
T10	Delay from DVDD18 off to DOVDD off	0	ms
T11	Delay from DOVDD off to AVDD off	0	ms

Chief Ray Angle

Pixel Array Information

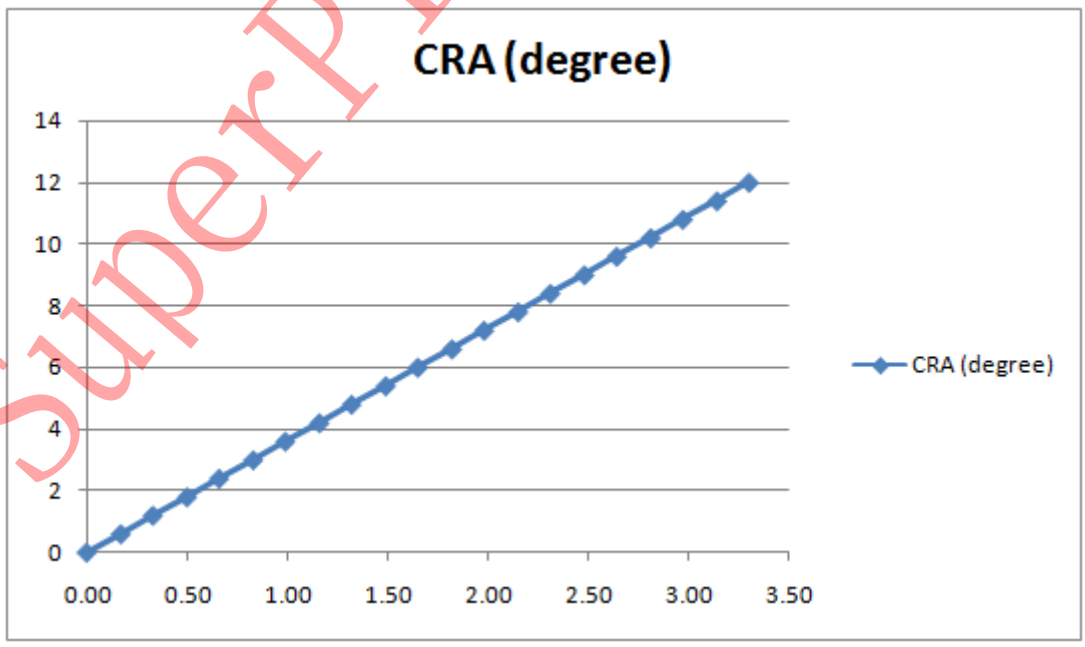
Unit Pixel Size: 3.0μm

		Value
Active pixel array	X-axis	1920
	Y-axis	1080
RIC(mm)	X-axis edge	2.880
	Y-axis edge	1.620
	Diagonal edge	3.304

RIC: Radius from the Image Center

CRA Information

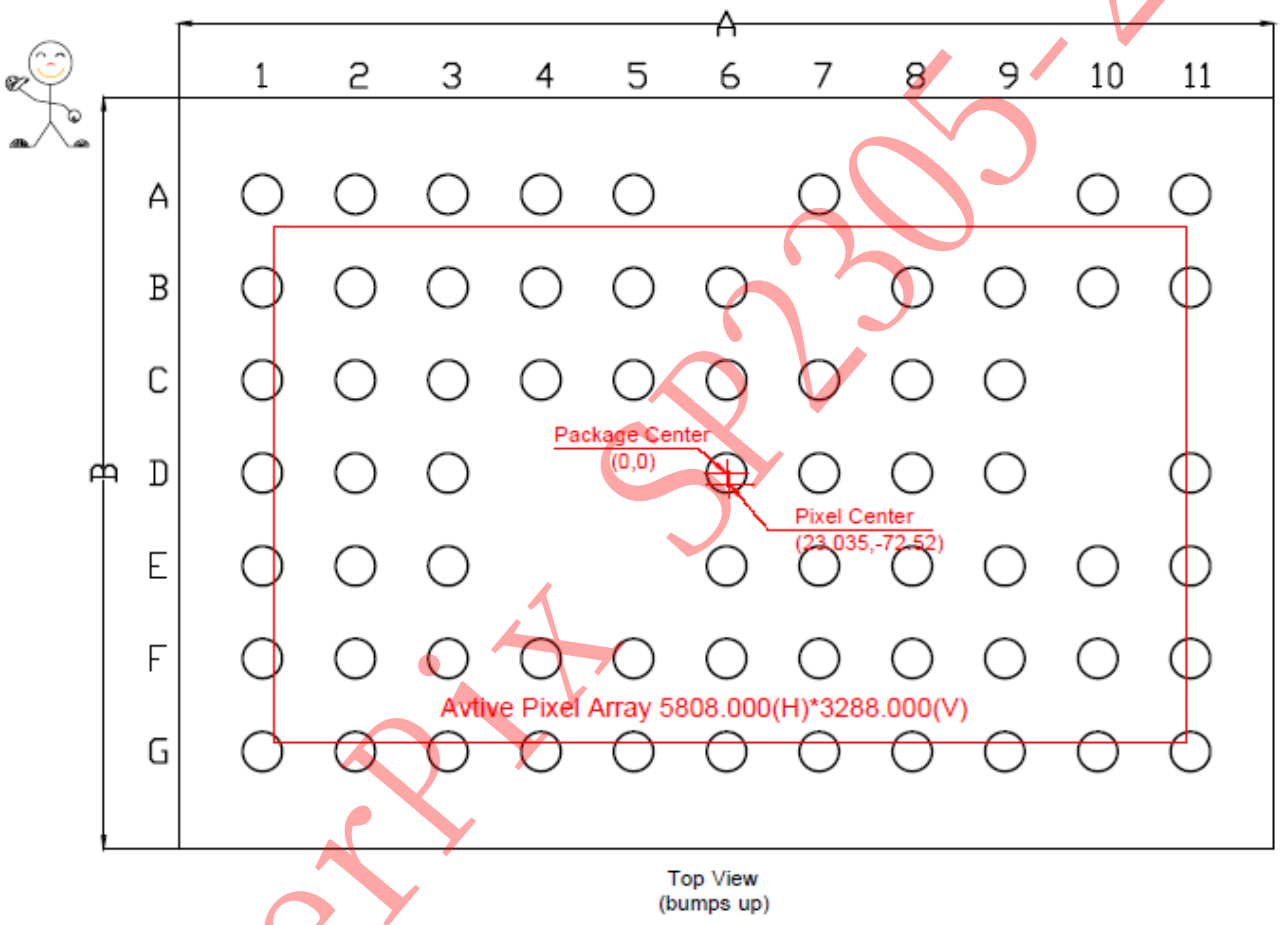
Field (%)	Image height (mm)	CRA (degree)
0%	0.00	0
5%	0.17	0.6
10%	0.33	1.2
15%	0.50	1.8
20%	0.66	2.4
25%	0.83	3
30%	0.99	3.6
35%	1.16	4.2
40%	1.32	4.8
45%	1.49	5.4
50%	1.65	6
55%	1.82	6.6
60%	1.98	7.2
65%	2.15	7.8
70%	2.31	8.4
75%	2.48	9
80%	2.64	9.6
85%	2.81	10.2
90%	2.97	10.8
95%	3.14	11.4
100%	3.30	12



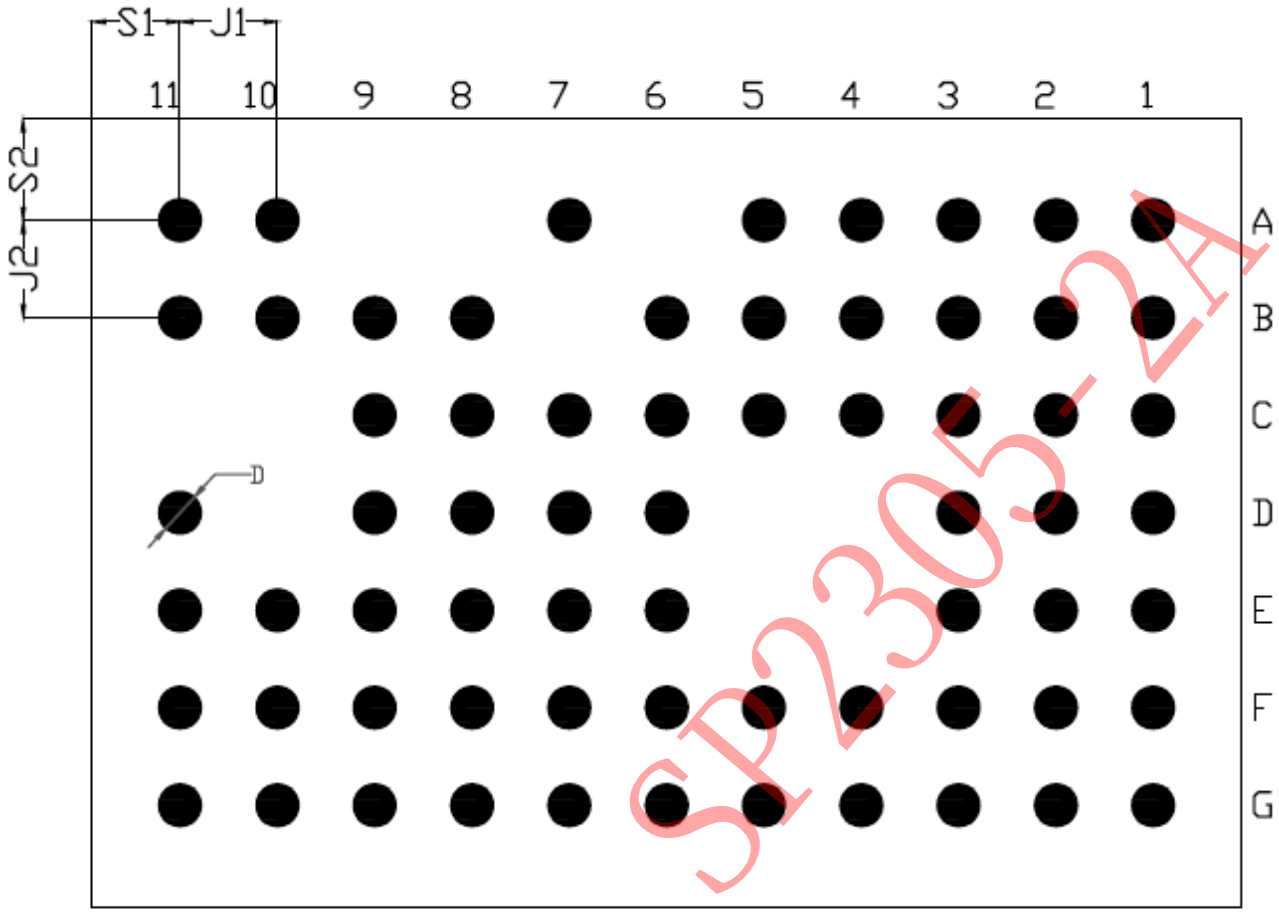
Package Information

Package Dimension

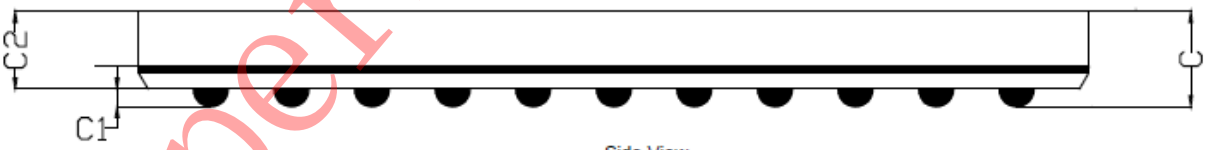
Unit: um



Top View
(bumps up)



Bottom View
(bumps up)



Side View

Table 2 Package Information

Package Dimensions	Symbol	Nominal	Min.	Max.	Unit
Package Body Dimension X	A	6961	6936	6986	μm
Package Body Dimension Y	B	4760	4735	4785	μm
Package Height	C	731	671	791	μm
Ball Height	C1	120	90	150	μm
Package Body Thickness	C2	611	576	646	μm
Ball Diameter	SΦ	230	200	260	μm
Total Pin Count	N	66	/	/	/
Pins Pitch X axis	J1	590	/	/	μm
Pins Pitch Y axis	J2	590	/	/	μm
Edge to Pin Center Distance along X	S1	525.5	495.5	555.5	μm
Edge to Pin Center Distance along Y	S2	610	580	640	μm

Table 3 Package Dimensions

	1	2	3	4	5	6
A	NC	DGND	EVSYNC	VSYNC	HSYNC	/
B	DVDDIO	DVDD18	D3	DVDDIO	D0	D1
C	AVDD	AVDD	DGND	DGND	DVDD18	DVDDIO
D	PUMN	AGND	DGND	/	/	DGND
E	AGND	AGND	DGND	/	/	DGND
F	AVDD	DGND	AVDD	DGND	DGND	DGND
G	NC	AGND	AGND	DVDD12	AGND	AGND
	7	8	9	10	11	
A	D2	/	/	D5/MDP1	NC	
B	/	D6/MDP0	D8/MCP	D4/MDN1	MCLK	
C	PCLK	D7/MDN0	D9/MCN	/	/	
D	DVDD18	PWDN	RST	/	I2CID	
E	DVDDIO	SBCL	SBDA	TEST	VPIX	
F	DGND	STROBE	DGND	AVDD	AGND	
G	AGND	AGND	AGND	AVDD	NC	

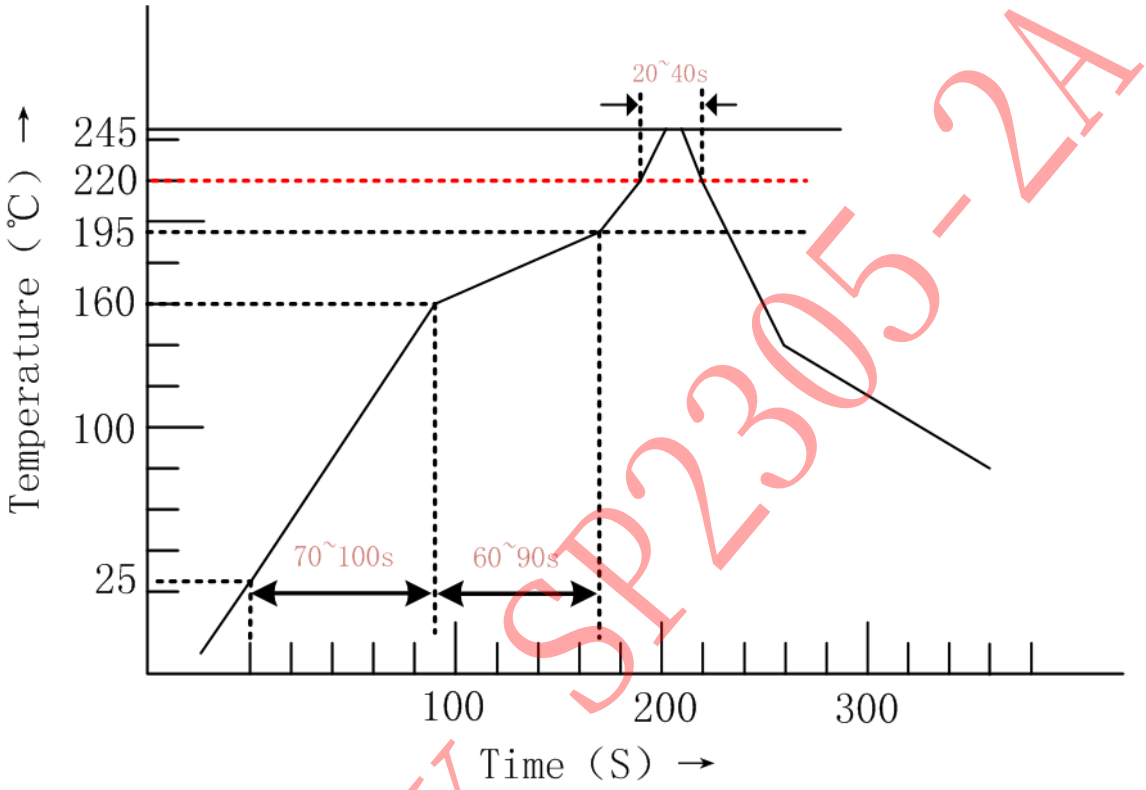
Table 4 Ball Information

PIN No.	PIN Name	I/O	Description
A1	NC	/	/
A2	DGND	DG	Digital Ground
A3	EVSYNC	I	External Vertical Sync Signal
A4	VSYNC	O	Vertical Sync Signal
A5	HSYNC	O	Horizontal Sync Signal
A7	D2	O	Data [2] output
A10	D5/MDP1	O	DATA[5] and MIPI OUTP1 output
A11	NC	/	/
B1	DVDDIO	DP	Digital Power 1.8V/2.8V
B2	DVDD18	DP	Digital Power 1.8V
B3	D3	O	Data[3] output
B4	DVDDIO	DP	Digital Power 1.8V/2.8V
B5	D0	O	Data[0] output
B6	D1	O	Data[1] output
B8	D6/MDP0	O	DATA[6] and MIPI OUTP0 output
B9	D8/MCP	O	DATA[8] and MIPI CLKP output
B10	D4/MDN1	O	DATA[4] and MIPI OUTN1 output
B11	MCLK	I	External clock input
C1	AVDD	AP	Analog Power 2.8V
C2	AVDD	AP	Analog Power 2.8V
C3	DGND	DG	Digital Ground
C4	DGND	DG	Digital Ground
C5	DVDD18	DP	Power for digital core circuit
C6	DVDDIO	DP	Digital Power 1.8V/2.8V
C7	PCLK	O	Pixel Output Clock
C8	D7/MDN0	O	DATA[7] and MIPI OUTN0 output
C9	D9/MCN	O	DATA[9] and MIPI CLKN output
D1	PUMN	/	/
D2	AGND	AG	Analog Ground
D3	DGND	DG	Digital Ground
D6	DGND	DG	Digital Ground
D7	DVDD18	DP	Digital Power 1.8V
D8	PWDN	I	"1" enable, "0" normal work
D9	RST	I	"0" enable, "1" normal work
D11	I2CID	I	I2C ID control
E1	AGND	AG	Analog Ground
E2	AGND	AG	Analog Ground
E3	DGND	DG	Digital Ground
E6	DGND	DG	Digital Ground
E7	DVDDIO	DP	Digital Power 1.8V/2.8V

PIN No.	PIN Name	I/O	Description
E8	SBCL	I	Slave I2C clk
E9	SBDA	I/O	Slave I2C Data
E10	TEST	Reference	Test pin
E11	VPIX	Reference	Pixel LDO OUTPUT, External Connect capacitance(1uF)
F1	AVDD	AP	Analog Power 2.8V
F2	DGND	DG	Digital Ground
F3	AVDD	AP	Analog Power 2.8V
F4	DGND	DG	Digital Ground
F5	DGND	DG	Digital Ground
F6	DGND	DG	Digital Ground
F7	DGND	DG	Digital Ground
F8	STROBE	O	Strobe output
F9	DGND	DG	Digital Ground
F10	AVDD	AP	Analog Power 2.8V
F11	AGND	AG	Analog Ground
G1	NC	/	/
G2	AGND	AG	Analog Ground
G3	AGND	AG	Analog Ground
G4	DVDD12	Reference	Internal analog reference
G5	AGND	AG	Analog Ground
G6	AGND	AG	Analog Ground
G7	AGND	AG	Analog Ground
G8	AGND	AG	Analog Ground
G9	AGND	AG	Analog Ground
G10	AVDD	AP	Analog Power 2.8V
G11	NC	/	/

Table 5 PIN Description

IR reflow specifications



Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Ts max To Tp)	2℃/second
Preheat -Temperature Min(Ts min) -Temperature Min(Ts max) -Time(Ts min to Ts max)	 160℃ 195℃ 60-90 seconds
Time maintained above: -Temperature (TL) -Time (TL)	 220℃ 20-40 seconds
Peak/Classification Temperature(Tp)	225-245℃
Ramp-Down Rate	- 4℃/second max
Time 25℃ to peak Temperature	3.5 minutes max

Table 6 IR Reflow

Registers

System Register

Address	Register name	Bits	Description	Default
Clock register				
P0:0x2f	pll_ctrl_buf	7~0	[7]: pll_clk_sel 0 – disable bypass PLL 1 – enable bypass PLL [6:2]: pll_nc [1:0]: pll_mc PLL output =[PLL input/(pll_mc+1)]*[(pll_nc+3)/(pll_outdiv+1)] The parameters of the registers will be enabled in next frame.	0x10
P0:0x30	clk_mode_buf	7~0	[6:4]: pclk_ctrl 000 – pclk = pll_clk 001 – pclk = pll_clk/2 010 – pclk = pll_clk/4 011 – pclk = pll_clk/6 100 – pclk = pll_clk/8 101 – pclk = pll_clk/12 [7]: pclk_gate_en [3:2]: clk_pcp_ctrl 00 – clk_pcp = pll_clk/2 01 – clk_pcp = pll_clk/6 10 – clk_pcp = pll_clk/8 11 – clk_pcp = eclk [1:0]: clk_ncp_ctrl 00 – clk_ncp = pll_clk/2 01 – clk_ncp = pll_clk/6 10 – clk_ncp = pll_clk/8 11 – clk_ncp = eclk The parameters of the registers will be enabled in next frame.	0x0f
P0:0x33	dac_clk_gating_en_buf, dac_clk_mode_buf, cis_clk_mode_buf	5~0	[3]: dac_clk_gating_en_buf 1 – enable dac_clk gating 0 – disable dac_clk gating [2:1]: dac_clk_mode_buf, 00 – dac_clk = pll_clk/2 01 – dac_clk = pll_clk/4 10 – dac_clk = pll_clk/6	0x01

<table>
<tr><td></td><td></td><td></td><td>11 – dac_clk = pll_clk/8
[0]: cis_clk_mode_buf
0 – timer_clk = pclk_pre
1 – timer_clk = pclk_pre/2
The parameters of the registers will be enabled in next frame.</td><td></td></tr>
<tr><td>P0:0x34</td><td>buf_pll_outdiv</td><td>1~0</td><td>Pll frequency divider control
PLL output =[PLL input/(pll_mc+1)]*[(pll_nc+3)/(pll_outdiv+1)]
The parameters of the registers will be enabled in next frame.</td><td>0x01</td></tr>
<tr><td>P0:0x35</td><td>pll_bias_ctl,
pll_dctl,</td><td>6~0</td><td>[6:5]: pll_bias_ctl
PLL chargepump current control
<table><tr><td>pll_bias_ctl</td><td>Current</td></tr><tr><td>00</td><td>10u</td></tr><tr><td>01(default)</td><td>20u</td></tr><tr><td>10</td><td>30u</td></tr><tr><td>11</td><td>40u</td></tr></table>[4:3] pll_dctl
Choose PLL’s PFD delay time to remove dead zone.
<table><tr><td>_pll_dctl<1:0></td><td>delay(s)</td></tr><tr><td>00(default)</td><td>478p</td></tr><tr><td>01</td><td>932p</td></tr><tr><td>10</td><td>1.334n</td></tr><tr><td>11</td><td>1.736n</td></tr></table></td><td>0x00</td></tr>
<tr><td>P0:0x39</td><td>buf_pclk_inv</td><td>0</td><td>buf_pclk_inv
PAD PCLK reverse enable signal
1 – enable PCLK reverse
0 – disable PCLK reverse
The parameters of the registers will be enabled in next frame.</td><td>0x01</td></tr>
<tr><td colspan="5">Soft reset register</td></tr>
<tr><td>P0:0x20</td><td>soft_rst</td><td>0</td><td>soft_rst
soft reset signal
1 – disable soft reset
0 – enable soft reset
The register cannot be self clear.</td><td>0x01</td></tr>
<tr><td colspan="5">Power down register</td></tr>
<tr><td>P0:0x36</td><td>pwd_pll</td><td>0</td><td>pwd_pll
The power down control of PLL.
1 – enable power down of PLL
0 – disable power down of PLL</td><td>0x00</td></tr>
</table>

P0:0x37	pwd_asp	0	pwd_asp The power down control of ASP 1 – enable power down of ASP 0 – disable power down of ASP	0x00
Parallel port register				
P0:0x1b	evsync_oe_buf strobe_oe_buf out_end_buf out_ens_buf out_enp_buf	4~0	[4]: evsync_oe_buf PAD evsync output enable signal 1 – disable output 0 – enable output [3]: strobe_oe_buf PAD strobe output enable signal 1 – disable output 0 – enable output [2]: out_end_buf PAD dataout[9:0] output enable signal 1 – disable output 0 – enable output [1]: out_ens_buf PAD VSYNC and HSYNC output enable signal 1 – disable output 0 – enable output [0]: out_enp_buf PAD PCLK output enable signal 1 – disable output 0 – enable output The parameters of the registers will be enabled in next frame.	0x1f
P0:0x1d	ds_data ds_pclk ds_hsync ds_vsync	7~0	[7:6]: ds_data The driver current select signal of PAD dataout[9:0]. [5:4]: ds_pclk The driver current select signal of PAD PCLK. [3:2]: ds_hsync The driver current select signal of PAD HSYNC. [1:0]: ds_vsync The driver current select signal of PAD VSYNC.	0x55
P0:0x1f	evsync_ie	0	[0]: evsync_ie PAD evsync input enable signal 1 – enable input 0 – disable input	0x00
P0:0x40	ext_sync_mst_en, ext_sync_en	1~0	[1]: ext_sync_mst_en Enable master mode of external sync function.	0x00

			1 – SP2305-2A is master of external sync 0 – SP2305-2A is slave of external sync [0]: ext_sync_en Enable signal of external sync function 1 – enable external sync 0 – disable external sync	
I2C register				
P0:0x50	i2c_dev_addr_en	0	i2c_dev_addr_en i2c_dev_addr enable signal 1 – enable i2c_dev_addr 0 – disable i2c_dev_addr	0x00
P0:0x51	i2c_dev_addr	6~0	i2c_dev_addr manual I2C device address	0x3d
Other register				
P0:0x02	chip_id	7~0	chip_id (read only)	0x27
P0:0x03	chip_id	7~0	chip_id(read only)	0x35
P0:0xfd	Page_flg	2~0	[2:0]: Page_flg Page number	0x00

Sensor Register

Address	Register name	Bits	Description	Default
resolution & exposure & analog gain				
P1:0x01	exp_rpc_en	0	Enable of Frame sync signal 1 – enable 0 – disable	0x00
P1:0x03	buf_exp_8msb	7~0	Exposure time in the "H" unit. 1~65535(0x0001~0xffff)	0x01
P1:0x04	buf_exp_8lsb	7~0		0x86
P1:0x23	rpc	7~0	Pga gain control(read only) low 8bits, corresponding to the register P1:0x24.	0x20
P1:0x24	pga_gain_ctl[7:0]	7~0	Pga gain manual control, low 8bits. The entire pga gain control is P1:{0x38[0],0x24} (1X~31X,0x000~0x1ff)	0x20
P1:0x31	bypass_dsp v_sub_en v_binning_en mode_vga mode_720p	4~0	Resolution selection. 0x00 – 1936x1096 0x01 – 1288x728 0x02 – 648x488 0x04 – 968x548 0x08 – 968x548 0x10 – 2004x1104	0x00
P1:0x38	rpc[8] pga_gain_msb8	4~0	[4]: Pga gain control (read only) high 1bit, corresponding to the register P1:0x38[0]. [0]: pga_gain_msb8 pga gain control, high 1bit	0x00
P1:0x3d	exp_short_ctl	4~0	Short exp time control in binning mode [4]: long exp/short exp timing reverse enable 1 – enable 0 – disable [3:0]: ratio of long exp and short exp. 0000 – exp_short = exp_time 0001 – exp_short = exp_time/2 0010 – exp_short = exp_time/4 0011 – exp_short = exp_time/8 0100 – exp_short = exp_time/16 0101 – exp_short = exp_time/32 0110 – exp_short = exp_time/64 0111 – exp_short = exp_time/128	0x00

			1000 – exp_short = exp_time/256	
P1:0x3f	updown mirror	1~0	[1]: vertical upside down [0]: horizontal mirror 0x00 – normal(no flip) 0x01 – horizontal flip 0x02 – vertical flip 0x03 – both horizontal and vertical flip	0x00
P1:0xe8	rpc_tmp1	7~0	Pga gain control, low 8bits(read only) Earlier one frame to take effect than the register of P1:0x23	readonly
Digital gain				
P1:0x39	dig_gain_buf	7~0	Global digital gain(1X~2X) 0x80 equals to 1X 0xff equals to 2X Accuracy is 1/128.	0x80
P1:0x40	r_gain_buf	7~0	Digital gain,red channel(1~2X) 0x80 equals to 1X 0xff equals to 2X Accuracy is 1/128	0x80
P1:0x41	gr_gain_buf	7~0	Digital gain,gr channel(1~2X) 0x80 equals to 1X 0xff equals to 2X Accuracy is 1/128	0x80
P1:0x42	gb_gain_buf	7~0	Digital gain,gb channel(1~2X) 0x80 equals to 1X 0xff equals to 2X Accuracy is 1/128	0x80
P1:0x43	b_gain_buf	7~0	Digital gain,blue channel(1~2X) 0x80 equals to 1X 0xff equals to 2X Accuracy is 1/128	0x80
Frame_length & row_length				
P1:0x05	vblank_buf_8msb	7~0	Vertical blank in the “H” unit. 0~65535(0x0000~0xffff)	0x00
P1:0x06	vblank_buf_8lsb	7~0		0x00
P1:0x08	vpos_blank	3~0	Time width between posedge of vsync and posedge of the first hsync, in the “H”unit.	0x01
P1:0x09	hblank_4msb	3~0	Horizontal blank in the “timer_clk” unit.0~4095(0x000~0xfff)	0x00

P1:0x0a	hblank_8lsb	7~0		0x00
P1:0x0d	frame_exp_seperate_en	4	[4]: Frame_exp_seperate_en When enabled,the frame length equals to the value of register P1:{0x0e,0x0f} 1 – enable 0 – disable	0x00
P1:0x0e	frame_length_num_8msb	7~0	Frame length for manual frame length setting, used with P1:0x0d[4] enabled.	0x04
P1:0x0f	frame_length_num_8msb	7~0		0x50
P1:0x28	ana_v_dummy_size	7~0	Specify the vertical row number upward and downward of the active readout area, respectively for 720P and VGA mode.	0x08
P1:0x3a	vdelay_buf_8msb	7~0	Vertical blank,in the “H” unit.	0x00
P1:0x3b	vdelay_buf_8lsb	7~0		0x00
P1:0x4e	frame_length_readonly_8msb	7~0	Frame length, in the “H” unit. (Read only)	0x00
P1:0x4f	frame_length_readonly_8lsb	7~0		0x00
P1:0x8c	hs_period_num_5msb	4~0	Row length, in the “timer_clk” unit. (Read only)	0x00
P1:0x8d	hs_period_num_8lsb	7~0		0x00
BLC				
P1:0x86	blc_gain_blue	7~0	Blc_gain for blue channel(1X~2X) Accuracy is 1/128	0x80
P1:0x87	blc_gain_red	7~0	Blc_gain for red channel(1X~2X) Accuracy is 1/128	0x80
P1:0x88	blc_gain_gr	7~0	Blc_gain for gr channel(1X~2X) Accuracy is 1/128	0x80
P1:0x89	blc_gain_gb	7~0	Blc_gain for gb channel(1X~2X) Accuracy is 1/128	0x80
P1:0xe0	black_level_br_msb	7~0	[6:4]: Black level calibration value, b 3msb [2:0]: Black level calibration value, r 3msb	Read only
P1:0xe1	black_level_gb_8lsb	7~0	Black level calibration value, gb 8lsb	Read only
P1:0xe2	black_level_b_8lsb	7~0	Black level calibration value, b 8lsb	Read only

P1:0xe3	black_level_r_8lsb	7~0	Black level calibration value, r 8lsb	Read only
P1:0xe4	black_level_gr_8lsb	7~0	Black level calibration value, gr 8lsb	Read only
P1:0xe5	black_level_g_msb	7~0	[6:4]: Black level calibration value, gb 3msb [2:0]: Black level calibration value, gr 3msb	Read only
P1:0xf0	gb_suboffset[7:0]	7~0	Blacklevel offset,gb channel,low 8bits The total register is 9bits with msb P1:0xf8[7]. (-256~255,0x100~0x0ff) The highest bit is the sign bit.	0x00
P1:0xf1	blue_suboffset[7:0]	7~0	Blacklevel offset,blue channel,low 8bits The total register is 9bits with msb P1:0xf8[6]. (-256~255,0x100~0x0ff) The highest bit is the sign bit.	0x00
P1:0xf2	red_suboffset[7:0]	7~0	Blacklevel offset,red channel,low 8bits The total register is 9bits with msb P1:0xf8[5]. (-256~255,0x100~0x0ff) The highest bit is the sign bit.	0x00
P1:0xf3	gr_suboffset[7:0]	7~0	Blacklevel offset,gr channel,low 8bits The total register is 9bits with msb P1:0xf8[4]. (-256~255,0x100~0x0ff) The highest bit is the sign bit.	0x00
P1:0xf4	shift_gb	7~0	Blacklevel shift,gb channel (0~255,0x00~0xff)	0x00
P1:0xf5	shift_blue	7~0	Blacklevel shift,blue channel (0~255,0x00~0xff)	0x00
P1:0xf6	shift_red	7~0	Blacklevel shift,red channel (0~255,0x00~0xff)	0x00
P1:0xf7	shift_gr	7~0	Blacklevel shift,gr channel (0~255,0x00~0xff)	0x00
P1:0xf8	gb_suboffset[8], blue_suboffset[8], red_suboffset[8], gr_suboffset[8], bl_position_set2, bl_position_set	7~0	[7]: Blacklevel offset, gb channel, high 1bit,which is the sign bit. [6]: Blacklevel offset,blue channel, high 1bit.which is the sign bit. [5]: Blacklevel offset,red channel, high 1bit,which is the sign bit. [4]: Blacklevel offset, gr channel, high 1bit,which is the sign bit. [3:2]: bl_position_set2 Black level position control for calibration. [1:0]: bl_position_set Black level position control for statistic.	0x00
P1:0xf9	blc_bpc_in_p_8lsb	7~0	Blacklevel positive data for bad pixel replacement , encoded in absolute value	0x20

P1:0xfa	blc_bpc_in_n_8lsb	7~0	Blacklevel negtive data for bad pixel replacement , encoded in absolute value	0x20
P1:0xfb	abl	7~0	[7]: blc_test_en 1 – High 10bits output mode 0 – Low 10bits output mode [6]: blc_filter_en 1 – Dark row median filter enable 0 – Dark row median filter disable [5]: blc_gain_en 1 – Blacklevel gain expansion enable 0 – Blacklevel gain expansion disable [4]: blc_bpc_en 1 – Dark row bpc enable 0 – Dark row bpc disable [2:1]: blc_mode 00 – 1 frame average mode 01 – 4 frames average mode 10 – 8 frames average mode 11 – 1 frame average mode [0]: blc_en 1 – Blacklevel enable 0 – Blacklevel disable	0x00
P1:0xfc	blc_bpc_th_p_8lsb	7~0	Blacklevel positive threshold for bad pixel , encoded in absolute value	0x40
P1:0xfe	blc_bpc_th_n_8lsb	7~0	Blacklevel negtive threshold for bad pixel , encoded in absolute value	0x40
RWN				
P1:0xc0	rwn_ctl	3~0	Row-wise noise reduction control [3]: rwn_darkrow_en Control the rwn function of dark rows to be on/off. 1 – on 0 – off [2]: rwn_mode 1 – single channel statistics 0 – double channel statistics [1]: rwn_bpc_en Control the rwn bpc function to be on/off 1 – on 0 – off [0]: rwn_en Control the total rwn function to be on/off. 1 – on	0x00

			0 – off	
P1:0xc1	rwn_bpc_th_p_1msb	0	Rwn bpc positive threshold, encoded in absolute value	0x00
P1:0xc2	rwn_bpc_th_p_8lsb	7~0		0x0c
P1:0xc3	rwn_bpc_th_n_1msb	0	Rwn bpc negative threshold, encoded in absolute value	0x00
P1:0xc4	rwn_bpc_th_n_8lsb	7~0		0x0c
P1:0xc5	rwn_bpc_in_p_1msb	0	Rwn bpc positive data for replacement, encoded in absolute value	0x00
P1:0xc6	rwn_bpc_in_p_8lsb	7~0		0x08
P1:0xc7	rwn_bpc_in_n_1msb	0	Rwn bpc negative data for replacement, encoded in absolute value	0x00
P1:0xc8	rwn_bpc_in_n_8lsb	7~0		0x08
Dual sensor synchronization				
P1:0x0b	exter_sync_ctl	7~0	External frame synchronize control signal [6]: exter_frame_num_x256_en When enabled, 1lsb of exter_sync_frame_num(P1:0x17) equals 256 frames 1 – enable 0 – disable [5]: exter_del_en 1 – enable 0 – disable [4]: exter_sync_manual_en Configure a pos in this bit to trigger a sync output in master mode [3]: exter_sync_auto_en Sensor in master mode will send sync signal every exter_sync_frame_num(P1:0x17) frames automatically 1 – enable 0 – disable [1]: external sync slave mode 1 – enable 0 – disable [0]: external sync master mode 1 – enable	0x00

			0 – disable	
P1:0x0c	exter_sync_out_width	7~0	Width of sync signal output when sensor is configured as master, in the “dac_clk” unit.	0x08
P1:0x17	exter_sync_frame_num	7~0	interval frame number of auto External frame synchronize pulse	0x0a
Strobe				
P1:0x27	col_bin_avg_en strobe_level	4~0	[4]: col_bin_avg_en Control the weight coefficient of digital column binning. 1 – 22 0 – 31 [0]: strobe_level Specify the fixed level of strobe signal 1 – high level 0 – low level	0x00
P1:0x34	strobe_ctrl	7~0	[7]: strobe_req [6]: strobe_inv [5:4]: xeon_width [3]: strobe_level_en [2]: led3_en [1]: led12_en [0]: xeon_en	0x00
P1:0x35	strobe_del_num	7~0	Frame number to be deleted for strobe function, in the “frame” unit.	0x00
P1:0x36	strobe_add_exp_8msb	7~0	Exposure time added for strobe led12 mode, in the “H” unit.	0x00
P1:0x37	strobe_add_exp_8lsb	7~0		0x20
Timing control				
P1:0x10	rst_num_1msb	0	Rst_num period of reset dac_code. (dac_clk unit)	0x00
P1:0x11	rst_num_8lsb	7~0		0x20
P1:0x12	sig_num_3msb	2~0	Sig_num period of signal dac_code. (dac_clk unit)	0x04
P1:0x13	sig_num_8lsb	7~0		0x00
P1:0x14	rst1_init_3msb	2~0	Rst1_init value of dac_code	0x03

P1:0x15	rst1_init_8lsb	7~0		0xff
P1:0x16	Dac_timing_sel FPN_33ms_data_en FPN_33ms_timing_sel	3~0	[3]: Dac_timing_sel Control the timing of col_bl_latch 1 – normal timing 0 – always high [2]: FPN_33ms_data_en Control the row address in vertical blank region. 1 – force the invalid address to 0 0 – force the invalid address to 2047 [1:0]: FPN_33ms_timing_sel Control the timing in vertical blank region.	0x08
P1:0x1a	image_lag_test sc0_timing_sel ref_timing_sel ncp_timing_sel pcp_timing_sel rch_set bwi_timing_sel col_en_timing_sel	7~0	[7]: image_lag_test 1 – image lat test timing 0 – normal timing [6]: sc0_timing_sel 1 – normal timing 0 – sc0 is always low [5]: ref_timing_sel 1 – normal timing 0 – ref_ctrl is always high [4]: ncp_timing_sel 1 – normal timing 0 – ncp_sw_ctrl is always high [3]: pcp_timing_sel 1 – normal timing 0 – pcp_sw_ctrl is always high [2]: rch_set 1 – rch=1 when reading the even rows,rch=0 when reading the odd rows 0 – rch=0 when reading the even rows,rch=1 when reading the odd rows [0]: bwi_timing_sel 1 – bwi1&bwi2 normal timing 0 – bwi1&bwi2 test timing [0]: col_en_timing_sel 1 – col_en normal timing 0 – col_en test timing	0x7b
P1:0x1c	blk_timing_sel nb_timing_sel vref2_timing_sel tg_blc_timing_sel vlow_timing_sel col_test_tx extra_reset_en	7~0	[7]: blk_timing_sel 1 – blk normal timing 0 – blk is always high [6]: nb_timing_sel 1 – nb_sw normal timing 0 – nb_sw is always high [5]: vref2_timing_sel	0xe8

	timing_no_wait_en		1 – vref2_sw normal timing 0 – vref2_sw is always high [4]: tg_blc_timing_sel 1 – dark row tg particular timing 0 – dark row tg normal timing [3]: vlow_timing_sel 1 – vlow_sw_ctrl normal timing 0 – vlow_sw_ctrl is always high [2]: col_test_tx 1 – tg test timing 0 – tg normal timing [1]: extra_reset_en 1 – double shutter timing 0 – normal timing [0]: timing_no_wait_en Control the timing to wait until the column counts completely. 1 – no wait 0 – wait	
P1:0x30	binning31_large binning31_en binning22_en	2~0	Control binning dac_code mode [2]: binning31_large [1]: binning31_en [0]: binning22_en	0x01
P1:0x32	rst_num2_1msb	0	rst_num2 period of reset dac_code, in the “dac_clk” unit.	0x00
P1:0x33	rst_num2_8lsb	7~0		0x30
P1:0x3c	dac_mode	1~0	Dac_code mode control. 00 – linear,no DDS 01 – speedup,no DDS 10 – linear,DDS 11 – speedup,DDS	0x03
P1:0x50	p0	7~0	p0 cycle for Pixel timing(dac_clk unit)	0x12
P1:0x51	p1	7~0	p1 cycle for Pixel timing(dac_clk unit)	0x1a
P1:0x52	p2	7~0	p2 cycle for Pixel timing(dac_clk unit)	0x20
P1:0x53	P3	7~0	P3 cycle for Pixel timing(dac_clk unit)	0x10
P1:0x55	p5	7~0	p5 cycle for Pixel timing(dac_clk unit)	0x13
P1:0x56	p6	7~0	p6 cycle for Pixel timing(dac_clk unit)	0x02

P1:0x57	P7_1msb	0	p7 cycle for Pixel timing(dac_clk unit)	0x00
P1:0x58	P7_8lsb	7~0		0x30
P1:0x59	p8	7~0	p8 cycle for Pixel timing(dac_clk unit)	0x01
P1:0x5a	p9	7~0	p9 cycle for Pixel timing(dac_clk unit)	0x02
P1:0x5b	p10	7~0	P10 cycle for Pixel timing(dac_clk unit)	0x08
P1:0x5d	p12	7~0	p12 cycle for Pixel timing(dac_clk unit)	0x15
P1:0x5e	p13	7~0	p13 cycle for Pixel timing(dac_clk unit)	0x00
P1:0x5f	p14	7~0	p14 cycle for Pixel timing(dac_clk unit)	0x00
P1:0x61	p15	7~0	p15 cycle for Pixel timing(dac_clk unit)	0x0f
P1:0x62	p16	7~0	p16 cycle for Pixel timing(dac_clk unit)	0x00
P1:0x63	p17	7~0	p17 cycle for Pixel timing(dac_clk unit)	0x02
P1:0x64	p18	7~0	p18 cycle for Pixel timing(dac_clk unit)	0x40
P1:0x65	p19	7~0	p19 cycle for Pixel timing(dac_clk unit)	0x00
P1:0x66	p20	7~0	p20 cycle for Pixel timing(dac_clk unit)	0x66
P1:0x67	p21	7~0	p21 cycle for Pixel timing(dac_clk unit)	0x00
P1:0x68	p22	7~0	p22 cycle for Pixel timing(dac_clk unit)	0x68
P1:0x69	p23	7~0	p23 cycle for Pixel timing(dac_clk unit)	0x20
P1:0x6a	p24	7~0	p24 cycle for Pixel timing(dac_clk unit)	0x34
P1:0x6b	p25	7~0	p25 cycle for Pixel timing(dac_clk unit)	0x10
P1:0x6c	p26	7~0	p26 cycle for Pixel timing(dac_clk unit)	0x10
P1:0x6e	p27	7~0	p27 cycle for Pixel timing(dac_clk unit)	0x02

P1:0x6f	p28	7~0	p28 cycle for Pixel timing(dac_clk unit)	0x20
P1:0x70	p29	7~0	p29 cycle for Pixel timing(dac_clk unit)	0x20
P1:0x71	p30	7~0	p30 cycle for Pixel timing(dac_clk unit)	0x10
P1:0x72	p31	7~0	p31 cycle for Pixel timing(dac_clk unit)	0x70
P1:0x73	p32	7~0	p32 cycle for Pixel timing(dac_clk unit)	0x05
P1:0x74	p33_1msb	0	p33 cycle for Pixel timing(dac_clk unit)	0x00
P1:0x75	p33_8lsb	7~0		0x40
P1:0x76	p34	7~0	p34 cycle for Pixel timing(dac_clk unit)	0x05
P1:0x77	p35 p36	7~0	[7:4]: p35 cycle for Pixel timing(dac_clk unit) [3:0]: p36 cycle for Pixel timing(dac_clk unit)	0xa6
P1:0x78	p37 p38	7~0	[7:4]: p37 cycle for Pixel timing(dac_clk unit) [3:0]: p38 cycle for Pixel timing(dac_clk unit)	0xe6
P1:0x79	p39 p40	7~0	[7:4]: p39 cycle for Pixel timing(dac_clk unit) [3:0]: p40 cycle for Pixel timing(dac_clk unit)	0x42
P1:0x7a	p41	7~0	p41 cycle for Pixel timing(dac_clk unit)	0x02
P1:0x7b	p42	7~0	p42 cycle for Pixel timing(dac_clk unit)	0x02
P1:0x7c	p43	7~0	p43 cycle for Pixel timing(dac_clk unit)	0x02
P1:0x7d	p44	7~0	p44 cycle for Pixel timing(dac_clk unit)	0x10
P1:0x7e	p45	7~0	p45 cycle for Pixel timing(dac_clk unit)	0x10
P1:0x7f	p46	7~0	p46 cycle for Pixel timing(dac_clk unit)	0x00
P1:0x80	p47	7~0	p47 cycle for Pixel timing(dac_clk unit)	0x10
P1:0x81	p48	7~0	p48 cycle for Pixel timing(dac_clk unit)	0x10
P1:0x82	p50 p51	3~0	[7:4]: p50 cycle for Pixel timing(dac_clk unit) [3:0]: p51 cycle for Pixel timing(dac_clk unit)	0x2f
P1:0x83	p52	3~0	p52 cycle for Pixel timing(dac_clk unit)	0x02

P1:0x84	p53	7~0	p53 cycle for Pixel timing(dac_clk unit)	0x50
P1:0x85	p60	7~0	p60 cycle for Pixel timing(dac_clk unit)	0x00
P1:0x8a	rh rl	7~0	[7:4]:rh [3:0]:rl Timing parameter of pixel_bias_ctrl	0xcc
P1:0x8b	sh sl	7~0	[7:4]: sh [3:0]: sl Timing parameter of pixel_bias_ctrl	0xcc
P1:0xb7	b2_num_A1_3msb	2~0	b2_num_A1 period for binning dac_code boost2, in the “dac_clk” unit.	0x01
P1:0xb8	b2_num_A1_8lsb	7~0		0x80
P1:0xb9	b4_num_A1_3msb	2~0	b4_num_A1 period for binning dac_code boost4, in the “dac_clk” unit.	0x01
P1:0xba	b4_num_A1_8lsb	7~0		0xe0
P1:0xbb	b2_num_A2_3msb	2~0	b2_num_A2 period for binning dac_code boost2,in the “dac_clk” unit.	0x00
P1:0xbc	b2_num_A2_8lsb	7~0		0x80
P1:0xbd	b4_num_A2_3msb	2~0	b4_num_A2 period for binning dac_code boost4, in the “dac_clk” unit.	0x00
P1:0xbe	b4_num_A2_8lsb	7~0		0xa0
P1:0xce	rst_num2_bin_8lsb	7~0	rst_num2_bin for binning rst dac_code	0x80
P1:0xcf	rst_num2_bin_2msb	1~0		0x00
P1:0xd0	boost_en	1~0	dac_code boost enable 00 – no boost 01 – boost with only step 2 10 – boost with only step 4 11 – boost with both step 2 and step 4	0x03
P1:0xd1	b2_num_3msb	2~0	b2_num period for normal dac_code boost2,in the “dac_clk” unit.	0x02
P1:0xd2	b2_num_8lsb	7~0		0x40
P1:0xd3	b4_num_3msb	2~0	b4_num period for normal dac_code boost4, in the “dac_clk” unit.	0x02
P1:0xd4	b4_num_8lsb	7~0		0xc0

P1:0xd5	A1 A2	6~0	[6:4]: A1 [2:0]: A2 Control binning dac_code steps.	0x31
P1:0xd6	rst_num_bin_8lsb	7~0	rst_num_bin for binning rst dac_code	0x80
P1:0xd7	rst_num_bin_2msb	1~0		0x00
P1:0xd8	sig_num_bin_8lsb	7~0	sig_num_bin for binning signal dac_code	0x00
P1:0xd9	sig_num_bin_3msb	2~0		0x04
P1:0xda	rcnt_num_A1_8lsb	7~0	rcnt_num_A1 for binning reset counter	0xc0
P1:0xdb	rcnt_num_A1_2msb	1~0		0x00
P1:0xdc	scnt_num_A1_8lsb	7~0	scnt_num_A1 for binning signal counter	0x40
P1:0xdd	scnt_num_A1_2msb	1~0		0x02
P1:0xde	rcnt_num_A2_8lsb	7~0	rcnt_num_A2 for binning reset counter	0x40
P1:0xdf	rcnt_num_A2_2msb	1~0		0x00
P1:0xe9	binning13_code_en	0	binning13_code_en Control binning dac_code mode	0x01
P1:0xea	scnt_num_A2_8lsb	7~0	scnt_num_A2 period for binning reset counter, in the “dac_clk” unit.	0xco
P1:0xeb	scnt_num_A2_2msb	7~0		0x00
P1:0xec	rcnt_num_2msb	7~0	Rcnt_num calculated in timing_gen.	Read only
P1:0xed	rcnt_num_8lsb	7~0		Read only
P1:0xee	scnt_num_4msb	7~0	Scnt_num calculated in timing_gen.	Read only
P1:0xef	scnt_num_8lsb	7~0		Read only
Delete frame function				
P1:0x18	del_frame_num switch_del_frame_en pwd_del_frame_en rst_del_en,	7~0	[7:6]: del_frame_num Control the frame number to be deleted when resolution switching or pwd recovery. [5]: switch_del_frame_en	0x40

	rst_colrow_en		Control the function of deleting bad frames when resolution switches. 1 – enable 0 – disable [4]: pwd_del_frame_en Control the function of deleting bad frames when pwd recovery. 1 – enable 0 – disable [1]: rst_del_en When enabled, the sensor will delete the first synchronized frame 1 – enable 0 – disable [0]: rst_colrow_en Sensor column and row reset control 1 – enable 0 – disable	
Analog control				
P1:0x19	icomp1 icomp2	7~0	[7:4]: icomp1 Control the first stage comparator bias current [3:0]: icomp2 Control the second stage comparator bias current	0xc1
P1:0x1e	en_dac vref2_ds_sel	1~0	[1]: en_dac Enable current DAC [0]: vref2_ds_sel Reference voltage driver of the second stage comparator	0x02
P1:0x1f	cp1_en cp2_en blcmp_bias pll_icp_sel	5~0	[5]: cp1_en The clock driver of positive charge pump [4]: cp2_en The clock driver of positive charge pump [3:2]: blcmp_bias Column blackout bias control [1:0]: pll_icp_sel PLL chargepump current control	0x31
P1:0x20	vncp_en vncp_sel	6~0	[6:4]: vncp_en Select the driver ability of NCP [3:0]: vncp_sel Select the output voltage of NCP for tx	0x7b
P1:0x21	pcp_rst_sel	6~0	[6:4]: pcp_rst_sel Select the output voltage of charge pump for restg	0x40
P1:0x25	bl_en	7~0	[7]: bl_en	0x20

	vblsel tcon1		Black out control signal of column [6:3]: vblsel Sunspot detection voltage [2:0]: tcon1 test control	
P1:0x26	vref2_com_sel vlow_com_sel vlow_ds_sel	7~0	[7:6]: vref2_com_sel Reference voltage of the second stage comparator control [5:2]: vlow_com_sel Reference voltage of FD low voltage [1:0]: vlow_ds_sel Reference voltage driver of FD low voltage	0x5a
P1:0x29	sc1_sel sa_mode	1~0	[1]: sc1_sel Select PMOS switch [0]: sa_mode Sense amp mode select	0x03
P1:0x2a	adc_range_ctl rgcnt_ctl rgcol_ctl	7~0	[7:5]: Adc range control [4:2]: rgcnt_ctl Select output voltage of counter reguator [1:0]: rgcol_ctl Regulator of column Decoder control	0xaa
P1:0x2b	sa_irst_ctl sa_pw1_ctl	4~0	[4:2]: sa_irst_ctl Latch pulse width control of SA [1:0]: sa_pw1_ctl Reset pulse width control of SA	0x02
P1:0x2c	adc_high_8bit pvdd_sel cntclk_delay	6~0	[6]: adc_high_8bit when set to high, dataout = datain when set to low, dataout = {datain[7:0],2'h0} [5:4]: pvdd_sel Select pixel LDO output voltage [3:0]: cntclk_delay Delay counter clock	0x60
P1:0x2d	colclk_delay dacclk_delay	7~0	[7:4]: colclk_delay Delay column decoder clock [3:0]: dacclk_delay Delay DAC clock	0x00
P1:0x2e	dclk_delay saclk_delay	7~0	[7:4]: dclk_delay Delay dclk clock [3:0]: saclk_delay Delay sense amplifier clock	0x00
P1:0xe7	reg_update_mode reg_update_cmd	1~0	[1]: reg_update_mode [0]: reg_update_cmd Control the register to take effect imediately.	0x00

MIPI register

Address	Register name	Bits	Description	Default
P1:0x8e	h_size_mipi_4msb	3~0	MIPI column number	0x07
P1:0x8f	h_size_mipi_8lsb	7~0	MIPI column number	0x90
P1:0x90	v_size_mipi_3msb	2~0	MIPI line number	0x04
P1:0x91	v_size_mipi_8lsb	7~0	MIPI line number	0x48
P1:0x92	drv_pre_ctrl drv_pre_sel lp_ctrl	6~0	[6:5]: MIPI driver control,[6]data,[5]clock [4:3]: MIPI driver selected,[4]data,[3]clock [2]: Lp driver ability [1:0]: lp voltage level	0x02
P1:0x93	r_clk_post	4~0	clk lane post time control	0x0a
P1:0x94	r_lpx_ck, r_lpx_dat	7~0	[7:4]: clk lane lpx time control [3:0]: Data lane lpx time control	0x33
P1:0x95	r_clk_prepare, r_hs_prepare	7~0	[7:4]: clock lane prepare time control [3:0]: Data lane prepare time control	0x22
P1:0x96	r_hs_zero	4~0	Data lane zero time control	0x06
P1:0x97	data ID	7~0	[7:6]: virtual lane sel [5:0]: data type sel 0x2a – raw8 0x2b – raw10	0x2b
P1:0x98	r_clk_trail, r_hs_trail	7~0	[7:4]: clk lane trail time control [3:0]: Data lane trail time control	0x23
P1:0x9c	r_clk_zero	5~0	clk lane zero time control	0x09
P1:0x9d	hs_mode, hs_lev[6:0]	7~0	[7]: MIPI clock mode control 0 – mipi_clk continuous(default) 1 – switch [6]: hs voltage ctrl: 0 [5:4]: data1,hs_level: 01 [3:2]: data0,hs_level: 01 [1:0]: clock,hs_level: 01	0x15
P1:0xa0	Mipi_en_buf	0	Mipi_en_buf	0x00
P1:0xa1	mipi_ls_start_num tx_speed_area_sel	4~0	[4:3]: MIPI FS packet to LS packet time control [2:0]: MIPI transmission speed select	0x02
P1:0xa2	r_init_m	7~0	MIPI initial time control bit	0x0b
P1:0xa3	r_init_l	7~0	MIPI initial time control bit	0x40
P1:0xa4	r_exit, r_wakeup_mh	5~0	[5:2]: r_exit, Data lane exit time control [1:0]: MIPI wakeup time control bit 17~16	0x40
P1:0xa5	r_wakeup_m	7~0	MIPI wakeup time control bit	0x86
P1:0xa6	r_wakeup_l	7~0	MIPI wakeup time control bit	0x88
P1:0xa7	dc_test_lp_lk	7~0	MIPI output control when MIPI work in	0x3f

			MIPI DC test mode [7]: MIPI clock output control 1 – MIPI clock pad output in HS state 0 – MIPI clock pad output in LP state [6]: MIPI data output control 1 – MIPI clock pad output in HS state 0 – MIPI clock pad output in LP state [5:4]: MIPI ckp/ckn voltage control [3:2]: MIPI d0p/d0n voltage control [1:0]: MIPI d1p/d1n voltage control	
P1:0xa8	dc_test_data_hs	7~0	MIPI output control when MIPI work in MIPI DC test mode	0xff
P1:0xae	frame_end_dly[7:0]	7~0	Time control between Long packet and FE packet	0x65
P1:0xaf	frame_end_dly[15:8]	7~0		0x00
P1:0xb1	hs_mode_vf hs_phase shutdowna	7~0	[7]: MIPI clk switch control 1: MIPI clk enter LP state when vblank time 0: MIPI clk enter LP state when vblank time and hblank time [5:3]: ph_delay [2:1]: control the phase between MIPI clk and data 00 – 1/4UI 01 – 1/2UI 10 – 3/4UI [0]: Mipi phy shutdown control 1 – enable dphy 0 – Mipi dphy shutdown	0x82
P1:0xb2	hs_mode2 double pause_ck, lp_sst_en, init, ulp_mode, ls_mode testmode	7~0	[7]: MIPI clk lane start mode 1 – MIPI clk lane enter HS mode when MIPI work 0 – MIPI clk enter LP mode when MIPI work [6]: double lane ctrl 1 – mipi work in double lane mode 0 – mipi work in single lane mode [5]: MIPI DC test mode enable 1 – MIPI work in DC test mode 0 – MIPI work in normal mode [4]: MIPI output pad control 1 – MIPI output pad driving ground when MIPI isn't working 0 – MIPI output pad tri-stated when MIPI isn't working [3]: MIPI initial mode enable	0x40

			1 – MIPI work in initial mode 0 – MIPI work in normal mode [2] MIPI ULP mode enable 1 – MIPI work in ULP mode 0 – MIPI work in normal mode [1] MIPI line sync mode enable [0] test mode ,MIPI test color bar 1 – MIPI output test pattern 0 – MIPI output ISP Image	
P1:0xb3	mipi_pll_nc mipi_pll_mc	6~0	[6:2]: mipi pll nc control [1:0]: mipi pll mc control	0x09
P1:0xb4	mipi_pll_bias mipi_pll_sel mipi_pll_en mipi_pll_outdiv	5~0	[5:4]: mipi pll current control [3]: mipi pll bypass enable [2]: mipi pll enable 1 – mipi pll work normally 0 – mipi pll powerdown [1:0]: mipi pll output clock frequency	0x11
P1:0xb5	mipi_icp_ctl, mipi_pll_dctl	7~0	[7:4]: mipi pll current control [3:0]: PFD delay control	0x00

ISP Register

Address	Register name	Bits	Description	Default
State register				
P2:0x05	fix_state_en fix_state_mode	4~0	[4]: fix_state_en:fix the state enable 1 – enable fix state 0 – disable fix state [2:0]: fix_state_mode:fix which mode of the state	0x00
P2:0x10	exp_nr_outd_8hsb	7~0	exp_nr_outd_8hsb the exposal threshold high 8bits from normal into outdoor	0x00
P2:0x11	exp_nr_outd_8lsb	7~0	exp_nr_outd_8lsb: the exposal threshold low 8bits from normal into outdoor	0x8b
P2:0x12	exp_outd_nr_8hsb	7~0	exp_outd_nr_8hsb the exposal threshold high 8bits from outdoor into normal	0x00
P2:0x13	exp_outd_nr_8lsb	7~0	exp_outd_nr_8lsb the exposal threshold low 8bits from outdoor into normal	0x8d
P2:0x14	exp_heq_dummy_8hsm	7~0	exp_heq_dummy_8hsm the exposal threshold high 8bits between normal and dummy	0x04
P2:0x15	exp_heq_dummy_8lsm	7~0	exp_heq_dummy_8lsm the exposal threshold low 8bits between normal and dummy	0x60
P2:0x16	exp_heq_low_8hsm	7~0	exp_heq_low_8hsm: the exposal threshold high 8bits between normal and lowlight	0x04
P2:0x17	exp_heq_low_8lsm	7~0	exp_heq_low_8lsm the exposal threshold low 8bits between normal and lowlight	0x60
P2:0x18	rpc_heq_low	7~0	rpc_heq_low the rpc threshold between normal and lowlight	0xc0
P2:0x19	rpc_heq_dummy	7~0	rpc_heq_dummy the rpc threshold between normal and dummy	0x80
Package register				
P2:0x35	outmode1	1~0	[1]: unpro_raw_out_en:unprocess raw output enable 1 – enable unprocess raw	0x00

			0 – disable unprocess raw	
P2:0x36	outmode2	7~0	[3]: VSYNC Inversion [2] : HSYNC Inversion	0x00
memory register				
P2:0x5e	line_buf_standby mem_down_en auto_first_en br_first	3~0	[3]: line_buf_standby:memory CEN 1 – disable memory work 0 – enable memory work [2]: mem_down_en: memory shut down enable when hblank 1 – enable memory shut down 0 – disable memory shut down [1]: auto_first_en:auto br_frst enable whatever updown or mirror 1 – enable auto br first 0 – disable auto br first [0]: br_first:output b/r first or g first 1 – b/r first output 0 – gb/gr first output	0x07
P2:0x5f	Error_flag_mem Test_done_mem bist	0	[4]: Error_flag_mem 1 – there is error 0 – there is no error [1]: test_done_mem 1 – test have done 0 – test haven't done [0]: memory bist test enable 1 – enable memory bist test 0 – disable memory bist test	0x00
Bpc register				
P2:0x34	isp_mode	7~0	[7]: bpc_dpix_en: double bad pixel enable 1 – enable double bad pixel 0 – disable double bad pixel [6]: bpc_flt_en: filtrate bpc field enable 1 – enable bpc field 0 – disable bpc field [3]: demo_en:demo_gf bypass enable 1 – enable demo_gf work 0 – disable demo_gf work	0xff
P2:0x5d	awbgain_position_set bayer_order	4~0	[4]: awbgain_position_set: awbgain position reverse 1 – enable awbgain_position revise 0 – disable awbgain_position revise [1:0]: bayer_order:bayer raw order 00 – GBGB 01 – BGBG	0x01

			10 – GRGR 11 – RGRG	
P2:0x60	lsc_bpc_en	7~0	[3]: BPC in dummy enable 0 – disable 1 – enable [2]: BPC in outdoor enable 0 – disable 1 – enable [1]: BPC in normal enable 0 – disable 1 – enable [0]: BPC in low light enable 0 – disable 1 – enable	0xff
P2:0x61	vsync_delay_num	1~0	The line number of vsync delay	0x00
P2:0x62	row_start[7:0]	7~0	row_start[7:0] low 8 bits of starting point of row counting	0x01
P2:0x63	row_start[10:8]	2~0	row_start[10:8] high 3 bits of starting point of row counting	0x00
P2:0x90	dp_dif_th_b_normal	7~0	Double bad pixel black threshold in normal	0x1e
P2:0x91	dp_dif_th_b_dummy	7~0	Double bad pixel black threshold in dummy	0x1e
P2:0x92	dp_dif_th_b_low	7~0	Double bad pixel black threshold in lowlight	0x1e
P3:0xc0	dp_pos_en	0	Otp send dpix coordinate enable 1 – enable Otp send dpix coordinate 0 – disable Otp send dpix coordinate	0x00
P4:0x12	isp_regf_12	7~0	bpc_vt_eff:bpc offset ratio value	0x00
P4:0x13	isp_regf_13	7~0	bpc_wt_eff bpc white min threshold	0x00
P4:0x14	isp_regf_14	7~0	bpc_dt_eff bpc black max threshold	0x14
P4:0x15	isp_regf_15	7~0	bpc_range_thr_outdoor dbpc range threshold in outdoor	0x80
P4:0x16	isp_regf_16	7~0	bpc_range_thr_nr dbpc range threshold in normal	0x80
P4:0x17	isp_regf_17	7~0	bpc_range_thr_dummy dbpc range threshold in dummy	0x80
P4:0x18	isp_regf_18	7~0	bpc_range_thr_low dbpc range threshold in lowlight	0x80
P4:0x19	isp_regf_19	7~0	bpc_dif_thr_outdoor	0x10

			bpc grad difference threshold in outdoor	
P4:0x1a	isp_regf_1a	7~0	bpc_dif_thr_nr bpc grad difference threshold in normal	0x10
P4:0x1b	isp_regf_1b	7~0	bpc_dif_thr_dummy bpc grad difference threshold in dummy	0x10
P4:0x1c	isp_regf_1c	7~0	bpc_dif_thr_low bpc grad difference threshold in lowlight	0x10
P4:0x1d	isp_regf_1d	7~0	bpc_grad_thr_outdoor bpc edge grad threshold in outdoor	0x10
P4:0x1e	isp_regf_1e	7~0	bpc_grad_thr_nr bpc edge grad threshold in normal	0x10
P4:0x1f	isp_regf_1f	7~0	bpc_grad_thr_dummy bpc edge grad threshold in dummy	0x10
P4:0x20	isp_regf_20	7~0	bpc_grad_thr_low bpc edge grad threshold in lowlight	0x10
P4:0x21	isp_regf_21	7~0	white_range_thr_outdoor: Below this interval pixel value judgment point without relative difference, but the absolute difference in outdoor	0x46
P4:0x22	isp_regf_22	7~0	white_range_thr_nr Below this interval pixel value judgment point without relative difference, but the absolute difference in normal	0x46
P4:0x23	isp_regf_23	7~0	white_range_thr_dummy Below this interval pixel value judgment point without relative difference, but the absolute difference in dummy	0x46
P4:0x24	isp_regf_24	7~0	white_range_thr_low Below this interval pixel value judgment point without relative difference, but the absolute difference in lowlight	0x46
P4:0x25	isp_regf_25	7~0	white_delta_thr_outdoor determine the absolute difference of the use of bright pixels in outdoor	0x0a
P4:0x26	isp_regf_26	7~0	white_delta_thr_normal determine the absolute difference of the use of bright pixels in normal	0x0a
P4:0x27	isp_regf_27	7~0	white_delta_thr_dummy determine the absolute difference of the use of bright pixels in dummy	0x0a
P4:0x28	isp_regf_28	7~0	white_delta_thr_low determine the absolute difference of the use of bright pixels in lowlight	0x0a
P4:0x29	isp_regf_29	7~0	black_delta_thr_outdoor	0x0a

			determine the absolute difference of the use of dark pixels in outdoor	
P4:0x2a	isp_regf_2a	7~0	black_delta_thr_normal determine the absolute difference of the use of dark pixels in normal	0x0a
P4:0x2b	isp_regf_2b	7~0	black_delta_thr_dummy determine the absolute difference of the use of dark pixels in dummy	0x0a
P4:0x2c	isp_regf_2c	7~0	black_delta_thr_low determine the absolute difference of the use of dark pixels in lowlight	0x0a
P4:0x2d	isp_regf_2d	7~0	bpc_flag_thr_outdoor The third row of the central point and the first line of the three number of comparison, threshold control in outdoor	0x0a
P4:0x2e	isp_regf_2e	7~0	bpc_flag_thr_normal The third row of the central point and the first line of the three number of comparison, threshold control in normal	0x0a
P4:0x2f	isp_regf_2f	7~0	bpc_flag_thr_dummy The third row of the central point and the first line of the three number of comparison, threshold control in dummy	0x0a
P4:0x30	isp_regf_30	7~0	bpc_flag_thr_low The third row of the central point and the first line of the three number of comparison, threshold control in lowlight	0x0a
P4:0x31	isp_regf_31	7~0	dpix_wht_ofst_outdoor dpix white min ofst value in outdoor	0x32
P4:0x32	isp_regf_32	7~0	dpix_wht_ofst_normal: dpix white min ofst value in normal	0x32
P4:0x33	isp_regf_33	7~0	dpix_wht_ofst_dummy dpix white min ofst value in dummy	0x32
P4:0x34	isp_regf_34	7~0	dpix_wht_ofst_low dpix white min ofst value in lowlight	0x32
P4:0x35	isp_regf_35	7~0	dpix_blk_ofst_outdoor dpix black min ofst value in outdoor	0x20
P4:0x36	isp_regf_36	7~0	dpix_blk_ofst_normal dpix black min ofst value in normal	0x20
P4:0x37	isp_regf_37	7~0	dpix_blk_ofst_dummy dpix black min ofst value in dummy	0x20
P4:0x38	isp_regf_38	7~0	dpix_blk_ofst_low dpix black min ofst value in lowlight	0x20
P4:0x39	isp_regf_39	7~0	[7:6]: dpix_wht_ratio_outdoor	0x00

			Double bad pixel white ratio in outdoor [5:4]: dpix_wht_ratio_normal Double bad pixel white ratio in normal [3:2]: dpix_wht_ratio_dummy Double bad pixel white ratio in dummy [1:0]: dpix_wht_ratio_low Double bad pixel white ratio in lowlight	
P4:0x3a	isp_regf_3a	7~0	[7:6]: dpix_blk_ratio_outdoor Double bad pixel black ratio in outdoor [5:4]: dpix_blk_ratio_normal Double bad pixel black ratio in normal [3:2]: dpix_blk_ratio_dummy Double bad pixel black ratio in dummy [1:0]: dpix_blk_ratio_low Double bad pixel black ratio in lowlight	0xff
P4:0x3b	isp_regf_3b	7~0	dp_dif_th_w_outdoor Double bad pixel white threshold in outdoor	0x1e
P4:0x3c	isp_regf_3c	7~0	dp_dif_th_w_normal Double bad pixel white threshold in normal	0x1e
P4:0x3d	isp_regf_3d	7~0	dp_dif_th_w_dummy Double bad pixel white threshold in dummy	0x1e
P4:0x3e	isp_regf_3e	7~0	dp_dif_th_w_low Double bad pixel white threshold in lowlight	0x1e
P4:0x3f	isp_regf_3f	7~0	dp_dif_th_b_outdoor Double bad pixel black threshold in outdoor	0x1e
Demo_sif register				
P2:0xa0	dem_v_start_3msb	2~0	Image vertical start 3msb	0x00
P2:0xa1	dem_v_start_8lsb	7~0	Image vertical start 8lsb	0x00
P2:0xa2	dem_v_size_3msb	2~0	Image vertical size 3msb	0x04
P2:0xa3	dem_v_size_8lsb	7~0	Image vertical size 8lsb	0x48
P2:0xa4	dem_h_start_3msb	2~0	Image horizontal start 3msb	0x00
P2:0xa5	dem_h_start_8lsb	7~0	Image horizontal start 8lsb	0x00
P2:0xa6	dem_h_size_3msb	2~0	Image half horizontal size 3msb	0x03
P2:0xa7	dem_h_size_8lsb	7~0	Image half horizontal size 8lsb	0xc8
P2:0xc0	raw_r_offset_8lsb_outdoor	7~0	raw_r_offset_8lsb_outdoor the offset add on r channel in outdoor	0x00
P2:0xc1	raw_r_offset_8lsb_normal	7~0	raw_r_offset_8lsb_normal the offset add on r channel in normal	0x00
P2:0xc2	raw_r_offset_8lsb_dummy	7~0	raw_r_offset_8lsb_dummy	0x00

			the offset add on r channel in dummy	
P2:0xc3	raw_r_offset_8lsb_low	7~0	raw_r_offset_8lsb_low the offset add on r channel in lowlight	0x00
P2:0xc4	raw_r_offset_2msb_outdoor raw_r_offset_2msb_normal raw_r_offset_2msb_dummy raw_r_offset_2msb_low	7~0	[7:6]: raw_r_offset_2msb_outdoor the offset add on r channel in outdoor [5:4]: raw_r_offset_2msb_normal the offset add on r channel in normal [3:2]: raw_r_offset_2msb_dummy the offset add on r channel in dummy [1:0]: raw_r_offset_2msb_low the offset add on r channel in lowlight	0x00
P2:0xc5	raw_b_offset_8lsb_outdoor	7~0	raw_b_offset_8lsb_outdoor the offset add on b channel in outdoor	0x00
P2:0xc6	raw_b_offset_8lsb_normal	7~0	raw_b_offset_8lsb_normal the offset add on b channel in normal	0x00
P2:0xc7	raw_b_offset_8lsb_dummy	7~0	raw_b_offset_8lsb_dummy the offset add on b channel in dummy	0x00
P2:0xc8	raw_b_offset_8lsb_low	7~0	raw_b_offset_8lsb_low the offset add on b channel in lowlight	0x00
P2:0xc9	raw_b_offset_2msb_outdoor raw_b_offset_2msb_normal raw_b_offset_2msb_dummy raw_b_offset_2msb_low	7~0	[7:6]: raw_b_offset_2msb_outdoor the offset add on b channel in outdoor [5:4]: raw_b_offset_2msb_normal the offset add on b channel in normal [3:2]: raw_b_offset_2msb_dummy the offset add on b channel in dummy [1:0]: raw_b_offset_2msb_low: the offset add on b channel in lowlight	0x00
P2:0xca	raw_gr_offset_8lsb_outdoor	7~0	raw_gr_offset_8lsb_outdoor the offset add on gr channel in outdoor	0x00
P2:0xcb	raw_gr_offset_8lsb_normal	7~0	raw_gr_offset_8lsb_normal the offset add on gr channel in normal	0x00
P2:0xcc	raw_gr_offset_8lsb_dummy	7~0	raw_gr_offset_8lsb_dummy the offset add on gr channel in dummy	0x00
P2:0xcd	raw_gr_offset_8lsb_low	7~0	raw_gr_offset_8lsb_low the offset add on gr channel in lowlight	0x00
P2:0xce	raw_gr_offset_2msb_outdoo r raw_gr_offset_2msb_normal raw_gr_offset_2msb_dumm y raw_gr_offset_2msb_low	7~0	[7:6]: raw_gr_offset_2msb_outdoor the offset add on gr channel in outdoor [5:4]: raw_gr_offset_2msb_normal the offset add on gr channel in normal [3:2]: raw_gr_offset_2msb_dummy the offset add on gr channel in dummy [1:0]: raw_gr_offset_2msb_low the offset add on gr channel in lowlight	0x00
P2:0xcf	raw_gb_offset_8lsb_outdoor	7~0	raw_gb_offset_8lsb_outdoor	0x00

			the offset add on gb channel in outdoor	
P2:0xd0	raw_gb_offset_8lsb_normal	7~0	raw_gb_offset_8lsb_normal the offset add on gb channel in normal	0x00
P2:0xd1	raw_gb_offset_8lsb_dummy	7~0	raw_gb_offset_8lsb_dummy the offset add on gb channel in dummy	0x00
P2:0xd2	raw_gb_offset_8lsb_low	7~0	raw_gb_offset_8lsb_low the offset add on gb channel in lowlight	0x00
P2:0xd3	raw_gb_offset_2msb_outdoor raw_gb_offset_2msb_normal raw_gb_offset_2msb_dummy raw_gb_offset_2msb_low	7~0	[7:6]: raw_gb_offset_2msb_outdoor the offset add on gb channel in outdoor [7:6]: raw_gb_offset_2msb_normal the offset add on gb channel in normal [7:6]: raw_gb_offset_2msb_dummy the offset add on gb channel in dummy [7:6]: raw_gb_offset_2msb_low the offset add on gb channel in lowlight	0x00

OTP cell/register

Address	Cell/Register	Bits	Description	Default
OTP IP interface register				
P3:0xe0	tpgm[7:0]	7~0	OTP Programming time set 8lsb	0xea
P3:0xe1	tpgm[13:8]	5~0	OTP Programming time set 6msb	0x01
P3:0xe2	Tsup_cs	7~0	OTP operation Address setup time set	0x01
P3:0xe3	Thp_cs	7~0	OTP operation Address hold time set	0x01
P3:0xe4	Tsq	7~0	OTP access time set	0x02
P3:0xe5	Trd	7~0	OTP read time set	0x17
P3:0xe6	tgap	7~0	Time gap set where between steady outputs data to read enable signals, this will improve the timing.	0x04
OTP status register				
P3:0xe7	pgm_permit	0	Otp programming permit flag. 0 – forbid PGM process, 1 – PGM process permit.	0x00
P3:0xec	{otp_pgm_flag, read_flag, bat_rd_flag, otp_busy}	3~0	[3]: otp_pgm_flag: otp program flag [2]: read_flag : byte read flag [2]: bat_rd_flag: otp batch read flag [0]: otp_busy: otp busy flag All the flags read only.	0x00
OTP mode control register				
P3:0xc0	dp_pos_en	0	dp_pos_en enable signal of transferring position of dead pixel from OTP to ISP 1 – enable the transferring 0 – disable the transferring	0x00
P3:0xea	data_byt_wr	7~0	data_byt_wr Data required to program to OTP in byte program mode	0x00
P3:0xeb	addr_byt_wr	7~0	addr_byt_wr OTP cell address in byte program mode	0x00
P3:0xe8	otp_pgm_en	0	Start program otp. WARNING: before using this command, you should make sure that the otp is NOT BUSY and you have	0x00

			written the EXACT ADDRESS a SUITABLE value WHEN program operation permit.	
P3:0xd0	Page_half_flag Otp_batch_en	0	[2:1]: Page_half_flag select signal of OTP batch program address 00 – select OTP 0x00 ~ 0x3f to program 01 – select OTP 0x40 ~ 0x7f to program 10 – select OTP 0x80 ~ 0xbf to program 11 – select OTP 0xc0 ~ 0xff to program [0]: Otp_batch_en 1 – start batch program 0 – disable batch program	0x00
OTP batch buffer				
P4:0x00	flag_load0	7~0	[4:0]: flag_load0 flag_load0[4]: Block 4 programmed flag 1 – Block 4 is programmed; 0 – Block 4 is empty; flag_load0[3]:Block 3 programmed flag 1 – Block 3 is programmed; 0 – Block 3 is empty; flag_load0[2]:Block 2 programmed flag 1 – Block 2 is programmed; 0 – Block 2 is empty; flag_load0[1]:Block 1 programmed flag 1 – Block 1 is programmed; 0 – Block 1 is empty; flag_load0[0]:Block 0 programmed flag 1 – Block 0 is programmed; 0 – Block 0 is empty;	0x00
P4:0x01	flag_load1	7~0	flag_load1 reserved flag register	0x00
P4:0x02	line_code	7~0	line_code Production Identification	0x00
P4:0x03	lot_year lot_month	7~0	lot_year lot_month Production Identification	0x00
P4:0x04	lot_day	7~0	lot_day Production Identification	0x00
P4:0x05	lot_snum	7~0	lot_snum	0x00

			Production Identification	
P4:0x06	wafer_id	7~0	wafer_id Production Identification	0x00
P4:0x07	wafer_x	7~0	wafer_x Production Identification	0x00
P4:0x08	wafer_y	7~0	wafer_y Production Identification	0x00
P4:0x09	otp_r_gain	7~0	user register 1 reserved register for user	0x80
P4:0x0a	otp_b_gain	7~0	user register 2 reserved register for user	0x80
P4:0x0b	otp_gr_gain	7~0	user register 3 reserved register for user	0x80
P4:0x0c	otp_gb_gain	7~0	user register 4 reserved register for user	0x80
P4:0x0d	user_rsv_01	7~0	user register 5 reserved register for user	0x00
P4:0x0e	user_rsv_02	7~0	user register 6 reserved register for user	0x00
P4:0x0f	user_rsv_03	7~0	user register 7 reserved register for user	0x00
P4:0x10	user_rsv_04	7~0	user register 8 reserved register for user	0x00
P4:0x11	user_rsv_05	3~0	user register 9 reserved register for user	0x00
P4:0x12	isp_regf_12	7~0	isp_regf_12 12th byte data in batch operation mode	0x00
P4:0x13	isp_regf_13	7~0	isp_regf_13 13th byte data in batch operation mode	0x00
P4:0x14	isp_regf_14	7~0	isp_regf_14 14th byte data in batch operation mode	0x14
P4:0x15	isp_regf_15	7~0	isp_regf_15 15th byte data in batch operation mode	0x80
P4:0x16	isp_regf_16	7~0	isp_regf_16 16th byte data in batch operation mode	0x80
P4:0x17	isp_regf_17	7~0	isp_regf_17 17th byte data in batch operation mode	0x80
P4:0x18	isp_regf_18	7~0	isp_regf_18 18th byte data in batch operation mode	0x80
P4:0x19	isp_regf_19	7~0	isp_regf_19 19th byte data in batch operation mode	0x10
P4:0x1a	isp_regf_1a	7~0	isp_regf_1a 1ath byte data in batch operation mode	0x10
P4:0x1b	isp_regf_1b	7~0	isp_regf_1b	0x10

			1bth byte data in batch operation mode	
P4:0x1c	isp_regf_1c	7~0	isp_regf_1c 1cth byte data in batch operation mode	0x10
P4:0x1d	isp_regf_1d	7~0	isp_regf_1d 1dth byte data in batch operation mode	0x10
P4:0x1e	isp_regf_1e	7~0	isp_regf_1e 1eth byte data in batch operation mode	0x10
P4:0x1f	isp_regf_1f	7~0	isp_regf_1f 1fth byte data in batch operation mode	0x10
P4:0x20	isp_regf_20	7~0	isp_regf_20 20th byte data in batch operation mode	0x10
P4:0x21	isp_regf_21	7~0	isp_regf_21 21th byte data in batch operation mode	0x46
P4:0x22	isp_regf_22	7~0	isp_regf_22 22th byte data in batch operation mode	0x46
P4:0x23	isp_regf_23	7~0	isp_regf_23 23th byte data in batch operation mode	0x46
P4:0x24	isp_regf_24	7~0	isp_regf_24 24th byte data in batch operation mode	0x46
P4:0x25	isp_regf_25	7~0	isp_regf_25 25th byte data in batch operation mode	0x0a
P4:0x26	isp_regf_26	7~0	isp_regf_26 26th byte data in batch operation mode	0x0a
P4:0x27	isp_regf_27	7~0	isp_regf_27 27th byte data in batch operation mode	0x0a
P4:0x28	isp_regf_28	7~0	isp_regf_28 28th byte data in batch operation mode	0x0a
P4:0x29	isp_regf_29	7~0	isp_regf_29 29th byte data in batch operation mode	0x0a
P4:0x2a	isp_regf_2a	7~0	isp_regf_2a 2ath byte data in batch operation mode	0x0a
P4:0x2b	isp_regf_2b	7~0	isp_regf_2b 2bth byte data in batch operation mode	0x0a
P4:0x2c	isp_regf_2c	7~0	isp_regf_2c 2cth byte data in batch operation mode	0x0a
P4:0x2d	isp_regf_2d	7~0	isp_regf_2d 2dth byte data in batch operation mode	0x0a
P4:0x2e	isp_regf_2e	7~0	isp_regf_2e 2eth byte data in batch operation mode	0x0a
P4:0x2f	isp_regf_2f	7~0	isp_regf_2f 2fth byte data in batch operation mode	0x0a
P4:0x30	isp_regf_30	7~0	isp_regf_30 30th byte data in batch operation mode	0x0a
P4:0x31	isp_regf_31	7~0	isp_regf_31	0x32

			31th byte data in batch operation mode	
P4:0x32	isp_regf_32	7~0	isp_regf_32 32th byte data in batch operation mode	0x32
P4:0x33	isp_regf_33	7~0	isp_regf_33 33th byte data in batch operation mode	0x32
P4:0x34	isp_regf_34	7~0	isp_regf_34 34th byte data in batch operation mode	0x32
P4:0x35	isp_regf_35	7~0	isp_regf_35 35th byte data in batch operation mode	0x20
P4:0x36	isp_regf_36	7~0	isp_regf_36 36th byte data in batch operation mode	0x20
P4:0x37	isp_regf_37	7~0	isp_regf_37 37th byte data in batch operation mode	0x20
P4:0x38	isp_regf_38	7~0	isp_regf_38 38th byte data in batch operation mode	0x20
P4:0x39	isp_regf_39	7~0	isp_regf_39 39th byte data in batch operation mode	0x00
P4:0x3a	isp_regf_3a	7~0	isp_regf_3a 3ath byte data in batch operation mode	0xff
P4:0x3b	isp_regf_3b	7~0	isp_regf_3b 3bth byte data in batch operation mode	0x1e
P4:0x3c	isp_regf_3c	7~0	isp_regf_3c 3cth byte data in batch operation mode	0x1e
P4:0x3d	isp_regf_3d	7~0	isp_regf_3d 3dth byte data in batch operation mode	0x1e
P4:0x3e	isp_regf_3e	7~0	isp_regf_3e 3eth byte data in batch operation mode	0x1e
P4:0x3f	isp_regf_3f	7~0	isp_regf_3f 3fth byte data in batch operation mode	0x1e
Mapped register of OTP cell				
OTP 0x00	data_byt_wr	7~0	mapped to P5:0x00 register	0x00
…	…	…	...	…
OTP 0x3f	data_byt_wr	7~0	mapped to P5:0x3f register	0x00

Page Selection

Address	Register name	Bits	Description	Default
0xfd	page_flg_d2	3~0	[2:0] : page select 000 – page0 001 – page1 010 – page2 100 – otp	0x00

Revision History

Version #	Date	Modification
Specification 1.0	2019.08.15	1. The first release for designer.