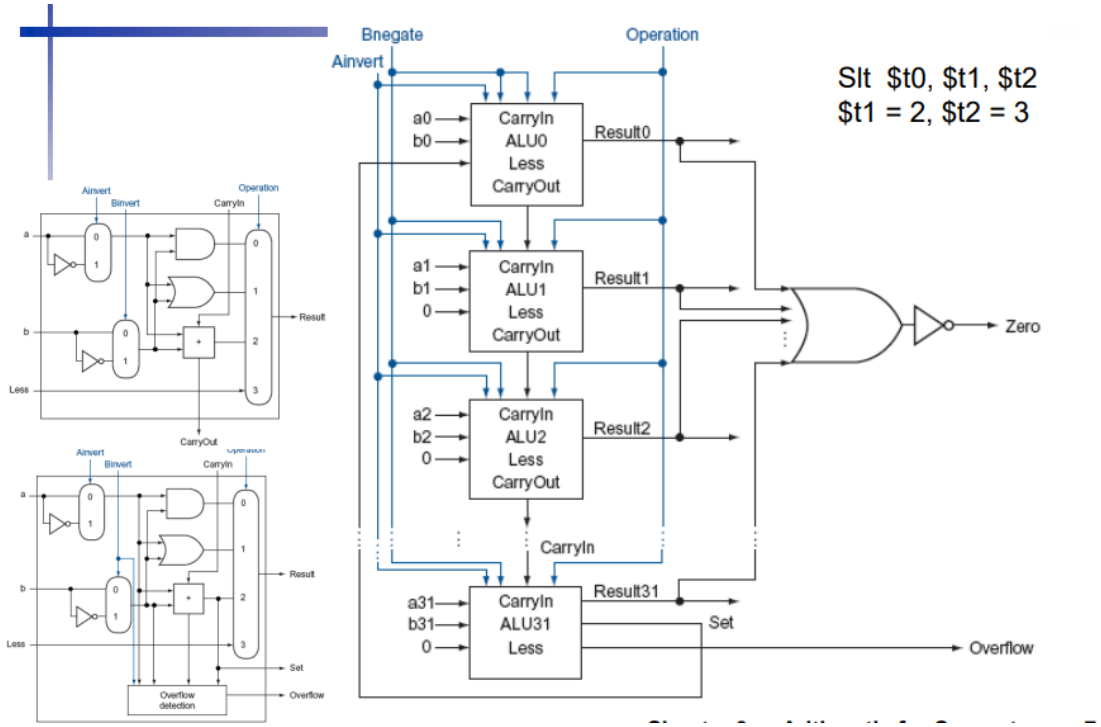
Computer Organization

Architecture diagrams:

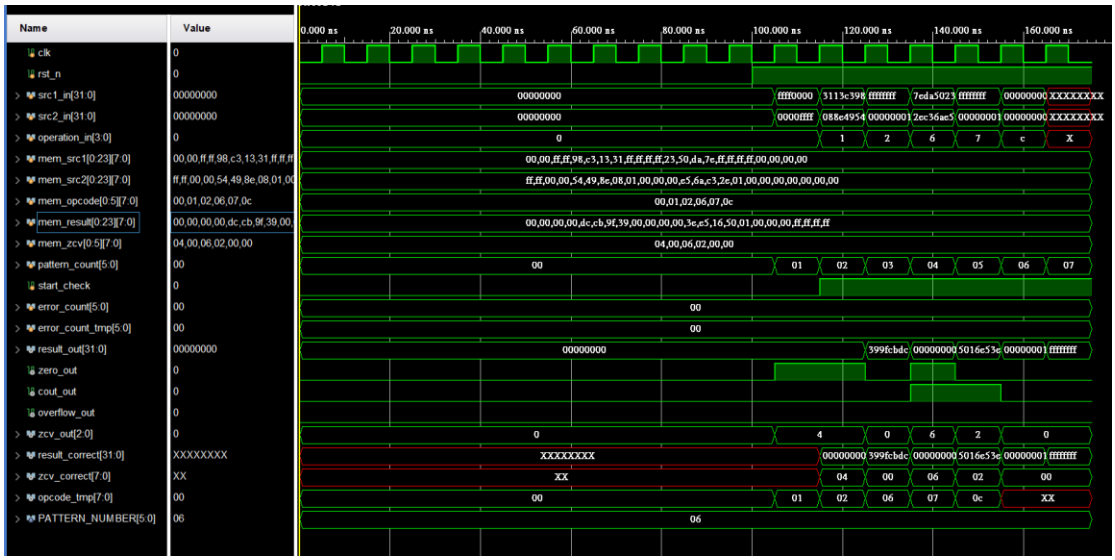


For the first 31 one-bit alu, if operation equals to 00, the output “result” is a and b. If operation equals to 01, the output “result” is a or b. If operation equals to 10, the output “result” is a add b. If operation equals to 11, the output “result” is “less”. “Ainvert” and “Binvert” can control when to do addition and when to do subtraction. Except for the first one-bit alu, the intput “less” in other alu is 0. Compared to the first 31 one-bit alu, the last one has “set”, which is the result of a xor b xor cin. Besides, “set” connects to “less” of the first one-bit alu. If we want to do slt, “Binvert” equals to 1 so that we do a subtract b. If the result is negativie, “set” equals to 1 because it is a signed bit, and the output of 32-bit alu equals to 1.

Hardware module analysis:

1. Alu_top：It means the first 31 blocks in the diagram. The output “result” leads to “zero” in the future, and “cout” will be the input “cin” in the next blocks.
2. Alu_last：It means the last block in the diagram. Compared to “alu_top”, alu_last has “set” which connects to the input port “less” in the first “alu_top”.
3. Alu：The whole design which contains 31 alu_top and 1 alu_last.

Experiment result:



For example, src1_in = ffff0000, src2_in = 0000ffff, operation_in = 0000, which means the result should be src1_in and src2_in (00000000).
Take another example, src1_in = 3113c398, src2_in = 088c4954, operation_in = 0001, which means the result should be src1_in or src2_in (399fcbdc).

Problems you met and solutions:

1. In the beginning, the console jumped the error like “[place 30-494] the design is empty resolution: check if opt_design has removed all the leaf cells of your design. check whether you have instantiated and connected all of the top level ports.” every time. I searched the Internet for a long time then I noticed that the method I added the testbench to the project was wrong. I should add simulation sources instead of design sources. Besides, I should click “run behavior simulation” instead of “run implementation”.
2. It’s hard for me too debug in the beginning, so I tried to understand how the testbench works. After researching, I knew that zcv_out means zero_out, cout_out, overflow_out. It helps me a lot in the future.

Summary:

Given an operation, “alu” can behave like what the operation corresponds to. After finishing lab1, I understand “alu” more deeply than before. Besides, I am more familiar to Vivado so that I can understand the labs in the future more efficiently.