G.R.O.U.P.
Part 4

# Parts List

- *Inputs*
  - Clock-1 bit, the clock, feeds into the clock on the register Accumulator
  - Input-32-bits, binary integer for input
  - Opcode-4-bits, binary code to indicate the operation
- *Outputs*
  - Error-1 bit, true if an error state has occurred
  - Value-32 bits, the current output of the register Accumulator
- *Interfaces*
  - ACC.D, 32-bits, the next value into the register
  - ACC.Q, 32-bits, the current value from the register
  - Decoder.S0, 1 bit, lowest bit from the opcode
  - Decoder.S1, 1 bit, next lowest bit from the opcode
  - Decoder.S2, 1 bit, second highest bit from the opcode
  - Decoder.S3, 1-bit, highest bit from the opcode
  - ADD/SUB.A, 32-bits, current ACC Q value
  - ADD/SUB.B, 32-bits, input
  - ADD/SUB.Op, 1-bit, Operation be it Add or Sub
  - ADD/SUB.S, 32-bits, actual sum
  - ADD/SUB.V, 1-bit, overflow status
  - ADD/SUB.C, 1-bit, carry/borrow status
  - ADD/SUB.Cout, 1-bit, carry out value for error checking
  - MULT.A, 16-bits, takes lower 16 bits of current ACC Q value
  - MULT.B, 16-bits, takes lower 16 bits of input
  - MULT.P, 32-bits, product feeds into channel 7 of MUX
  - DIV.A, 32-bits, current ACC Q value
  - DIV.B, 32-bits, input
  - DIV.Q, 32-bits, quotient
  - MUX.b, 32-bits, output of the multiplexer into ACC
  - MUX.Ch0, 32 bits, feedback for the current value of ACC into multiplexer
  - MUX.CH1, 32 bits, results of addition into the multiplexer
  - MUX.Ch2, 32 bits, results of subtraction into the multiplexer
  - MUX.Ch3, 32 bits, results of AND into the multiplexer
  - MUX.Ch4, 32 bits, results of OR into the multiplexer
  - MUX.Ch5, 32 bits, results of NOT into the multiplexer
  - MUX.Ch6, 32 bits, results of XOR into the multiplexer
  - MUX.Ch7, 32 bits, results of multiplication into the multiplexer
  - MUX.Ch8, 32 bits, 32-bit 0 value used to reset the ACC
  - MUX.Ch9, 32 bits, results of division into the multiplexor
  - MUX.Ch10 – Ch14 are 32-bits channels, unused (not shown due to unused)
  - Mux.Ch15, 32 bits, 32-bit 0 value used as a reset to not put garbage in the system
  - MUX.S, 16-bits, the one-hot control into the multiplexer

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- *Gates*
  - XOR Gate, 32 bits, one channel is input, and the other channel is current ACC Q value
  - AND Gate, 32 bits, one channel is input, and the other channel is current ACC Q value
  - OR Gate, 32 bits, one channel is input, and the other channel is current ACC Q value
  - NOT Gate, 32 bits, only one channel is current ACC Q value

- *Combinational Logic Components*
  - Decoder, 4-to-16 bits, converts opcode into Multiplexer selection and encoder
  - Multiplexer, 16-channel, 32-bit multiplexor for result operation
  - Encoder, 4-bit, results in operational value
  - Adder/Subtractor, 32-bit
  - Multiplier, 16-bit, channel A is current lower 16-bits of ACC Q value, channel B is lower 16-bits of input
  - Divider, 32-bit, channel A is current ACC Q value, channel B is input value

- *Sequential Logic Components*
  - ACC, 32-Bit D Register that contains the current system value
- *Modules*
  - Error Check-Tests for an error in subtraction, inputs Cout carry out status and Opcode.
  - Test Bench-Main module, runs clock and stimulus.
  - Breadboard-convenient module to allow easy assembly.