```
/* Default linker script, for normal executables */
OUTPUT_FORMAT("elf32-msp430")
OUTPUT_ARCH("msp430")
/* INCLUDE memory.x begin */
MEMORY {
                   : ORIGIN = 0x0000, LENGTH = 0x0010 /* END=0x0010, size 16 */
  sfr
 peripheral_8bit : ORIGIN = 0x0010, LENGTH = 0x00f0 /* END=0x0100, size 240 */
peripheral_16bit : ORIGIN = 0x0100, LENGTH = 0x0100 /* END=0x0200, size 256 */
                   : ORIGIN = 0x1000, LENGTH = 0x0400 /* END=0x1400, size 1K as 1 1024-byte segments
  bs1
*/
                : ORIGIN = 0x2000, LENGTH = 0x1000 /* END=0x2400, size 4K */
 ram (wx)
                 : ORIGIN = 0xc400, LENGTH = 0x3b80 /* END=0xff80, size 15K */
 rom (rx)
                 : ORIGIN = 0xff80, LENGTH = 0x0008 /* END=0xff88, size 8 as 1 8-byte segments */
  signature
                 : ORIGIN = 0xff80, LENGTH = 0x0080 /* END=0x10000, size 128 as 64 2-byte segments
  vectors
  /* Remaining banks are absent */
 infomem
            : ORIGIN = 0 \times 1800, LENGTH = 0 \times 0200
                 : ORIGIN = 0x0000, LENGTH = 0x0000
: ORIGIN = 0x0000, LENGTH = 0x0000
  infoa
  infob
 infoc : ORIGIN = 0x0000, LENGTH = 0x0000 infod : ORIGIN = 0x0000, LENGTH = 0x0000 ram2 (wx) : ORIGIN = 0x0000, LENGTH = 0x00000
  ram_mirror (wx) : ORIGIN = 0x0000, LENGTH = 0x0000
 tinyram (wx) : ORIGIN = 0x0000, LENGTH = 0x0000

: ORIGIN = 0x0000, LENGTH = 0x0000

- 0x00000000, LENGTH = 0x0000
 usbram (wx) : ORIGIN = ปั่งปับบัง, LENGTH = 0x000000000 : ORIGIN = 0x000000000, LENGTH = 0x000000000
REGION_ALIAS("REGION_TEXT", rom);
REGION_ALIAS("REGION_DATA", ram);
REGION_ALIAS("REGION_FAR_ROM", far_rom); /* Legacy name, no longer used */
REGION_ALIAS("REGION_FAR_TEXT", far_rom);
REGION_ALIAS("REGION_FAR_DATA", ram2);
/* INCLUDE memory.x end */
/*INCLUDE periph.x begin */
/* This file supports MSP430FR2433 devices. */
/* Version: 1.193 */
/***********************************
* STANDARD BITS
**************************************
* STATUS REGISTER BITS
***********************************
/**********************
/**********************************
 PERIPHERAL FILE MAP
*************************
/***********************************
************************************
ADCCTL1
ADCCTL1 L
__ADCCTL1_H
__ADCCTL2
__ADCCTL2_L
__ADCHI_ H
```

```
_ADCMEM0
                   = 0x0712;
                    = 0x0712;
 ADCMEMO_L
                   = 0x0713;
 _ADCMEMO_H
 ADCIE
                   = 0x071A;
 ADCIE L
                   = 0x071A;
 ADCIE H
                   = 0x071B;
 ADCIFG
                   = 0x071C;
                   = 0x071C;
 _ADCIFG_L
 _ADCIFG_H
                   = 0 \times 071D;
                    = 0x071E;
 ADCIV
                   = 0x071E;
 ADCIV L
 ADCIV H
                    = 0x071F;
Backup Memory Module
*************************************
 BAKMEM0
                   = 0x0660;
 BAKMEMO_L
                   = 0x0660;
 BAKMEMO_H
                   = 0x0661;
 BAKMEM1
                   = 0x0662:
                   = 0x0662;
 BAKMEM1_L
 BAKMEM1_H
                   = 0x0663;
 BAKMEM2
                   = 0x0664;
                  = 0x0664;
 BAKMEM2_L
                  = 0x0665;
 BAKMEM2_H
                  = 0x0666;
 BAKMEM3
 BAKMEM3 L
                  = 0x0666:
                 = 0x0667;
 BAKMEM3_H
 BAKMEM4
                  = 0x0668;
 BAKMEM4_L
                 = 0x0668;
 BAKMEM4_H
                 = 0x0669;
 BAKMEM5
                  = 0x066A;
 BAKMEM5_L
                  = 0x066A;
 BAKMEM5 H
                   = 0x066B;
                   = 0x066C;
 BAKMEM6
 BAKMEM6_L
                   = 0x066C;
 BAKMEM6_H
                   = 0x066D;
 BAKMEM7
                   = 0x066E;
                   = 0 \times 066E;
 BAKMEM7_L
                  = 0x066F;
 BAKMEM7_H
                   = 0 \times 0670;
 BAKMEM8
 BAKMEM8 L
                  = 0x0670;
                   = 0x0671;
 BAKMEM8_H
 BAKMEM9
                   = 0x0672;
 BAKMEM9_L
                   = 0x0672;
 BAKMEM9_H
                   = 0x0673;
                   = 0x0674;
 BAKMEM10
                   = 0x0674;
 BAKMEM10_L
 BAKMEM10_H
                   = 0x0675;
 BAKMEM11
                   = 0x0676;
 BAKMEM11_L
                   = 0x0676;
                  = 0 \times 0677;
 BAKMEM11_H
 BAKMEM12
                   = 0x0678;
                  = 0x0678;
 BAKMEM12_L
                 = 0 \times 0679;
 BAKMEM12 H
                  = 0x067A;
 BAKMEM13
                 = 0x067A;
 BAKMEM13 L
                 = 0x067B;
 BAKMEM13_H
 BAKMEM14
                 = 0 \times 067C;
                 = 0x067C;
= 0x067D;
 BAKMEM14_L
 BAKMEM14_H
                  = 0 \times 067E;
 BAKMEM15
                   = 0x067E;
 BAKMEM15_L
 BAKMEM15 H
                    = 0x067F;
/**********
 CRC Module
 CRCDI
                   = 0x01C0;
                   = 0x01C0;
 _CRCDI_L
 _CRCDI_H
                   = 0x01C1;
 CRCDIRB
                  = 0x01C2;
 CRCDIRB L
                  = 0x01C2;
 CRCDIRB_H
                  = 0x01C3;
```

```
_CRCINIRES = 0x01C4;
_CRCINIRES_L = 0x01C4;
_CRCINIRES_H = 0x01C5;
_CRCRESR = 0x01C6;
_CRCRESR I = 0x01C6;
__CRCINIRES
                           = 0 \times 01C6;
  CRCRESR L
  CRCRESR H
                             = 0x01C7;
/************************************
* CLOCK SYSTEM CONTROL
*************************
                  = 0x0180;
  CSCTL0
                           = 0x0180:
  CSCTL0 L
                      - 0x0180;

- 0x0181;

- 0x0182;

- 0x0182;

- 0x0183;

- 0x0184;

- 0x0185;

- 0x0186;

- 0x0186;

- 0x0187;

- 0x0188;

- 0x0188;

- 0x0188;

- 0x0184;

- 0x018A;

- 0x018A;

- 0x018B;

- 0x018C;

- 0x019C;

- 0x019O;

- 0x019O;

- 0x019O;

- 0x019O;
                          = 0x0181;
  CSCTL0_H
  CSCTL1
__CSCTL1_L
  _CSCTL1_H
  _CSCTL2
_CSCTL2_L
  CSCTL2_H
 _CSCTL3
_CSCTL3_L
_CSCTL3_H
  CSCTL3
  _CSCTL4
  _CSCTL4
_CSCTL4_L
_CSCTL4_H
  CSCTL5
  _CSCTL5_L
  _CSCTL5_H
__CSCTL6
__CSCTL6_L
__CSCTL6_H
__CSCTL7
  _CSCTL7_L
  _CSCTL7_H
 CSCTL8
  _CSCTL8_L
  _CSCTL8_H
                             = 0x0191;
* FRAM Memory
***********************************
  _FRCTL0 = 0x01A0;
_FRCTL0_L = 0x01A0;
_FRCTL0_H = 0x01A1;
                       = 0x01A4;
= 0x01A4;
= 0x01A5;
= 0x01A6;
__GCCTL0
__GCCTL0_L
  GCCTL0_H
  _GCCTL1
  /***********************
  HARDWARE MULTIPLIER 32Bit
***********************
  MPY = 0x04C0;
                          = 0x04C0;
= 0x04C1;
= 0x04C2;
  MPY L
  MPY_H
                         = 0x04C2;

= 0x04C2;

= 0x04C4;

= 0x04C4;

= 0x04C6;

= 0x04C6;

= 0x04C6;

= 0x04C7;

= 0x04C8;

= 0x04C8;

= 0x04C8;

= 0x04C9;

= 0x04CA;

= 0x04CA;

= 0x04CC;

= 0x04CC;

= 0x04CC;
  MPYS
  MPYS L
  MPYS_H
  MAC
  MAC L
  MAC_H
  MACS
  MACS_L
  MACS H
  0P2
  0P2_L
  _OP2_H
  RESL0
  RESLO_L
  RESLO_H
  RESHI
  RESHI L
  RESHI_H
                            = 0x04CD;
```

```
SUMEXT
                     = 0 \times 04CE;
                     = 0x04CE;
  SUMEXT_L
                     = 0x04CF;
  SUMEXT_H
                     = 0 \times 04 D0:
  MPY32L
  MPY32L_L
                      = 0x04D0;
                    = 0x04D0;
= 0x04D1;
= 0x04D2;
= 0x04D2;
 MPY32L H
 MPY32H
 _MPY32H_L
                    = 0x04D3;
 MPY32H_H
  MPYS32L
                     = 0x04D4;
  MPYS32L_L
                    = 0x04D4:
  MPYS32L_H
                    = 0x04D5;
 MPYS32H
                     = 0x04D6;
 MPYS32H_L
                    = 0 \times 04 D6;
  MPYS32H_H
                     = 0x04D7;
 MAC32L
                     = 0x04D8;
                    = 0x04D8;
  MAC32L_L
  MAC32L_H
                    = 0x04D9;
                    = 0x04DA;
= 0x04DA;
= 0x04DB;
= 0x04DC;
  MAC32H
  MAC32H_L
 MAC32H_H
  MACS32L
                   = 0x04DC;
= 0x04DC;
= 0x04DD;
= 0x04DE;
  MACS32L_L
  MACS32L_H
  MACS32H
                    = 0x04DE;
= 0x04DF;
= 0x04E0;
  MACS32H L
 MACS32H_H
__0P2L
                   = 0x04E0;
= 0x04E0;
= 0x04E1;
= 0x04E2;
= 0x04E3;
= 0x04E4;
= 0x04E4;
= 0x04E6;
= 0x04E6
 _OP2L_L
  OP2L_H
 OP2H
  OP2H_L
  OP2H_H
  RES0
  RES0_L
 RESO_H
  RES1
                    = 0x04E6;
= 0x04E6;
= 0x04E7;
= 0x04E8;
  RES1_L
  RES1_H
  RES2
                    = 0x04E8;
  RES2 L
                    = 0x04E9;
  RES2_H
 RES3
                     = 0x04EA;
  RES3 L
                     = 0x04EA;
  RES3_H
                      = 0x04EB;
                     = 0 \times 04 EC;
  MPY32CTL0
  MPY32CTL0 L
                      = 0x04EC
                = UXU4EC,
= 0x04ED;
  MPY32CTL0 H
/***********************
  PMM - Power Management System for FR2xx/FR4xx
*************************
              = 0x0120;
  PMMCTL0
                   = 0x0120;
= 0x0120;
= 0x0121;
= 0x0122;
= 0x0122;
= 0x0123;
= 0x0124;
= 0x0124;
= 0x0124;
= 0x0125;
= 0x012A;
  PMMCTL0_L
  PMMCTL0 H
  PMMCTL1
  PMMCTL1 L
  PMMCTL1_H
  PMMCTL2
  PMMCTL2 L
  PMMCTL2_H
  PMMIFG
                    = 0x012A;
= 0x012B;
= 0x012E;
  PMMIFG_L
  PMMIFG_H
  PMMIE
  PMMIE_L
                      = 0x012E
                      = 0x012F;
  PMMIE_H
  PM5CTL0
                      = 0x0130;
  PM5CTL0_L
                      = 0x0130;
  PM5CTL0_H
                       = 0x0131;
* DIGITAL I/O Port1/2 Pull up / Pull down Resistors
************************
```

```
__PAIN
                   = 0x0200;
                    = 0x0200;
 PAIN_L
 PAIN H
                    = 0x0201;
 PAOUT
                    = 0x0202;
 PAOUT L
                    = 0x0202;
 PAOUT H
                    = 0x0203;
                  = 0x0204;
= 0x0204;
= 0x0204;
 _PADIR
 _PADIR_L
                  = 0 \times 0205;
 _PADIR_H
                  = 0x0206;
 PAREN
                  = 0 \times 0206;
 PAREN L
 PAREN H
                  = 0x0207;
 PASEL0
                  = 0x020A;
                 = 0x020A;
= 0x020B;
 _PASEL0_L
 PASEL0_H
 _PASEL1
                  = 0x020C;
                 = 0x020C;
= 0x020D;
 PASEL1_L
 PASEL1_H
                  = 0x0218;
= 0x0218;
 PAIES
                 = 0x0219;
= 0x0219;
= 0x021A;
 PAIES_L
 _PAIES_H
 PAIE
                 = 0x021A;
= 0x021B;
= 0x021C;
 _PAIE_L
 PAIE_H
 PAIFG
                  = 0x021C;
 PAIFG L
                  = 0 \times 021D;
 PAIFG_H
__P1IV
                   = 0 \times 020E;
 P2IV
                   = 0x021E;
* DIGITAL I/O Port3 Pull up / Pull down Resistors
************************************
 PBIN
                    = 0x0220;
 PBIN_L
                    = 0x0220;
                    = 0x0221;
 PBIN_H
 _PB0UT
                    = 0x0222;
 PBOUT_L
                    = 0x0222;
                   = 0x0223;
 _PBOUT_H
                   = 0x0224;
 PBDIR
                   = 0x0224;
 PBDIR L
 PBDIR_H
                  = 0x0225;
 PBREN
                  = 0x0226;
___PBREN_L
                  = 0x0226;
___PBREN_H
                  = 0 \times 0227;
                 = 0x022A;
= 0x022A;
 PBSEL0
 PBSEL0_L
                  = 0 \times 022B;
 PBSEL0_H
 PBSEL1
                   = 0x022C;
 PBSEL1 L
                    = 0x022C;
            = 0x022D;
 PBSEL1_H
/*********
 Real-Time Clock (RTC) Counter
 RTCCTL
                    = 0x0300;
 RTCCTL_L
                   = 0x0300;
                  = 0 \times 0301;
 _RTCCTL_H
                  = 0x0304;
 RTCIV
                 = 0x0304;
= 0x0305;
= 0x0308;
__RTCIV_L
RTCIV H
__RTCMOD
                  = 0 \times 0308;
 RTCMOD L
                  = 0 \times 0309;
 RTCMOD_H
                    = 0x030C;
 RTCCNT
                    = 0x030C;
 RTCCNT L
                    = 0x030D;
 RTCCNT_H
/**********************************
* SFR - Special Function Register Module
 SFRIE1
                    = 0x0100;
                   = 0x0100;
 SFRIE1_L
                   = 0x0101;
 SFRIE1 H
 SFRIFG1
                    = 0x0102;
```

```
= 0x0102;
= 0x0103;
   _SFRIFG1_L
     _SFRIFG1_L
_SFRIFG1_H
                                                                = 0 \times 0104;
     SFRRPCR
     SFRRPCR L
                                                                 = 0 \times 0104;
                                                                       = 0x0105;
      SFRRPCR H
* SYS - System Module
                                   = 0x0140;
= 0x0140;
= 0x0141;
    _SYSCTL
  SYSCTL_L
SYSCTL_H
SYSCTL_H
SYSBSLC
SYSBSLC_L
SYSBSLC_L
SYSBSLC_H
SYSJMBC
SYSJMBC_L
SYSJMBC_H
SYSJMBIO_L
SYSJMBOO_L
SYSCFGO_L
SYS
     SYSCTL_L
     SYSCTL H
                                            = 0x0164;
= 0x0165;
     SYSCFG2 L
      SYSCFG2_H
<u>/*</u>******************
     Timer0_A3
**************************************
     TAOCTL = 0 \times 0380;
                                                          = 0x0380;
= 0x0382;
= 0x0384;
= 0x0390;
= 0x0392;
= 0x0394;
= 0x0396;
= 0x03AE;
     TA0CCTL0
     TA0CCTL1
    TA0CCTL2
    TA0R
    TA0CCR0
     TA0CCR1
    TA0CCR2
     TA0IV
                                                                       = 0x03A0;
     TA0EX0
/***********************************
* Timer1_A3
************************************
                                                                    = 0x03C0;
     TA1CTL
                                                                 = 0x03C2;
      TA1CCTL0
                                                                 = 0x03C4;
     _TA1CCTL1
                                                                = 0x03C6;
     TA1CCTL2
                                                                = 0x03D0;
    TA1R
   TA1CCR0
                                                                  = 0x03D2;
```

```
TA1CCR1
                    = 0x03D4;
                    = 0x03D6;
 TA1CCR2
 TA1IV
                   = 0x03EE;
                     = 0x03E0;
 TA1EX0
* Timer2 A2
                     = 0x0400;
 _TA2CTL
 _TA2CCTL0
                    = 0 \times 0402;
                    = 0x0404;
 TA2CCTL1
                    = 0x0410:
 TA2R
 TA2CCR0
                   = 0x0412
 TA2CCR1
                   = 0x0414;
                 = 0x042E;
 _TA2IV
 TA2EX0
                    = 0x0420;
 Timer3_A2
**************************************
                    = 0 \times 0440;
 TA3CTL
                   = 0x0442;
= 0x0444;
 TA3CCTL0
 _TA3CCTL1
                    = 0x0450;
 TA3R
                  = 0x0452;
= 0x0454;
= 0x046E;
 TA3CCR0
 _TA3CCR1
 TA3IV
                    = 0x0460:
 TA3EX0
/*********
*************************
 UCA0CTLW0
                    = 0 \times 0500;
                  = 0x0500;
= 0x0500;
= 0x0501;
= 0x0502;
= 0x0502;
= 0x0506;
= 0x0506;
= 0x0506;
 _UCA0CTLW0_L
 _UCA0CTLW0_H
 UCA0CTLW1
 UCA0CTLW1_L
 UCA0CTLW1_H
 UCA0BRW
 UCA0BRW_L
 UCA0BRW_H
                   = 0x0508;
 UCA0MCTLW
                   = 0x0508;
 UCA0MCTLW_L
                   = 0x0509;
 UCA0MCTLW_H
 UCA0STATW
                   = 0x050A;
 UCA0RXBUF
                   = 0x050C;
                  = 0x050C;
= 0x050D;
 UCA0RXBUF_L
 UCA0RXBUF_H
                  = 0x050D;
= 0x050E;
= 0x050F;
= 0x0510;
= 0x0512;
= 0x0512;
= 0x0513;
= 0x0514
 UCA0TXBUF
 UCA0TXBUF_L
 UCA0TXBUF_H
 UCA0ABCTL
 UCA0IRCTL
 UCA0IRCTL_L
UCA0IRCTL_H
 UCA01E
                  = 0x051A;
= 0x051B;
= 0x051C;
 UCA0IE_L
 UCA0IE_H
 UCA0IFG
                   = 0x051C;
 UCA0IFG_L
 UCA0IFG_H
                   = 0x051D;
 UCA0IV
                     = 0x051E;
/******
 USCI A1
***********************************
                    = 0x0520;
 UCA1CTLW0
                    = 0x0520;
 _UCA1CTLW0_L
 UCA1CTLW0_H
                     = 0x0521;
                    = 0x0522;
 UCA1CTLW1
                   = 0x0522;
 UCA1CTLW1_L
                   = 0x0523;
 UCA1CTLW1_H
 UCA1BRW
                    = 0x0526;
                   = 0x0526;
 UCA1BRW_L
                   = 0x0527;
 UCA1BRW H
 UCA1MCTLW
                    = 0x0528;
```

```
= 0x0528;
= 0x0529;
 _UCA1MCTLW_L
 UCA1MCTLW_H
 UCA1STATW
                 = 0x052A;
 _UCA11XBUF_L
_UCA1TXBUF_H
_UCA1ABCTL
                = 0x0532;
= 0x0532;
= 0x0533;
 UCA1IRCTL
 _UCA1IRCTL_L
_UCA1IRCTL_H
              = 0x053A;
= 0x053A;
= 0x053B;
= 0x053C;
= 0x053C;
 UCA1IE
 UCA1IE_L
 UCA1IE_H
 UCA1IFG
 UCA1IFG_L
            = 0x053D;
 UCA1IFG H
                  = 0x053E;
 UCA1IV
USCI B0
UCBOCTLWO = 0x0540;
                   = 0x0560;
 UCB0I2CSA
                   = 0x0560;
 _UCB012CSA_L
_UCB012CSA_H
 UCB0I2CSA L
                   = 0x0561;
                  = 0x056A;
 UCB0IE
                 = 0x056A;
 UCB0IE_L
                 = 0 \times 056B;
 UCB0IE_H
 UCB0IFG
                 = 0 \times 056C;
                = 0x056C;
= 0x056D;
 UCB0IFG_L
 UCB0IFG_H
 UCB0IV
                   = 0x056E;
```

```
WATCHDOG TIMER A
************************************
 WDTCTI
                    = 0x01CC;
 WDTCTL_L
                    = 0x01CC
                    = 0x01CD;
 WDTCTL H
 TLV Descriptors
Interrupt Vectors (offset from 0xFF80 + 0x10 for Password)
************************
/*INCLUDE periph.x end */
SECTIONS
{
  /* Read-only sections, merged into text segment. */
                 : { *(.hash)
: { *(.dynsym)
  .dynsym
                  : { *(.dynstr)
  .dynstr
                 : { *(.gnu.version)
  .gnu.version
  .gnu.version_d : { *(.gnu.version_d) }
 .rela.rodata : { *(.rela.rodata .rela.rodata.* .rela.gnu.linkonce.r.*)
.rel.data : { *(.rel.data .rel.data.* .rela.gnu.linkonce.d.*)
.rela.data : { *(.rela.data .rela.data.* .rela.gnu.linkonce.d.*)
.rel.bss : { *(.rel.bss .rel.bss.* .rel.gnu.linkonce.b.*)
                : { *(.rela.bss .rela.bss.* .rela.gnu.linkonce.b.*)
  .rela.bss
                : { *(.rel.ctors)
  .rel.ctors
  rela.ctors : { *(.rela.ctors) }
              : { *(.rel.dtors)
  .rel.dtors
               : { *(.rela.dtors) }
  .rela.dtors
               : { *(.rel.got)
  .rel.got
                                  }
               : { *(.rela.got)
  .rela.got
                                  }
               : { *(.rel.plt)
  .rel.plt
                                  }
               : { *(.rela.plt)
  .rela.plt
  .text :
 {
     . = ALIGN(2);
    KEEP(*(.init .init.*))
    KEEP(*(.init0)) /* Start here after reset.
                                                             */
    KEEP(*(.init1)) /* User definable.
                                                             */
    KEEP(*(.init2)) /* Initialize stack.
                                                             */
    KEEP(*(.init3)) /* Initialize hardware, user definable.
                                                             */
    KEEP(*(.init4)) /* Copy data to .data, clear bss.
                                                             */
    KEEP(*(.init5)) /* User definable.
    KEEP(*(.init6)) /* C++ constructors.
                                                             */
    KEEP(*(.init7)) /* User definable.
                                                             */
    KEEP(*(.init8)) /* User definable.
                                                             */
    KEEP(*(.init9)) /* Call main().
    KEEP(*(.fini9)) /* Falls into here after main(). User definable.
    KEEP(*(.fini8)) /* User definable.
    KEEP(*(.fini7)) /* User definable.
                                                                 */
    KEEP(*(.fini6))
                    /* C++ destructors.
                                                                 */
    KEEP(*(.fini5))
                    /* User definable.
    KEEP(*(.fini4))
                    /* User definable.
    KEEP(*(.fini3))
                    /* User definable.
    KEEP(*(.fini2)) /* User definable.
                                                                 */
    KEEP(*(.fini1)) /* User definable.
    KEEP(*(.fini0)) /* Infinite loop after program termination.
    KEEP(*(.fini .fini.*))
     . = ALIGN(2);
```

```
_ctors_start = . ;
  KEEP(*(.ctors))
   \_ctors_end = . ;
    _{dtors\_start} = . ;
  KEEP(*(.dtors))
  __dtors_end = . ;
   . = ALIGN(2);
  *(.text .text.* .gnu.linkonce.t.*)
   . = ALIGN(2);
} > REGION_TEXT
.rodata
   . = ALIGN(2);
  *(.rodata .rodata.* .gnu.linkonce.r.*)
  . = ALIGN(2);
} > REGION_TEXT
_etext = .; /* Past last read-only (loadable) segment */
.data :
{
   . = ALIGN(2);
  PROVIDE (__data_start = .) ;
  *(.data .data.* .gnu.linkonce.d.*)
   . = ALIGN(2);
   _edata = . ; /* Past last read-write (loadable) segment */
} > REGION_DATA AT > REGION_TEXT
PROVIDE (__data_load_start = LOADADDR(.data) );
PROVIDE (__data_size = SIZEOF(.data) );
{
  PROVIDE (__bss_start = .) ;
  *(.bss .bss.*)
  *(COMMON)
   . = ALIGN(2);
  PROVIDE (\_bss\_end = .);
 > REGION_DATA
PROVIDE (__bss_size = SIZEOF(.bss) );
.noinit
  PROVIDE (__noinit_start = .) ;
  *(.noinit .noinit.*)
   . = ALIGN(2);
  PROVIDE (__noinit_end = .) ;
} > REGION_DATA
 . = ALIGN(2);
 .infomem
  *(.infomem)
   . = ALIGN(2);
  *(.infomem.*)
 > infomem
.infomemnobits
  *(.infomemnobits)
   . = ALIGN(2);
  *(.infomemnobits.*)
} > infomem
.infoa
  *(.infoa .infoa.*)
} > infoa
.infob
  *(.infob .infob.*)
 > infob
.infoc
  *(.infoc .infoc.*)
 > infoc
.infod
  *(.infod .infod.*)
```

```
} > infod
.vectors :
   PROVIDE (__vectors_start = .) ;
  KEEP(*(.vectors*))
   _{vectors\_end} = . ;
} > vectors
.fartext :
    . = ALIGN(2);
  *(.fartext)
    . = ALIGN(2);
  *(.fartext.*)
   _efartext = .;
  > REGION_FAR_ROM
/* Stabs for profiling information*/
.profiler 0 : { *(.profiler) }
/* Stabs debugging sections.
.stab 0 : { *(.stab) }
.stabstr 0 : { *(.stabstr) }
.stab.excl 0 : { *(.stab.excl) }
.stab.exclstr 0 : { *(.stab.exclstr) }
.stab.index 0 : { *(.stab.index) }
.stab.indexstr 0 : { *(.stab.index) }
.stab.indexstr 0 : { *(.stab.indexstr) }
.comment 0 : { *(.comment) }
/* DWARF debug sections.
   Symbols in the DWARF debugging sections are relative to the beginning
   of the section so we begin them at 0. */
/* DWARF 1 */
                    0 : { *(.debug) }
. debug
                    0 : { *(.line) }
.line
/* GNU DWARF 1 extensions */
.debug_srcinfo 0 : { *(.debug_srcinfo) }
.debug_sfnames 0 : { *(.debug_sfnames) }
/* DWARF 1.1 and DWARF 2 */
.debug_aranges 0 : { *(.debug_aranges) }
.debug_pubnames 0 : { *(.debug_pubnames) }
/* DWARF 2 */
                    0 : { *(.debug_info) *(.gnu.linkonce.wi.*) }
0 : { *(.debug_abbrev) }
.debug_info
.debug_abbrev
                    0 : { *(.debug_line) }
.debug_line
                    0 : { *(.debug_frame) }
.debug_frame
                    0 : { *(.debug_str) }
.debug_str
                    0 : { *(.debug_loc) }
.debug_loc
.debug_macinfo 0 : { *(.debug_macinfo) }
/* DWARF 3 */
.debug_pubtypes 0 : { *(.debug_pubtypes) }
.debug_ranges 0 : { *(.debug_ranges) }
 PROVIDE (__stack = ORIGIN(ram) + LENGTH(ram));
 PROVIDE (__data_start_rom = _etext);
PROVIDE (__data_end_rom = _etext + SIZEOF (.data));
```