JEDEC STANDARD

Addendum No. 1 to JESD209A - Low Power Double Data Rate (LPDDR) SDRAM, 1.2 V I/O

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ADDENDUM NO. 1 TO JESD209A
LOW POWER DOUBLE DATA RATE (LPDDR) SDRAM, 1.2 V I/O

(From JEDEC Board Ballot JCB-08-77, formulated under the cognizance of the JC42.6 Subcommittee on low Power Memory.)

1   Scope

This document defines the Low Power Double Data Rate (LPDDR) SDRAM 1.2 V I/O specification, including AC and DC operating conditions, extended mode register settings, and I-V characteristics.

The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant 64 Mb through 2 Gb for x16 and x32 Low Power Double Data Rate SDRAM devices with 1.2 V I/O. System designs based on the required aspects of this specification will be supported by all LPDDR SDRAM vendors providing compliant devices.

This specification was created based on the LPDDR specification (JESD209A). Updates to this specification for 1.2 V I/O operation were considered and balloted. The accumulation of these ballots were then incorporated to prepare this LPDDR SDRAM specification addendum.

1.1   Applicable Documents

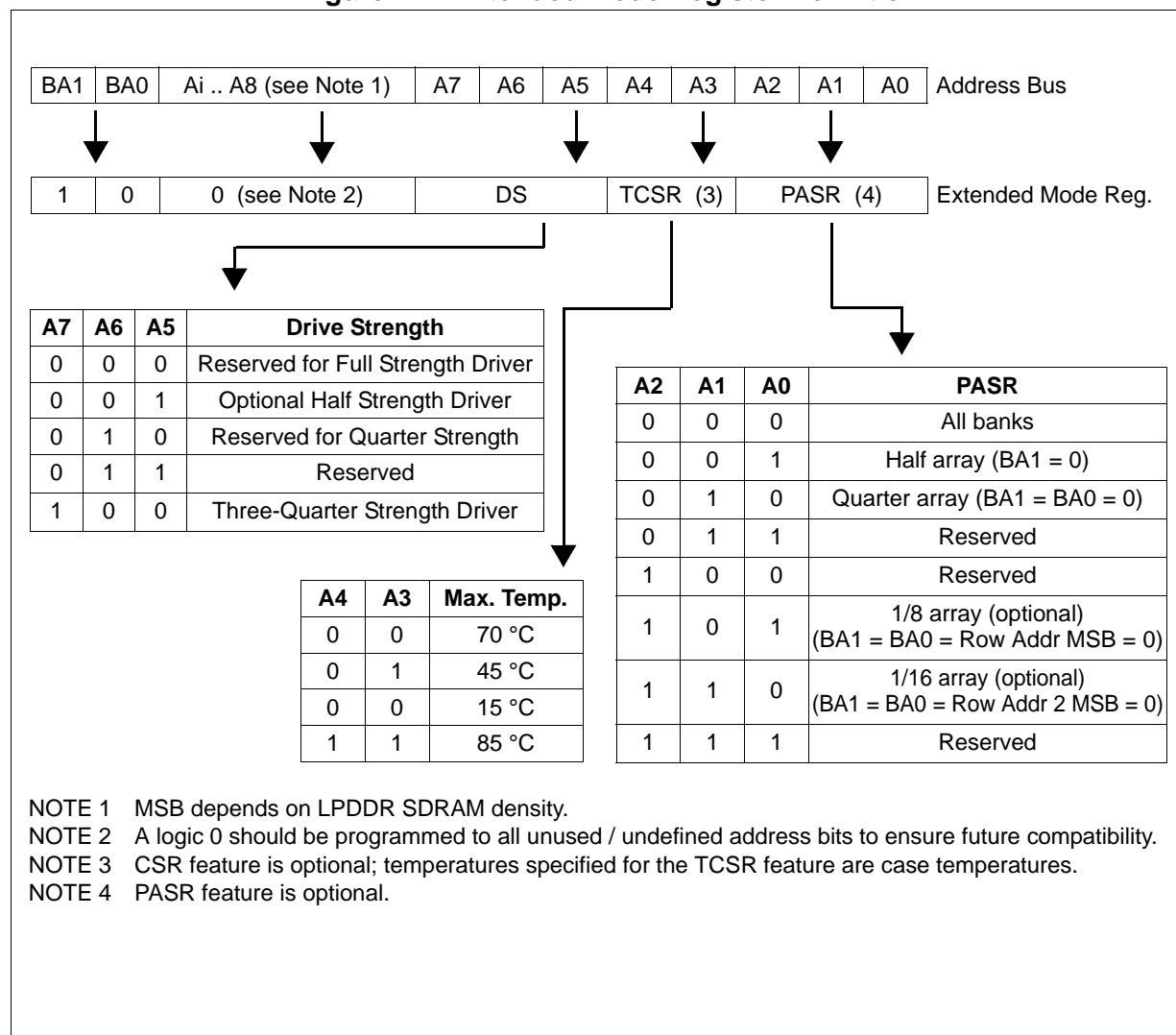1. JESD209A, Low Power Double Data Rate (LPDDR) SDRAM Standard

2   Extended Mode Register

This Extended Mode Register definition for 1.2 V I/O replaces the Extended Mode Register in JESD209A when 1.2 V I/O operation is required.

Address bits A0-A2 specify PASR, A3-A4 the TCSR, A5-A7 the Drive Strength. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

The drive strength may be set to half (optional) or three-quarter strength via address bits A5, A6, and A7. The I-V curves for half drive strength (optional) and three quarter-strength drivers for 1.2 V I/O are included in this document, see Figure 2 and Figure 3.

Figure 1 — Extended Mode Register Definition

BA1	BA0	Ai .. A8 (see Note 1)	A7	A6	A5	A4	A3	A2	A1	A0	Address Bus

1	0	0 (see Note 2)	DS	TCSR (3)	PASR (4)	Extended Mode Reg.

A7	A6	A5	Drive Strength
0	0	0	Reserved for Full Strength Driver
0	0	1	Optional Half Strength Driver
0	1	0	Reserved for Quarter Strength
0	1	1	Reserved
1	0	0	Three-Quarter Strength Driver

A2	A1	A0	PASR
0	0	0	All banks
0	0	1	Half array (BA1 = 0)
0	1	0	Quarter array (BA1 = BA0 = 0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	1/8 array (optional) (BA1 = BA0 = Row Addr MSB = 0)
1	1	0	1/16 array (optional) (BA1 = BA0 = Row Addr 2 MSB = 0)
1	1	1	Reserved

A4	A3	Max. Temp.
0	0	70 °C
0	1	45 °C
0	0	15 °C
1	1	85 °C

NOTE 1   MSB depends on LPDDR SDRAM density.
NOTE 2   A logic 0 should be programmed to all unused / undefined address bits to ensure future compatibility.
NOTE 3   CSR feature is optional; temperatures specified for the TCSR feature are case temperatures.
NOTE 4   PASR feature is optional.

3   AC/DC Operating Conditions

This section describes the updated AC/DC operating conditions required for 1.2 V I/O. Requirements in this section supercede the requirements in JESD209A when 1.2 V I/O operation is used.

Table 1 — Electrical Characteristics and AC/DC Operating Conditions 1.2V I/O

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNIT	NOTES
Supply Voltage	VDD	1.7	1.9	V	-
I/O Supply Voltage	VDDQ	1.14	1.30	V	-
Address and Command Inputs (A0 - An, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)					
Input High Voltage	VIH	0.9 ∗ VDDQ	VDDQ +0.2	V	-
Input Low Voltage	VIL	-0.2	0.1 ∗ VDDQ	V	-
Clock Inputs (CK, $\overline{CK}$)					
DC Input Voltage	VIN	-0.2	VDDQ +0.2	V	-
DC Input Differential Voltage	VID(DC)	0.4 ∗ VDDQ	VDDQ +0.4	V	2
AC Input Differential Voltage	VID(AC)	0.6 ∗ VDDQ	VDDQ +0.4	V	2
AC Differential Crosspoint Voltage	VIX	0.4 ∗ VDDQ	0.6 ∗ VDDQ	V	3
Data Inputs (DQ, DM, DQS)					
DC Input High Voltage	VIHD(DC)	0.8 ∗ VDDQ	VDDQ +0.2	V	-
DC Input Low Voltage	VILD(DC)	-0.2	0.2 ∗ VDDQ	V	-
AC Input High Voltage	VIHD(AC)	0.9 ∗ VDDQ	VDDQ +0.2	V	-
AC Input Low Voltage	VILD(AC)	-0.2	0.1 ∗ VDDQ	V	-
Data Outputs (DQ, DQS)					
DC Output High Voltage (IOH = -0.1mA)	VOH	0.9 ∗ VDDQ	-	V	-
DC Output Low Voltage (IOL = 0.1mA)	VOL	-	0.1 ∗ VDDQ	V	-

NOTE 1   All voltages referenced to VSS and VSSQ must be same potential.

NOTE 2   VID(DC) and VID(AC) are magnitude of the difference between the input level on CK and the input level on CBK.

NOTE 3   The value of VIX is expected to be 0.5*VDDQ and must track variations in the DC level of the same.

3   AC/DC Operating Conditions (cont'd)

3.1   Driver Characteristics for 1.2 V I/O

LPDDR SDRAM output driver characteristics are defined for three-quarter drive strength and optional half drive strength operation as selected in the Extended Mode Register. Table 2 shows the data in a tabular format suitable for input into simulation tools. Figure 2 and Figure 3 show the driver strength characteristics graphically.

Table 2 — I-V Curves for Three-Quarters and Optional Half Drive Strength

VOLTAGE [V]	THREE-QUARTERS STRENGTH DRIVER				HALF STRENGTH DRIVER (optional)			
	PULL-DOWN CURRENT [mA]		PULL-UP CURRENT [mA]		PULL-DOWN CURRENT [mA]		PULL-UP CURRENT [mA]	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.10	1.96	9.38	-1.96	-9.38	1.27	6.15	-1.27	-6.15
0.20	3.92	12.97	-3.92	-12.97	2.55	8.42	-2.55	-8.42
0.30	5.88	15.87	-5.88	-15.87	3.82	10.15	-3.82	-10.15
0.40	7.84	18.33	-7.84	-18.33	5.09	11.60	-5.09	-11.60
0.50	9.80	20.34	-9.80	-20.34	6.36	13.25	-6.36	-13.25
0.60	11.10	22.63	-11.10	-22.63	7.20	14.67	-7.20	-14.67
0.70	11.10	25.03	-11.10	-25.03	7.20	15.91	-7.20	-15.91
0.80	11.10	27.14	-11.10	-27.14	7.20	17.38	-7.20	-17.38
0.90	11.10	29.91	-11.10	-29.91	7.20	18.99	-7.20	-18.99
1.00	11.10	32.18	-11.10	-32.18	7.20	20.60	-7.20	-20.60
1.10	11.10	34.95	-11.10	-34.95	7.20	22.21	-7.20	-22.21
1.20	11.10	37.78	-11.10	-37.78	7.20	23.82	-7.20	-23.82
1.30		40.58		-40.58		25.53		-25.53

NOTE 1   Based on nominal impedance of 37 Ohms (three-quarters) and 55 Ohms (half: optional) at $V_{DDQ}/2$

NOTE 2   The full variation in driver current from minimum to maximum due to process, temperature and voltage will lie within the outer bounding lines of the I-V curve.
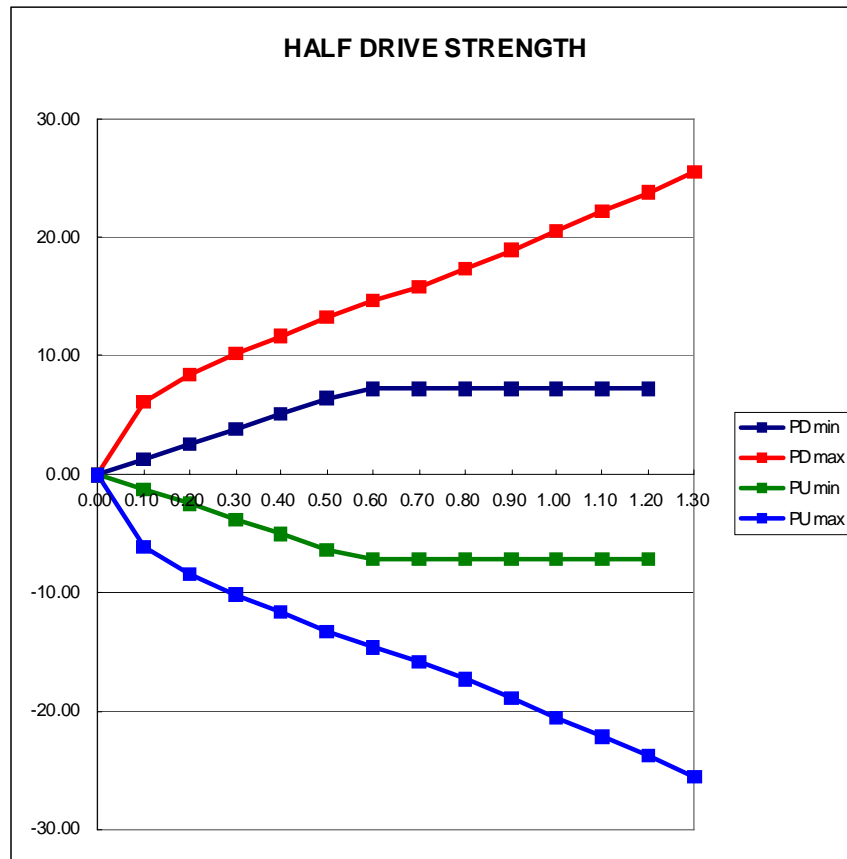
3   AC/DC Operating Conditions (cont'd)

Figure 2 — I-V Curves for Three-Quarter Drive Strength
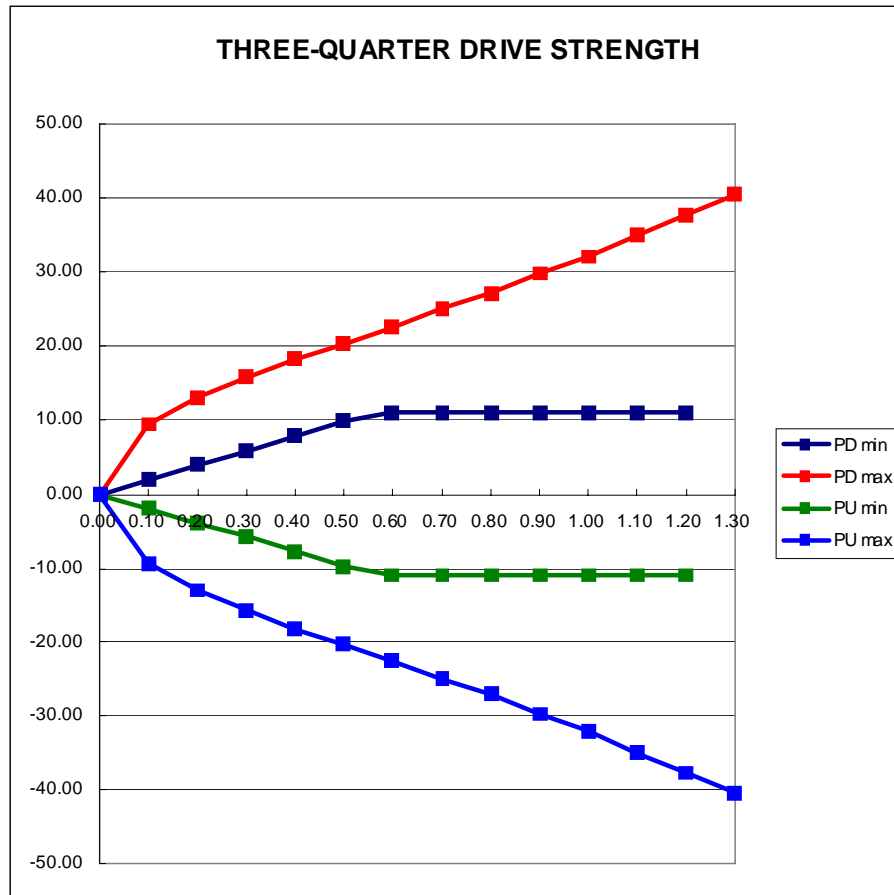
3   AC/DC Operating Conditions (cont'd)

Figure 3 — I-V Curves for Half Drive Strength (Optional)

HALF DRIVE STRENGTH