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Low Power Double Data Rate 2 (LPDDR2)

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LOW POWER DOUBLE DATA RATE 2 (LPDDR2)

(From JEDEC Board ballot JCB-09-01, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memory.)

1 Scope

This document defines the LPDDR2 specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. This specification covers the following technologies: LPDDR2-S2A, LPDDR2-S2B, LPDDR2-S4A, LPDDR2-S4B, LPDDR2-N-A, and LPDDR2-N-B. The purpose of this specification is to define the minimum set of requirements for JEDEC compliant 64 Mb through 8 Gb for x8, x16, and x32 SDRAM devices as well as 64 Mb through 32 Gb for x8, x16, and x32 for NVM devices. This specification was created using aspects of the following specifications: DDR2 (JESD79-2), DDR3 (JESD79-3), LPDDR (JESD209), and LPDDR-NVM (N07-NV1A). Each aspect of the specification were considered and approved by committee ballot(s). The accumulation of these ballots were then incorporated to prepare the LPDDR2 specification.

2 Package ballout & addressing

2.1 LPDDR2 SDRAM NVM package ballout

This area is currently under development, this is a place holder for future material.

2.2 LPDDR2 Pad Sequence

Table 1 — LPDDR2 Pad Sequence

CA Pad Sequence						DQ Pad Sequence													
						x32					x16					x8			
S4	S2A	S2B	N-A	N-B		S4	S2A	S2B	N-A	N-B	S4	S2A	S2B	N-A	N-B	S2A	S2B	N-A	N-B
VDD2		VDD2		VDD2		VDD2		VDD2		VDD2	VDD2		VDD2		VDD2		VDD2		VDD2
VSS		VSS		VSS		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS		VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1
VDD1	VDD1	VDD1	VDD1	VDD1		VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1
VDD2		VDD2		VDD2		VDDQ	VDDQ*1	VDDQ*1	VDDQ*1	VDDQ*1									
VSS		VSS		VSS		VSSQ	VSSQ	VSSQ	VSSQ	VSSQ									
						DQ31	DQ31	DQ31	DQ31	DQ31									
						DQ30	DQ30	DQ30	DQ30	DQ30									
						VDDQ	VDDQ	VDDQ	VDDQ	VDDQ									
						DQ29	DQ29	DQ29	DQ29	DQ29									
						DQ28	DQ28	DQ28	DQ28	DQ28									
						VSSQ	VSSQ	VSSQ	VSSQ	VSSQ									
						DQ27	DQ27	DQ27	DQ27	DQ27									
						DQ26	DQ26	DQ26	DQ26	DQ26									
						VDDQ	VDDQ	VDDQ	VDDQ	VDDQ									
						DQ25	DQ25	DQ25	DQ25	DQ25									
						DQ24	DQ24	DQ24	DQ24	DQ24									
						VSSQ	VSSQ	VSSQ	VSSQ	VSSQ									
						DQS3_t	DQS3_t	DQS3_t	DQS3_t	DQS3_t									
						DQS3_c	DQS3_c	DQS3_c	DQS3_c	DQS3_c									
						VDDQ	VDDQ	VDDQ	VDDQ	VDDQ									
						DM3	DM3	DM3	DM3	DM3									
						VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ				
						DQ15	DQ15	DQ15	DQ15	DQ15	DQ15	DQ15	DQ15	DQ15	DQ15				
						DQ14	DQ14	DQ14	DQ14	DQ14	DQ14	DQ14	DQ14	DQ14	DQ14				
						VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ				
						DQ13	DQ13	DQ13	DQ13	DQ13	DQ13	DQ13	DQ13	DQ13	DQ13				
						DQ12	DQ12	DQ12	DQ12	DQ12	DQ12	DQ12	DQ12	DQ12	DQ12				
						VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ				
						DQ11	DQ11	DQ11	DQ11	DQ11	DQ11	DQ11	DQ11	DQ11	DQ11				
						DQ10	DQ10	DQ10	DQ10	DQ10	DQ10	DQ10	DQ10	DQ10	DQ10				
						VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ				
ZQ			ZQ	ZQ		DQ9	DQ9	DQ9	DQ9	DQ9	DQ9	DQ9	DQ9	DQ9	DQ9				
CA9	CA9	CA9	CA9	CA9		DQ8	DQ8	DQ8	DQ8	DQ8	DQ8	DQ8	DQ8	DQ8	DQ8				
CA8	CA8	CA8	CA8	CA8		VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ				
VSSCA	VSSCA	VSSCA	VSSCA	VSSCA		DQS1_t	DQS1_t	DQS1_t	DQS1_t	DQS1_t	DQS1_t	DQS1_t	DQS1_t	DQS1_t	DQS1_t				
VDDCA	VDDCA	VDDCA	VDDCA	VDDCA		DQS1_c	DQS1_c	DQS1_c	DQS1_c	DQS1_c	DQS1_c	DQS1_c	DQS1_c	DQS1_c	DQS1_c				
CA7	CA7	CA7	CA7	CA7		VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ				
CA6	CA6	CA6	CA6	CA6		DM1	DM1	DM1	DM1	DM1	DM1	DM1	DM1	DM1	DM1				
CA5	CA5	CA5	CA5	CA5		VSSQ	VSSQ*1	VSSQ*1	VSSQ*1	VSSQ*1	VSSQ	VSSQ*1	VSSQ*1	VSSQ*1	VSSQ*1				
	VDD1		VDD1			VDDQ	VDDQ*1	VDDQ*1	VDDQ*1	VDDQ*1	VDDQ	VDDQ*1	VDDQ*1	VDDQ*1	VDDQ*1				
VDD2		VDD2		VDD2			VDD1		VDD1			VDD1		VDD1		VDD1		VDD1	
Vref(CA)	Vref(CA)	Vref(CA)	Vref(CA)	Vref(CA)		VDD2		VDD2		VDD2	VDD2		VDD2		VDD2		VDD2		VDD2
VSS	VSS	VSS	VSS	VSS		VSS	VSS	VSS	VSS*1	VSS*1	VSS	VSS	VSS	VSS*1	VSS*1	VSS	VSS	VSS*1	VSS
VDDCA	VDDCA	VDDCA	VDDCA	VDDCA		Vref(DQ)	Vref(DQ)	Vref(DQ)	Vref(DQ)	Vref(DQ)	Vref(DQ)	Vref(DQ)	Vref(DQ)	Vref(DQ)	Vref(DQ)	Vref(DQ)	Vref(DQ)	Vref(DQ)	Vref(DQ)
CK_c	CK_c	CK_c	CK_c	CK_c															
CK_t	CK_t	CK_t	CK_t	CK_t															
VSSCA	VSSCA	VSSCA	VSSCA	VSSCA		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
CKE	CKE	CKE	CKE	CKE		VDD2		VDD2		VDD2*1	VDD2		VDD2		VDD2*1		VDD2		VDD2*1
CS_N	CS_N	CS_N	CS_N	CS_N			VDD1		VDD1*1			VDD1		VDD1*1		VDD1		VDD1*1	
CA4	CA4	CA4	CA4	CA4		VDDQ	VDDQ*1	VDDQ*1	VDDQ*1	VDDQ*1	VDDQ	VDDQ*1	VDDQ*1	VDDQ*1	VDDQ*1	VDDQ*1	VDDQ*1	VDDQ*1	VDDQ*1
CA3	CA3	CA3	CA3	CA3		VSSQ	VSSQ*1	VSSQ*1	VSSQ*1	VSSQ*1	VSSQ	VSSQ*1	VSSQ*1	VSSQ*1	VSSQ*1	VSSQ*1	VSSQ*1	VSSQ*1	VSSQ*1
CA2	CA2	CA2	CA2	CA2		DM0	DM0	DM0	DM0	DM0	DM0	DM0	DM0	DM0	DM0	DM0	DM0	DM0	DM0
VDDCA	VDDCA	VDDCA	VDDCA	VDDCA		VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ
VSSCA	VSSCA	VSSCA	VSSCA	VSSCA		DQS0_c	DQS0_c	DQS0_c	DQS0_c	DQS0_c	DQS0_c	DQS0_c	DQS0_c	DQS0_c	DQS0_c	DQS0_c	DQS0_c	DQS0_c	DQS0_c
CA1	CA1	CA1	CA1	CA1		DQS0_t	DQS0_t	DQS0_t	DQS0_t	DQS0_t	DQS0_t	DQS0_t	DQS0_t	DQS0_t	DQS0_t	DQS0_t	DQS0_t	DQS0_t	DQS0_t
CA0	CA0	CA0	CA0	CA0		VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ
						DQ7	DQ7	DQ7	DQ7	DQ7	DQ7	DQ7	DQ7	DQ7	DQ7	DQ7	DQ7	DQ7	DQ7
						DQ6	DQ6	DQ6	DQ6	DQ6	DQ6	DQ6	DQ6	DQ6	DQ6	DQ6	DQ6	DQ6	DQ6
						VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ
						DQ5	DQ5	DQ5	DQ5	DQ5	DQ5	DQ5	DQ5	DQ5	DQ5	DQ5	DQ5	DQ5	DQ5
						DQ4	DQ4	DQ4	DQ4	DQ4	DQ4	DQ4	DQ4	DQ4	DQ4	DQ4	DQ4	DQ4	DQ4
						VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ
						DQ3	DQ3	DQ3	DQ3	DQ3	DQ3	DQ3	DQ3	DQ3	DQ3	DQ3	DQ3	DQ3	DQ3
						DQ2	DQ2	DQ2	DQ2	DQ2	DQ2	DQ2	DQ2	DQ2	DQ2	DQ2	DQ2	DQ2	DQ2
						VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ
						DQ1	DQ1	DQ1	DQ1	DQ1	DQ1	DQ1	DQ1	DQ1	DQ1	DQ1	DQ1	DQ1	DQ1
						DQ0	DQ0	DQ0	DQ0	DQ0	DQ0	DQ0	DQ0	DQ0	DQ0	DQ0	DQ0	DQ0	DQ0
						VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ	VSSQ
						DM2	DM2	DM2	DM2	DM2									
						VDDQ	VDDQ	VDDQ	VDDQ	VDDQ									
						DQS2_c	DQS2_c	DQS2_c	DQS2_c	DQS2_c									
						DQS2_t	DQS2_t	DQS2_t	DQS2_t	DQS2_t									
						VSSQ	VSSQ	VSSQ	VSSQ	VSSQ									
						DQ23	DQ23	DQ23	DQ23	DQ23									
						DQ22	DQ22	DQ22	DQ22	DQ22									
						VDDQ	VDDQ	VDDQ	VDDQ	VDDQ									
						DQ21	DQ21	DQ21	DQ21	DQ21									
						DQ20	DQ20	DQ20	DQ20	DQ20									
						VSSQ	VSSQ	VSSQ	VSSQ	VSSQ									
						DQ19	DQ19	DQ19	DQ19	DQ19									
						DQ18	DQ18	DQ18	DQ18	DQ18									
						VDDQ	VDDQ	VDDQ	VDDQ	VDDQ									
						DQ17	DQ17	DQ17	DQ17	DQ17									
						DQ16	DQ16	DQ16	DQ16	DQ16									
						VSSQ	VSSQ	VSSQ	VSSQ	VSSQ									
VSS		VSS		VSS		VDDQ	VDDQ*1	VDDQ*1	VDDQ*1	VDDQ*1									
VDD2		VDD2		VDD2					VACC	VACC				VACC	VACC			VACC	VACC
VDD1	VDD1	VDD1	VDD1	VDD1		VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1
VSS	VSS	VSS	VSS	VSS		VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1	VSS*1
VSS		VSS		VSS		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
VDD2		VDD2		VDD2		VDD2		VDD2		VDD2	VDD2		VDD2		VDD2		VDD2		VDD2

NOTE 1 Pads with (*1) are optional.

NOTE 2 Ordering of DQ bits shall be maintained in the system, including within the package and on the PCB. DQ byte swapping and DQ bit Swapping are not allowed in the system.

2.3 Input/output functional description

2.3.1 Pad Definition and Description

Table 2 — Pad Definition and Description

Name	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table on page 135 for command code descriptions. CKE is sampled at the positive Clock edge.
CS_n	Input	**Chip Select:** CS_n is considered part of the command code. See Command Truth Table on page 135 for command code descriptions. CS_n is sampled at the positive Clock edge.
CA0 - CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code. See Command Truth Table on page 135 for command code descriptions.
DQ0-DQ7 (x8) DQ0 - DQ15 (x16) DQ0 - DQ31 (x32)	I/O	**Data Inputs/Output:** Bi-directional data bus
DQS0_t, DQS0_c (x8) DQS0_t, DQS0_c, DQS1_t, DQS1_c (x16) DQS0_t - DQS3_t, DQS0_c - DQS3_c (x32)	I/O	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x8, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7. For x16, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7; DQS1_t and DQS1_c to the data on DQ8 - DQ15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31.
DM0 (x8) DM0-DM1 (x16) DM0 - DM3 (x32)	Input	**Input Data Mask:** For LPDDR2 devices that do not support the DNV feature, DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS_c). DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.

Name	Type	Description
DM0/DNV0 (x8) DM0/DNV0-DM1/DNV1 (x16) DM0/DNV0 - DM3/DNV3 (x32)	I/0	**Input Data Mask/Data Not Valid:** For LPDDR2 devices that support the DNV feature, DM/DNV is bidirectional (used for write and read data). It is output with read data, input with write data. DM/DNV is the input mask signal for write data and is an output signal validating a read burst. For data write accesses: Input data is masked when DM/DNV is sampled HIGH coincident with DQ input data during a WRITE access. DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31. For data read accesses: See "LPDDR2: Data Not Valid" on page 80 for detailed description of DNV functionality. DNV0, DNV1, DNV2, and DNV3 are driven coincident with output read data. DNV0, DNV1, DNV2, and DNV3 are driven with the same value and shall be sampled with DQS0, DQS1, DQS2, and DQS3 respectively. The DM/DNV loading shall match the DQ and DQS_t (or DQS_c) loading.
V_{DD1}	Supply	**Core Power Supply 1:** Core power supply for LPDDR2-N and LPDDR2-SX devices.
V_{DD2}	Supply	**Core Power Supply 2:** Core power supply for LPDDR2-S2B, LPDDR2-S4 and LPDDR2-N-B devices.
V_{DDCA}	Supply	**Input Receiver Power Supply:** Power supply for CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
V_{DDQ}	Supply	**I/O Power Supply:** Power supply for Data input/output buffers.
V_{ACC}	Supply	**NVM Acceleration Supply:** NVM device specific embedded operation acceleration. V_{ACC} enables some NVM device specific functionality. When not used for NVM device specific functionality, V_{ACC} shall be driven to a level of V_{DD1}.
$V_{REF(CA)}$	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
$V_{REF(DQ)}$	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all Data input buffers.
V_{SS}	Supply	**Ground**
V_{SSCA}	Supply	**Ground for Input Receivers**
V_{SSQ}	Supply	**I/O Ground**
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

NOTE 1 Data includes DQ and DM.

2.4 LPDDR2 SDRAM Addressing

Table 3 — LPDDR2 SDRAM Addressing

Items		64Mb	128Mb	256Mb	512Mb	1Gb		2Gb		4Gb	8Gb
Device Type		S2/S4	S2/S4	S2/S4	S2/S4	S2	S4	S2	S4	S2/S4	S2/S4
Number of Banks		4	4	4	4	4	8	4	8	8	8
Bank Addresses		BA0-BA1	BA0-BA1	BA0-BA1	BA0-BA1	BA0-BA1	BA0-BA2	BA0-BA1	BA0-BA2	BA0-BA2	BA0-BA2
t_{REFI}(us)[*2]		15.6	15.6	7.8	7.8	7.8	7.8	3.9	3.9	3.9	3.9
x8	Row Addresses	R0-R11	R0-R11	R0-R12	R0-R12	R0-R13	R0-R12	R0-R14	R0-R13	R0-R13	R0-R14
	Column Addresses[*1]	C0-C8	C0-C9	C0-C9	C0-C10	C0-C10	C0-C10	C0-C10	C0-C10	C0-C11	C0-C11
x16	Row Addresses	R0-R11	R0-R11	R0-R12	R0-R12	R0-R13	R0-R12	R0-R14	R0-R13	R0-R13	R0-R14
	Column Addresses[*1]	C0-C7	C0-C8	C0-C8	C0-C9	C0-C9	C0-C9	C0-C9	C0-C9	C0-C10	C0-C10
x32	Row Addresses	R0-R11	R0-R11	R0-R12	R0-R12	R0-R13	R0-R12	R0-R14	R0-R13	R0-R13	R0-R14
	Column Addresses[*1]	C0-C6	C0-C7	C0-C7	C0-C8	C0-C8	C0-C8	C0-C8	C0-C8	C0-C9	C0-C9

NOTE 1 The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

NOTE 2 t_{REFI} values for all bank refresh is Tc = -25~85 °C, Tc means Operating Case Temperature

NOTE 3 Row and Column Address values on the CA bus that are not used are “don’t care.”

2.5 LPDDR2 NVM Addressing

2.5.1 Three-Phase Addressing

The memory controller delivers an array address to the memory in three phases (See Figure 1 on page 6 and Figure 2 on page 7). The Command Truth Table on page 135 defines the required assignment of logical address bits to CA pins. Scrambling of the logical address bits in any order different than those described in the Command truth table is prohibited.

During a Preactive command, part of a row address (driven on the CA input pins) is stored in a Row Address Buffer (RAB) selected by BA2-BA0.

During an Activate command, BA2-BA0 select an RAB to retrieve the first part of the row address. Meanwhile, the remainder of the row address is driven on the CA input pins. These two parts of the row address select one row from the memory array. Activate also causes internal sensing circuits to transfer that memory content into a Row Data Buffer (RDB) also selected by BA2-BA0.

An {RAB, RDB} pair selected by BA2-BA0 is referred to as a Row Buffer (RB). BA2-BA0 do not address any portion of the array and only select an RAB into which address is placed and/or an RDB into which data is placed. The controller may use any value of BA2-BA0 for any array location.

During a Read or Write command BA2-BA0 selects an RDB, and the column address is driven on the CA input pins to choose the starting address of the read or write burst.

The Preactive command is optional when the desired RAB already contains the desired partial row address. The Activate command is optional when the desired RDB already contains the desired memory content.

Upon completion of Device Auto-Initialization, all Row Buffers are in the Idle state, and RABs contain 0x0000 and all RDBs contain indeterminate values.

2.5.1 Three-Phase Addressing (cont'd)

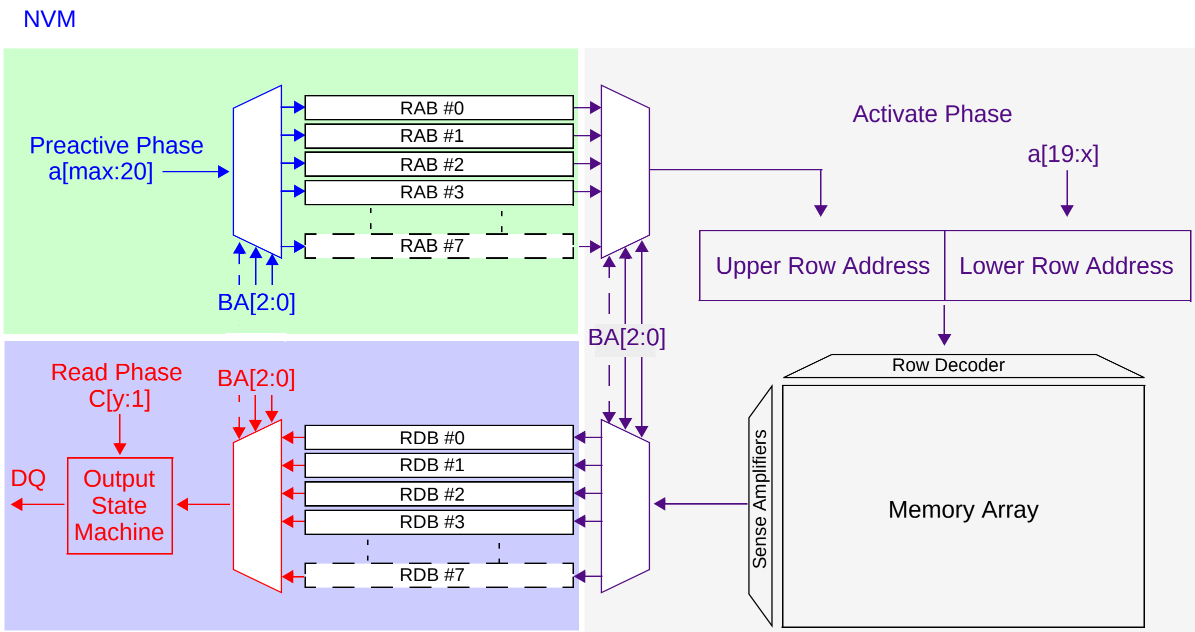


Figure 1 — LPDDR2-N: Three-Phase Address Read

NOTE 1 In the Preactive phase, a[max] is dependent on the density of the NVM device.

NOTE 2 In the Activate phase, the lower order row address bit a[x] is dependent on the size of the Row Data Buffer (RDB).

NOTE 3 In the Read phase, column address bit C[y] is dependent on the size of the Row Data Buffer (RDB) and the data bus width.

NOTE 4 An {RAB, RDB} pair selected by BA[2:0] is referred to as a Row Buffer (RB).

NOTE 5 The least significant column address C0 is implied to be zero and is not transmitted on the CA bus.

NOTE 6 An {RAB, RDB} pair can be associated with any portion of the memory array.

2.5.1 Three-Phase Addressing (cont'd)

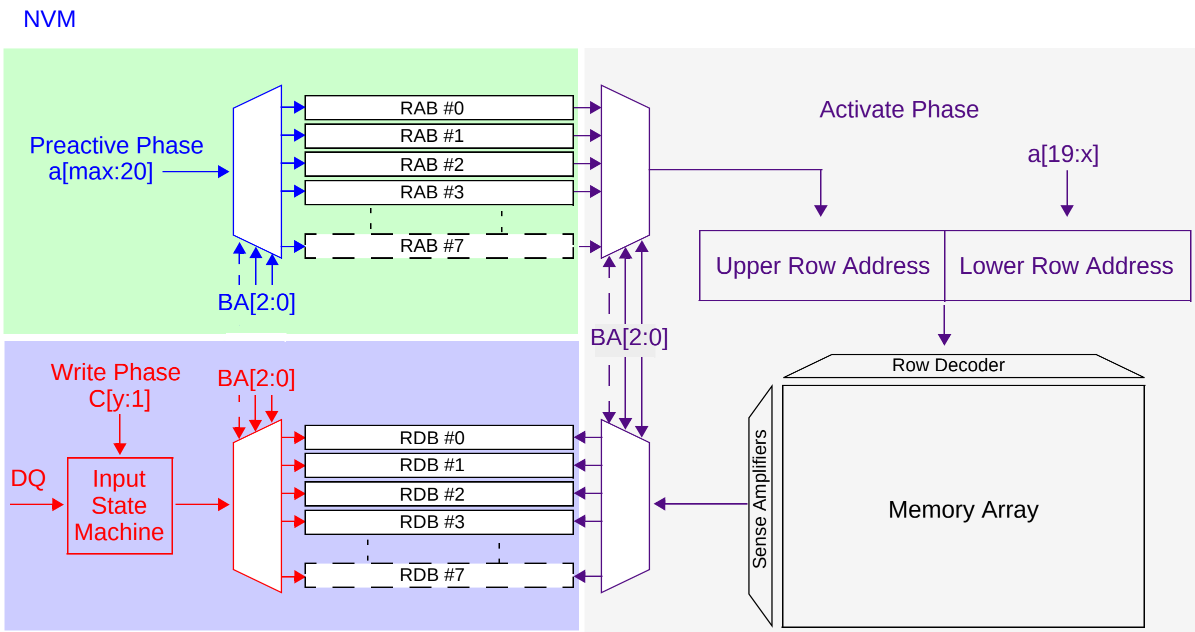


Figure 2 — LPDDR2-N: Three-Phase Address Write

NOTE 1 In the Preactive phase, a[max] is dependent on the density of the NVM device.

NOTE 2 In the Activate phase, the lower order row address bit a[x] is dependent on the size of the Row Data Buffer (RDB).

NOTE 3 In the Read phase, column address bit C[y] is dependent on the size of the Row Data Buffer (RDB) and the data bus width.

NOTE 4 An {RAB, RDB} pair selected by BA[2:0] is referred to as a Row Buffer (RB).

NOTE 5 The least significant column address C0 is implied to be zero and is not transmitted on the CA bus.

Table 4 — 64 Mb Addressing

Configuration	8 Mb x 8	4 Mb x 16	2 Mb x 32
# of Row Buffers*2,3	4	4	4
Upper Row Address (PREACTIVE)	a22-a20	a22-a20	a22-a20
Lower Row Address (ACTIVE)*1	a19-A5	a19-a5	a19-a5
Column Address (READ/WRITE)*1,4	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size*1	32 Bytes	32 Bytes	32 Bytes

Table 5 — 128 Mb Addressing

Configuration	16 Mb x 8	8 Mb x 16	4 Mb x 32
# of Row Buffers*2,3	4	4	4
Upper Row Address (PREACTIVE)	a23-a20	a23-a20	a23-a20
Lower Row Address (ACTIVE)*1	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE)*1,4	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size*1	32 Bytes	32 Bytes	32 Bytes

2.5.1 Three-Phase Addressing (cont'd)

Table 6 — 256 Mb addressing

Configuration	32 Mb x 8	16 Mb x 16	8 Mb x 32
# of Row Buffers*2,3	4	4	4
Upper Row Address (PREACTIVE)	a24-a20	a24-a20	a24-a20
Lower Row Address (ACTIVE)*1	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE)*1,4	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size*1	32 Bytes	32 Bytes	32 Bytes

Table 7 — 512 Mb addressing

Configuration	64 Mb x 8	32 Mb x 16	16 Mb x 32
# of Row Buffers*2,3	4	4	4
Upper Row Address (PREACTIVE)	a25-a20	a25-a20	a25-a20
Lower Row Address (ACTIVE)*1	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE)*1,4	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size *1	32 Bytes	32 Bytes	32 Bytes

Table 8 — 1 Gb addressing

Configuration	128 Mb x 8	64 Mb x 16	32 Mb x 32
# of Row Buffers*2,3	4	4	4
Upper Row Address (PREACTIVE)	a26-a20	a26-a20	a26-a20
Lower Row Address (ACTIVE)*1	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE)*1,4	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size *1	32 Bytes	32 Bytes	32 Bytes

Table 9 — 2 Gb addressing

Configuration	256 Mb x 8	128 Mb x 16	64 Mb x 32
# of Row Buffers*2,3	4	4	4
Upper Row Address (PREACTIVE)	a27-a20	a27-a20	a27-a20
Lower Row Address (ACTIVE)*1	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE)*1,4	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size *1	32 Bytes	32 Bytes	32 Bytes

Table 10 — 4 Gb addressing

Configuration	512 Mb x 8	256 Mb x 16	128 Mb x 32
# of Row Buffers*2,3	4	4	4
Upper Row Address (PREACTIVE)	a28-a20	a28-a20	a28-a20
Lower Row Address (ACTIVE)*1	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE)*1,4	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size *1	32 Bytes	32 Bytes	32 Bytes

2.5.1 Three-Phase Addressing (cont'd)

Table 11 — 8 Gb addressing

Configuration	1 Gb x 8	512 Mb x 16	256 Mb x 32
# of Row Buffers*2,3	4	4	4
Upper Row Address (PREACTIVE)	a29-a20	a29-a20	a29-a20
Lower Row Address (ACTIVE)*1	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE)*1,4	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size *1	32 Bytes	32 Bytes	32 Bytes

Table 12 — 16 Gb addressing

Configuration	2 Gb x 8	1 Gb x 16	512 Mb x 32
# of Row Buffers*2,3	4	4	4
Upper Row Address (PREACTIVE)	a30-a20	a30-a20	a30-a20
Lower Row Address (ACTIVE)*1	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE)*1,4	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size *1	32 Bytes	32 Bytes	32 Bytes

Table 13 — 32 Gb addressing

Configuration	4 Gb x 8	2 Gb x 16	1 Gb x 32
# of Row Buffers*2,3	4	4	4
Upper Row Address (PREACTIVE)	a31-a20	a31-a20	a31-a20
Lower Row Address (ACTIVE)*1	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE)*1,4	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size *1	32 Bytes	32 Bytes	32 Bytes

Notes for Tables 4-13

NOTE 1 All tables above show examples using minimum 32 Byte RDB Size, see Table 14 on page 10 for other RDB sizes.

NOTE 2 The number of Row Buffers can be 4 or 8. A controller may use a smaller number of Row Buffers provided that the appropriate most significant BA addresses are driven to "0".

NOTE 3 One Row Buffer consists of a pair of one Row Address Buffer (RAB) and one Row Data Buffer (RDB), selected by Buffer Address, BA0-BA2 (CA7r-CA9r).

NOTE 4 The least significant column address C0 is implied to be zero and is not transmitted on the CA bus.

NOTE 5 Row and Column Address values on the CA bus that are not used are "don't care."

2.5.1 Three-Phase Addressing (cont'd)

Table 14 — Addressing Dependent on RDB Size

RDB Size	Configuration	x8	x16	x32
32 Byte	Lower Row Address	a19-a5	a19-a5	a19-a5
	Column Address	a4-a1(C4-C1)	a4-a2(C3-C1)	a4-a3(C2-C1)
64 Byte	Lower Row Address	a19-a6	a19-a6	a19-a6
	Column Address	a5-a1(C5-C1)	a5-a2(C4-C1)	a5-a3(C3-C1)
128 Byte	Lower Row Address	a19-a7	a19-a7	a19-a7
	Column Address	a6-a1(C6-C1)	a6-a2(C5-C1)	a6-a3(C4-C1)
256 Byte	Lower Row Address	a19-a8	a19-a8	a19-a8
	Column Address	a7-a1(C7-C1)	a7-a2(C6-C1)	a7-a3(C5-C1)
512 Byte	Lower Row Address	a19-a9	a19-a9	a19-a9
	Column Address	a8-a1(C8-C1)	a8-a2(C7-C1)	a8-a3(C6-C1)
1 KB	Lower Row Address	a19-a10	a19-a10	a19-a10
	Column Address	a9-a1(C9-C1)	a9-a2(C8-C1)	a9-a3(C7-C1)
2 KB	Lower Row Address	a19-a11	a19-a11	a19-a11
	Column Address	a10-a1(C10-C1)	a10-a2(C9-C1)	a10-a3(C8-C1)
4 KB	Lower Row Address	a19-a12	a19-a12	a19-a12
	Column Address	a11-a1(C11-C1)	a11-a2(C10-C1)	a11-a3(C9-C1)

NOTE 1 The least significant column address C0 is implied to be zero and is not transmitted on the CA bus.

NOTE 2 Row and Column Address values on the CA bus that are not used are "don't care."

3 Functional description

LPDDR2-S is a high-speed SDRAM device internally configured as a 4 or 8-Bank memory.

LPDDR2-N is a high-speed Non-Volatile Memory device, internally configured to have 4 or 8 Row Buffers.

These devices contain the following number of bits:

64 Mb has 67,108,864 bits
128 Mb has 134,217,728 bits
256 Mb has 268,435,456 bits
512 Mb has 536,870,912 bits
1 Gb has 1,073,741,824 bits
2 Gb has 2,147,483,648 bits
4 Gb has 4,294,967,296 bits
8 Gb has 8,589,934,592 bits

The following densities apply to LPDDR2-NVM devices only:
16 Gb has 17,179,869,184 bits
32 Gb has 34,359,738,368 bits

All LPDDR2 devices use a double data rate archiecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

LPDDR2-S2 also uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S2 effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal SDRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

LPDDR2-S4 and LPDDR2-N also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 and LPDDR2-N effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM/NVM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For LPDDR2-SX devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

For LPDDR2-N devices, accesses begin with the registration of an Preactive command, followed by an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Preactive and Activate commands are used to select the row and the Row Buffer to be accessed. The address bits registered coincident with the Read or Write command are used to select the Row Buffer and the starting column location for the burst access.

For LPDDR2-NVM devices, operations other than “array reads” are performed by accessing an overlay window that is mapped over the array space of the memory. The Overlay Window Base Address (OWBA) is programmed using the Mode Registers. The overlay window is enabled and disabled by using the Mode Register. When the overlay window is disabled, all array accesses map to the memory array. When the overlay window is enabled, reads and writes to Overlay Window within the array memory space access the Overlay Window.

Prior to normal operation, the LPDDR2 must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

3.1 Simplified LPDDR2 Bus Interface State Diagram

The simplified LPDDR2 bus interface state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see "LPDDR2 Command Definitions and Timing Diagrams" on page 70.

3.1 Simplified LPDDR2 Bus Interface State Diagram (cont'd)

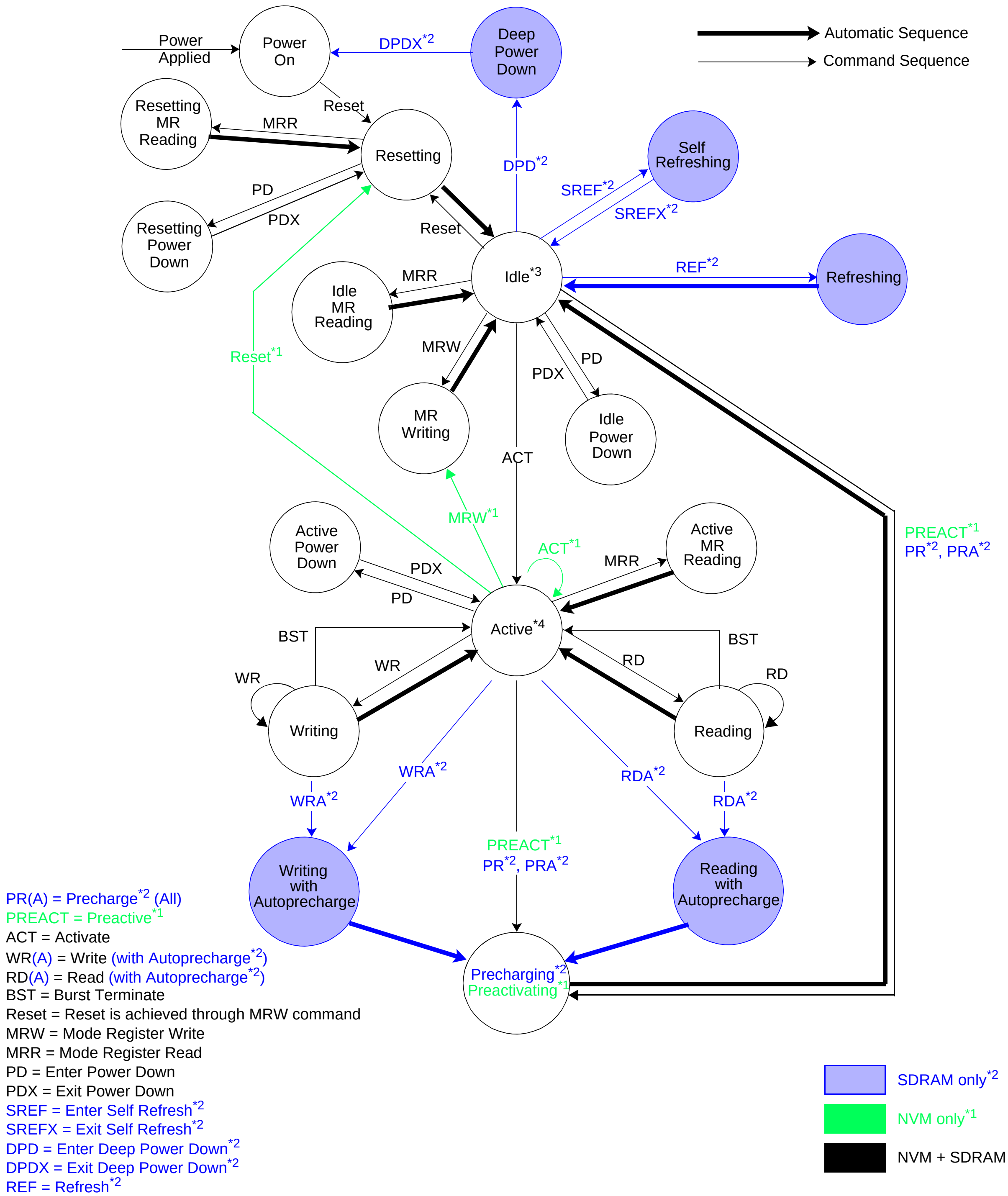


Figure 3 — LPDDR2: Simplified Bus Interface State Diagram

NOTE 1 These transitions apply for LPDDR2-N devices only.
NOTE 2 These transitions apply for LPDDR2-SX devices only.
NOTE 3 For LPDDR2-SDRAM in the Idle state, all banks are precharged.
NOTE 4 For LPDDR2-NVM in the Active state, one or more Row Buffers have been activated.
NOTE 5 Use caution with this diagram. It is intented to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one Bank/Row Buffer are not captured in full detail.
NOTE 6 Resetting duration is variable. Poll DAI status bit to detect state transition to Idle.
NOTE 7 Reset command sets all Row Address Buffers to 0x0000.

3.2 Simplified LPDDR2-SX State Diagram

LPDDR2-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see “LPDDR2 Command Definitions and Timing Diagrams” on page 70.

3.2 Simplified LPDDR2-SX State Diagram (cont'd)

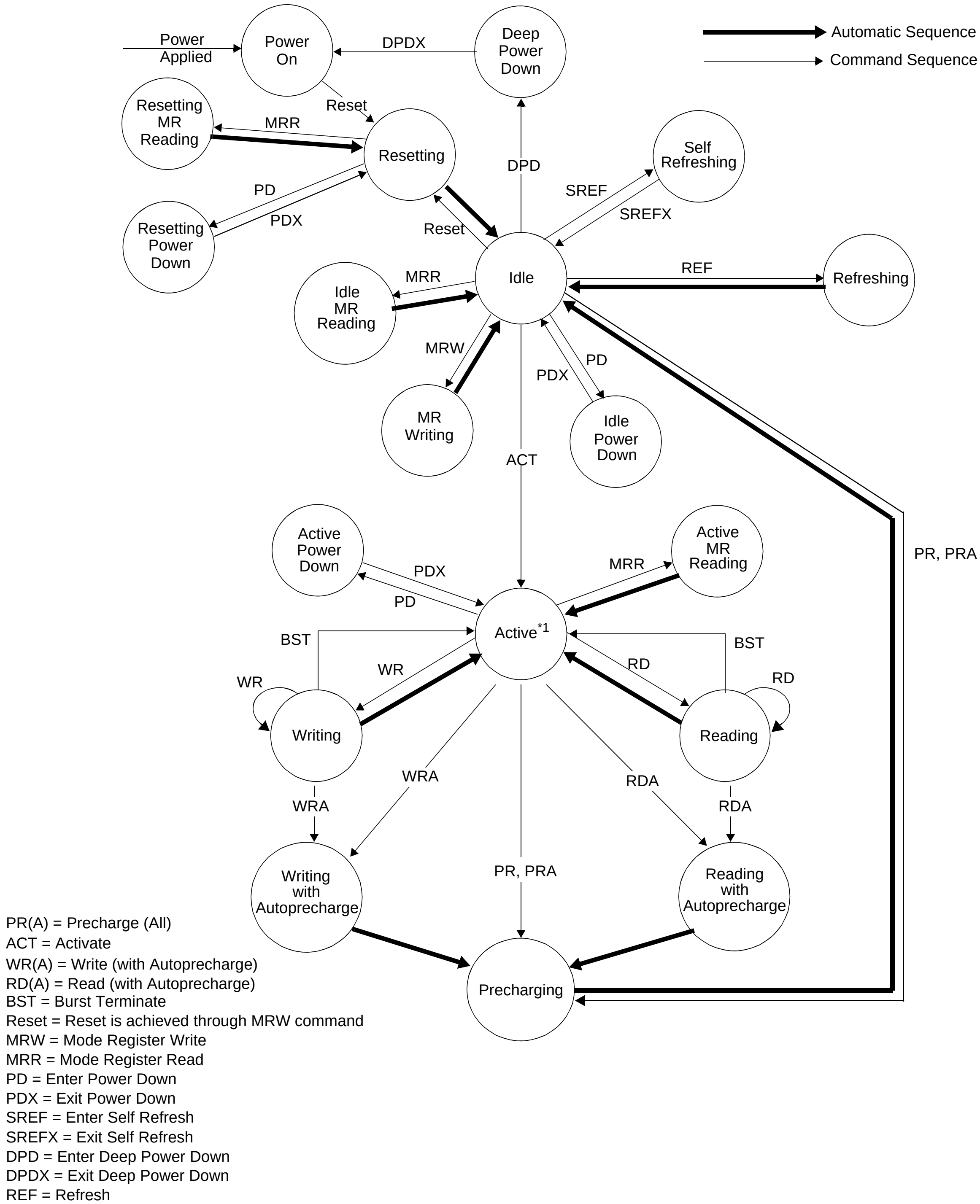


Figure 4 — LPDDR2-S: Simplified Bus Interface State Diagram

NOTE 1 For LPDDR2-SDRAM in the Idle state, all banks are precharged.

3.3 Simplified LPDDR2-N Simplified Bus State Diagram

LPDDR2-NVM simplified bus interface state diagram provides a simplified illustration of allowed bus interface state transitions and the related commands to control them. For a more detalied definition of the device bus interface, the information provided by the state diagram should be integrated with the truth tables and timing specification.

For the command definition see section See “LPDDR2 Command Definitions and Timing Diagrams” on page 70

LPDDR2-NVM has two types of states: stable states, which are entered and exited with a command, and transitory states, which are entered with a command and exited automatically.

LPDDR2-NVM stable states are: Power-on, Idle, Active, Resetting Power Down, Idle Power Down, and Active Power Down.

LPDDR2-NVM transitory states are: Resetting, Resetting MR Reading, Idle MR Reading, MR Writing, Active MR Reading, Reading, Writing and Preactivating.

LPDDR2-NVM state diagram is shown in Figure 5 on page 18, where each state transition, due to a command, is represented with a numbered arc.

Follows the description of all the allowed commands for any given state. The arc number of each transition is included in the description in parenthesis.

3.3.1 Power On and Resetting states

(1) After power up, the device goes in the Power On state.

(2) The Reset command is the only command allowed in this state, and when issued, it brings all Row Buffers (RB) into the Resetting state after $\mathbf{t}_{INIT4}$.

(3) Mode Register Read (MRR) command can be issued from the Resetting state. MRR allows retrieving useful information such as: memory type, memory characteristics, or the Resetting status through the DAI bit. The device enters in Resetting Mode Register Reading state when MRR command is registered, and goes back automatically to Resetting state after $\mathbf{t}_{MRR}$.

(4) Enter Power Down command brings all Row Buffers into the Resetting Power Down state. For the complete description of Power Down entry, see “Power-down” on page 125.

(5) Exit Power Down command brings all Row Buffers from the Resetting Power Down state back to the Resetting state after $\mathbf{t}_{XP}$. For the complete description of Power Down exit, see “Power-down” on page 125.

The duration of Resetting, $\mathbf{t}_{INIT5}$, is device specific and it is not defined in this document. The memory controller shall poll DAI bit to determine the completion of the device initialization. Upon completion of device initialization, all Row Buffers are in the Idle state and all RABs have a default value of 0x0000.

3.3.2 Idle state

From the Idle state, the following commands are allowed: Reset, Mode Register Write, Mode Register Read, Preactive, Activate and Enter Power Down.

(6) Reset command brings all Row Buffers into the Resetting state after $\mathbf{t}_{INIT4}$.

(7) Mode Register Write command brings all Row Buffers to the MR Writing state. All Row Buffers return to the Idle state after $\mathbf{t}_{MRW}$.

(8) Mode Register Read command brings the Row Buffer to the Idle MR Reading state. The Row Buffer goes automatically back to the Idle state after $\mathbf{t}_{MRR}$.

(9) Preactive command brings the Row Buffer to the Preactivating state. The Row Buffer goes automatically back to the Idle state after $\mathbf{t}_{RP}$.

3.3.2 Idle state (cont'd)

(10) Activate command brings the Row Buffer from the Idle state to the Row Activating state, which is not explicitly shown in the state diagram. The Row Buffer goes automatically from the Row Activating state to the Active state after $\mathbf{t}_{RCD}$.

(11) Enter Power Down command brings the Row Buffer into the Idle Power Down state. For the complete description of power down entry see "Power-down" on page 125.

(12) Exit Power Down command brings the Row Buffer from the Idle Power Down state back to the Idle state after $\mathbf{t}_{XP}$. For the complete description of power down exit see "Power-down" on page 125.

3.3.3 Active state

From the Active state, the following commands are allowed: Reset, Mode Register Write, Mode Register Read, Preactive, Activate, Read, Write and Enter Power Down.

(13) Reset command brings all Row Buffers into the Resetting state after $\mathbf{t}_{INIT4}$.

(14) Mode Register Write command brings all Row Buffers to the MR Writing state. All Row Buffers return to the Idle state after $\mathbf{t}_{MRW}$.

(15) Mode Register Read command brings the Row Buffer to the Active MR Reading state. The Row Buffer goes automatically back to the Active state after $\mathbf{t}_{MRR}$.

(16) Preactive command brings the Row Buffer to the Preactivating state. The Row Buffer goes automatically to the Idle state after $\mathbf{t}_{RP}$.

(17) Activate command brings the Row Buffer from the Active state to the Row Activating state, which is not explicitly shown in the state diagram. The Row Buffer goes automatically back to the Active state after $\mathbf{t}_{RCD}$.

(18) Read command moves the Row Buffer to the Reading state. The Row Buffer goes automatically back to the Row Active state after BL/2 clock cycles, or after a Burst Terminate command. See "Burst Read Command" on page 74 for timing restrictions to apply between the Read command and a following Read, Write, Mode Register Write, Mode Register Read, Preactive, Activate or Enter Power Down commands that might occur. If a new Read command is issued within BL/2 clock cycles, the Row Buffer remains in the Reading state.

(19) Write command moves the Row Buffer to the Writing state. The Row Buffer goes automatically back to the Row Active state after BL/2 clock cycles, or after a Burst Terminate command. See "Burst Write Operation" on page 82 for timing restrictions to apply between the Write command and the following Write, Read, Mode Register Write, Mode Register Read, Preactive, Activate or Enter Power Down commands that might occur. If a new Write command is issued within BL/2 clock cycles, the Row buffer remains in the Writing state.

(20) Enter Power Down command brings the Row Buffer into the Active Power Down state. For the complete description of power down entry see "Power-down" on page 125.

(21) Exit Power Down command brings the Row Buffer from the Active Power Down state back to the Row Active state after $\mathbf{t}_{XP}$. For the complete description of power down exit see "Power-down" on page 125.

3.3.3 Active state (cont'd)

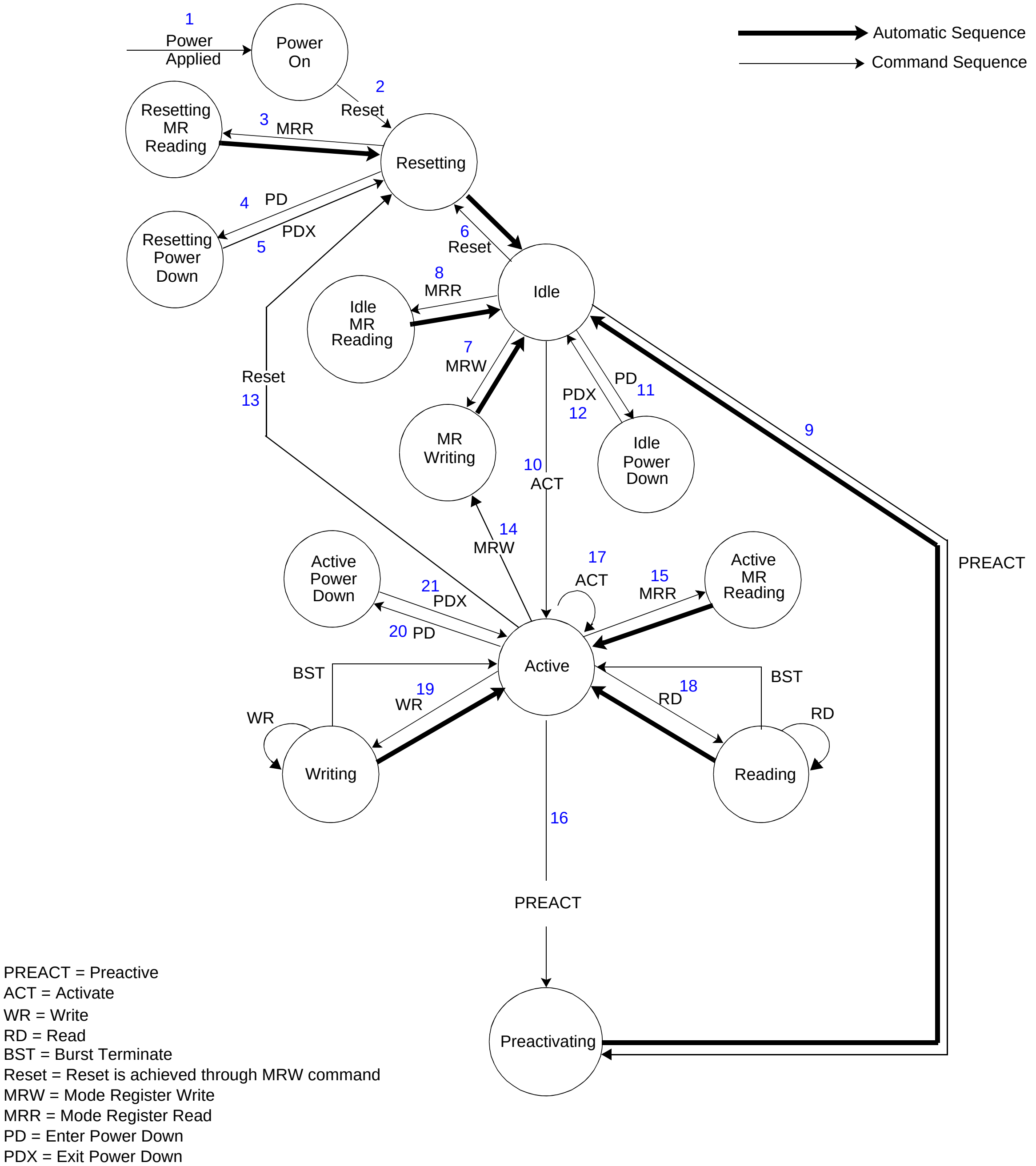


Figure 5 — LPDDR2-N: Simplified Bus Interface State Diagram

NOTE 1 For LPDDR2-NVM in the Active state, one or more Row Buffers have been activated.
NOTE 2 Use caution with this diagram. It is intented to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one Row Buffer are not captured in full detail.
NOTE 3 Resetting duration is variable. Poll DAI status bit to detect state transition to Idle.
NOTE 4 Reset command sets all Row Address Buffers to 0x0000.

3.4 Power-up, Initialization, and Power-Off

LPDDR2 Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

3.4.1 Power Ramp and Device Initialization

The following sequence shall be used to power up an LPDDR2 device. Unless specified otherwise, these steps are mandatory and apply to S2, S4 and N devices.

1. Power Ramp

   While applying power (after Ta), CKE shall be held at a logic low level (=< 0.2 x VDDCA), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.
   On or before the completion of the power ramp (Tb) CKE must be held low.

   DQ, DM, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up.

   The following conditions apply:

   Ta is the point where *any* power supply first reaches 300 mV.

   After Ta is reached, VDD1 must be greater than VDD2 - 200 mV.

   After Ta is reached, VDD1 and VDD2 must be greater than VDDCA - 200 mV.

   After Ta is reached, VDD1 and VDD2 must be greater than VDDQ - 200 mV.

   After Ta is reached, VREF must always be less than all other supply voltages.

   The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100 mV.

   The above conditions apply between Ta and power-off (controlled or uncontrolled).

   Tb is the point when all supply voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.

   For supply and reference voltage operating conditions, see Table 7.1 on page 147, Table 70 on page 147, and Table 71 on page 147.

   Power ramp duration t_{INIT0} (Tb - Ta) must be no greater than 20 ms.

   NOTE VDD2 is not present in some systems. Rules related to VDD2 in those cases do not apply.

2. CKE and clock:
   Beginning at Tb, CKE must remain low for at least t_{INIT1} = 100 ns, after which it may be asserted high. Clock must be stable at least t_{INIT2} = 5 x tCK prior to the first low to high transition of CKE (Tc). CKE, CS_n and CA inputs must observe setup and hold time (tIS, tIH) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

   The clock period shall be within the range defined for $t_{CK\mathbf{b}}$ (18 ns to 100 ns), if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met. Furthermore, some AC parameters (e.g. t_{DQSCK}) may have relaxed timings (e.g. $t_{DQSCK\mathbf{b}}$) before the system is appropriately configured.

   While keeping CKE high, issue NOP commands for at least t_{INIT3} = 200 us. (Td).

3. Reset command:
   After t_{INIT3} is satisfied, a MRW(Reset) command shall be issued (Td). The memory controller may optionally issue a Precharge-All command (for LPDDR2-SX) or Preactive (for LPDDR2-N) prior to the MRW Reset command. For LPDDR2-N devices, the subsequent MRW Reset command will set each Row Address Buffers (RAB) to 0x0000 overwriting the value stored by the previous preactive command. Wait for at least t_{INIT4} = 1 µs while keeping CKE asserted and issuing NOP commands.

3.4.1 Power Ramp and Device Initialization (cont'd)

4. Mode Registers Reads and Device Auto-Initialization (DAI) polling:
   After t_{INIT4} is satisfied (Te) only MRR commands and power-down entry/exit commands are allowed.
   Therefore, after Te, CKE may go low in accordance to Power-Down entry and exit specification (see "Power-down" on page 125).

   The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of tINIT5 before proceeding.
   As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.
   After the DAI-bit (MR0, "DAI") is set to zero "DAI complete" by the memory device, the device is in idle state (**Tf**). The state of the DAI status bit can be determined by an MRR command to MR0.

   All SDRAM devices will set the DAI-bit no later than t_{INIT5} (10 us) after the Reset command. The memory controller shall wait a minimum of tINIT5 or until the DAI-bit is set before proceeding.

   For NVM devices, repetitive polling of the DAI-Bit is required to determine when this bit has internally been set to zero "DAI complete" by the memory device. A Value for t_{INIT5} value is not defined for NVMs in this document because it is device dependent. The only way to determine when Device Auto-Initialization is complete is to poll DAI. To obtain the shortest boot up time and ensure compatibility with any future NVM device it is recommended to not rely on any predetermined t_{INIT5} value.

   After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 "Device Information" etc.).
5. ZQ Calibration:
   After t_{INIT5} (**Tf**), an MRW ZQ Initialization Calibration command may be issued to the memory (MR10). For LPDDR2 devices which do not support the ZQ Calibration command, this command shall be ignored. This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after tZQINIT.
6. Normal Operation:
   After t_{ZQINIT} (**Tg**), MRW commands shall be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration.
   To support simple boot from the NVM, some Mode Registers are reset to default values during Device Auto-Initialization. See the Mode Register section of this specification for default values.
   The LPDDR2 device will now be in IDLE state and ready for any valid command.
   After **Tg**, the clock frequency may be changed according to the clock frequency change procedure described in section "Input clock stop and frequency change" on page 133 of this specification.

3.4.1 Power Ramp and Device Initialization (cont'd)

Table 15 — Timing Parameters for initialization

Symbol	Value		Unit	Comment
	min	max		
t_{INIT0}		20	ms	Maximum Power Ramp Time
t_{INIT1}	100		ns	Minimum CKE low time after completion of power ramp
t_{INIT2}	5		tCK	Minimum stable clock before first CKE high
t_{INIT3}	200		µs	Minimum Idle time after first CKE assertion
t_{INIT4}	1		µs	Minimum Idle time after Reset command
t_{INIT5}		S: 10	µs	Maximum duration of Device Auto-Initialization
		N: vendor	µs	
t_{ZQINIT}	1		µs	ZQ Initial Calibration for LPDDR2-S4 and LPDDR2-N devices
t_{CKb}	18	100	ns	Clock cycle time during boot

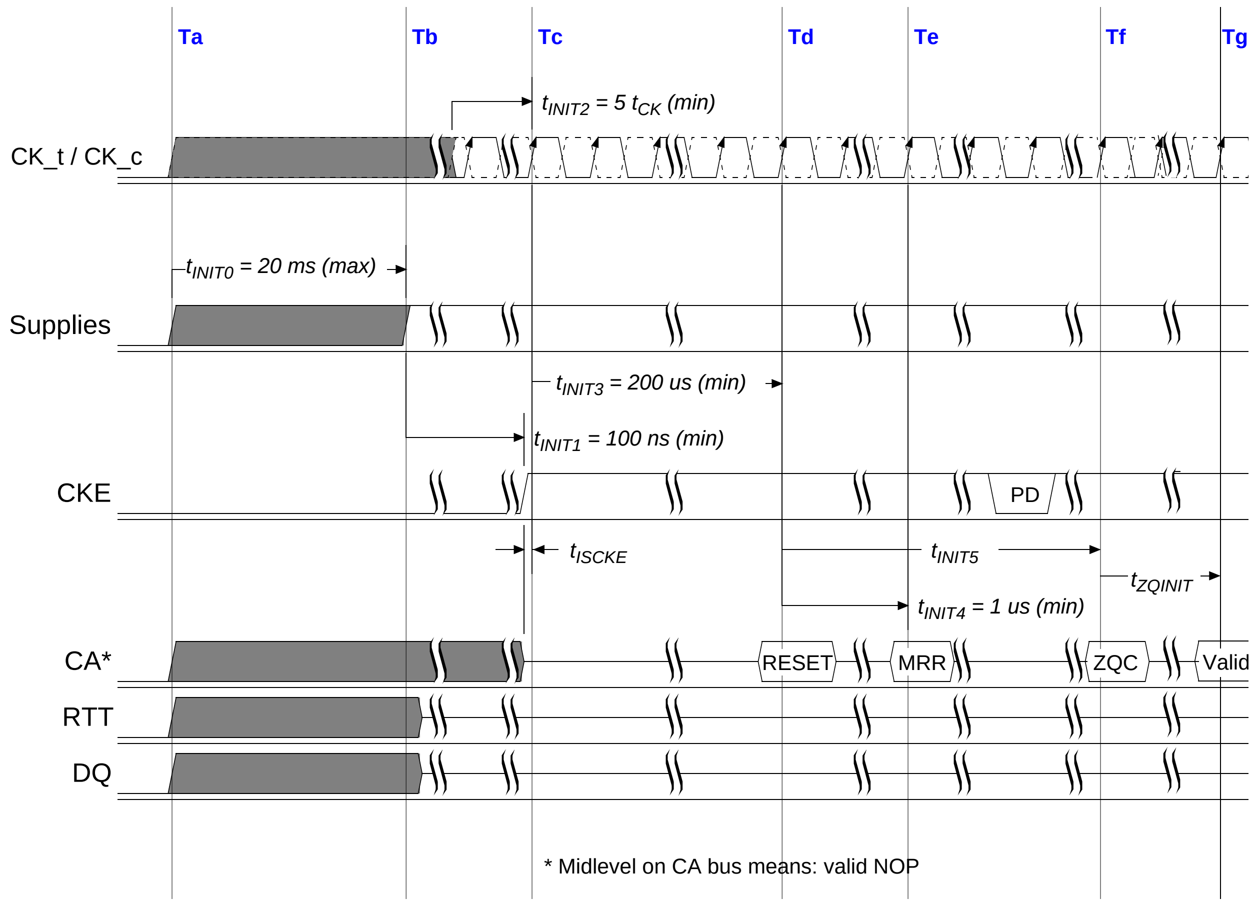


Figure 6 — Power Ramp and Initialization Sequence

3.4.2 Initialization after Reset (without Power ramp):

If the RESET command is issued outside the power up initialization sequence, the reinitialization procedure shall begin with step 3 (Td).

3.4.3 Power-off Sequence

The following sequence shall be used to power off the LPDDR2 device. Unless specified otherwise, these steps are mandatory and apply to S2, S4 and N devices.

While removing power, CKE shall be held at a logic low level (=< 0.2 x VDDCA), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

For LPDDR2-N devices, all embedded operations must be finished or aborted and the device must be in the ready state (Status Register, bit 7 = “1”) prior to Power-off.

DQ, DM, DQS_t, and DQS_c voltage levels must be between VSSQ and VDDQ during power off sequence to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between VSSCA and VDDCA during power off sequence to avoid latch-up.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table.

Tz is the point where *all* power supplies are below 300 mV. After Tz, the device is powered off.

The time between Tx and Tz (t_{POFF}) shall be less than 20ms.

The following conditions apply:

Between Tx and Tz, VDD1 must be greater than VDD2 - 200 mV.

Between Tx and Tz, VDD1 and VDD2 must be greater than VDDCA - 200 mV.

Between Tx and Tz, VDD1 and VDD2 must be greater than VDDQ - 200 mV.

Between Tx and Tz, VREF must always be less than all other supply voltages.

The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100 mV.

For supply and reference voltage operating conditions, see Table 7.1 on page 147, Table 70 on page 147, and Table 71 on page 147.

NOTE VDD2 is not present in some systems. Rules related to VDD2 in those cases do not apply.

Table 16 — Timing Parameters Power-Off

Symbol	Value		Unit	Comment
	min	max		
t_{POFF}	-	20	ms	Maximum Power-Off ramp time

3.4.4 Uncontrolled Power-Off Sequence

The following sequence shall be used to power off the LPDDR2 device under uncontrolled condition. Unless specified otherwise, these steps are mandatory and apply to S2, S4 and N devices.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.

Tz is the point where all power supply first reaches 300 mV. After Tz, the device is powered off.

The time between Tx and Tz (t_{POFF}) shall be less than 20ms. The relative level between supply voltages are uncontrolled during this period.

VDD1 and VDD2 shall decrease with a slope lower than 0.5 V/usec between Tx and Tz.

Uncontrolled power off sequence can be applied only up to 400 times in the life of the device.

3.5 Mode Register Definition

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM

Table 17 shows the 16 common mode registers for LPDDR2 SDRAM and NVM. Table 18 shows only LPDDR2 SDRAM mode registers and Table 19 shows only LPDDR2 NVM mode registers. Additionally Table 20 shows RFU mode registers and Reset Command.

Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written.

Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

Table 17 — Mode Register Assignment in LPDDR2 SDRAM/NVM(Common part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00_H	Device Info.	R	(RFU)					DNVI	DI	DAI	go to MR0
1	01_H	Device Feature 1	W	nWR (for AP)			WC	BT	BL			go to MR1
2	02_H	Device Feature 2	W	(RFU)				RL & WL				go to MR2
3	03_H	I/O Config-1	W	(RFU)				DS				go to MR3
4	04_H	SDRAM Refr. R.	R	TUF	(RFU)				Refresh Rate			go to MR4
		NVM Temp. Alert	R	TUF	(RFU)				NVM Temp. Alert			
5	05_H	Basic Config-1	R	LPDDR2 Manufacturer ID								go to MR5
6	06_H	Basic Config-2	R	Revision ID1								go to MR6
7	07_H	Basic Config-3	R	Revision ID2								go to MR7
8	08_H	Basic Config-4	R	I/O width		Density				Type		go to MR8
9	09_H	Test Mode	W	Vendor-Specific Test Mode								go to MR9
10	$0A_H$	IO Calibration	W	Calibration Code								go to MR10
11:15	$0B_H$~$0F_H$	(reserved)		(RFU)								go to MR11

Table 18 — Mode Register Assignment in LPDDR2 SDRAM/NVM (SDRAM part)

MR#	MA <7:0>	Function	access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
16	10_H	PASR_Bank (S4)	W	Bank Mask								go to MR16
		PASR_Bank (S2)		(RFU)						PASR		
17	11_H	PASR_Seg	W	Segment Mask (S4 SDRAM only)								go to MR17
18-19	12_H-13_H	(Reserved)		(RFU)								go to MR18

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

Table 19 — Mode Register Assignment in LPDDR2 SDRAM/NVM (NVM part)

MR#	MA <7:0>	Function	access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
20	**14_H**	NVM Geometry	R	(RFU)		tRCD De-Rating		RB Number	RDB size			**go to MR20**
21	**15_H**	NVM tRCD	R	tRCD Value (2nd order)				tRCD Value (1st order)				**go to MR21**
22-23	**16_H-17_H**	(Reserved)		(RFU)								**go to MR22**
24	**18_H**	Overlay Window Enable	R/W	(RFU)						OWD	OWE	**go to MR24**
25	**19_H**	OW Base-Addr 1	R/W	OW base-addr 31 (a19 ~ a13)							0	**go to MR25**
26	**$1A_H$**	OW Base-Addr 2	R/W	OW base-addr 2 (a27 ~ a20)								
27	**$1B_H$**	OW Base-Addr 3	R/W	(RFU)				OW base-addr 3 (a31 ~ a28)				
28	**$1C_H$**	(Reserved)		(RFU)								**go to MR28**
29	**$1D_H$**	DNV Long Delay	R	tDNV Value (2nd order)				tDNV Value (1st order)				**go to MR29**
30-31	**$1E_H$-$1F_H$**	(Reserved)		(RFU)								**go to MR30**

Table 20 — Mode Register Assignment in LPDDR2 SDRAM/NVM (DQ Calibration and Reset Command)

MR#	MA <7:0>	Function	access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
32	**20_H**	DQ Calibration Pattern A	R	See "DQ Calibration" on page 117								**go to MR32**
33:39	**21_H~27_H**	(Do Not Use)										**go to MR33**
40	**28_H**	DQ Calibration Pattern B	R	See "DQ Calibration" on page 117								**go to MR40**
41:47	**29_H~$2F_H$**	(Do Not Use)										**go to MR41**
48:62	**30_H~$3E_H$**	(Reserved)		(RFU)								**go to MR48**
63	**$3F_H$**	Reset	W	X								**go to MR63**
64:126	**40_H~$7E_H$**	(Reserved)		(RFU)								**go to MR64**
127	**$7F_H$**	(Do Not Use)										**go to MR127**
128:190	**80_H~BE_H**	(Reserved for Vendor Use)		(RFU)								**go to MR128**
191	**BF_H**	(Do Not Use)										**go to MR191**
192:254	**$C0_H$~FE_H**	(Reserved for Vendor Use)		(RFU)								**go to MR192**
255	**FF_H**	(Do Not Use)										**go to MR255**

The following notes apply to tables 17-20:

NOTE 1 RFU bits shall be set to '0' during Mode Register writes.

NOTE 2 RFU bits shall be read as '0' during Mode Register reads.

NOTE 3 All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS shall be toggled.

NOTE 4vAll Mode Registers that are specified as RFU shall not be written.

NOTE 5 See Vendor Device Datasheets for details on Vendor Specific Mode Registers.

NOTE 6 Writes to read-only registers shall have no impact on the functionality of the device.

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR0 Device Information (MA<7:0> = 00$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)					DNVI	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	**0$_B$:** DAI complete **1$_B$:** DAI still in progress	
DI (Device Information)	Read-only	OP1	**0$_B$:** S2 or S4 SDRAM **1$_B$:** NVM	
DNVI (Data Not Valid Information)	Read-only	OP2	**0$_B$:** DNV not supported **1$_B$:** DNV supported	

NOTE 1 LPDDR2 SDRAM will not implement DNV functionality.

NOTE 2 If DNV functionality is not implemented, the device shall not drive the DM/DNV signals.

MR1 Device Feature 1 (MA<7:0> = 01$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write-only	OP<2:0>	**010$_B$:** BL4 (default) **011$_B$:** BL8 **100$_B$:** BL16 **All others:** reserved	
BT	Write-only	OP<3>	**0$_B$:** Sequential (default) **1$_B$:** Interleaved (allowed for SDRAM only)	1
WC	Write-only	OP<4>	**0$_B$:** Wrap (default) **1$_B$:** No wrap (allowed for SDRAM BL4 only)	
nWR	Write-only	OP<7:5>	**001$_B$:** nWR=3 (default) **010$_B$:** nWR=4 **011$_B$:** nWR=5 **100$_B$:** nWR=6 **101$_B$:** nWR=7 **110$_B$:** nWR=8 **All others:** reserved	2

NOTE 1 BL 16, interleaved is not an official combination to be supported.

NOTE 2 Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

NOTE 3 BL16 is not supported by LPDDR2-NVM with Row Data Buffer size equal to 32-Byte and Data Bus Width equal to 32-bit.

NOTE 4 OP7:OP5 are reserved for LPDDR2-NVM.

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

Table 21 — Burst Sequence by BL, BT, and WC

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	0_B	0_B	wrap	any	4	0	1	2	3												
X	X	1_B	0_B				2	3	0	1												
X	X	X	0_B	nw	any		y	y+1	y+2	y+3												
X	0_B	0_B	0_B	wrap	seq	8	0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	4	5	6	7	0	1								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	0	1	2	3	4	5								
X	0_B	0_B	0_B		int		0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	0	1	6	7	4	5								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	4	5	2	3	0	1								
X	X	X	0_B	nw	any		**illegal (not allowed)**															
0_B	0_B	0_B	0_B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0_B	0_B	1_B	0_B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0_B	1_B	0_B	0_B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0_B	1_B	1_B	0_B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1_B	0_B	0_B	0_B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1_B	0_B	1_B	0_B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1_B	1_B	0_B	0_B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1_B	1_B	1_B	0_B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
X	X	X	0_B		int		**illegal (not allowed)**															
X	X	X	0_B	nw	any		**illegal (not allowed)**															

1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C1 - C0.
3. For BL=8, the burst address represents C2 - C0.
4. For BL=16, the burst address represents C3 - C0.
5. For no-wrap (nw), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary. The variable y may start at any address with C0 equal to 0 and may not start at any address in Table 22 below for the respective density and bus width combinations.

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont’d)

Table 22 — LPDDR2-SX Non Wrap Restrictions

	64Mb	128Mb/256Mb	512Mb/1Gb/2Gb	4Gb/8Gb
Not across full page boundary				
x8	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001	FFE, FFF, 000, 001
x16	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001
x32	7E, 7F, 00, 01	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001
Not across sub page boundary				
x8	07E, 07F, 080, 081 0FE, 0FF, 100, 101 17E, 17F, 180, 181	0FE, 0FF, 100, 101 1FE, 1FF, 200, 201 2FE, 2FF, 300, 301	1FE, 1FF, 200, 201 3FE, 3FF, 400, 401 5FE, 5FF, 600, 601	3FE, 3FF, 400, 401 7FE, 7FF, 800, 801 BFE, BFF, C00, C01
x16	7E, 7F, 80, 81	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401
x32	None	None	None	None

NOTE 1 Non-wrap BL=4 data-orders shown above are prohibited.

MR2 Device Feature 2 (MA<7:0> = 02$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

RL & WL	Write-only	OP<3:0>	**0001_B:** RL = 3 / WL = 1 (default) **0010_B:** RL = 4 / WL = 2 **0011_B:** RL = 5 / WL = 2 **0100_B:** RL = 6 / WL = 3 **0101_B:** RL = 7 / WL = 4 **0110_B:** RL = 8 / WL = 4 **All others:** reserved	

MR3 I/O Configuration 1 (MA<7:0> = 03$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP<3:0>	**0000_B:** reserved **0001_B:** 34.3-ohm typical **0010_B:** 40-ohm typical (default) **0011_B:** 48-ohm typical **0100_B:** 60-ohm typical **0101_B:** reserved for 68.6-ohm typical **0110_B:** 80-ohm typical **0111_B:** 120-ohm typical (optional) **All others:** reserved	

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR4 Device Temperature (MA<7:0> = 04_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		
TUF	(RFU)				NVM Temperature Alert		

SDRAM Refresh Rate	Read-only	OP<2:0>	**000_B:** SDRAM Low temperature operating limit exceeded **001_B:** 4x t_{REFI}, 4x t_{REFIpb}, 4x t_{REFW} **010_B:** 2x t_{REFI}, 2x t_{REFIpb}, 2x t_{REFW} **011_B:** 1x t_{REFI}, 1x t_{REFIpb}, 1x t_{REFW} (<=85°C) **100_B:** Reserved **101_B:** 0.25x t_{REFI}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, do not de-rate SDRAM AC timing **110_B:** 0.25x t_{REFI}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, de-rate SDRAM AC timing **111_B:** SDRAM High temperature operating limit exceeded
NVM Temperature Alert	Read-only	OP<2:0>	**000_B:** NVM Low temperature operating limit exceeded **001_B:** Reserved **010_B:** Reserved **011_B:** Temperature Alert not active, do not de-rate NVM AC timing (<=85°C) **100_B:** Temperature Alert not active, de-rate NVM AC timing **101_B:** Temperature Alert active, do not de-rate NVM AC timing **110_B:** Temperature Alert active, de-rate NVM AC timings **111_B:** NVM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	**0_B:** OP<2:0> value has not changed since last read of MR4. **1_B:** OP<2:0> value has changed since last read of MR4.

NOTE 1 A Mode Register Read from MR4 will reset OP7 to '0'.

NOTE 2 OP7 is reset to '0' at power-up.

NOTE 3 If OP2 equals '1', the device temperature is greater than 85°C.

NOTE 4 OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.

NOTE 5 LPDDR2 might not operate properly when OP[2:0] = 000_B or 111_B.

NOTE 6 For specified operating temperature range and maximum operating temperature refer to Table 72 on page 148.

NOTE 7 LPDDR2-SX devices shall be de-rated by adding 1.875 ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in Table 103 on page 181. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.

NOTE 8 LPDDR2-NVM devices shall be de-rated by adding the value found at location OP5:OP4 in MR20 to the following core timing parameters: tRCD, tRC, tRAS, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in Table 103 on page 181. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.

NOTE 9 See "Temperature Sensor" on page 116 for information on the recommended frequency of reading MR4.

3.5.1Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont’d)

MR5 Basic Configuration 1 (MA<7:0> = 05_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							

LPDDR2 Manufacturer ID	Read-only	OP<7:0>	0000 0000B : Reserved 0000 0001B : Samsung 0000 0010B : Qimonda 0000 0011B : Elpida 0000 0100B : Etron 0000 0101B : Nanya 0000 0110B : Hynix 0000 0111B : Mosel 0000 1000B : Winbond 0000 1001B : ESMT 0000 1010B : Reserved 0000 1011B : Spansion 0000 1100B : SST 0000 1101B : ZMOS 0000 1110B : Intel 1111 1110B : Numonyx 1111 1111B : Micron All Others : Reserved	

MR6 Basic Configuration 2 (MA<7:0> = 06_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP<7:0>	**00000000_B:** A-version	

NOTE 1 MR6 is Vendor Specific.

MR7 Basic Configuration 3 (MA<7:0> = 07_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP<7:0>	**00000000_B:** A-version	

NOTE 1 MR7 is Vendor Specific.

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR8 Basic Configuration 4 (MA<7:0> = 08B$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP<1:0>	**00$_B$:** S4 SDRAM **01$_B$:** S2 SDRAM **10$_B$:** N NVM **11$_B$:** Reserved	
Density	Read-only	OP<5:2>	**0000$_B$:** 64Mb **0001$_B$:** 128Mb **0010$_B$:** 256Mb **0011$_B$:** 512Mb **0100$_B$:** 1Gb **0101$_B$:** 2Gb **0110$_B$:** 4Gb **0111$_B$:** 8Gb **1000$_B$:** 16Gb **1001$_B$:** 32Gb **all others:** reserved	
I/O width	Read-only	OP<7:6>	**00$_B$:** x32 **01$_B$:** x16 **10$_B$:** x8 **11$_B$:** not used	

MR9 Test Mode (MA<7:0> = 09$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10 Calibration (MA<7:0> = 0A$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write-only	OP<7:0>	**0xFF:** Calibration command after initialization **0xAB:** Long calibration **0x56:** Short calibration **0xC3:** ZQ Reset **others:** Reserved

NOTE 1 Host processor shall not write MR10 with "Reserved" values

NOTE 2 LPDDR2 devices shall ignore calibration command when a "Reserved" value is written into MR10.

NOTE 3 See AC timing table for the calibration latency.

NOTE 4 If ZQ is connected to V_{SSCA} through R_{ZQ}, either the ZQ calibration function (see "Mode Register Write ZQ Calibration Command" on page 122) or default calibration (through the ZQreset command) is supported. If ZQ is connected to V_{DDCA}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

NOTE 5 LPDDR2 devices that do not support calibration shall ignore the ZQ Calibration command.

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR11:15 (Reserved) (MA<7:0> = $0B_H$-$0F_H$):

MR16 PASR Bank Mask (MA<7:0> = 010_H): S2 and S4 SDRAM only

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
S2 SDRAM	(RFU)						PASR	
S4 SDRAM	Bank Mask (4-bank or 8-bank)							

S2 SDRAM:

PASR Map	Write-only	OP<1:0>	**00_B:** Full array (default) **01_B:** 1/2 array - \BA1=0 for 4-banks, BA2=0 for 8-banks **10_B:** 1/4 array - BA1=BA0=0 for 4-banks, BA2=BA1=0 for 8-banks **11_B:** 1/8 array - Not used for 4-banks, BA2=BA1=BA0=0 for 8-banks	

S4 SDRAM:

Bank <7:0> Mask	Write-only	OP<7:0>	**0_B:** refresh enable to the bank (=unmasked, default) **1_B:** refresh blocked (=masked)	1

1. For 4-bank S4 SDRAM, only OP<3:0> are used.

OP	Bank Mask	4-Bank S4 SDRAM	8-Bank S4 SDRAM
0	XXXXXXX1	**Bank 0**	**Bank 0**
1	XXXXXX1X	**Bank 1**	**Bank 1**
2	XXXXX1XX	**Bank 2**	**Bank 2**
3	XXXX1XXX	**Bank 3**	**Bank 3**
4	XXX1XXXX	**-**	**Bank 4**
5	XX1XXXXX	**-**	**Bank 5**
6	X1XXXXXX	**-**	**Bank 6**
7	1XXXXXXX	**-**	**Bank 7**

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR17 PASR Segment Mask (MA<7:0> = 011_H): 1Gb ~ 8Gb S4 SDRAM only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment <7:0> Mask	Write-only	OP<7:0>	**0_B:** refresh enable to the segment (=unmasked, default) **1_B:** refresh blocked (=masked)	

			1Gb	2Gb,4Gb	8Gb
Segment	OP	Segment Mask	R12:10	R13:11	R14:12
0	0	XXXXXXX1	**000_B**		
1	1	XXXXXX1X	**001_B**		
2	2	XXXXX1XX	**010_B**		
3	3	XXXX1XXX	**011_B**		
4	4	XXX1XXXX	**100_B**		
5	5	XX1XXXXX	**101_B**		
6	6	X1XXXXXX	**110_B**		
7	7	1XXXXXXX	**111_B**		

NOTE This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment

.

MR18-19 Reserved (MA<7:0> = 012_H - 013_H):

MR20 NVM Geometry (MA<7:0> = 014_H): NVM only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)		tRCD De-Rating		RB Number	RDB size		

RDB Size	Read-only	OP<2:0>	**000_B:** 32B **001_B:** 64B **010_B:** 128B **011_B:** 256B **100_B:** 512B **101_B:** 1024B **110_B:** 2048B **111_B:** 4096B	
RB Number	Read-only	OP<3>	**0_B**: 4 Row Buffers **1_B**: 8 Row Buffers	
tRCD De-rating ($t_{NVMDERATING}$)	Read-only	OP<5:4>	**00_B**: 0 ns **01_B**: 1.875 ns **10_B**: 3.75 ns **11_B**: 7.5 ns	

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR21 NVM tRCD (MA<7:0> = 15_H): NVM only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
t_{RCD} Value (2nd order)				t_{RCD} Value (1st order)			

t_{RCD} Value (1st order = value ns)	Read-only	OP<3:0>	**0000_B:** 0ns **0010_B:** 2ns **0100_B:** 4ns **0110_B:** 6ns **1000_B:** 8ns **1010_B:** 10ns **1100_B:** 12ns **1110_B:** 14ns	**0001_B:** 1ns **0011_B:** 3ns **0101_B:** 5ns **0111_B:** 7ns **1001_B:** 9ns **1011_B:** 11ns **1101_B:** 13ns **1111_B:** 15ns
t_{RCD} Value (2nd order = valuex16 ns)	Read-only	OP<7:4>	**0000_B:** 0ns **0010_B:** 32ns **0100_B:** 64ns **0110_B:** 96ns **1000_B:** 128ns **1010_B:** 160ns **1100_B:** 192ns **1110_B:** 224ns	**0001_B:** 16ns **0011_B:** 48ns **0101_B:** 80ns **0111_B:** 112ns **1001_B:** 144ns **1011_B:** 176ns **1101_B:** 208ns **1111_B:** 240ns

NOTE 1 t_{RCD} value is obtained adding 1st order value to the 2nd order value

MR22:23 (Reserved) (MA<7:0> = 16_H:17_H):

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR24 Overlay Window Enable (MA<7:0> = 18_H): NVM Only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)						OWD	OWE

Overlay Window Disable (OWD)	OP<1>	Read	**Reserved**	Note 4
		Write	0_B: Nop 1_B: Disable Overlay Window	Notr 4
Overlay Window Enable (OWE)	OP<0>	Read	0_B: Overlay Window Disabled (Default) 1_B: Overlay Window Enabled	Notr 5
		Write	0_B: Nop 1_B: Enable Overlay Window	Note 5

NOTE 1 Overlay Window Disable (OP1) shall be set to disable the Overlay Window (See Section on the NVM Overlay Window for more details). OP1 is set by an MRW command with OP1 = "1". When read, OP1 returns as a reserved value, "0".

NOTE 2 Overlay Window Enable (OP0) shall be set to enable the Overlay Window (See Section on the NVM Overlay Window for more details). OP0 is set by an MRW command with OP0 = "1". When read, OP0 returns the status of the Overlay Window. When read, OP0 will reflect whether the Overlay Window is enabled (OP0 = "1") or disabled (OP0 = "0").

NOTE 3 All values for MR24 are reset by the device to "0" during Device Auto-Initialization.

NOTE 4 Only one bit is allowed to be set during any single MRW.

MR25:27 OW Base Address 1~3 (MA<7:0> = 19_H-$1B_H$): NVM only

MR		OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
25	**19_H**	a19	a18	a17	a16	a15	a14	a13	0
26	**$1A_H$**	a27	a26	a25	a24	a23	a22	a21	a20
27	**$1B_H$**	(RFU)				a31	a30	a29	a28

NOTE 1 a12 - a0 are implied to be 0.The Overlay Window is aligned on a 8-Kbyte boundary.
NOTE 2 Mode Registers 25-27 are readable are writeable
NOTE 3 Only the value '0' can be written to RFU bit. When read RFU bit shall output '0'.
NOTE 4 Only the value '0' can be written to OP0 in MR25.
NOTE 5 Only the value '0' can be written to unused row address values outside of the device address space.
NOTE 6 When read, unused row address values outside of the device address space shall return '0'.

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR28 (Reserved) (MA<7:0> = $1C_H$):

MR29 NVM tDNV (MA<7:0> = $1D_H$): NVM only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
tDNV Value (2nd order)				tDNV Value (1st order)			

tDNV Value (1st order = value ns)	Read-only	OP<3:0>	**0000_B**: 0us **0010_B**: 2us **0100_B**: 4us **0110_B**: 6us **1000_B**: 8us **1010_B**: 10us **1100_B**: 12us **1110_B**: 14us	**0001_B**: 1us **0011_B**: 3us **0101_B**: 5us **0111_B**: 7us **1001_B**: 9us **1011_B**: 11us **1101_B**: 13us **1111_B**: 15us
tDNV Value (2nd order = valuex16 us)	Read-only	OP<7:4>	**0000_B**: 0us **0010_B**: 32us **0100_B**: 64us **0110_B**: 96us **1000_B**: 128us **1010_B**: 160us **1100_B**: 192us **1110_B**: 224us	**0001_B**: 16us **0011_B**: 48us **0101_B**: 80us **0111_B**: 112us **1001_B**: 144us **1011_B**: 176us **1101_B**: 208us **1111_B**: 240us

MR30:31 (NVM Reserved) (MA<7:0> = $1E_H$-$1F_H$):

MR32 DQ Calibration Pattern A (MA<7:0> = 20_H):

Reads to MR32 return DQ Calibration Pattern "A". See "DQ Calibration" on page 117.

MR33:39 (Do Not Use) (MA<7:0> = 21_H-27_H):

MR40 DQ Calibration Pattern B (MA<7:0> = 28_H):

Reads to MR40 return DQ Calibration Pattern "B". See "DQ Calibration" on page 117.

MR41:47 (Do Not Use) (MA<7:0> = 29_H-$2F_H$):

MR48:62 (Reserved) (MA<7:0> = 30_H-$3E_H$):

MR63 Reset (MA<7:0> = $3F_H$): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

NOTE 1 For additonal information on MRW RESET see "Mode Register Write Command" on page 119.

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont’d)

MR64:126 (Reserved) (MA<7:0> = 40_H-$7E_H$):

MR127 (Do Not Use) (MA<7:0> = $7F_H$):

MR128:190 (Reserved for Vendor Use) (MA<7:0> = 80_H-BE_H):

MR191 (Do Not Use) (MA<7:0> = BF_H):

MR192:254 (Reserved for Vendor Use) (MA<7:0> = $C0_H$-FE_H):

MR255 (Do Not Use) (MA<7:0> = FF_H):

4 LPDDR2-N Software Interface

4.1 Overlay Window

LPDDR2-NVM functions are controlled using memory-mapped registers in an Overlay Window.

System software can locate the Overlay Window within the memory address range of the device by setting Overlay Window Base Address (OWBA) in Mode Registers 25, 26 and 27.
The Overlay Window can be positioned only at a 8-KByte aligned address within the address map.

The Overlay Window can be enabled by setting the OWE bit of MR24 to ‘1’, and it can be disabled by setting OWD bit of MR24 to ‘1’. If OWE bit and OWD bit are set to ‘0’ the Overlay Window status does not change. If OWD bit is set to ‘1’, OWE bit is automatically cleared to ‘0’.

Once the Overlay Window has been enabled, the address region associated with the overlay window is accessed by the memory controller like any other section of memory in the array. Preactive, Activate, and Read/Write commands are used to access the Overlay Window.

When the Overlay Window is enabled, read accesses to addresses outside the Overlay Window region will access the memory array.

Write commands to addresses outside the Overlay Window may not be allowed.

Within the Overlay Window, memory-mapped control registers are located at static offsets from the base address (OWBA). The Overlay Window region contains: program buffer, device information, registers to control memory array operation, etc.

While the Overlay Window is enabled, system software can write to (and/or read from) each memory-mapped control register at the address OWBA+RegisterStaticOffset according to register definitions shown on the Overlay Window: Control Register Offsets and Definitions Table on page 38.

While the Overlay Window is disabled, the memory-mapped registers are not available.

4.1.1 Map of Control Registers (offsets and definitions)

Table 23 describes the Overlay Window register map.

Table 23 — Overlay Window: Control Register Offsets and Definitions

Byte-Addressing		Type	Register Item	Default Value (hex)	Notes
Offset (hex)	# of bytes (decimal)				
0x001 – 0x000	2	R	Overlay Window Query String “P”	0x00 - 0x50	
0x003 – 0x002	2	R	Overlay Window Query String “F”	0x00 - 0x46	
0x005 – 0x004	2	R	Overlay Window Query String “O”	0x00 - 0x4F	
0x007 – 0x006	2	R	Overlay Window Query String “W”	0x00 - 0x57	
0x009 – 0x008	2	R	Overlay Window ID	0x00 - 0x20	
0x00B – 0x00A	2	R	Overlay Window Revision	Vendor-Specific	
0x00D – 0x00C	2	R	Overlay Window Size	Vendor-Specific	3
	2		Reserved for JEDEC		1,2
0x011 – 0x010	2	R	Program-Buffer Offset	Vendor-Specific	4
0x013 – 0x012	2	R	Program-Buffer Size	Vendor-Specific	5
0x021 – 0x020	2	R	JEDEC Manufacturer ID	Vendor-Specific	
0x023 – 0x022	2	R	JEDEC Device ID	Vendor-Specific	
0x03F – 0x024	28		Reserved for JEDEC		1,2
0x07F – 0x040	64	Vendor-Specific	Reserved for Vendor Use	Vendor-Specific	
0x081 – 0x080	2	W	Command Code	0x00 - 0x00	6
	2		Reserved for JEDEC		1,2
0x087 – 0x084	4	R/W	Command Data		
0x08B – 0x088	4	W	Command Address		7
	4		Reserved for JEDEC		1,2
0x093 – 0x090	4	W	Multi-Purpose Register		8
0x0BF - 0x094	44		Reserved for JEDEC		1,2
0x0C1 - 0x0C0	2	W	Command Execute	0x00 - 0x00	
0x0C7 - 0x0C2	6		Reserved for JEDEC		1,2
0x0C9 - 0x0C8	2	R/W	Suspend	0x00 - 0x00	
0x0CB - 0x0CA	2	R/W	Abort	0x00 - 0x00	
0x0CD - 0x0CC	2	R/W	Status Register	0x00 - 0x80	
0x0CF - 0x0CE	2		Reserved for JEDEC		
0x0DF - 0x0D0	16		Reserved for Vendor Use		
0x0FF – 0x0E0	32	-	Reserved for Vendor Use		
Vendor-Specific	Vendor-Specific	Vendor-Specific	Reserved for Vendor Use		
Vendor-Specific	Vendor-Specific	Vendor-Specific	Program-Buffer		

NOTE 1 System Software shall not write to any Reserved register any value other than 0.
NOTE 2 When read, Reserved registers and Write-Only registers will return indeterminate data.
NOTE 3 Number of bytes in this Overlay Window.
NOTE 4 Program-Buffer Offset is the byte-addressing offset of the beginning of the Program-Buffer in this Overlay Window.
NOTE 5 Program-Buffer Size is the number of bytes in the Program-Buffer in this Overlay Window.
NOTE 6 The memory shall reset this register to Default Value after Device Auto-Initialization, and after complettion of prior command
NOTE 7 Command Address = a[31:0] of byte-address. System software shall write “0” to any most-significant bits of a[31:23] not used by the memory device.
NOTE 8 Multi-Purpose Register is used as DataCount[31:0] in the buffer-program command. DataCount[31:0] = number of contiguous bytes to be programmed using the Program-Buffer. All products allow, but some products may not require, system software to write to this register. DataCount, in conjunction with Command Address, shall not cause data to wrap beyond the end of the Program-Buffer.
NOTE 9 Only one of the following registers may be written to with a value other than 0x0000 during any Write burst: Command Execute, Suspend, Abort, and the Status Register.

4.1.1.1 Command Code Register

Device command codes (e.g., 0x0020 for Block Erase) are written to this register. Command execution occurs only after 0x0001 is written to the Command Execute Register.

See "LPDDR2-NVM Operations" on page 44, for a examples of how the Overlay Window Registers are used.

This register is cleared to its default value after command execution is completed.

Table 24 — Command Code Register

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x081 – 0x080	2	W	Command Code	0x00 - 0x00

4.1.1.2 Command Data Register

Command data might be written to this register. Results of queries might be provided through this register.

Table 25 — Command Data Register

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x087 – 0x084	4	R/W	Command Data	

4.1.1.3 Command Address Register

The command address (e.g., the first data address for buffered program operation, the block address for erase operation) is written to this registers. The address value (a[31:0]) shall be in byte units.

System software shall write "0" to any most-significant bits of a[31:23] not used by the memory device.

Table 26 — Command Address Register

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x08B – 0x088	4	W	Command Address	

4.1.1.4 Multi-Purpose Register

The Multi-Purpose Register is used in several operations. For example, it shall be loaded with the number of contiguous bytes to be programmed during a buffered program operation.

It shall be loaded with the last block address during a block lock/unlock/lock-down operation.

Table 27 — Multi-Purpose Register

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x093 – 0x090	4	W	Multi-Purpose Register	

4.1.1.5 Command Execute Register

Command execution begins when “0x0001” is written to this register. It is allowed to write this register only when the device is ready (DRB = “1”). The device executes the current command in the Command Code register. Before writing “0x0001” to the Command Execute register, the user can change the contents of the Command Code register (and any related parameters) any number of times.

It is allowed only to write “0x0001” to this register - writing any another value is prohibited, and may result in undefined operation.

Table 28 — Command Execute Register

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x0C1 - 0x0C0	2	W	Command Execute	0x00 - 0x00

4.1.1.6 Suspend Register

When “0x0001” is written to this register, an on-going erase or program operation is suspended. Writing to this register is allowed only while the device is busy performing an erase or program operation - writes during other times are ignored.

It is allowed only to write “0x0001” to this register - writing any other value can result in undefined operation.

The Suspend register returns “0x0001” from the time a Suspend command is written until the device is ready (DRB = “1”). The Suspend register returns “0x0000” in all other cases. Once the embedded operation has suspended (or completed), the Suspend register is reset by the device and returns “0x0000” when read.

Table 29 — Suspend Register

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x0C9 - 0x0C8	2	R/W	Suspend	0x00 - 0x00

The Status Register shall be read to check if the suspend request was successful: SR.6=1 indicates erase suspend was successful; SR.2=1 indicates program suspend was successful.

Otherwise, if the suspend request was not successful (SR.6=0; SR.2=0), the ongoing program or erase operation may have completed successfully before the suspend could take effect; system software should test all Status Register flags to be certain.

The Suspend Register resets to its default value after suspending the program or erase operation. Also, successful completion of any on-going program or erase operation will clear this register.

Once the device is suspended, the Resume command must be issued in order to continue the program or erase operation. Refer to section “Program/Erase Suspend” on page 65 for additional details.

Suspend feature is optional. If LPDDR2-NVM does not support suspend feature, Suspend Register can be set only to ‘0x0000’, and when read Suspend Register shall output the value ‘0x0000’.

4.1.1.7 Abort Register

When “0x0001” is written to this register, all on-going embedded operations are aborted. Writing to this register is allowed only while the device is busy performing an embedded operation - writes during other times are ignored.

It is allowed only to write “0x0001” to this register - writing any other value can result in undefined operation.

Table 30 — Abort Register

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x0CB - 0x0CA	2	R/W	Abort	0x00 - 0x00

The Abort register returns “0x0001” from the time a Abort command is written until the device is ready (DRB = “1”). The Abort register returns “0x0000” in all other cases. Once the embedded operation has aborted (or completed), the Abort register is reset by the device and returns “0x0000” when read.

This register resets to its default value by the device after all embedded operations have ceased and the device becomes ready (SR.7 = “1”). If any embedded operation is aborted and does not complete due to that abort, one or more error flags will be set in SR (SR.4 and/or SR.5).

Refer to section “Abort” on page 68 for additional details.

Abort feature is optional. If LPDDR2-NVM does not support abort feature, Abort Register can be set only to ‘0x0000’, and when read Abort Register shall output the value ‘0x0000’.

4.1.1.8 Status Register

The Status Register (SR) indicates the state (Ready or Busy) of the device, and status of program, erase, and the other embedded operations.

Table 31 — Status Register

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
0x0CD - 0x0CC	2	R/W	Status Register	0x00 - 0x80

In particular, SR.7 indicates the state of the device: SR.7 = ’1’ indicates the device is Ready; SR.7 = ’0’ indicates the device is Busy.

The following Status Register bits are related to the results of embedded operations: Control Mode Status Bit (SR.9), Object Mode Status Bit (SR.8), Erase Status (SR.5), Program Status (SR.4), Voltage Supply Error Status (SR.3), and Block Lock Status (SR.1). These bits are set by the device. These bits are cumulative and can only be cleared by writing a ‘1’ to the Status Register bit to be cleared (W12C is an acronym for “write one to clear”). If these bits are written with a ‘0’, their value will not change.

The following Status Register bits are related to the current state of any in process embedded operation: Device Busy (SR.7), Erase Suspended (SR.6), and Program Suspended (SR.2). These bits are set and cleared by the device. Only the value ‘0’ shall be written to this bits, which will be ignored.

Status Register bit SR.1, SR.2, SR.3, SR.4, SR.5, SR.6, SR. 8, and SR.9 are invalid while SR.7 = ‘0’ (DRB = ‘0’).

4.1.1.8 Status Register (cont'd)

Table 32 — Status Register details

Bit	Name	Type	Description
SR.15 : SR.10	(Reserved)	R Only	Reserved for future use.
SR.9	CMSB Control Mode Status Bit	W12C	[CMSB,OMSB] indicates additional error conditions for LPDDR2-NVM devices which support programming operations based on Programming Region. [CMSB,OMSB] = 00 -->Programming successful [CMSB,OMSB] = 01 --> Programming Error: programming attempt to an Object Mode Programming Region [CMSB,OMSB] = 10 --> Programming Error: programming attempt to an invalid Programming Region Element; [CMSB,OMSB] = 11 --> Programming Error: programming attempt using illegal command PSB will also be set along with [CMSB,OMSB] for the above error conditions.
SR.8	OMSB Object Mode Status Bit	W12C	
SR.7	DRB Device Ready Bit	R Only	DRB indicates Erase, Program, or other embedded operation completion in the device. 0 = Embedded controller is Busy 1 = Embedded controller is Ready bit SR.1, SR.2, SR.3, SR.4, SR.5, SR.6,SR. 8, and SR.9 are invalid while DRB = '0'.
SR.6	ESSB Erase Suspend Status Bit	R Only	ESSB indicates whether the device is in Erase Suspend. After issuing a Suspend command, the embedded controller halts and sets to '1' DRB and ESSB. ESSB remains set until the device receives a Resume command. 0 = Operation in progress/completed 1 = Operation suspended
SR.5	ESB Erase Status Bit	W12C	ESB is set to '1' if an attempted Erase failed. A Command Sequence Error is indicated when SR.4, SR.5 and SR.7 are set. 0 = Erase operation successful 1 = Erase Error
SR.4	PSB Program Status Bit	W12C	PSB is set to '1' if an attempted program failed. A Command Sequence Error is indicated when SR.4, SR.5 and SR.7 are set. 0 = Program operation successful 1 = Program Error
SR.3	VSESB Voltage Supply Error Status Bit	W12C	VSESB indicates whether the VACC level is valid voltage. 0 = VACC valid voltage level 1 = VACC invalid voltage level, operation aborted
SR.2	PSSB Program Suspend Status Bit	R Only	PSSB indicates whether the device is in Program Suspend. After receiving a Suspend command, the embedded controller halts execution and sets to '1' DSB and PSSB, which remains set until a Resume command is received. 0 = Operation in progress/completed 1 = Operation suspended
SR.1	BLSB Block Lock Status Bit	W12C	BLSB indicates whether Program or Erase was attempted on a locked block. If the block is locked, the embedded controller sets to '1' BLSB and aborts the operation. 0 = Unlocked 1 = Aborted Write attempt on a locked block
SR.0	(Reserved)	R Only	Reserved for future use.

NOTE 1 The "W12C" Status Register bits type are set by the device and can be cleared by writing '1' to them (W12C is an acronym for "write one to clear")
NOTE 2 The "R only" Status Register bits type can be written only with the value '0' when clearing the status bits.
NOTE 3 ESSB (SR.6) and ESB (SR.5) are reserved if a device does not require Erase features
NOTE 4 ESSB (SR.6) and PSSB (SR.2) are reset if the suspended program or/and erase is/are aborted by writing "0x0001" to the Abort Register.
NOTE 5 PSSB (SR.2) is reserved if a device does not support program suspend.
NOTE 6 ESB (SR.5) is set to '1' if an erase operation is aborted by writing "0x0001" to the Abort Register.
NOTE 7 PSB (SR.4) is set to '1' if a program operation is aborted by writing "0x0001" to the Abort Register.
NOTE 8 CMSB (SR.9) and OMSB (SR.8) are used to indicate error conditions for LPDDR2-NVM devices which support programming region modes. They are reserved in case programming region modes are not supported.
NOTE 9 All Reserved bits are driven to '0' by the device, and shall be written with '0'.
NOTE 10 LPDDR2-N devices may implement Vendor Specific features. Refer to Vendor Datasheets for a complete description of the NVM Status Register

4.1.1.9 Program-Buffer

The Program-Buffer is used during Buffered Program operation to input the data to be written in memory array. The Program-Buffer shall be filled prior writing “0x0001” to the Command Execute Register.

Refer to Vendor Datasheets for information about Program-Buffer offset and Program-Buffer size.

Table 33 — Program-Buffer

Byte-Addressing		Type	Register Item	Default Value (hex)
Offset (hex)	# of bytes (decimal)			
Vendor-Specific	Vendor-Specific	Vendor-Specific	Program-Buffer	

4.2 Data Byte Lane Assignment for Overlay Window Register

Registers included in the Overlay Window might have various size: 1-byte, 2-byte, 4-byte, etc.

Table 34 describes how each byte of an Overlay Window Register is mapped to data byte lane (DQ[7:0], DQ[15:8], DQ[23:16] and DQ[31:24]) in case of x8, x16 and x32 LPDDR2-NVM.

In particular, examples for 1-byte, 2-byte and 4-byte registers are shown.

To properly access the Overlay Window Register it is necessary to ensure the correct assignment of each data bit.

Table 34 — Overlay Window Register Byte Lane Assignment

Byte-Addressing		Register	Data Bus Width					
			x8		x16		x32	
Offset (hex)	# of bytes (decimal)		C1 C0	DQ	C1 C0	DQ	C1 C0	DQ
0x000	1	OneByte_Reg_A[7:0]	0 0	DQ[7:0]	0 0	DQ[7:0]	0 0	DQ[7:0]
0x001	1	OneByte_Reg_B[7:0]	0 1	DQ[7:0]		DQ[15:8]		DQ[15:8]
0x002	1	OneByte_Reg_C[7:0]	1 0	DQ[7:0]	0 1	DQ[7:0]		DQ[23:16]
0x003	1	OneByte_Reg_D[7:0]	1 1	DQ[7:0]		DQ[15:8]		DQ[31:24]
0x001 – 0x000	2	TwoBytes_Reg_A[7:0]	0 0	DQ[7:0]	0 0	DQ[7:0]	0 0	DQ[7:0]
		TwoBytes_Reg_A[15:8]	0 1	DQ[7:0]		DQ[15:8]		DQ[15:8]
0x003 – 0x002	2	TwoBytes_Reg_B[7:0]	1 0	DQ[7:0]	0 1	DQ[7:0]		DQ[23:16]
		TwoBytes_Reg_B[15:8]	1 1	DQ[7:0]		DQ[15:8]		DQ[31:24]
0x003 – 0x000	4	FourBytes_Reg_A[7:0]	0 0	DQ[7:0]	0 0	DQ[7:0]	0 0	DQ[7:0]
		FourBytes_Reg_A[15:8]	0 1	DQ[7:0]		DQ[15:8]		DQ[15:8]
		FourBytes_Reg_A[23:16]	1 0	DQ[7:0]	0 1	DQ[7:0]		DQ[23:16]
		FourBytes_Reg_A[31:24]	1 1	DQ[7:0]		DQ[15:8]		DQ[31:24]

4.3 LPDDR2-NVM Operations

LPDDR2-NVM can be produced from a variety of memory array technologies. This section is not intended to describe full details of LPDDR2-NVM operations.

The scope of this section is to provide a standard for some aspects of LPDDR2-NVM software interface, that might be in common among most of NVM technologies.

Based on this standard memory vendors will define their own memory specification, adding all necessary details for the proper use of the device. These details are technology dependant and not easy to predict for emerging or completely new technologies.

Some possible exceptions to the standard are mentioned. It is recommended to refer to the device specification for the complete description.

This section includes the following commands: NOP, Single Word Program, Buffered Program, Block Erase, Block Lock, Block Unlock, Block Lock-Down, Resume, Suspend, Command Execute, and Abort.

Table 35 defines the command code values to be written to the Command Code Register within the Overlay Window (see Overlay Window register map table).

An embedded controller handles all timings and verifies the correct execution of LPDDR2-NVM operations.

The commands can be initiated when the embedded controller is not busy (DRB = “1”). The Device Ready Bit (DRB) is read as part of the Status Register.

VACC shall not change during the period starting from at least 1us prior to the initiation of any embedded operation until that embedded operation is complete.

During the execution of an embedded operation, the device can be placed in Power Down mode by driving CKE low, see Power Down section for detailed description on how to enter and exit Power Down.

Table 35 — Command Codes

Operation	Code	Command	Note
NOP	0x0000	No Operation	1
Program	0x0041	Single Word Program	2
	0x0042	Single Word Overwrite	4
	0x00E9	Buffered Program	
	0x00EA	Buffered Overwrite	4
Erase	0x0020	Block Erase	
Block Lock	0x0061	Block Lock	
Block Unlock	0x0062	Block Unlock	
Block Lock-Down	0x0063	Block Lock-Down	
Resume	0x00D0	Resume	

NOTE 1 The Command Code Register default value is 0x0000 (NOP). If the Command Execute Register is set to ‘0x0001’ when Command Code Register is at the default value (0x0000), the device will become busy and then ready without executing any operation (NOP).

NOTE 2 Single Word Program is optional.

NOTE 3 For Mode Register accesses and commands, See “Mode Register Definition” on page 23.

NOTE 4 Single Word Overwrite and Buffered Overwrite are optional and are only supported by some NVM technologies and some LPDDR2-NVM devices.

4.4 Nomenclature

Table 36 — Definition of terms

Term	Definition
Block	A group of bits that erase with one erase command
Main Array	A group of blocks used for storing code or data
Partition	A group of blocks that share common program and erase circuitry

4.5 Acronyms

Table 37 — Definition of acronyms

Term	Definition
MR	Mode Register
MRR	Mode Register Read
MRW	Mode Register Write
OP0,OP1,...,OP7	OP0, OP1, ..., OP7 represent bit 0,1,...,7 of a Mode Register
CFI	Common Flash Interface
DU	Don’t Use
RFU	Reserved for Future Use
SR	Status Register
OW	Overlay Window
OWBA	Overlay Window Base Address
NVM	Non Volatile Memory
DDR	Double Data Rate
SDR	Single Data Rate

4.6 Conventions

Table 38 — Definition of conventions

Term	Definition
0x	Hexadecimal number prefix
0b	Binary number prefix
Byte	8 bits
Word	2 bytes = 16 bits
Kbit	1024 bits
KByte	1024 bytes
Mbit	1,048,576 bits
MByte	1,048,576 bytes
lower case ‘a’	It represents a logical address bit (e.g. a5)
MRj	It represents Mode Register number ‘j’ (e.g. MR22)
MRj.OPk	It represents bit ‘k’ of Mode Register ‘j’ (e.g. MR22.OP4)
A[m:n]	It denotes a group of similarly named signals, such address bus (e.g. FirstAdd[31:0])
Ak	It denotes the element ‘k’ of a group of signals, such an address bit (e.g. FirstAdd7)
OWBA+offset	It denotes the address value obtained adding ‘offset’ to ‘OWBA’ (e.g. OWBA+0x088)

4.7 Overlay Window Enable and Disable

When the Overlay Window is enabled, it overlaps a portion of the memory array area.

To enable the Overlay Window the value 0x01 shall be written to MR24. To disable the Overlay Window the value 0x02 shall be written to MR24.

The Overlay Window Base Address shall be stored to MR27, MR26 and MR25.

In particular, if OWBA[31:0] is the desired Overlay Window base address, MR27-MR25 shall be set as follows:
MR27[OP7:OP0] = {0,0,0,0,OWBA[31:28]}
MR26[OP7:OP0] = {OWBA[27:20]}
MR25[OP7:OP0] = {OWBA[19:13],0}

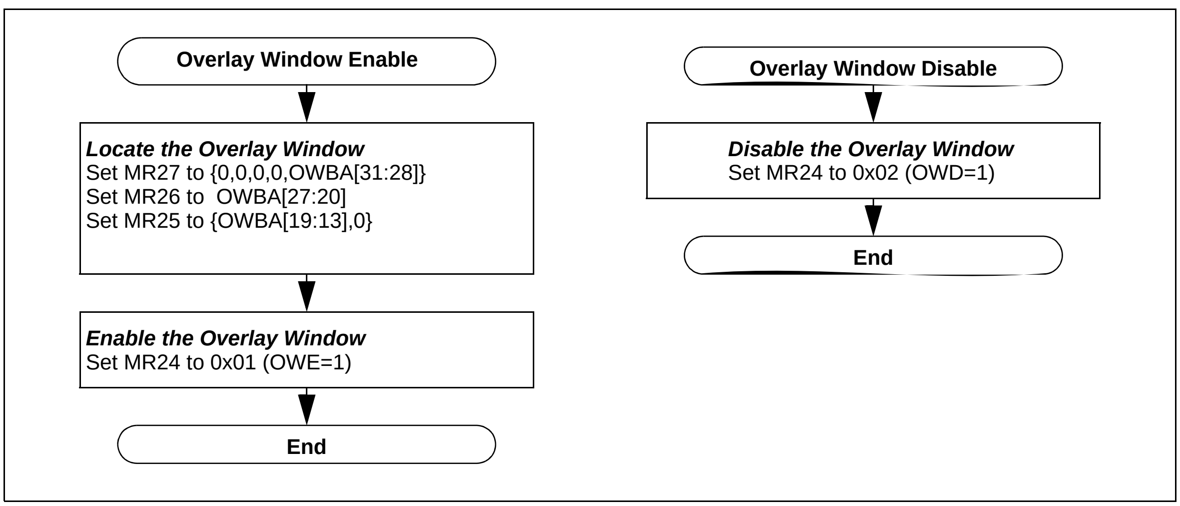
OWBA[12:0] value is assumed to be 0x0000, therefore the Overlay Window can be positioned only at a 8-KByte aligned address.

MR27, MR26 and MR25 shall be written only if the Overlay Window is disabled, OWBA shall be changed only if the MR24.OP0 is ‘0’ (OWE).

Software may open the Overlay Window, and close it immediately after it has accessed it. Alternatively, it may keep the Overlay Window open continuously on a fixed location of the memory map.

If the Overlay Window is enabled and the device is busy (DRB = ‘0’), write access to the Overlay Window is not allowed expect for the Suspend and Abort registers.

If the Overlay Window is enabled and the device is busy (DRB = ‘0’), read access to the Overlay Window is allowed. Some OW locations may have valid content only with device ready, refer to device datasheet for complete information.



NOTE OWBA is the byte address of the desired Overlay Window Base Address

Figure 7 — Overlay Window Enable and Disable

4.7.1 Block Lock Command

The Block Lock command is used to lock a block, a consecutive range of blocks, or all blocks and prevents program or erase operations from changing the data within this range. Some LPDDR2-N devices may support locking single blocks or a range of blocks, while other LPDDR2-N devices may only support locking all blocks.

Locked blocks are fully protected from program or erase operations. Any program or erase operations attempted on a locked block will return an error in the Status Register. The status of a locked block can be changed to unlocked using the Block Unlock command.

All blocks are locked after power-up or reset. In LPDDR2 memory, reset is achieved by writing MR63.

Block Lock operation is performed by the embedded processor. Block Lock operation shall not be interrupted by reset or abort (if supported), otherwise the result of this operation is unpredictable.

Block Lock status does not change if an ongoing operation other than Block Lock, Block Unlock and Block Lock-Down is aborted by writing 0x0001 to the Abort Register.

Block Lock operations cannot be suspended.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

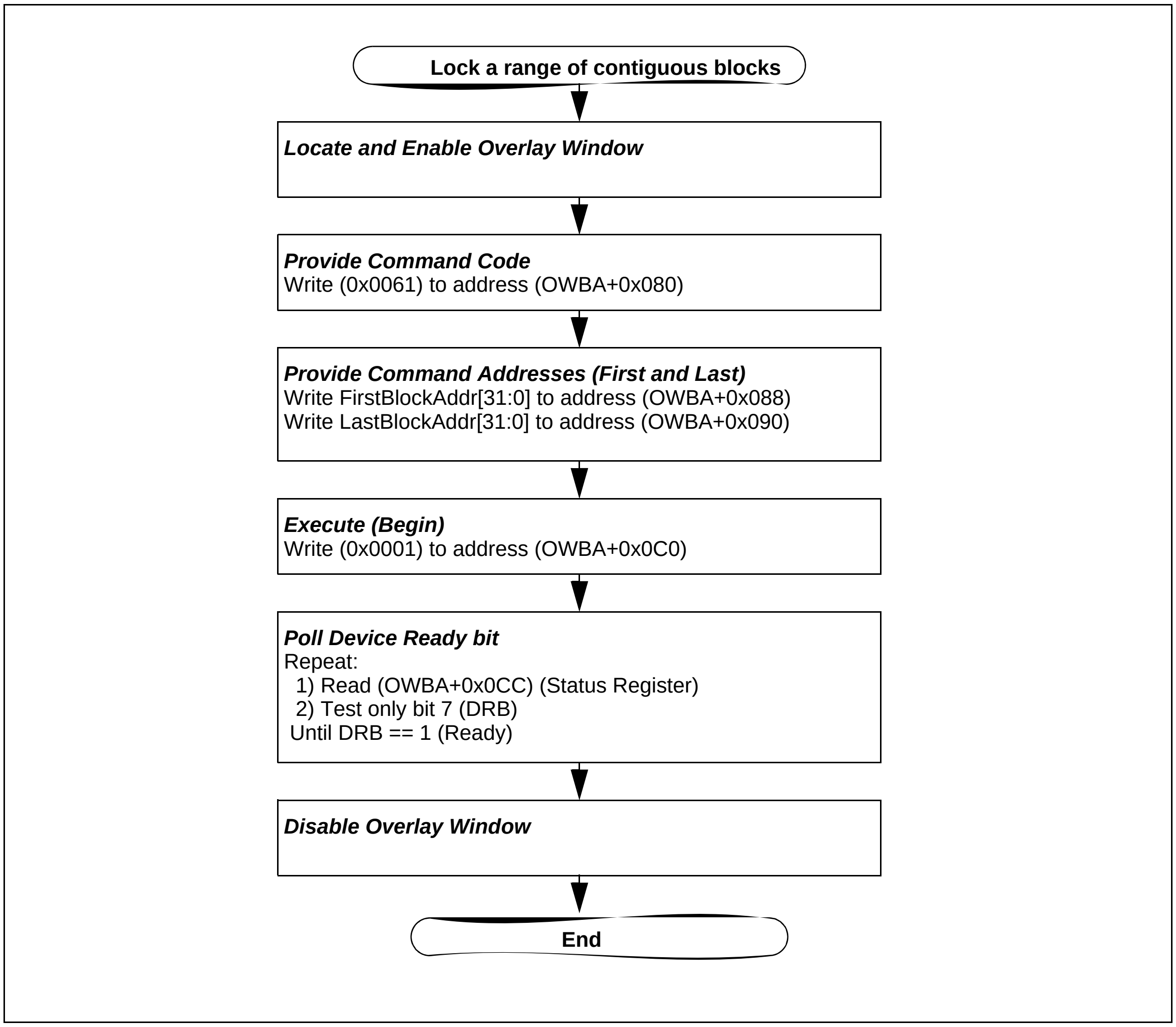
The Command Sequence is:
- Write 0x0061 to the Command Code Register,
- Write any address within the desired start block to the Command Address Register,
- Write any address within the desired stop block to the Multi-Purpose Register,
- Write 0x0001 to the Command Execute Register.

For LPDDR2-N devices that only support locking all blocks, the addresses in the Command Address Register and Multi-Purpose Register are not used and are “Do Not Care”.

NVM vendors may implement additional security features not described in the JEDEC spec. Users shall refer to the device datasheet for complete information.

Some NVM technologies might not have the notion of block, because they do not require and support the erase operation.

4.7.1 Block Lock Command (cont'd)



NOTE 1 The Overlay Window must be open to issue Block Lock command

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 FirstBlockAddr[31:0] is any byte address within the first block being locked. This step is not required for devices that only support locking all blocks with the Block Lock command.

NOTE 5 LastBlockAddr[31:0] is any byte address within the last block being locked. This step is not required for devices that only support locking all blocks with the Block Lock command.

NOTE 6 If the address written at the location OWBA+0x088 (FirstBlockAddr[31:0]) is greater than the address written at the location OWBA+0x090 (LastBlockAddr[31:0]) the block lock status will not change and the Status Register bits PSB and ESB are set. This error check is not required for devices that only support locking all blocks with the Block Lock command.

NOTE 7 Some LPDDR2-N devices will lock all blocks with the Block Lock command. Refer to vendor datasheets for complete information on the Block Lock command.

Figure 8 — Block Lock Command Flowchart

4.7.2 Block Unlock Command

The Block Unlock command is used to unlock a block or a consecutive range of blocks, allowing the block to be programmed or erased.

The status of a unlocked block can be changed to locked using the Block Lock command. Some LPDDR2-N devices may only support unlocking a single block or a range of blocks at any given time. For these devices, the blocks not selected by the Block Unlock command will be changed to locked after the completion of the Block Unlock command.

All blocks are locked after power-up or reset. In LPDDR2 memory, reset is achieved by writing MR63.

Block Unlock operation is performed by the embedded processor. Block Unlock operation shall not be interrupted by reset or abort (if supported), otherwise the result of this operation is unpredictable.

Block Lock status does not change if an ongoing operation other than Block Lock, Block Unlock and Block Lock-Down is aborted by writing 0x0001 to the Abort Register.

Block Unlock operations cannot be suspended.

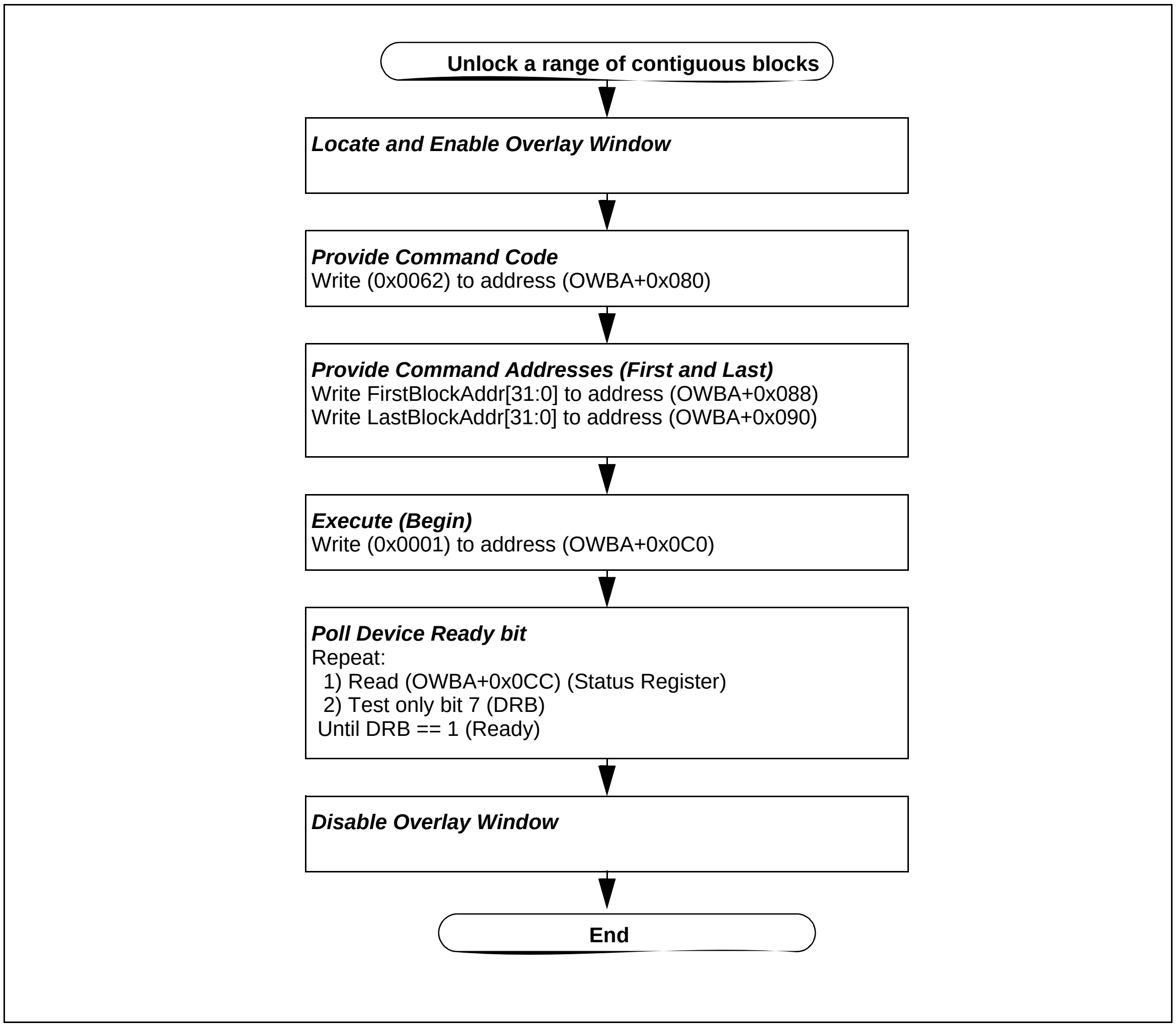
The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:
• Write 0x0062 to the Command Code Register,
• Write any address within the desired start block to the Command Address Registers,
• Write any address within the desired stop block to the Multi-Purpose Registers,
• Write 0x0001 to the Command Execute Register.

NVM vendors may implement additional security features not described in the JEDEC spec. Users shall refer to the device datasheet complete information.

Some NVM technologies might not have the notion of block, because they do not require and support the erase operation.

4.7.2 Block Unlock Command (cont’d)



NOTE 1 The Overlay Window must be open to issue Block Unlock command

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB==’1’) before starting the command sequence.

NOTE 4 FirstBlockAddr[31:0] is any byte address within the first block being unlocked.

NOTE 5 LastBlockAddr[31:0] is any byte address within the last block being unlocked.

NOTE 6 If the address written at the location OWBA+0x088 (FirstBlockAddr[31:0]) is greater than the address written at the location OWBA+0x090 (LastBlockAddr[31:0]) the block lock status will not change and the Status Register bits PSB and ESB are set.

NOTE 7 Some LPDDR2-N devices will unlock only one block or a range of blocks selected by the Block Unlock command. All other blocks will be locked by these devices. Refer to vendor datasheets for complete information on the Block Unlock command.

Figure 9 — Block Unlock Flowchart

4.7.3 Block Lock-Down Command

The Block Lock-Down command is used to lock-down a block or a consecutive range of blocks, and prevent program or erase operations from changing the data in it.

Locked-Down blocks are fully protected from program or erase operations. Any program or erase operations attempted on a locked-down block will return an error in the Status Register. The status of a locked-down block is reset to the default locked state only after removing and applying again the power supply.

All blocks are locked after power-up or reset. In LPDDR2 memory, reset is achieved by writing MR63.

Block Lock-Down operation is performed by the embedded processor. Block Lock-Down operation shall not be interrupted by reset or abort (if supported), otherwise the result of this operation is unpredictable.

Block Lock status does not change if an ongoing operation other than Block Lock, Block Unlock, and Block Lock-Down is aborted by writing 0x0001 to the Abort Register.

Block Lock-Down operations cannot be suspended.

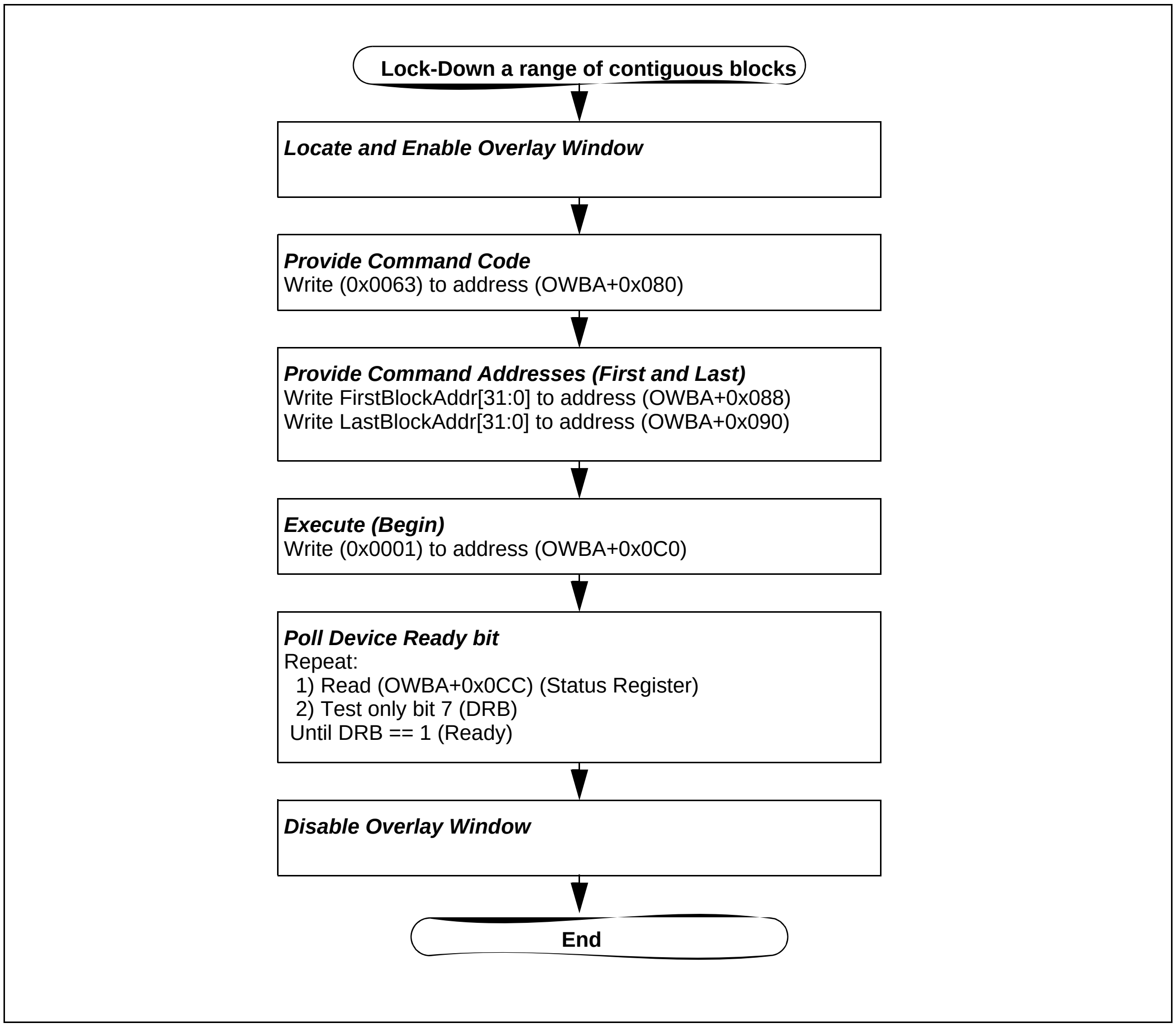
The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:
• Write 0x0063 to the Command Code Register,
• Write any address within the desired start block to the Command Address Registers,
• Write any address within the desired stop block to the Multi-Purpose Registers,
• Write 0x0001 to the Command Execute Register.

NVM vendors may implement additional security features not described in the JEDEC document. Users shall refer to the device datasheet for complete information.

Some NVM technologies might not have the notion of block, because they do not require and support the erase operation.

4.7.3 Block Lock-Down Command (cont'd)



NOTE 1 The Overlay Window must be open to issue Block Lock-Down command

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 FirstBlockAddr[31:0] is any byte address within the first block being locked

NOTE 5 LastBlockAddr[31:0] is any byte address within the last block being locked

NOTE 6 If the address written at the location OWBA+0x088 (FirstBlockAddr[31:0]) is greater than the address written at the location OWBA+0x090 (LastBlockAddr[31:0]) the block lock status will not change and the Status Register bits PSB and ESB are set.

Figure 10 — Block Lock-Down Command Flowchart

4.7.4 Block Erase Command

The Block Erase command is used to erase a Block. It sets all the bits within the selected Block to ’1’. All previous data in the Block is lost. If the Block is locked, the erase operation will abort, the data in the Block will not be changed and the Device Status Register will output the error.

The erase operation is performed by the embedded controller.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:
Write 0x0020 to the Command Code Register,
Write any address within the desired block to the Command Address Registers,
Write 0x0001 to the Command Execute Register

The erase operation can be suspended.

If a block being erased is locked during an erase suspend, the operation will complete normally when it is resumed.

The erase is aborted by writing MR63, or writing 0x0001 to the Abort Register (if supported).

As data integrity cannot be guaranteed when the Block Erase operation is aborted, the Block must be erased again.

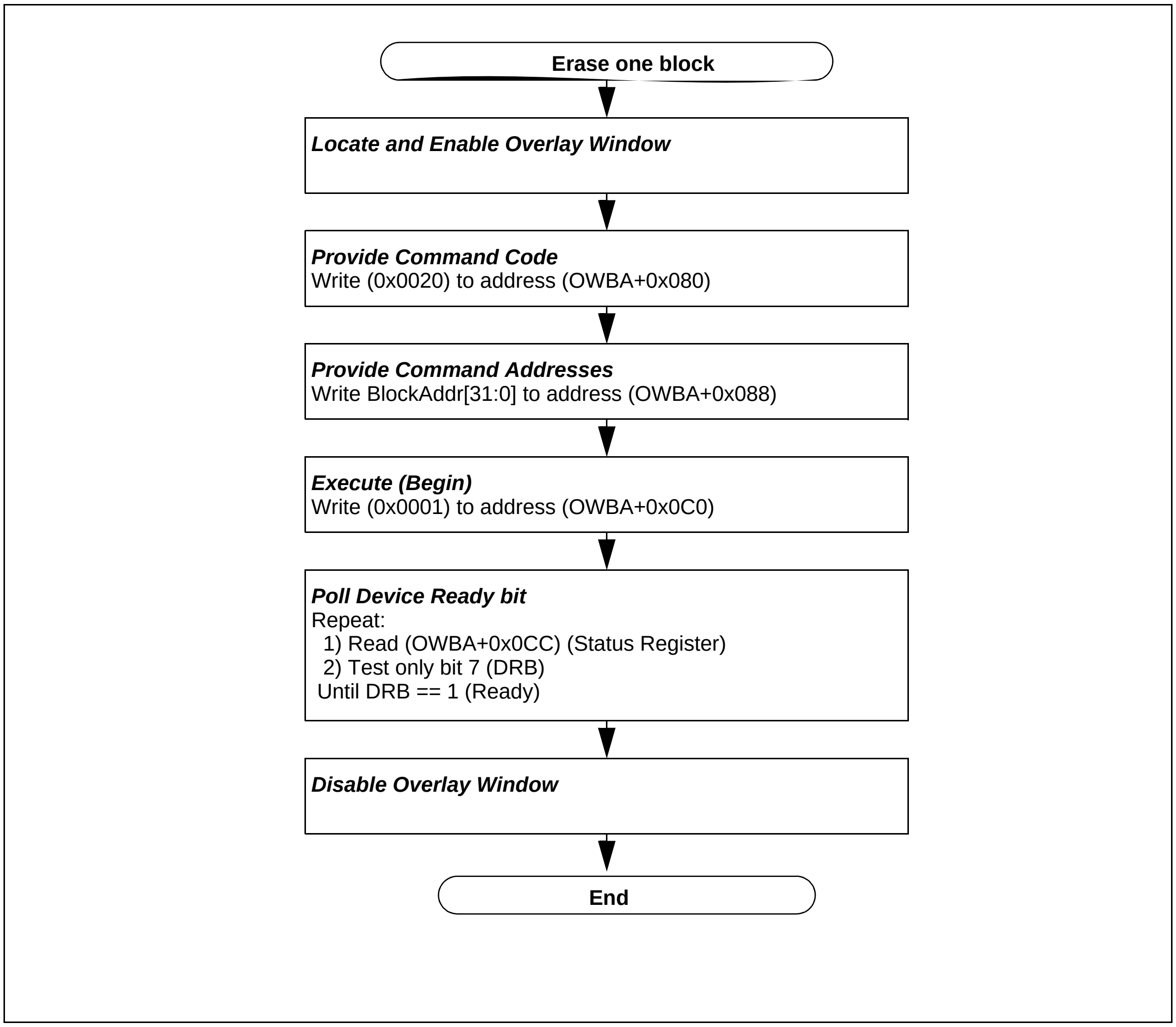
Note that some NVM technologies do not need Erase command, therefore some NVM devices will not support it.

Table 39 — Block Erase Error Conditions

7	6	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	1	0	0	0	0	0	Erase operation failure
1	0	1	0	0	0	1	0	Erase operation abort. An erase operation was attempted on a locked block.
1	0	1	0	1	0	0	0	Erase operation abort. VACC not at appropriate level for Erase operation.
1	0	1	1	0	0	0	0	Erase operation abort. Block address outside the LPDDR2-NVM address space.
1	0	1	1	0	0	0	0	Erase operation abort. Attempting to erase a block during Erase Suspend or Program Suspend.

4.7.4 Block Erase Command (cont'd)

Figure 11 shows the Block Erase Flowchart.



NOTE 1 The Overlay Window must be open to issue Block Erase command

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 BlockAddr[31:0] is any byte address within the block being erased

Figure 11 — Block Erase Flowchart

4.7.5 Single Word Program Command

The Single Word Program command is used to program a single word (2-byte data) to the memory array.

This is a legacy command and it is optional.

The program operation is performed by the embedded controller.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:
Write 0x0041 (or 0x0040) to the Command Code Register,
Write desired location address to the Command Address Register,
Write desired program data to the Command Data Register (Command Data[15:0] only),
Write 0x0001 to the Command Execute Register.

Programming can be performed in one block at a time.

The Status Register DRB bit, indicates the progress of the Program operation. It should be read to check whether the operation has completed or not.

After completion of the Program operation (DRB= 1), one of the Status Register error bits (4,3 and 1) going High means that an error was detected: either a failure occurred during programming, VACC is outside the allowed voltage range or an attempt to program a locked Block was made. See Section Device Status Register for detailed information.

The program operation can be suspended.

The program is aborted by writing MR63, or writing 0x0001 to the Abort Register (if supported).

As data integrity cannot be guaranteed when the program operation is aborted, the data must be reprogrammed.

Some NVM technologies support the Single Word Program command only under particular conditions.

For example, for LPDDR2-NVM device that has the notion of program region, Single Word Program Command is supported only by program regions configured in the Control Program mode, and with Command Address value belonging to a particular portion of the program region.

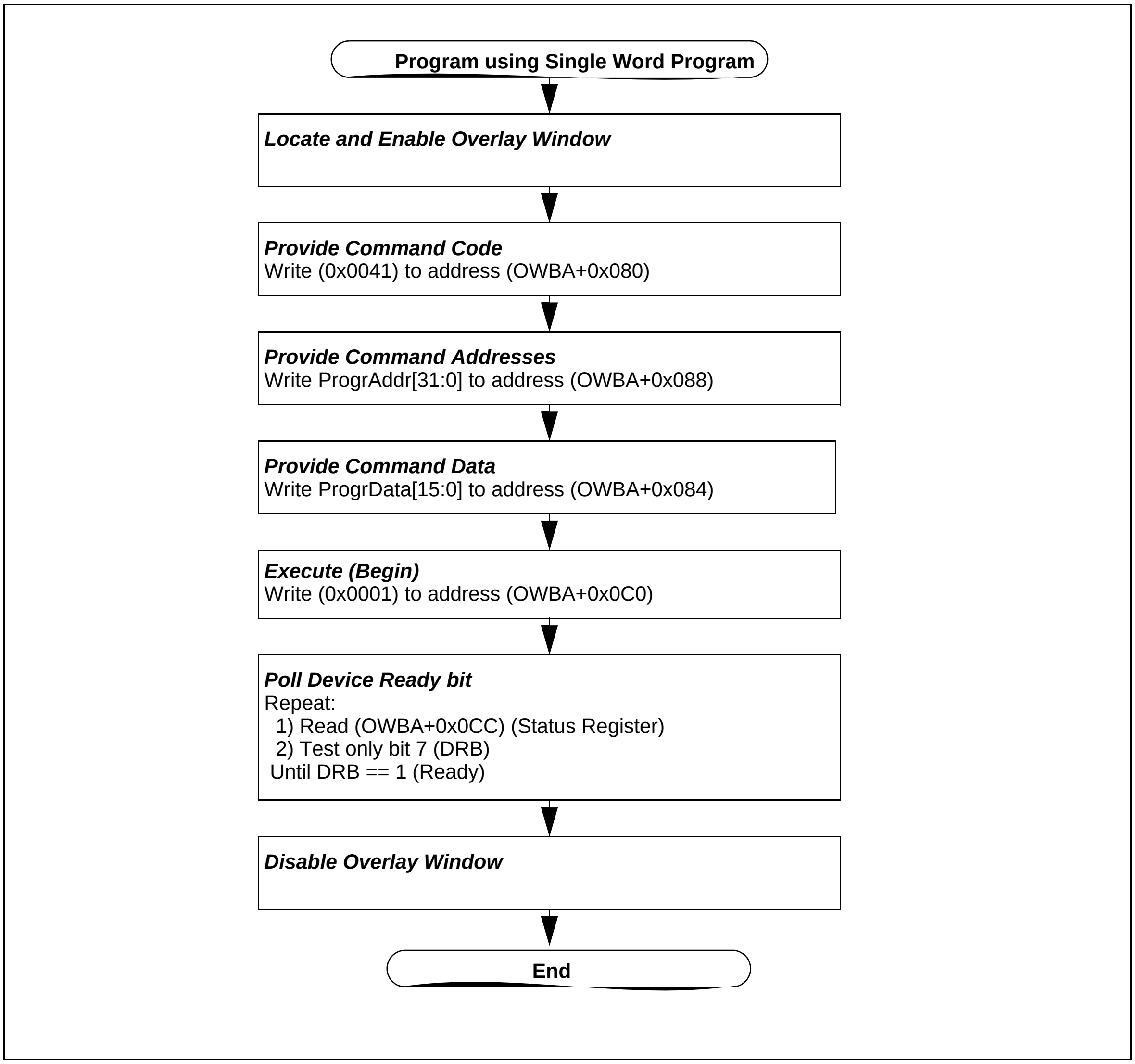
If a Single Word Program command is issued to a Program Region configured in the Object Program mode, the Program operation is aborted and PSB and OMSB Status Register bits are set.

For details about program region and program method see the application note.

Table 40 — Single Word Program Error Conditions

7	6	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Single Word Program operation failure.
1	0	0	1	0	0	1	0	Single Word Program operation abort. An program operation was attempted on a locked block.
1	0	0	1	1	0	0	0	Single Word Program operation abort. VACC not at appropriate level for Program operation.
1	0	1	1	0	0	0	0	Single Word Program operation abort. Program address outside the LPDDR2-NVM address space
1	0	1	1	0	0	0	0	Single Word Program operation abort. Attempting to program during Program Suspend.

4.7.5 Single Word Program Command (cont'd)



NOTE 1 The Overlay Window must be open to issue Single Word Program command

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB==’1’) before starting the command sequence.

NOTE 4 ProgrAddr[31:0] is the target byte address of the programming operation, and ProgrAddr[0] shall be ‘0’.

NOTE 5 ProgrData[15:0] is the desired 2-byte data to be programmed.

Figure 12 — Single Word Program Flowchart

4.7.6 Single Word Overwrite Command

Single Word Overwrite is supported only by some NVM technologies and some LPDDR2-NVM devices.

The Single Word Overwrite command is used to write a single word (2-byte data) to the memory array.

The overwrite command allows to change the status of each bit from ‘1’ to ‘0’ or from ‘0’ to ‘1’.

With the overwrite command the data is written to the memory array allowing to change each bit to ‘0’ or to ‘1’. With the program command only the data bits equal to ‘0’ are written to the memory array, while the data bits equal to ‘1’ are not.

The overwrite operation is performed by the embedded controller.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:
Write 0x0042 to the Command Code Register,
Write desired location address to the Command Address Register,
Write desired program data to the Command Data Register (Command Data[15:0] only),
Write 0x0001 to the Command Execute Register.

Overwriting can be performed in one block at a time.

The Status Register DRB bit, indicates the progress of the Overwrite operation. It should be read to check whether the operation has completed or not.

After completion of the overwrite operation (DRB= 1), one of the Status Register error bits (4, 3 and 1) going High means that an error was detected: either a failure occurred during overwriting, VACC is outside the allowed voltage range or an attempt to overwrite a locked Block was made. See “Status Register” on page 41 for detailed information.

The overwrite operation may be suspended.

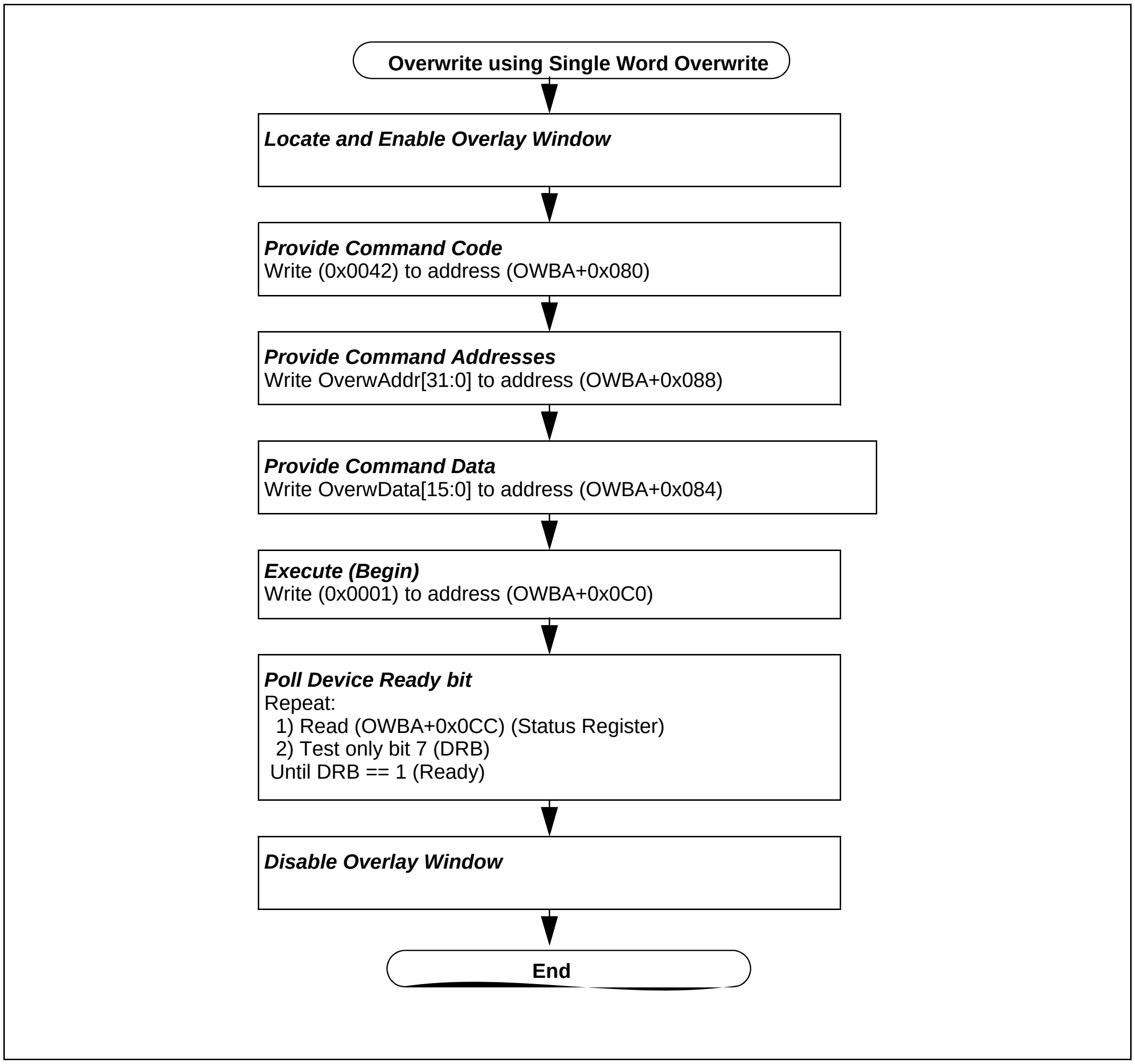
The overwrite is aborted by writing MR63, or writing 0x0001 to the Abort Register (if supported).

As data integrity cannot be guaranteed when the overwrite operation is aborted, the data must be rewritten.

Table 41 — Single Word Overwrite Error Conditions

7	6	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Single Word Overwrite operation failure.
1	0	0	1	0	0	1	0	Single Word Overwrite operation abort. An overwrite operation was attempted on a locked block.
1	0	0	1	1	0	0	0	Single Word Overwrite operation abort. Program voltage violation.
1	0	1	1	0	0	0	0	Single Word Overwrite operation abort. Overwrite address outside the LPDDR2-NVM address space
1	0	1	1	0	0	0	0	Single Word Overwrite operation abort. Attempting to program during Overwrite Suspend or Program Suspend.

4.7.6 Single Word Overwrite Command (cont'd)



NOTE 1 The Overlay Window must be open to issue Single Word Overwrite command

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 OverwAddr[31:0] is the target byte address of the overwriting operation, and OverwAddr[0] shall be '0'.

NOTE 5 OverwData[15:0] is the desired 2-byte data to be overwritten.

Figure 13 — Single Word Overwrite Flowchart

4.7.7 Buffered Program Command

The Buffered Program Command makes use of the device's Program Buffer to speed up programming.

The Buffered Program command dramatically reduces in-system programming time compared to other non-buffered program commands.

If N is the size of the Program Buffer within the Overlay Window, up to N-Bytes can be loaded into the Program Buffer and programmed into the specified N-Byte aligned location in the main array. The region is determined by bit [31: K] of the Command Address Register value, where $N=2^k$.

The first word data of the Program Buffer to be programmed depends on bit [K-1:0] of Command Address value. The programming operation proceeds for a contiguous number of bytes equal to the Data Count value. The Data Count value is in units of bytes and written in the Multi-Purpose Registers.

If the Command Address [K-1:0] value plus the Data Count Register value exceeds the program buffer boundary (N-byte), the programming operation ends without programming the memory array and the Status Register will show an error (0xB0).

The programming operation doesn't wrap within the program buffer and doesn't cross into the next programming region.

The Overlay Window must be open and the device must be ready (DRB= 1) before starting the command sequence.

The Command Sequence is:

Write the starting address to the Command Address registers,
Write the Data Count value (number of bytes to be programmed) to the Multi-Purpose Registers,
Write data into the Program Buffer. The Program Buffer fits within the N-byte aligned array space,
Write 0x00E9 to the Command Code Register,
Write 0x0001 to the Command Execute Register.

If the Block being programmed is locked an error will be set in the Status Register and the operation will abort without affecting the data in the memory array.

The Buffered Program operation can be suspended.

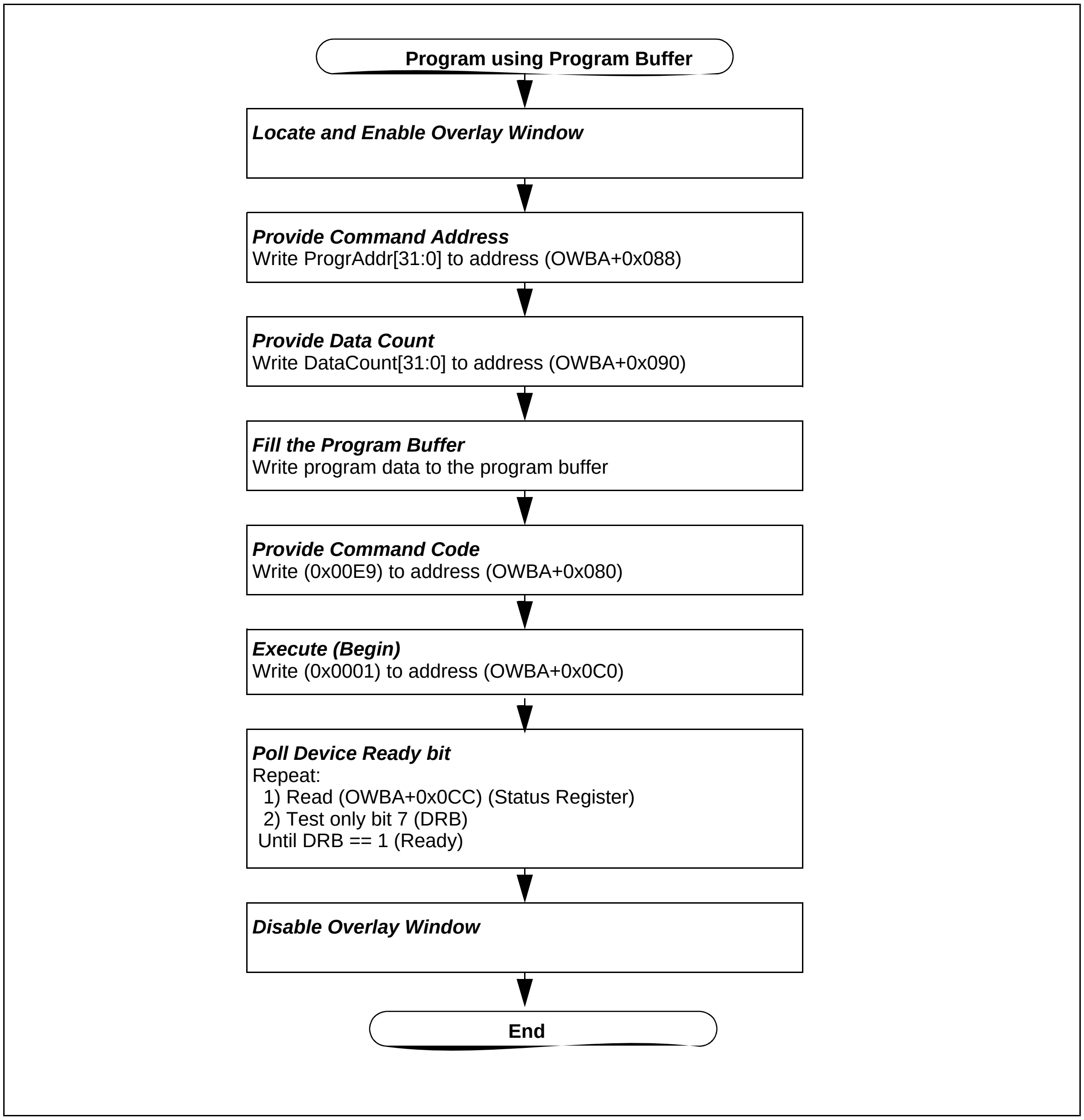
The program is aborted by writing MR63, or writing 0x0001 to the Abort Register (if supported). As data integrity cannot be guaranteed when the program operation is aborted, the memory array content must be considered invalid.

Table 42 — Buffered Program Error Conditions

7	6	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Buffered Program operation failure.
1	0	0	1	0	0	1	0	Buffered Program operation abort. An program operation was attempted on a locked block.
1	0	0	1	1	0	0	0	Buffered Program operation abort. Invalid VACC voltage.
1	0	1	1	0	0	0	0	Buffered Program operation abort. Program address outside the LPDDR2-NVM address space
1	0	1	1	0	0	0	0	Buffered Program operation abort. Attempting to program during Program Suspend.
1	0	1	1	0	0	0	0	Buffered Program operation abort. Command Address [K-1:0] value plus the Data Count Register value exceeds the program buffer boundary (it is greater than N byte).

4.7.7 Buffered Program Command (cont'd)

Figure 14 shows the Buffered Program Flowchart.



NOTE 1 The Overlay Window must be open to issue Buffered Program command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB==’1’) before starting the command sequence.

NOTE 4 DataCount[31:0] is amount of byte being programmed

NOTE 5 ProgrAddr[31:0] is the target byte address of the programming operation.

Figure 14 — Buffered Program Flowchart

4.7.8 Buffered Overwrite Command

This is a command supported only by some NVM technologies and LPDDR2-NVM devices.

The Buffered Overwrite Command makes use of the device's Program Buffer to speed up overwriting data to the memory array. The Buffered Overwrite command reduces in-system overwriting time compared to other non-buffered overwrite commands.

The overwrite command allows to change the status of each bit from '1' to '0' or from '0' to '1'.

With the overwrite command the data is written to the memory array allowing to change each bit to '0' or to '1'. With the program command only the data bits equal to '0' are written to the memory array, while the data bits equal to '1' are not.

If N is the size of the Program Buffer within the Overlay Window, up to N-Bytes can be loaded into the Program Buffer and overwritten into the specified N-Byte aligned location in the main array. The region is determined by bit [31: K] of the Command Address Register value, where $N=2^k$.

The first word data of the Program Buffer to be overwritten depends on bit [K-1:0] of Command Address value. The overwriting operation proceeds for a contiguous number of bytes equal to the Data Count value. The Data Count value is in units of bytes and written in the Multi-Purpose Registers.

If the Command Address [K-1:0] value plus the Data Count Register value exceeds the program buffer boundary (N-byte), the overwriting operation ends without overwriting the memory array and the Status Register will show an error (0xB0).

The overwriting operation doesn't wrap within the program buffer and doesn't cross into the next programming region.

The Overlay Window must be open and the device must be ready (DRB= 1) before starting the command sequence.

The Command Sequence is:

Write the starting address to the Command Address Registers,
Write the Data Count value (number of bytes to be overwritten) to the Multi-Purpose Registers,
Write data into the Program Buffer. The Program Buffer fits within the N-byte aligned array space,
Write 0x00EA to the Command Code Register,
Write 0x0001 to the Command Execute Register.

If the Block being overwritten is locked an error will be set in the Status Register and the operation will abort without affecting the data in the memory array.

The Buffered Overwrite operation can be suspended.

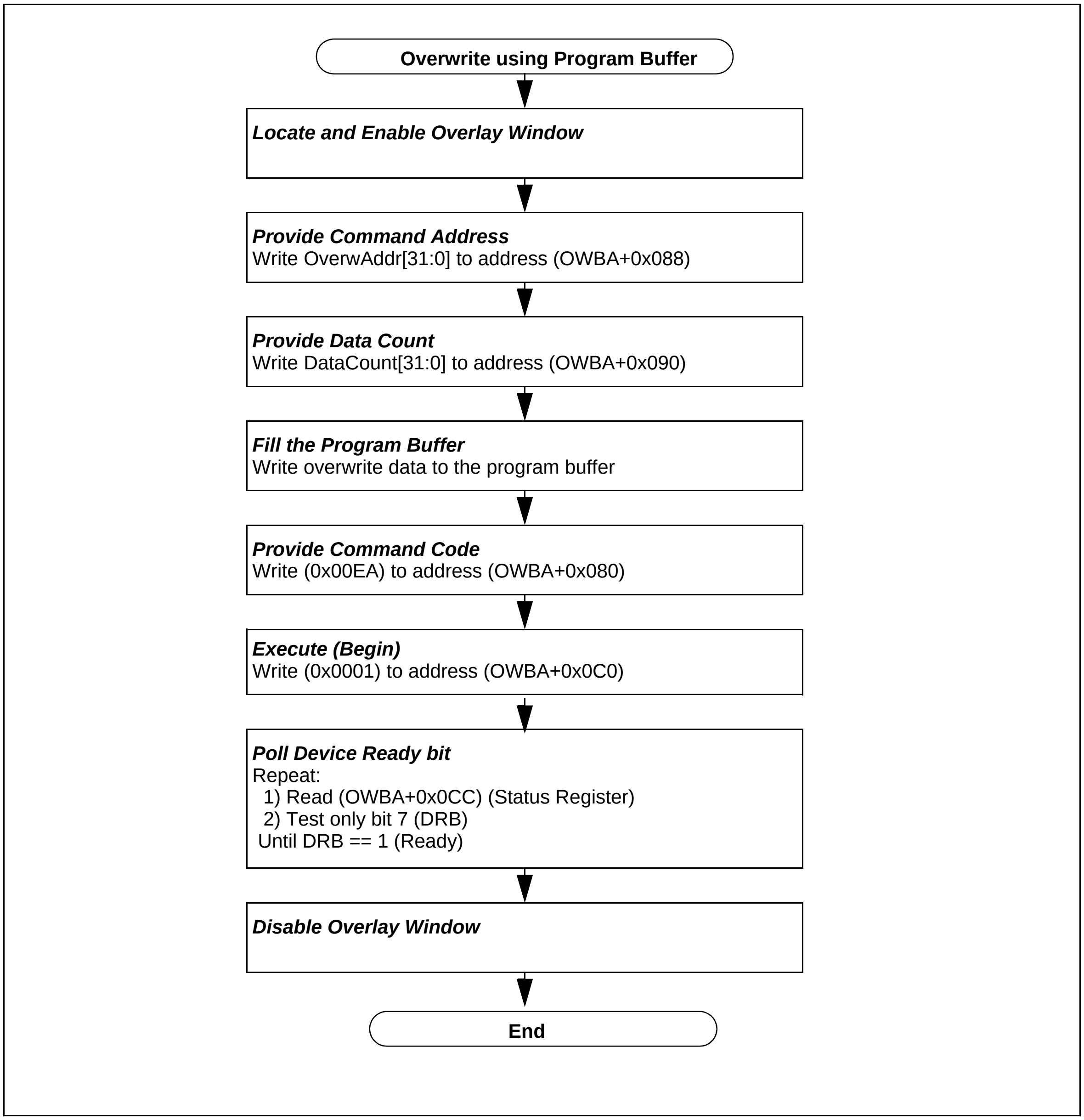
The overwrite is aborted writing MR63, or writing 0x0001 to the Abort Register (if supported). As data integrity cannot be guaranteed when the overwrite operation is aborted, the memory array content must be considered invalid.

Table 43 — Buffered Overwrite Error Conditions

7	6	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Buffered Overwrite operation failure.
1	0	0	1	0	0	1	0	Buffered Overwrite operation abort. An overwrite operation was attempted on a locked block.
1	0	0	1	1	0	0	0	Buffered Overwrite operation abort. Invalid VACC voltage.
1	0	1	1	0	0	0	0	Buffered Overwrite operation abort. Overwrite address outside the LPDDR2-NVM address space
1	0	1	1	0	0	0	0	Buffered Overwrite operation abort. Attempting to overwrite during Overwrite Suspend or Program Suspend.
1	0	1	1	0	0	0	0	Buffered Overwrite operation abort. Command Address [K-1:0] value plus the Data Count Register value exceeds the program buffer boundary (it is greater than N byte).

4.7.8 Buffered Overwrite Command (cont'd)

Figure 15 shows the Buffered Overwrite Flowchart.



NOTE 1 The Overlay Window must be open to issue Buffered Overwrite command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

NOTE 4 DataCount[31:0] is amount of byte being overwritten

NOTE 5 OverwAddr[31:0] is the target byte address of the overwriting operation.

Figure 15 — Buffered Overwrite Flowchart

4.7.9 Program/Erase Suspend

The Program/Erase Suspend request pauses a program or block erase operation. The Program/Erase Resume command is required to restart the suspended operation.

Program or erase operations can be suspended. For the complete list of embedded operations that can be suspended, refer to the device datasheet.

The Program/Erase Suspend request is issued by writing ‘0x0001’ to ‘1’ the Suspend Register.

Once the Embedded Controller has paused, bits DRB, ESSB and/or PSSB of the Status Register are set to ‘1’.

The following operations shall be allowed during Program/Erase Suspend:
– Program/Erase Resume
– Read Array (data from erase-suspended block or program-suspended locations is not valid)

Additionally, if the suspended operation was a Block Erase then the following commands are also accepted:
– Single Word Program (except in erase-suspended Block)
– Buffered Program (except in erase suspended Block)
– Block Lock
– Block Unlock

For the complete list of supported commands during Program or Erase Suspend refer to the device datasheet. Commands not supported during Program or Erase Suspend shall be ignored.

During an erase suspend the Block being erased can be protected by issuing the Block Lock. When the Program/Erase Resume command is issued the operation will complete.

During a program suspend it is not allowed to write the program buffer.

It is possible to accumulate multiple suspend operations. For example: suspend an erase operation, start a program operation, suspend the program operation, then read the array. If a Program command is issued during a Block Erase Suspend, the erase operation cannot be resumed until the program operation has completed.

During a Program/Erase Suspend, the device can be placed in Power Down mode by driving CKE low, see Power Down section for detailed description on how to enter and exit Power Down.

Program/Erase is aborted by writing MR63, or writing 0x0001 to the Abort Register (if supported).

Note that some NVM technologies do not need Erase command, therefore some NVM devices will not support it.

4.7.9 Program/Erase Suspend (cont'd)

Figure 16 shows the Program/Erase Suspend Request flowchart.

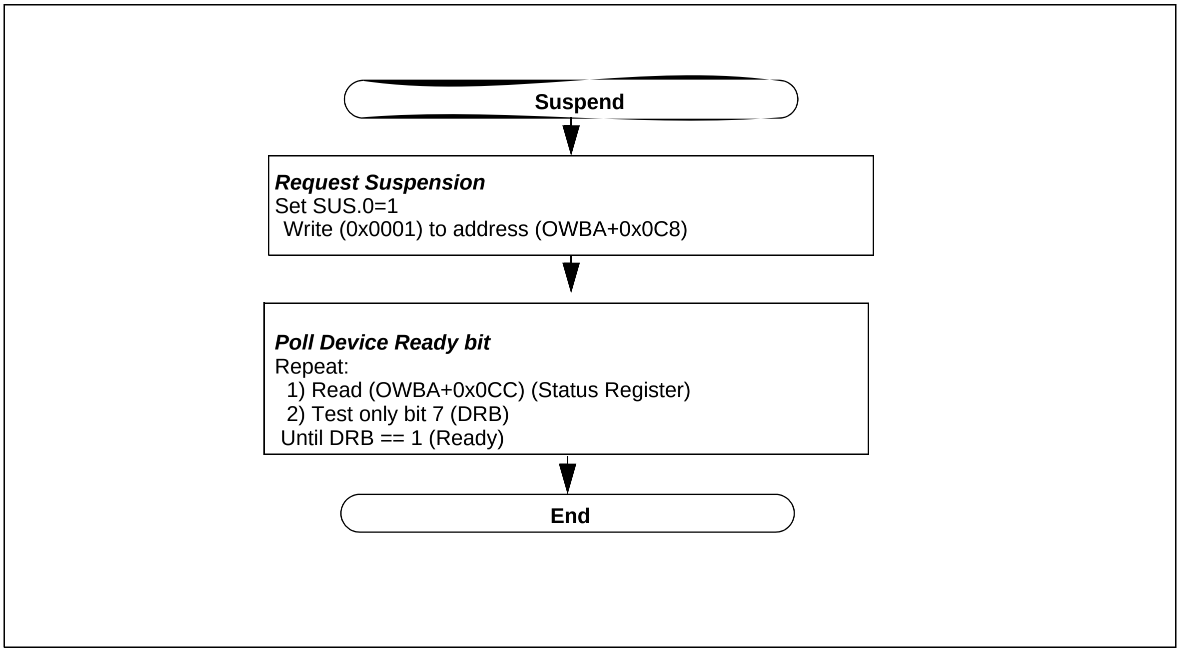


Figure 16 — Program/Erase Suspend Request Flowchart

4.7.10 Program/Erase Resume Command

The Program/Erase Resume command is used to restart a previously suspended program or erase operation.

For the complete list of embedded operations that can be resumed, refer to the device datasheet.

The Overlay Window must be open and the device must be ready (DRB = 1) before starting the command sequence.

The Command Sequence is:
Write 0x00D0 to the Command Code Register
Write 0x0001 to the Command Execute Register.

The command doesn't require to load any value to the Command Address Register within the Overlay Window. It is allowed to issue the Program/Erase resume command only when the embedded controller is in the Ready state and if a program or erase operations has been suspended.

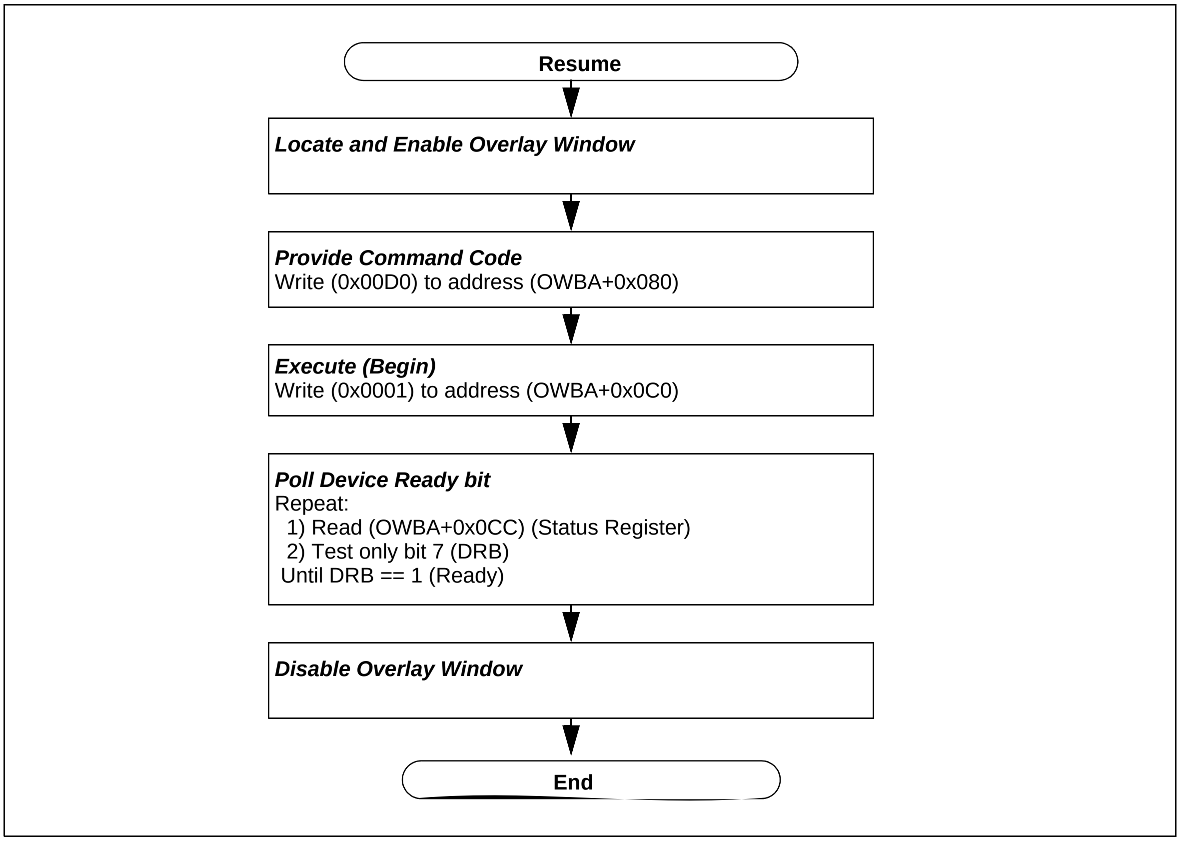
A Resume command when no operation is suspended will be ignored.

If a Program command is issued during a Block Erase Suspend, then the erase cannot be resumed until the program operation has completed.

If an Erase and a Program operation are suspended, the Resume command will Resume the Program command.

Note that some NVM technologies do not need Erase command, therefore some NVM devices will not support it.

Figure 17 shows the Program/Erase Resume command flowchart.



NOTE 1 The Overlay Window must be open to issue the Resume command.

NOTE 2 OWBA is the byte address of the Overlay Window Base Address.

NOTE 3 The device must be Ready (DRB=='1') before starting the command sequence.

Figure 17 — Program/Erase Resume Command Flowchart

4.7.11 Abort

The Abort request ends all embedded operations.

If any embedded operation is aborted and does not complete due to an abort request, the operation will fail and one or more Status Register bits will be set.

If the Abort request is issued while the device is in program or/and erase suspend, the operation can not be resumed, and the related suspend bits in the Status Register are cleared.

The Abort request is issued by writing ‘0x0001’ to the Abort Register.

Once the embedded controller has completed the abort request, bit DRB of the Status Register is set to ‘1’ and the Abort Register is set to ‘0x0000’ by the LPDDR2-NVM device.

Abort feature is optional. If LPDDR2-NVM does not support abort feature, Abort Register may be written only with 0x0000, and when read it shall output the value 0x0000.

Table 44 — Abort Error Conditions

7	6	5	4	3	2	1	0	Description
DRB	ESSB	ESB	PSB	VSESB	PSSB	BLSB	-	
1	0	0	1	0	0	0	0	Abort request issued during program operation. Abort request issued while program suspend.
1	0	1	0	0	0	0	0	Abort request issued during erase operation. Abort request issued while erase suspend.
1	0	1	1	0	0	0	0	Abort request issued during erase and program suspend. Abort request issued during program operation and erase suspend.

4.7.11 Abort (cont’d)

Figure 18 shows the Abort Request flowchart.

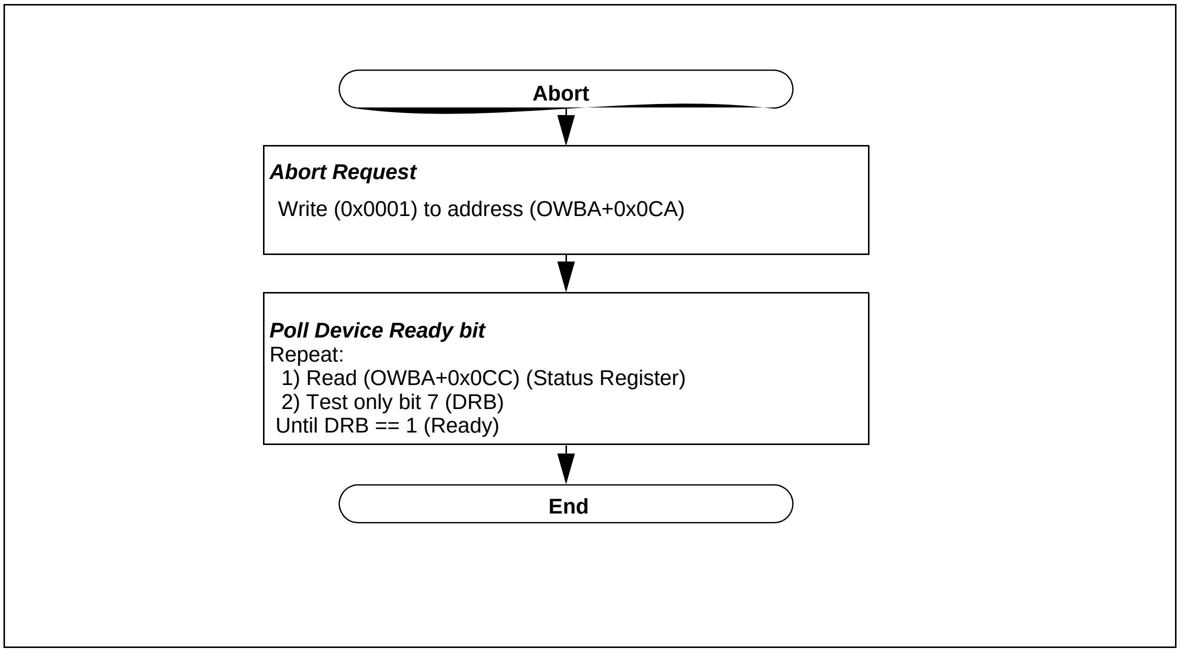


Figure 18 — Abort Request Flowchart

4.8 Dual operations and multiple partition architecture

In some LPDDR2-NVM devices, the memory array may be divided into two or more partitions (multiple partition architecture). Refer to vendor datasheets to determine support for multiple partition architecture.

LPDDR2-NVM devices that support multiple partition architecture provide greater flexibility for software developers to split the code and data spaces within the memory array. The dual operations feature simplifies the software management of the device by allowing code to be executed from one partition while another partition is being programmed or erased.

The dual operations feature means that while programming or erasing in one partition, read operations are possible in another partition with zero latency (only one partition at a time is allowed to be in program or erase mode).

If a read operation is required in a partition, which is programming or erasing, the program or erase operation can be suspended.

Also, if the suspended operation is erase then a program command can be issued to another block, so the device can have one block in erase suspend mode, one programming, and other partitions available for read operations.

For the complete list of dual operations allowed, refer to the device datasheet.

Table 45 — Simultaneous operations allowed in the same partition

Status of partition	Operations allowed in the same partition		
	Read (1)	Buffered Program	Block Erase
Idle	Yes	Yes	Yes
Programming (2)	No	No	No
Erasing	No	No	No
Program suspended	Yes (3)	No	No
Erase suspended	Yes (4)	Yes (5)	No

NOTE 1 Depending on the Overlay Window status and the target read address, data may come from the memory array or from the overlay window.

NOTE 2 Programming may occur during erase suspended.

NOTE 3 LPDDR2-NVM will output invalid data if the read operation occurs in the memory area that is being programmed.

NOTE 4 LPDDR2-NVM will output invalid data if the read operation occurs in the block that is being erased.

NOTE 5 Not allowed in the block that is being erased.

Table 46 — Simultaneous operations allowed in other partitions

Status of partition	Operations allowed in another partition		
	Read (1)	Buffered Program	Block Erase
Idle	Yes	Yes	Yes
Programming (2)	Yes	No	No
Erasing	Yes	No	No
Program suspended	Yes	No	No
Erase suspended	Yes	Yes	No

NOTE 1 Depending on the Overlay Window status and the target read address, data may come from the memory array or from the overlay window.

NOTE 2 Programming may occur during erase suspended.

5 LPDDR2 Command Definitions and Timing Diagrams

5.1 Activate Command

5.1.1 LPDDR2-SX: Activate Command

The SDRAM Activate command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 - BA2 are used to select the desired bank. The row address R0 through R14 is used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The LPDDR2 SDRAM can accept a read or write command at time t_{RCD} after the activate command is sent. Once a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Activate commands to different banks is t_{RRD}.

Certain restrictions on operation of the 8-bank devices must be observed. There are two rules. One for restricting the number of sequential Activate commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

• 8-bank device Sequential Bank Activation Restriction : No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling t_{FAW} window. Converting to clocks is done by dividing t_{FAW}[ns] by t_{CK}[ns], and rounding up to next integer value. As an example of the rolling window, if RU{ (t_{FAW} / t_{CK}) } is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9. REFpb also counts as bank-activation for the purposes of t_{FAW}.

• 8-bank device Precharge All Allowance : t_{RP} for a Precharge All command for an 8-bank device shall equal t_{RPab}, which is greater than t_{RPpb}.

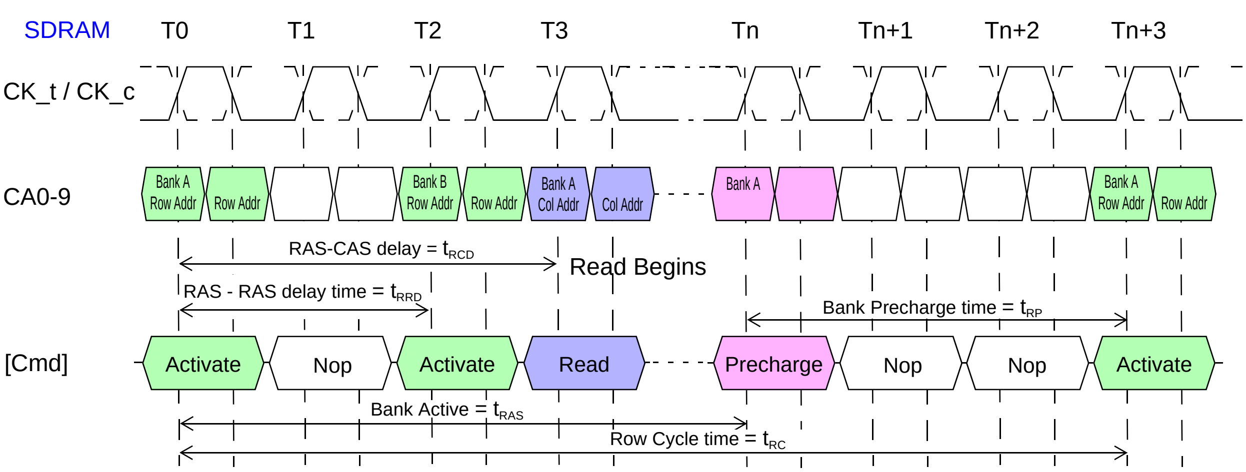


Figure 19 — LPDDR2-SX: Activate command cycle: t_{RCD} = 3, t_{RP} = 3, t_{RRD} = 2

NOTE 1 A Precharge-All command uses t_{RPab} timing, while a Single Bank Precharge command uses t_{RPpb} timing. In this figure, t_{RP} is used to denote either an All-bank Precharge or a Single Bank Precharge.

5.1.1 LPDDR2-SX: Activate Command (cont'd)

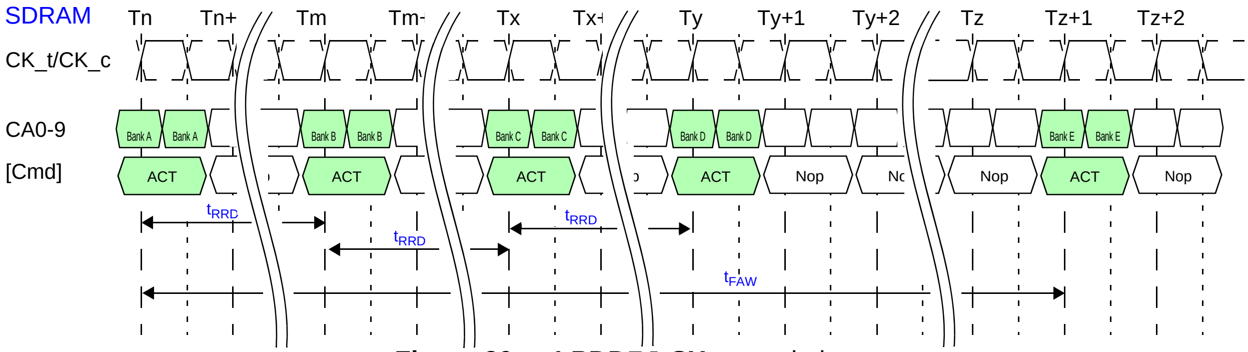


Figure 20 — LPDDR2-SX: t_{FAW} timing

NOTE 1: For 8-bank devices only. No more than 4 banks may be activated in a rolling t_{FAW} window.

5.1.2 LPDDR2-N: Activate Command

The NVM Activate command is issued by holding CS_n LOW, CA0 LOW and CA1 HIGH at the rising edge of the clock. The Row Buffer (RB) addresses BA0 - BA2 are used to select the desired {RAB, RDB} pair. Devices may have four or eight Row Buffer pairs. Row Buffers do not correspond directly to any portion of the array; the controller may use any value of BA0 - BA2 for any array location.

Row address a5 through a19 is used in conjunction with the selected RAB contents to determine which row to load into the destination RDB. The memory controller shall not issue Activate commands causing any single row to be open in more than one RDB at any point in time. All active RDBs shall contain data from unique row addresses. The Activate command must be applied before any Read or Write operation can be executed. The LPDDR2 NVM can accept a read or write command at time t_{RCD} after the activate command is sent. The activate and preactive times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive Activate commands to the same Row Buffer pair is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Activate commands to different Row Buffer pairs is t_{RRD}.

Table 47 — Row Address Buffer selection for Preactive by BA inputs

BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Selected {RAB, RDB} (4-RB devices)	Selected {RAB, RDB} (8-RB devices)
0	0	0	RB 0	RB 0
0	0	1	RB 1	RB 1
0	1	0	RB 2	RB 2
0	1	1	RB 3	RB 3
1	0	0	RB 0	RB 4
1	0	1	RB 1	RB 5
1	1	0	RB 2	RB 6
1	1	1	RB 3	RB 7

5.1.2 LPDDR2-N: Activate Command (cont'd)

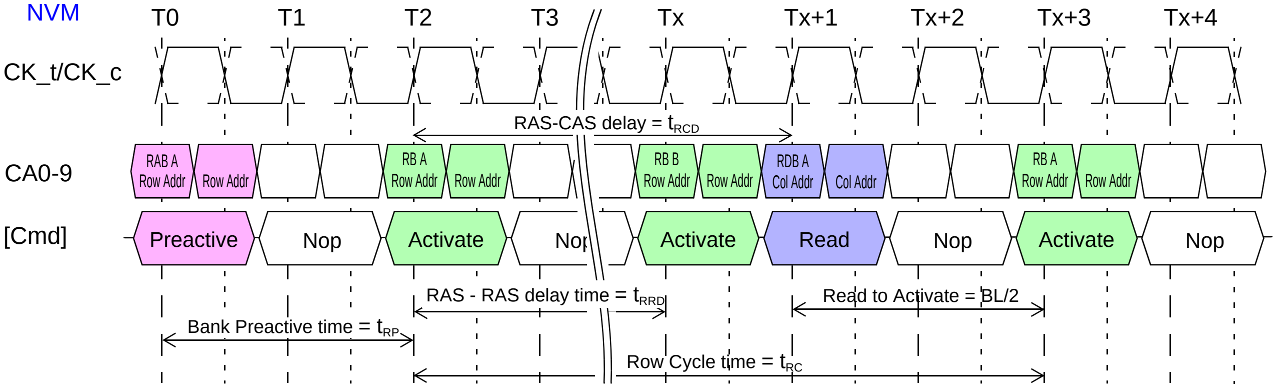
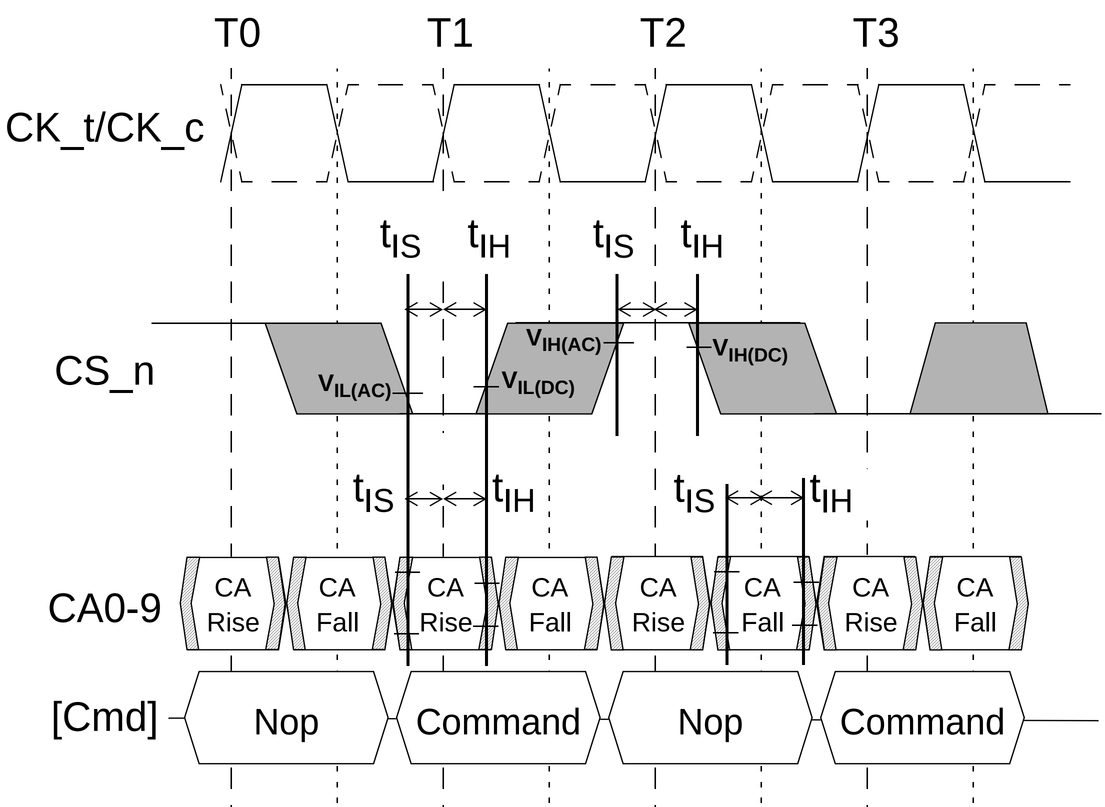


Figure 21 — LPDDR2-N: Activate command cycle: t_{RP} = 2, BL = 4

5.2 LPDDR2 Command Input Setup and Hold Timing



NOTE Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

Figure 22 — LPDDR2: Command Input Setup and Hold Timing

5.3 Read and Write access modes

5.3.1 LPDDR2-SX: Read and Write access modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).

The LPDDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles.

For LPDDR2-S4 devices, a new burst access must not interrupt the previous 4-bit burst operation in case of BL = 4 setting. In case of BL = 8 and BL = 16 settings, Reads may be interrupted by Reads and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and t_{CCD} is met. For LPDDR2-S2 devices, Reads may interrupt Reads and Writes may interrupt Writes, provided that t_{CCD} is met. The minimum CAS to CAS delay is defined by t_{CCD}.

5.3.2 LPDDR2-N: Read and Write access modes

After an RB has been activated, a read or write cycle can be executed. This is accomplished by setting CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).

The LPDDR2 NVM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles. The boundary of the burst cycle is restricted to specific segments of the Row Data Buffer (RDB) size. For example, if the size of the RDB is 64 Bytes and the device has a 16 bit data bus interface, the page size of 512 bits is divided into 8, 4, or 2 uniquely addressable boundary segments depending on burst length, 8 for 4 bit burst, 4 for 8 bit burst, and 2 for 16 bit burst respectively. A 4-bit, 8-bit or 16-bit burst operation will occur entirely within one of the 8, 4 or 2 groups beginning with the column address supplied to the device during the Read or Write Command (C1-C4).

For LPDDR2-N devices, a new burst access must not interrupt the previous 4-bit burst operation in case of BL = 4 setting. In case of BL = 8 and BL = 16 settings, Reads may be interrupted by Reads and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and t_{CCD} is met. The minimum CAS to CAS delay is defined by t_{CCD}.

5.4 Burst Read Command

The Burst Read command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the t_{DQSCK} delay is measured. The first valid datum is available RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW t_{RPRE} before the first rising valid strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin edge aligned with the data strobe. The RL is programmed in the mode registers.

Timings for the data strobe are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

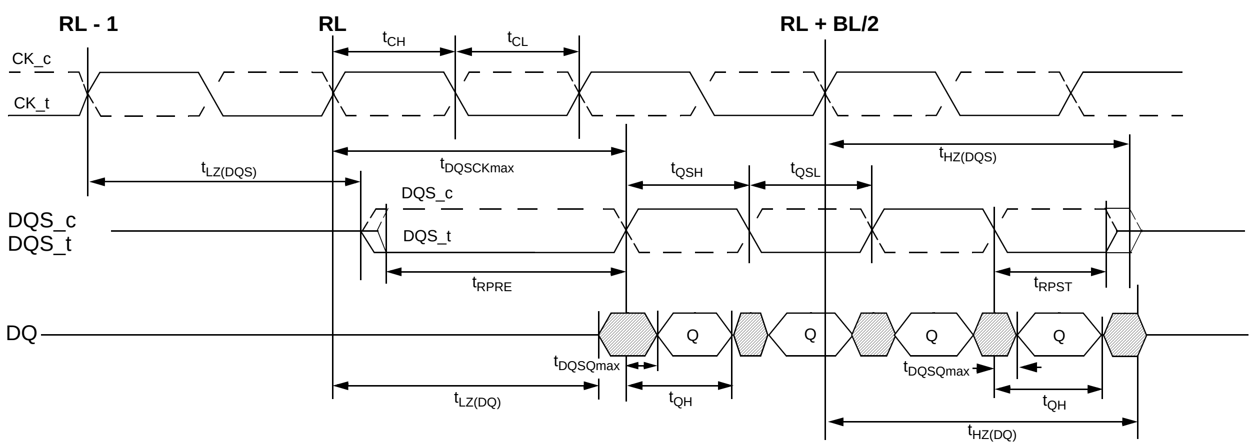


Figure 23 — Data output (read) timing ($t_{DQSCKmax}$)

NOTE 1 t_{DQSCK} may span multiple clock periods.

NOTE 2 An effective Burst Length of 4 is shown.

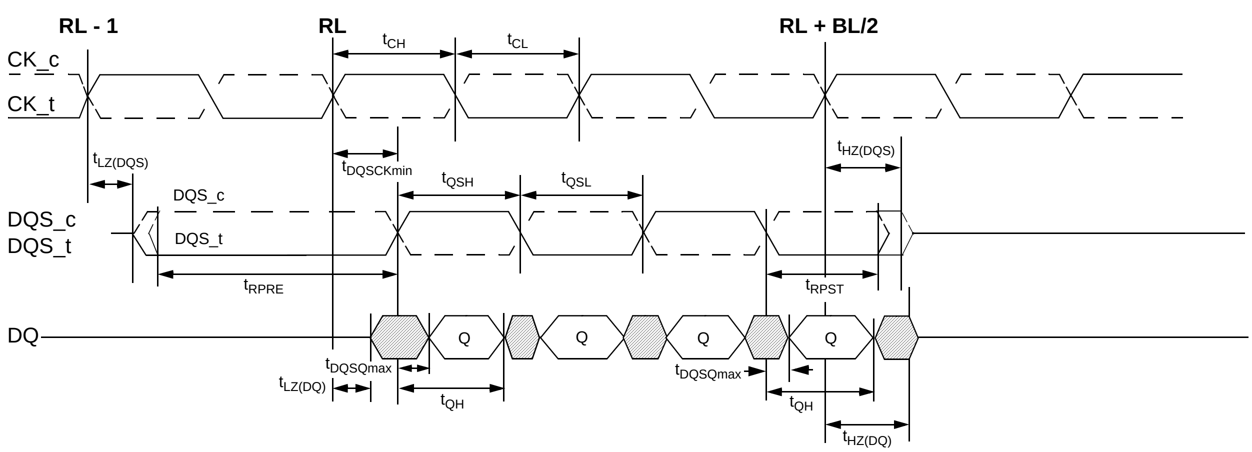


Figure 24 — Data output (read) timing ($t_{DQSCKmin}$)

NOTE 1 An effective Burst Length of 4 is shown.

5.4 Burst Read Command (cont'd)

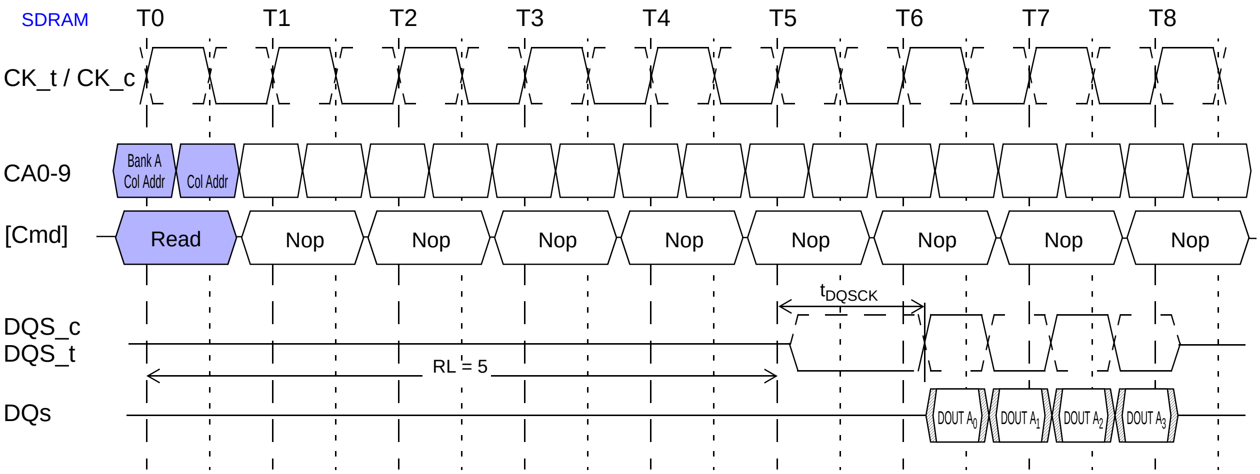


Figure 25 — LPDDR2-SX: Burst read: RL = 5, BL = 4, t_{DQSCK} > t_{CK}

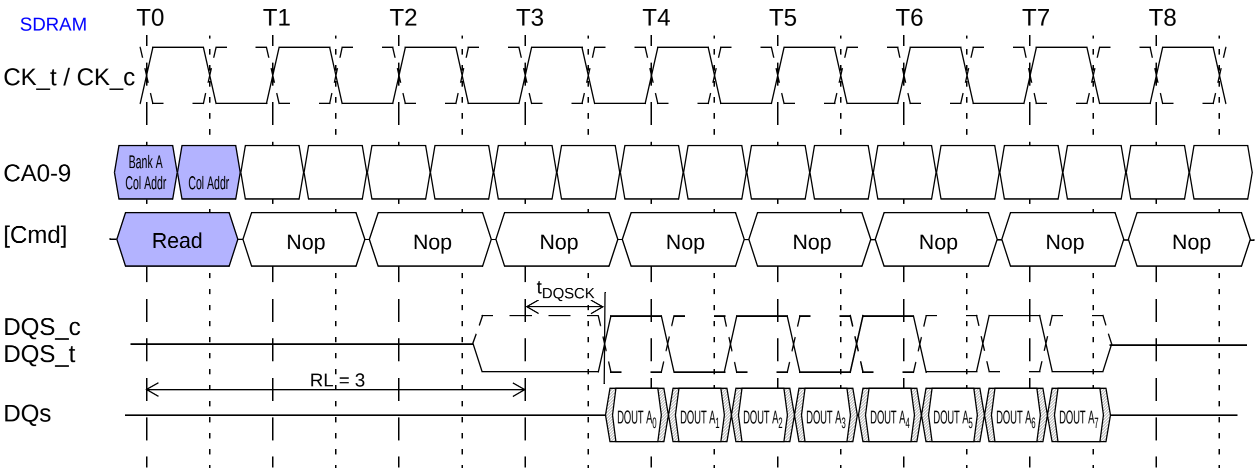


Figure 26 — LPDDR2-SX: Burst read: RL = 3, BL = 8, t_{DQSCK} < t_{CK}

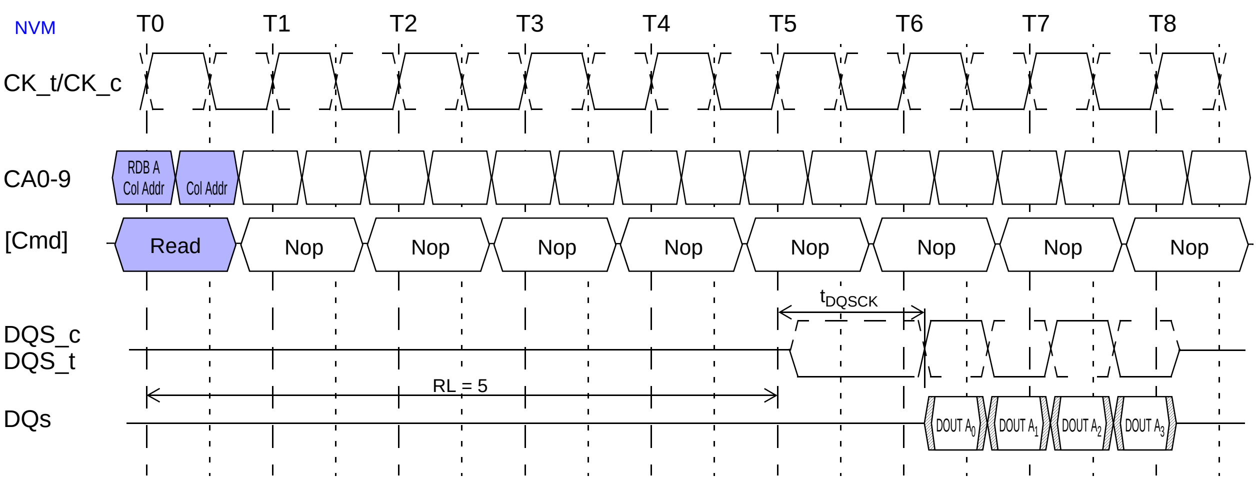


Figure 27 — LPDDR2-N: Burst read: RL = 5, BL = 4, t_{DQSCK} > t_{CK}

5.4 Burst Read Command (cont'd)

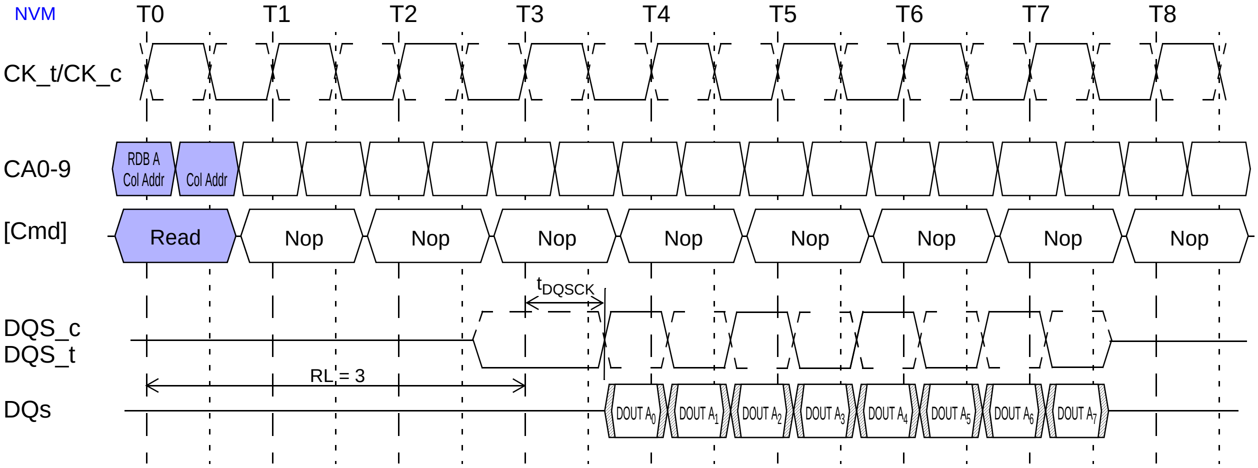


Figure 28 — LPDDR2-N: Burst read: RL = 3, BL = 8, t_{DQSCK} < t_{CK}

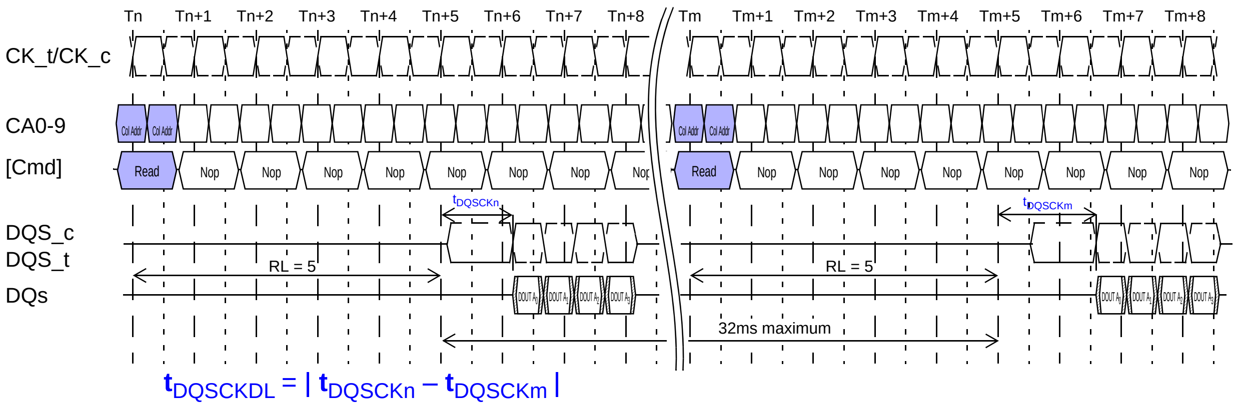


Figure 29 — LPDDR2: $t_{DQSCKDL}$ timing

NOTE 1 $t_{DQSCKDLmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn} ,t_{DQSCKm}} pair within any 32ms rolling window.

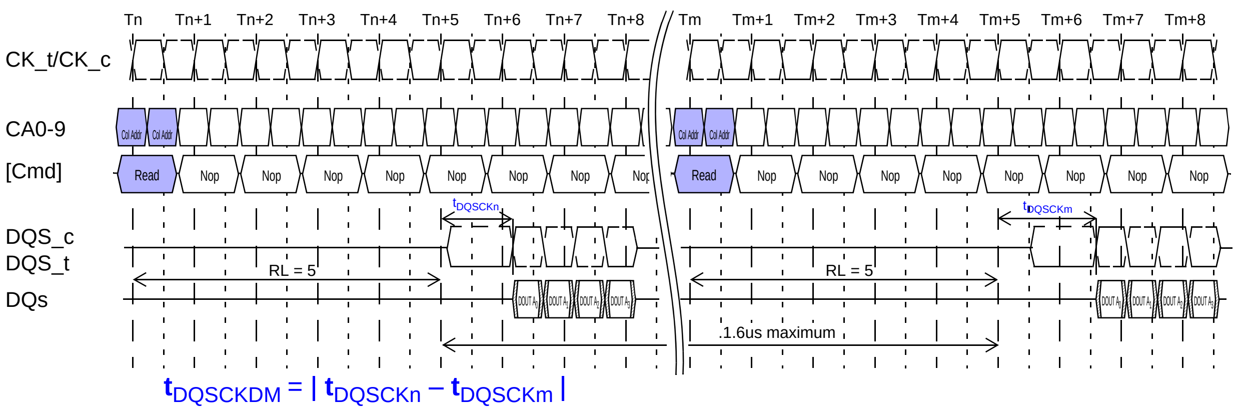


Figure 30 — LPDDR2: $t_{DQSCKDM}$ timing

NOTE 1 $t_{DQSCKDMmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn},t_{DQSCKm}} pair within any 1.6us rolling window.

5.4 Burst Read Command (cont'd)

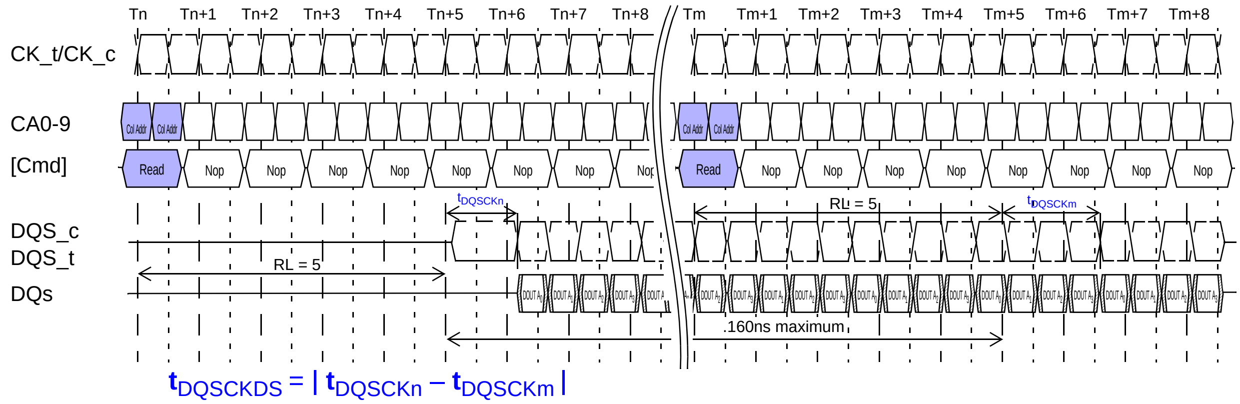


Figure 31 — LPDDR2: $t_{DQSCKDS}$ timing

NOTE 1 $t_{DQSCKDSmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn} ,t_{DQSCKm}} pair for reads within a consectutive burst within any 160ns rolling window.

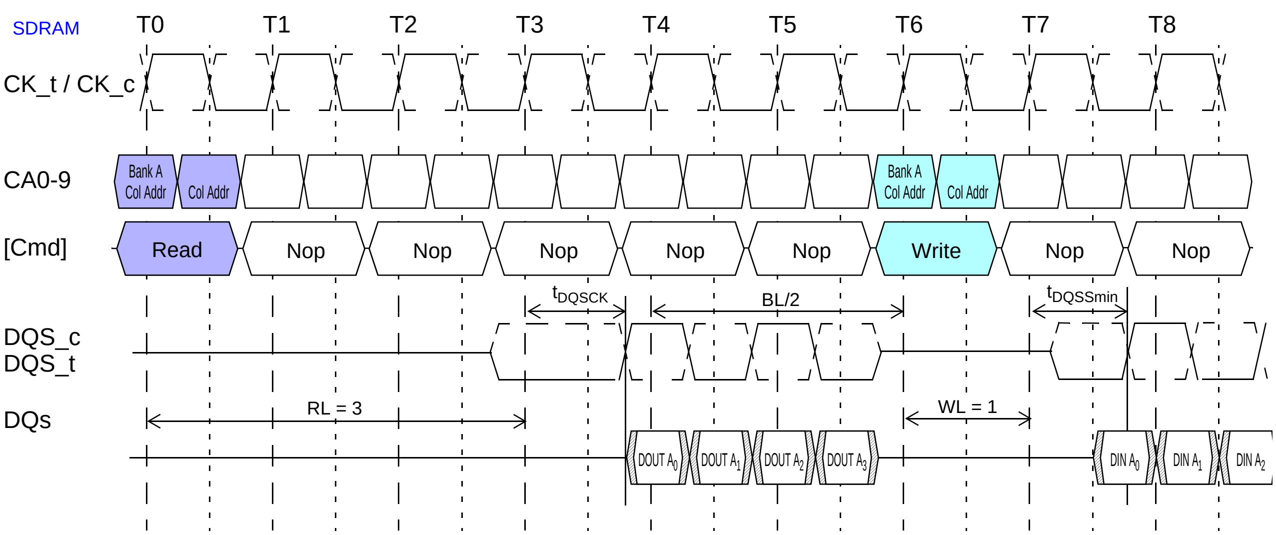


Figure 32 — LPDDR2-SX: Burst read followed by burst write: RL = 3, WL = 1, BL = 4

5.4 Burst Read Command (cont'd)

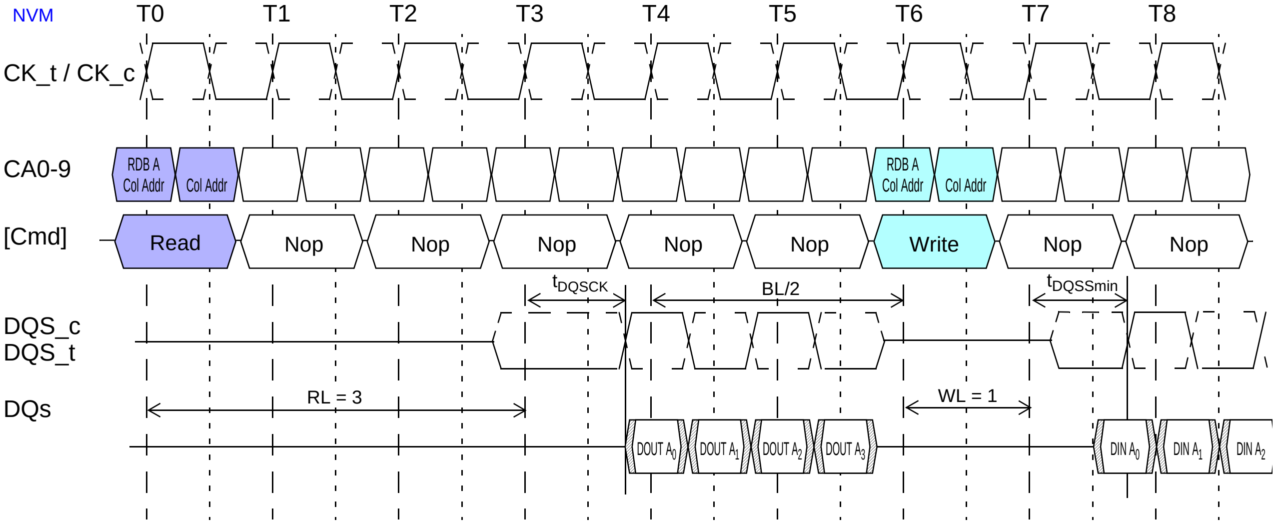


Figure 33 — LPDDR2-N: Burst read followed by burst write: RL = 3, WL = 1, BL = 4

The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum read to write latency is RL + RU(t_{DQSCK}max/t_{CK}) + BL/2 + 1 - WL clock cycles. Note that if a read burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated read burst should be used as "BL" to calculate the minimum read to write delay.

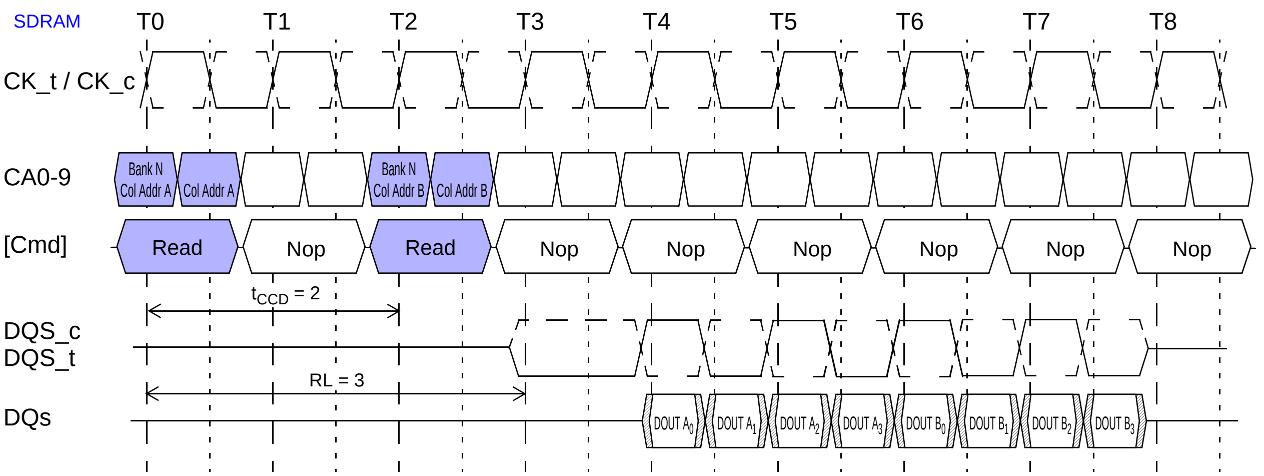


Figure 34 — LPDDR2-SX: Seamless burst read: RL = 3, BL = 4, t_{CCD} = 2

5.4 Burst Read Command (cont'd)

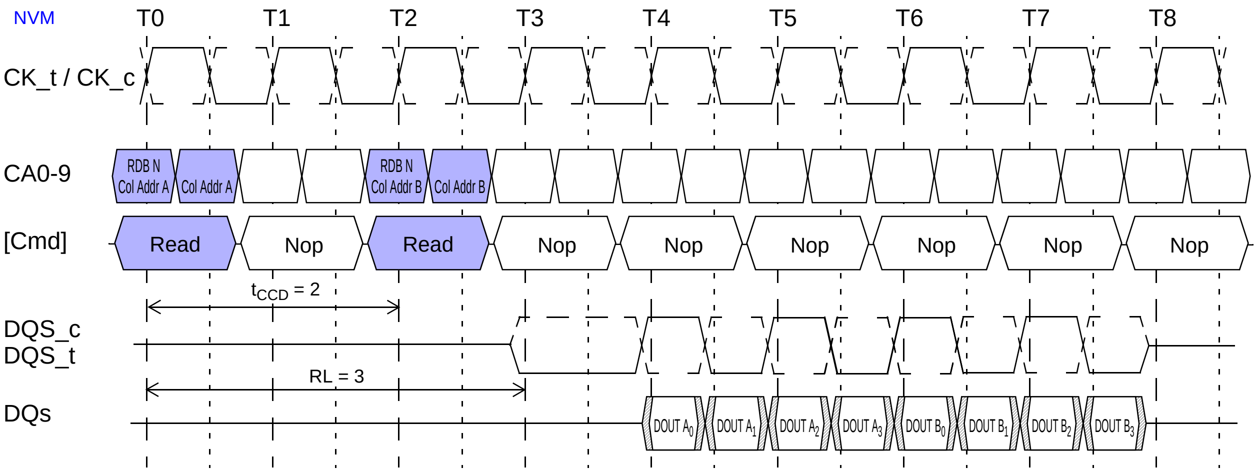


Figure 35 — LPDDR2-N: Seamless burst read: RL = 3, BL = 4, t_{CCD} = 2

The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, every 4 clocks for BL = 8 operation, and every 8 clocks for BL=16 operation.

For LPDDR2-SDRAM, this operation is allowed regardless of whether the accesses read the same or different banks as long as the banks are activated.

For LPDDR2-NVM, this operation is allowed regardless of whether the accesses read the same or different RDBs as long as the RDBs are activated.

5.4.1 Reads interrupted by a read

For LPDDR2-S4 and LPDDR2-N devices, burst read can be interrupted by another read on even clock cycles after the Read command, provided that t_{CCD} is met. For LPDDR2-S2 devices, burst reads may be interrupted by other reads on any subsequent clock, provided that t_{CCD} is met.

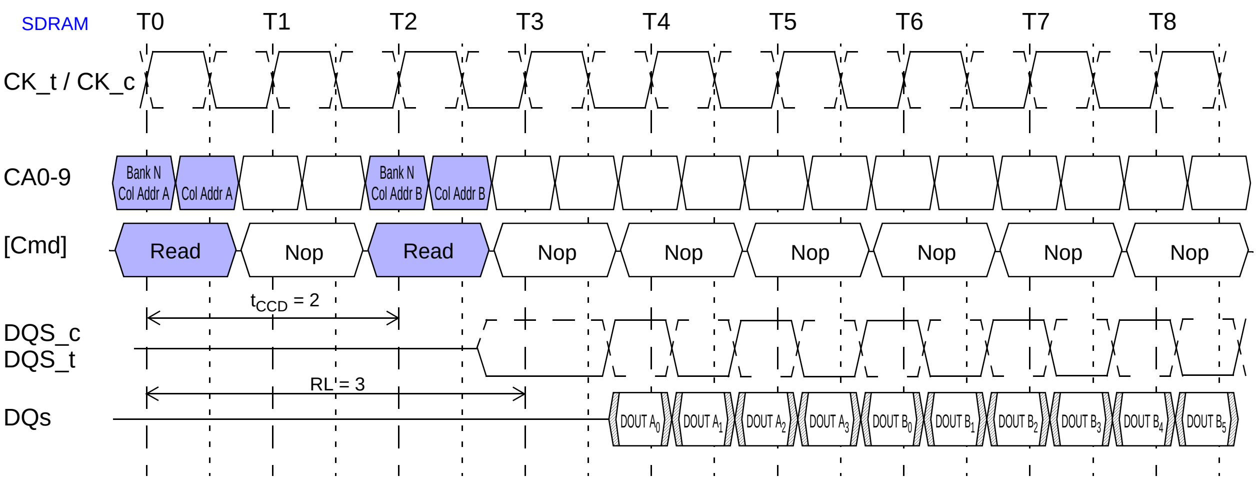


Figure 36 — LPDDR2-SX: Read burst interrupt example: RL = 3, BL = 8, t_{CCD} = 2

NOTE 1 For LPDDR2-S4 devices, read burst interrupt function is only allowed on burst of 8 and burst of 16.
NOTE 2 For LPDDR2-S4 devices, read burst interrupt may only occur on even clock cycles after the previous read commands, provided that t_{CCD} is met.
NOTE 3 For LPDDR2-S2 devices, read burst interrupt may occur on any clock cycle after the intial read command, provided that t_{CCD} is met.
NOTE 4 Reads can only be interrupted by other reads or the BST command.
NOTE 5 Read burst interruption is allowed to any bank inside DRAM.
NOTE 6 Read burst with Auto-Precharge is not allowed to be interrupted.
NOTE 7 The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

5.4.1 Reads interrupted by a read (cont'd)

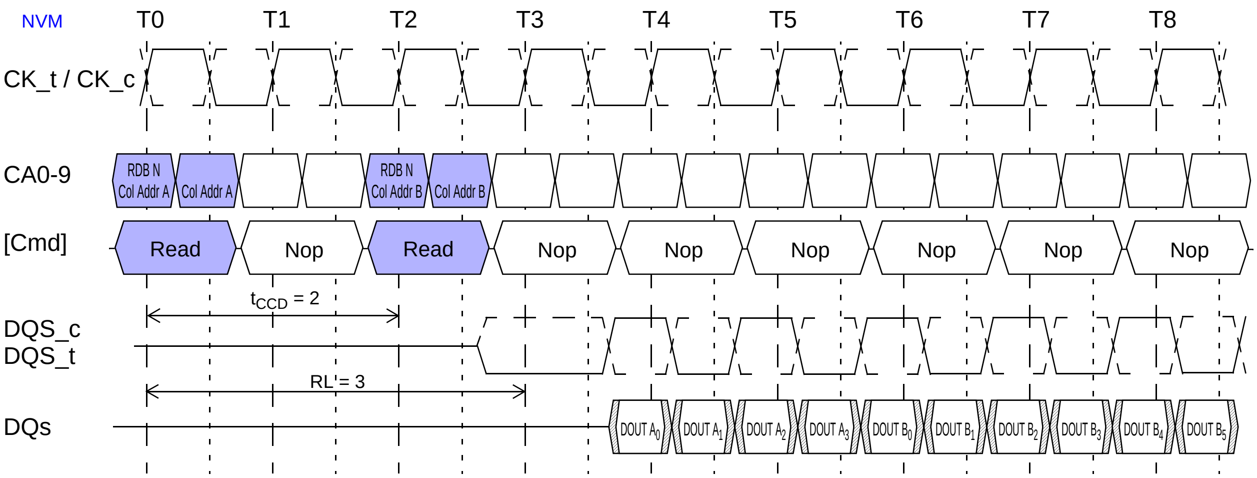


Figure 37 — LPDDR2-N: Read burst interrupt example: RL = 3, BL = 8, t_{CCD} = 2

NOTE 1 For LPDDR2-N devices, read burst interrupt function is only allowed on burst of 8 and burst of 16.
NOTE 2 For LPDDR2-N devices, read burst interrupt may only occur on even clock cycles after the previous read commands, provided that t_{CCD} is met.
NOTE 3 Reads can only be interrupted by other reads or the BST command.
NOTE 4 Read burst interruption is allowed to any RDB inside the NVM.
NOTE 5 The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

5.4.2 LPDDR2: Data Not Valid

LPDDR2 devices will implement Data Not Valid (DNV) signal if they set MR0 OP2 bit to "1", and will not implement Data Not Valid signal if they set MR0 OP2 bit to "0". LPDDR2-SX devices will not implement DNV. DNV signal, when implemented, is outputted from the memory device with DQ data. The DNV signal and the Data Mask signal (DM) share the same pin. For information on the DM signal usage, see "Write data mask" on page 70. DNV signals follow the same timings as the DQ signals for read bursts. DNV0, DNV1, DNV2, and DNV3 timings are referenced to DQS0, DQS1, DQS2, and DQS3 respectively.

LPDDR2 devices that support Data Not Valid shall drive all DNV signal(s) to the same level for each data beat during read bursts. The DNV signal(s) are valid only the first four beats of a read burst. The beat 0 of the DNV signal shall be driven LOW if the data in the burst is valid. Beat 0 of the DNV signal shall be driven HIGH if the data in the burst is invalid. Beat 1 of DNV indicates how the controller may retry the request, (DNV = LOW) for immediate retry or (DNV = HIGH) for retry after a pre-specified time in micro seconds in Mode Register 29 (MR29) on page 35. Beat 2 for immediate retries indicates whether the immediate retry should be with read command (DNV=LOW) or active command (DNV=HIGH), and for long retry (DNV=LOW). When DNV signal for beats 0, 1, and 2 are driven high, it indicates a currently reserved mode. Beat 3 is not used. Table 48 on page 80 displays DNV retry options.

For devices that implement Data Not Valid, DNV shall be driven to zero during the first data beat during MRR operations.

Table 48 — LPDDR2: Data Not Valid

DNV, beat 0	DNV, beat 1	DNV, beat 2	DNV, beat 3	Read Burst	Notes
0	X	X	X	Valid	3
1	0	0	X	Immediate Retry with Read	1
1	0	1	X	Immediate Retry with Activate	1
1	1	0	X	Retry Long with Read	2
1	1	1	X	Reserved	

NOTE 1 Immediate Retry indicates the controller may retry the request immediately with read or active command as specified.
NOTE 2 Retry Long indicates that the controller should wait for the pre-specified time before retrying the Read. An Active must be issued before the retry Read command. Optionally, a Preactive command may be issued before the Active command. A retry earlier than the pre-specified time may result in receiving another DNV signal.
NOTE 3 In case of Mode Register Read (MRR) command, DNV shall be driven to zero during the first data beat.

5.4.2 LPDDR2: Data Not Valid (cont'd)

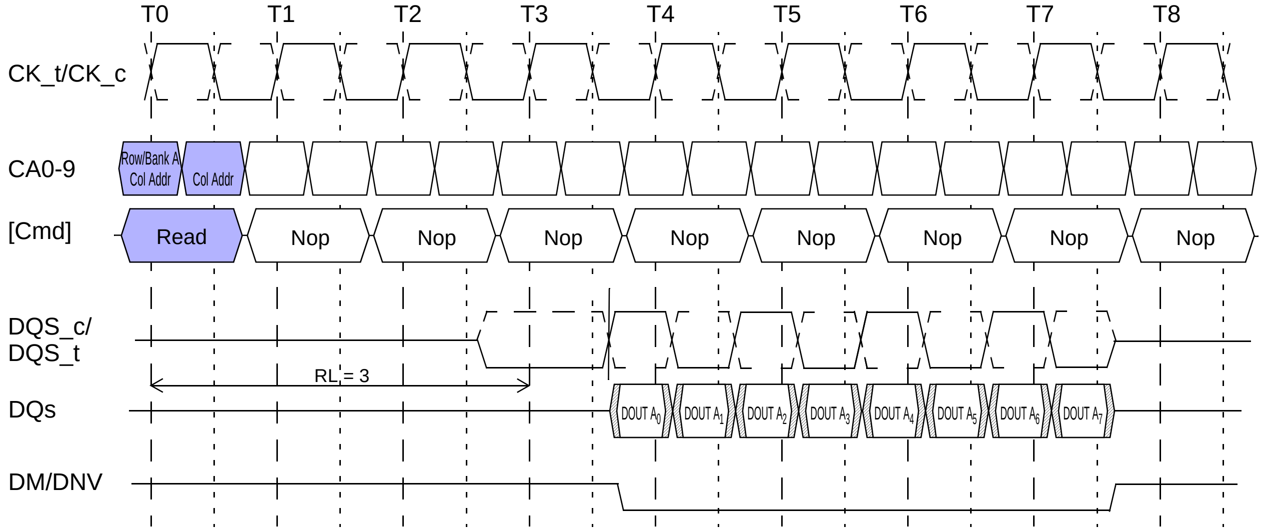


Figure 38 — LPDDR2: DNV with valid data: RL = 3, BL = 8

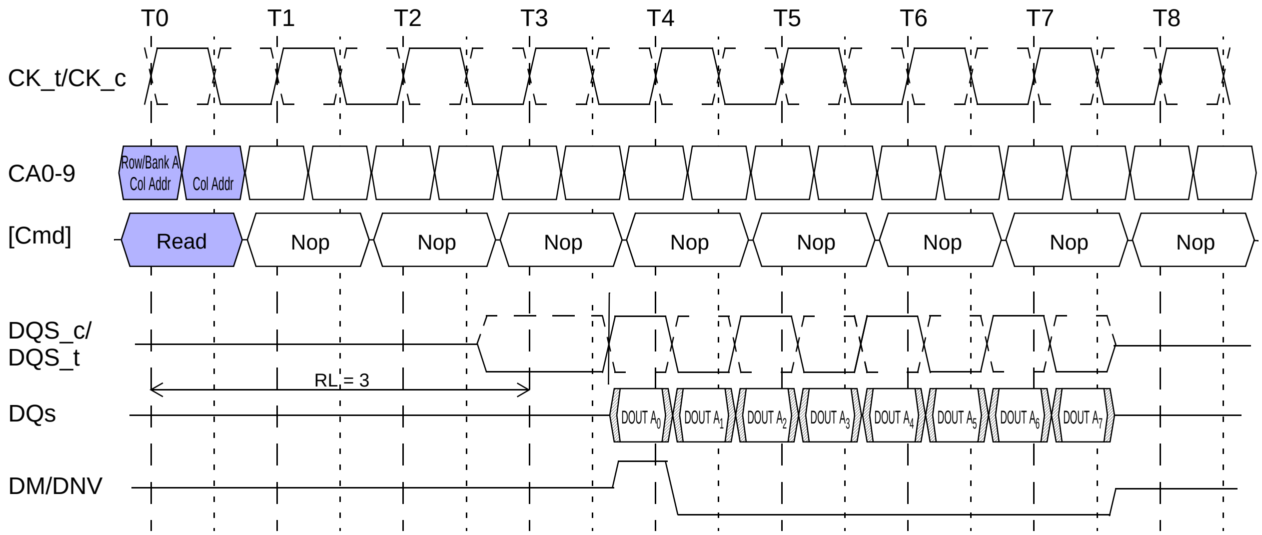


Figure 39 — LPDDR2: DNV with invalid data, retry with Read: RL = 3, BL = 8

5.5 Burst Write Operation

The Burst Write command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Write Latency (WL) is defined from the rising edge of the clock on which the Write Command is issued to the rising edge of the clock from which the t_{DQSS} delay is measured. The first valid datum shall be driven WL * t_{CK} + t_{DQSS} from the rising edge of the clock from which the Write command is issued. The data strobe signal (DQS) should be driven LOW t_{WPRE} prior to the data input. The data bits of the burst cycle must be applied to the DQ pins t_{DS} prior to the respective edge of the DQS and held valid until t_{DH} after that edge. The burst data are sampled on successive edges of the DQS until the burst length is completed, which is 4, 8, or 16 bit burst.

For LPDDR2-SDRAM devices, t_{WR} must be satisfied before a precharge command to the same bank may be issued after a burst write operation.

For LPDDR2-N devices, t_{WRA} must be satisfied before an Activate command to the same RDB may be issued after a burst write operation. A Preactive command may be sent at any time after a Write command.

Input timings are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

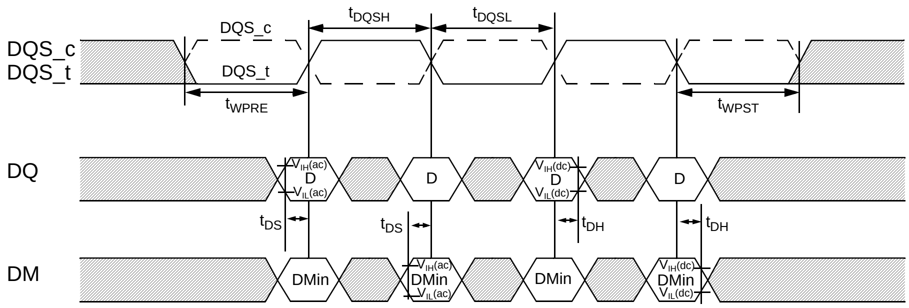


Figure 40 — Data input (write) timing

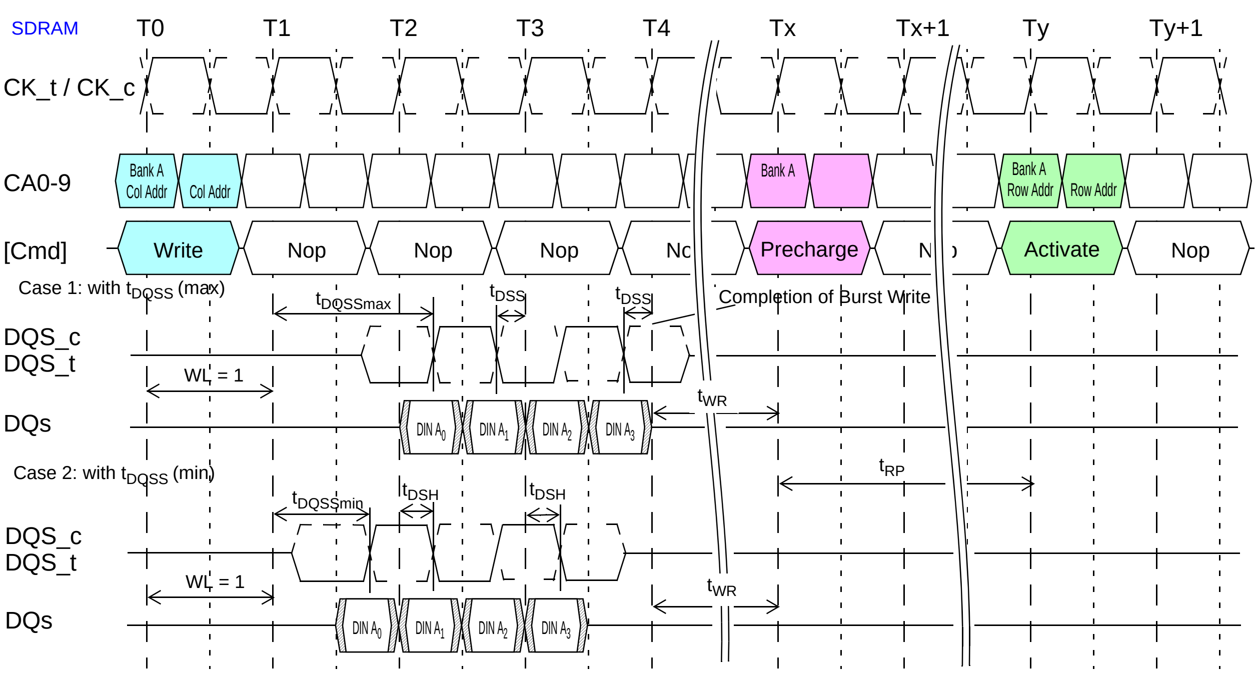


Figure 41 — LPDDR2-SX: Burst write : WL = 1, BL = 4

5.5 Burst Write Operation (cont'd)

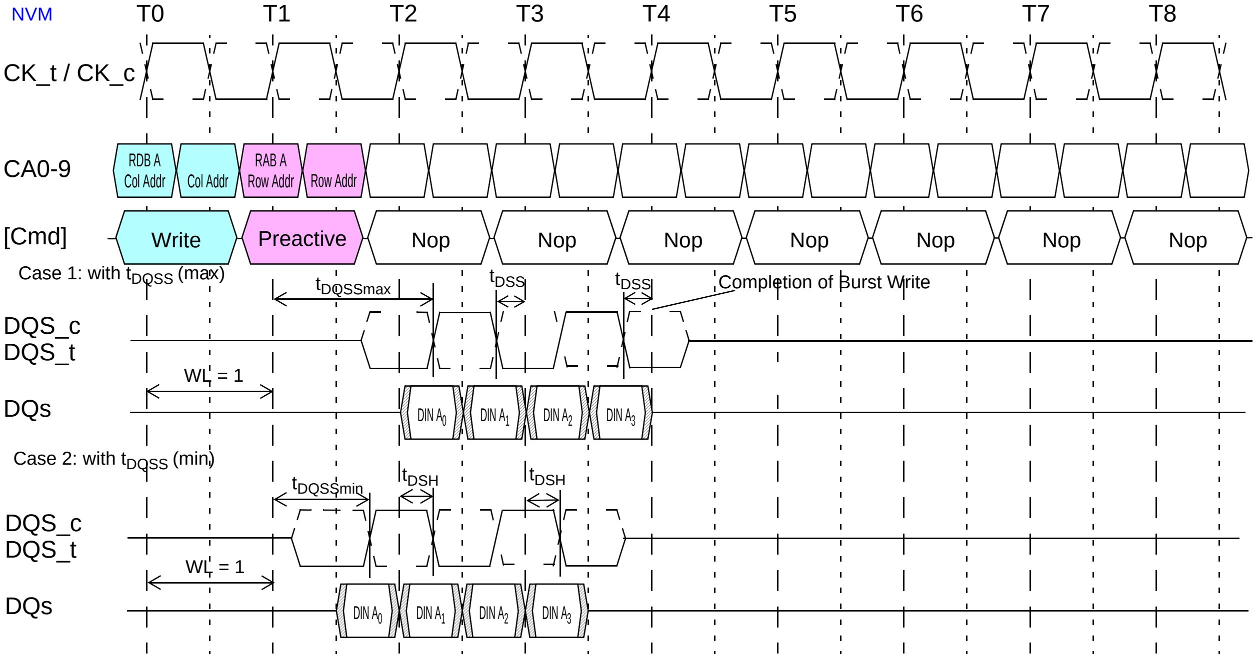


Figure 42 — LPDDR2-N: Burst write followed by Preactive: WL = 1, BL = 4

NOTE 1 A Preactive command may be issued on any clock cycle after a Write command and does not affect the ongoing burst.

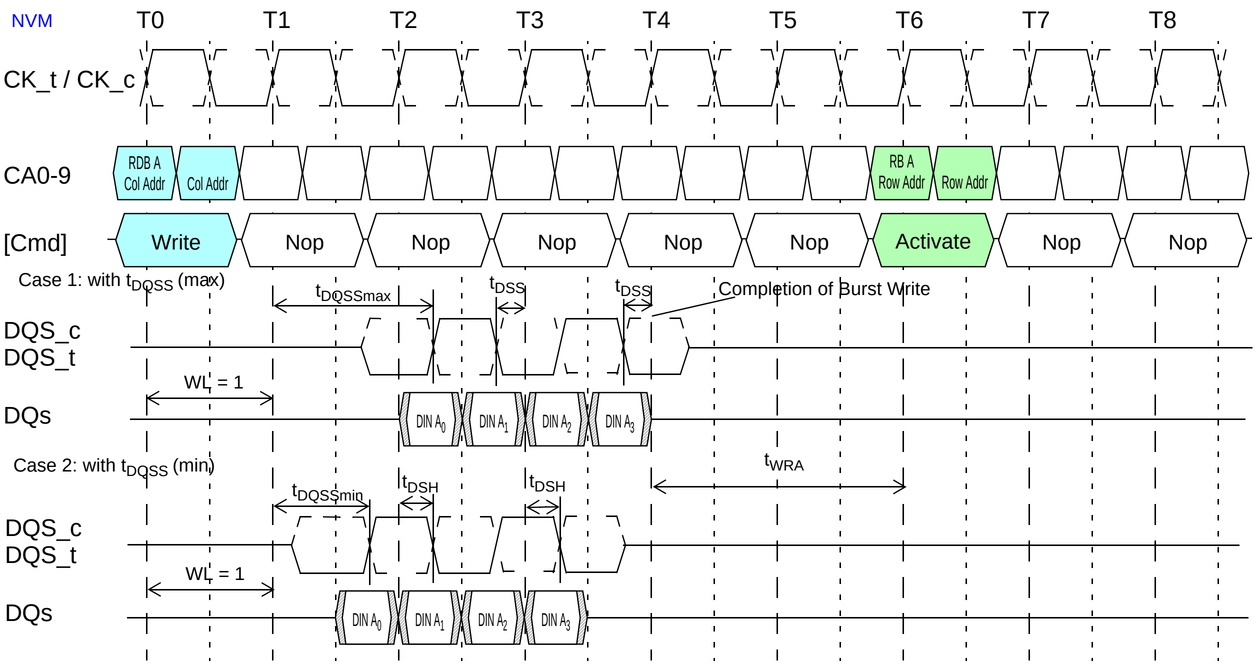


Figure 43 — LPDDR2-N: Burst write followed by Activate: WL = 1, BL = 4

5.5 Burst Write Operation (cont'd)

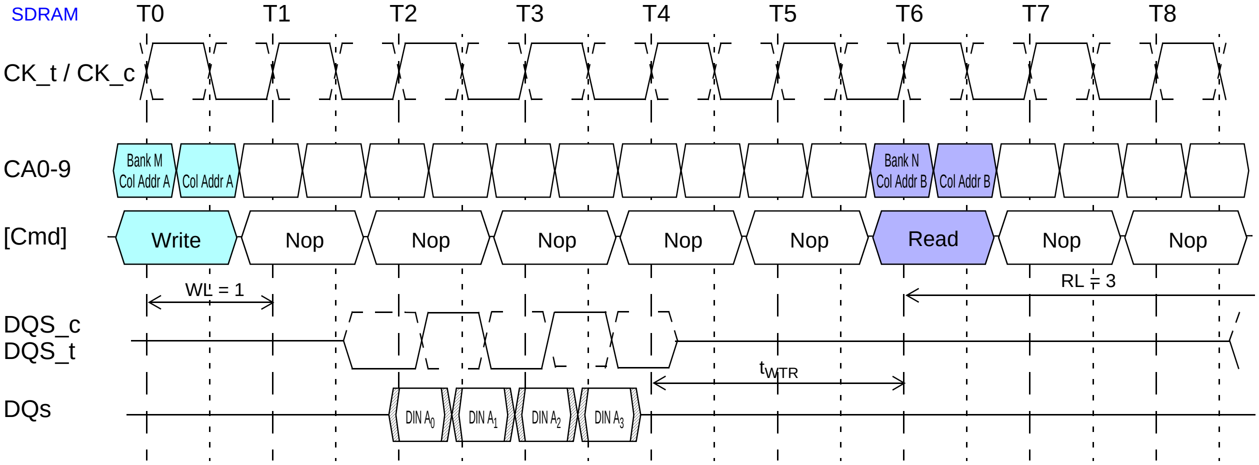


Figure 44 — LPDDR2-SX: Burst write followed by burst read: RL=3, WL = 1, BL = 4

NOTE 1 The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})].

NOTE 2 t_{WTR} starts at the rising edge of the clock after the last valid input datum.

NOTE 3 If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as "BL" to calculate the minimum write to read delay.

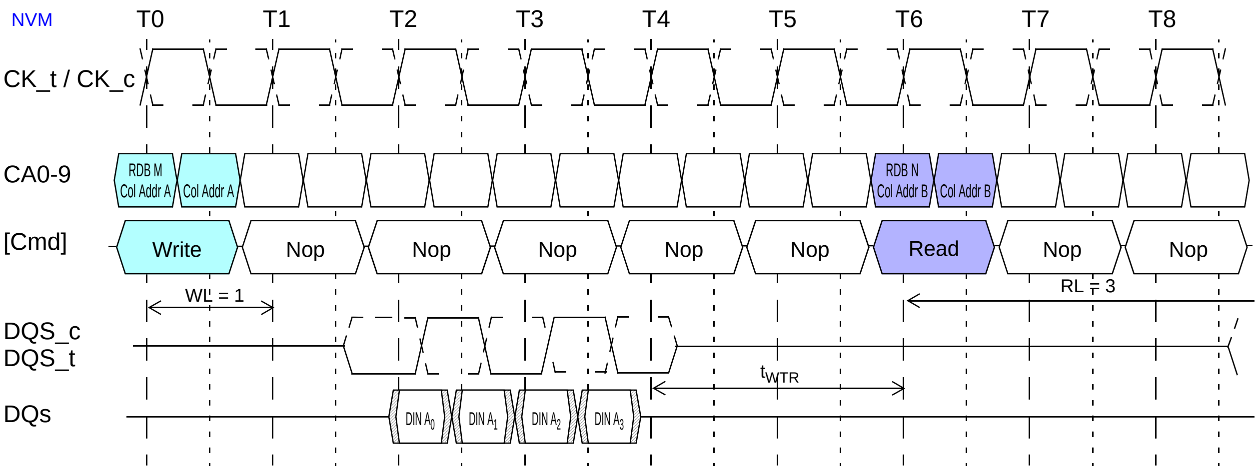


Figure 45 — LPDDR2-N: Burst write followed by burst read: RL=3, WL = 1, BL = 4

NOTE 1 The minimum number of clock cycles from the burst write command to the burst read command for any RDB is [WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})].

NOTE 2 t_{WTR} starts at the rising edge of the clock after the last valid input datum.

NOTE 3 If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as "BL" to calculate the minimum write to read delay.

5.5 Burst Write Operation (cont'd)

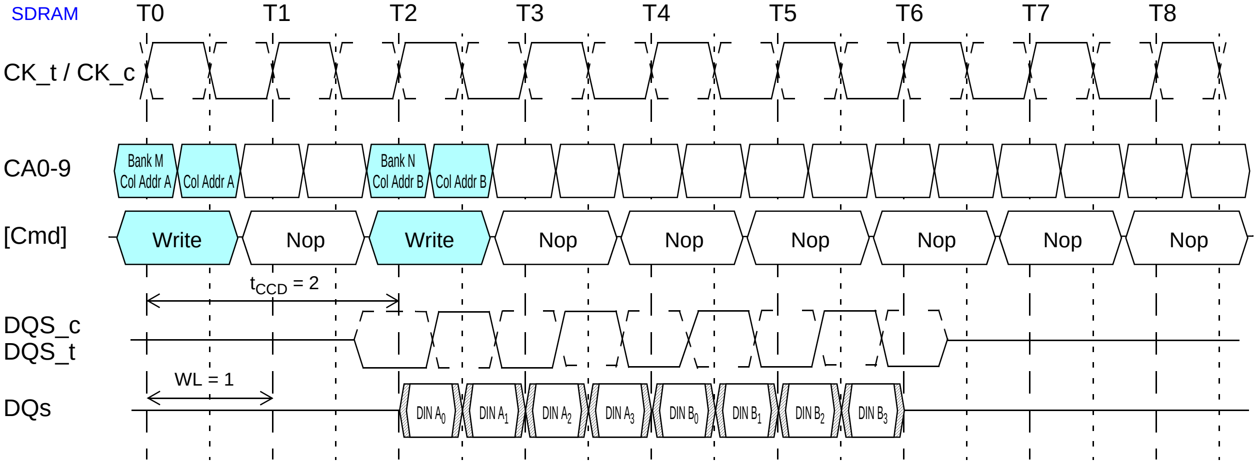


Figure 46 — LPDDR2-SX: Seamless burst write: WL = 1, BL = 4, t_{CCD} = 2

NOTE 1: The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL=16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

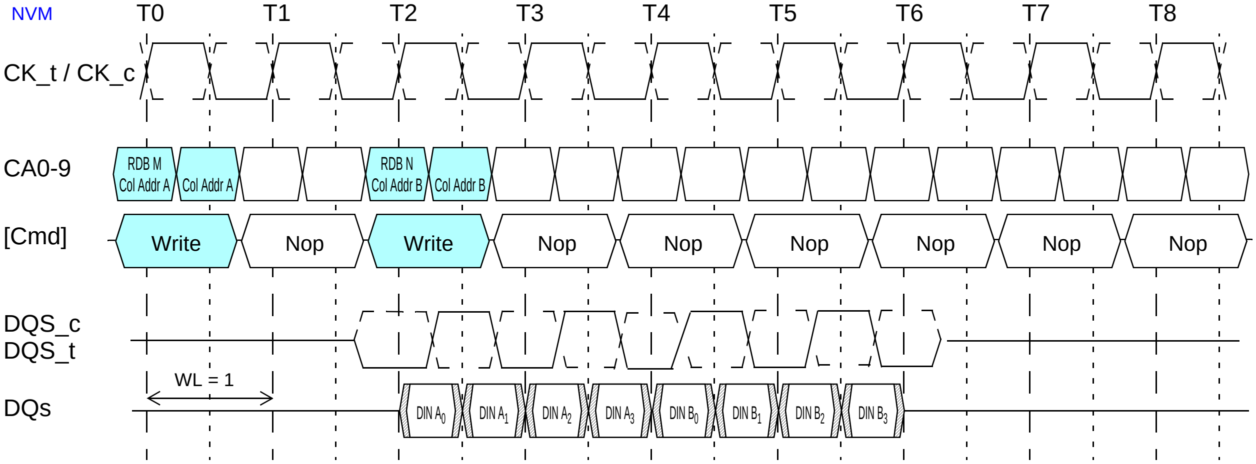


Figure 47 — LPDDR2-N: Seamless burst write: WL = 1, BL = 4

NOTE 1: The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL=16 operation. This operation is allowed regardless of same or different Row Buffers as long as the Row Buffers are activated.

5.5.1 Writes interrupted by a write

For LPDDR2-S4 and LPDDR2-N devices, burst write can only be interrupted by another write on even clock cycles after the Write command, provided that t_{CCD}(min) is met.

For LPDDR2-S2 devices, burst writes may be interrupted on any subsequent clock, provided that t_{CCD}(min) is met.

5.5.1 Writes interrupted by a write (cont'd)

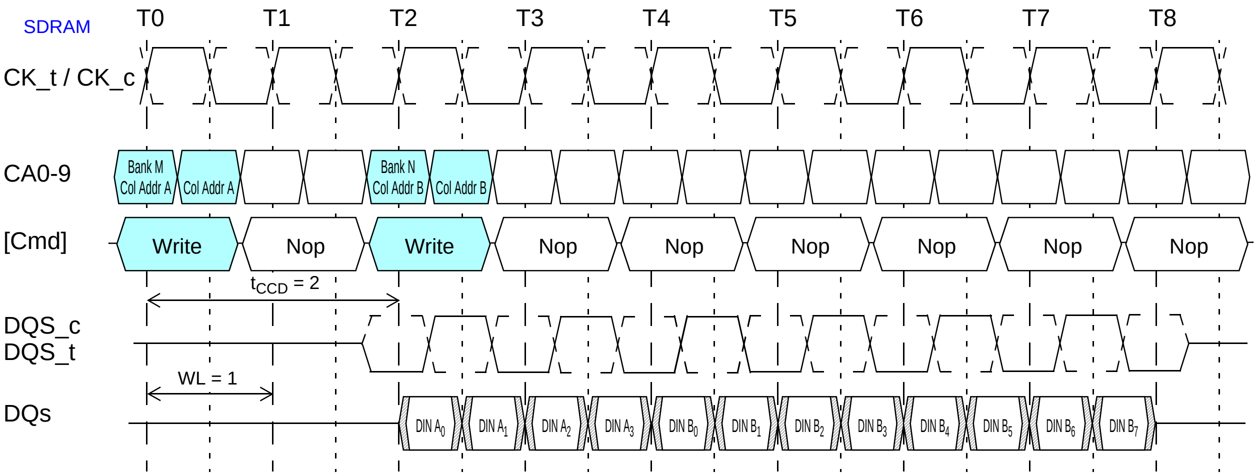


Figure 48 — LPDDR2-SX: Write burst interrupt timing: WL = 1, BL = 8, t_{CCD} = 2

NOTE 1 For LPDDR2-S4 devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.
NOTE 2 For LPDDR2-S4 devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that t_{CCD}(min) is met.
NOTE 3 For LPDDR2-S2 devices, write burst interrupt may occur on any clock after the initial write command, provided that t_{CCD}(min) is met.
NOTE 4 Writes can only be interrupted by other writes or the BST command.
NOTE 5 Write burst interruption is allowed to any bank inside DRAM.
NOTE 6 Write burst with Auto-Precharge is not allowed to be interrupted.
NOTE 7 The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.

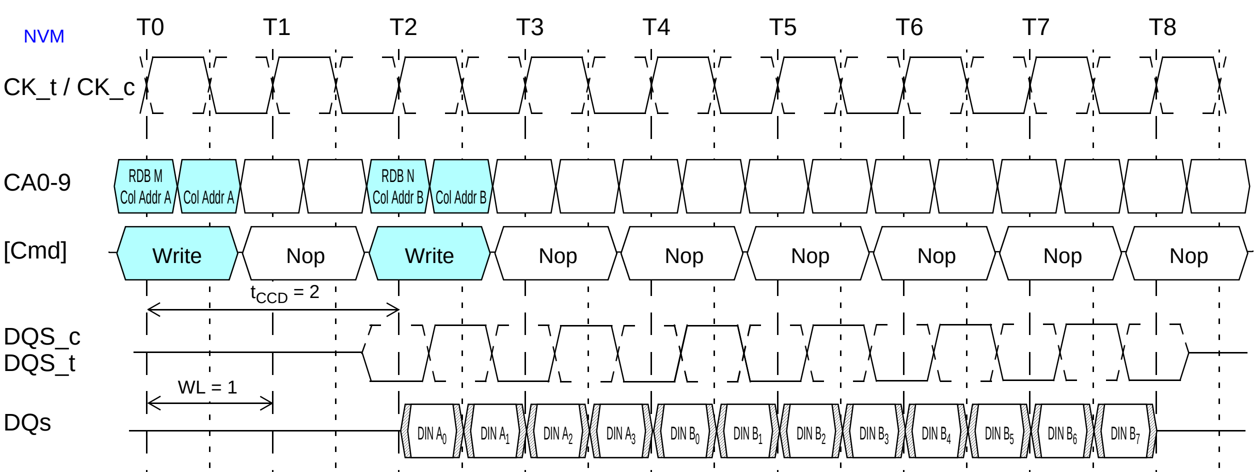


Figure 49 — LPDDR2-N: Write burst interrupt timing: WL = 1, BL = 8, t_{CCD} = 2

NOTE 1 For LPDDR2-N devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.
NOTE 2 For LPDDR2-N devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that t_{CCD}(min) is met.
NOTE 3 Writes can only be interrupted by other writes or the BST command.
NOTE 4 Write burst interruption is allowed to any RDB inside the NVM.
NOTE 5 The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.

5.6 Burst Terminate

The Burst Terminate (BST) command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of clock. A Burst Teminate command may only be issued to terminate an active Read or Write burst. Therefore, a Burst Terminate command may only be issued up to and including BL/2 - 1 clock cycles after a Read or Write command. The effective burst length of a Read or Write command truncated by a BST command is as follows:
Effective burst length = 2 x {Number of clock cycles from the Read or Write Command to the BST command}

Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as "BL" to calculate the minimum read to write or write to read delay.

The BST command only affects the most recent read or write command. The BST command truncates an ongoing read burst RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Burst Terminate command is issued. The BST command truncates an ongoing write burst WL * t_{CK} + t_{DQSS} after the rising edge of the clock where the Burst Terminate command is issued.

For LPDDR2-S2 devices, the 2-bit prefetch architecture allows the BST command to be issued in any cycle after a Write or Read command.

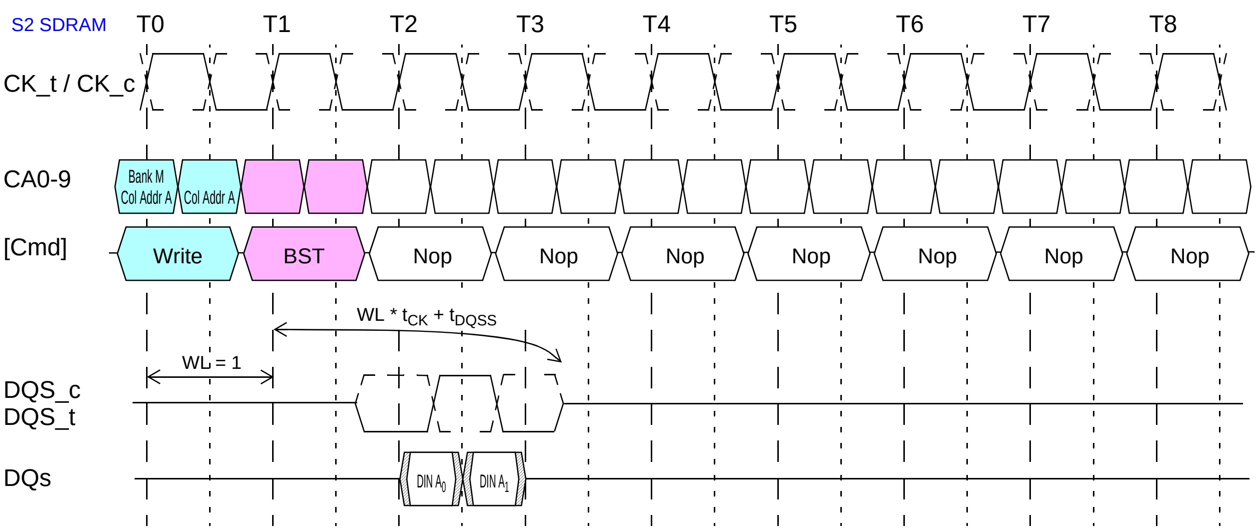


Figure 50 — LPDDR2-S2: Write burst truncated by BST: WL = 1, BL = 16

NOTE 1 The BST command truncates an ongoing write burst WL * t_{CK} + t_{DQSS} after the rising edge of the clock where the Burst Terminate command is issued.

NOTE 2 Additional BST commands are not allowed after T1 and may not be issued until after the next Read or Write command.

5.6 Burst Terminate (cont'd)

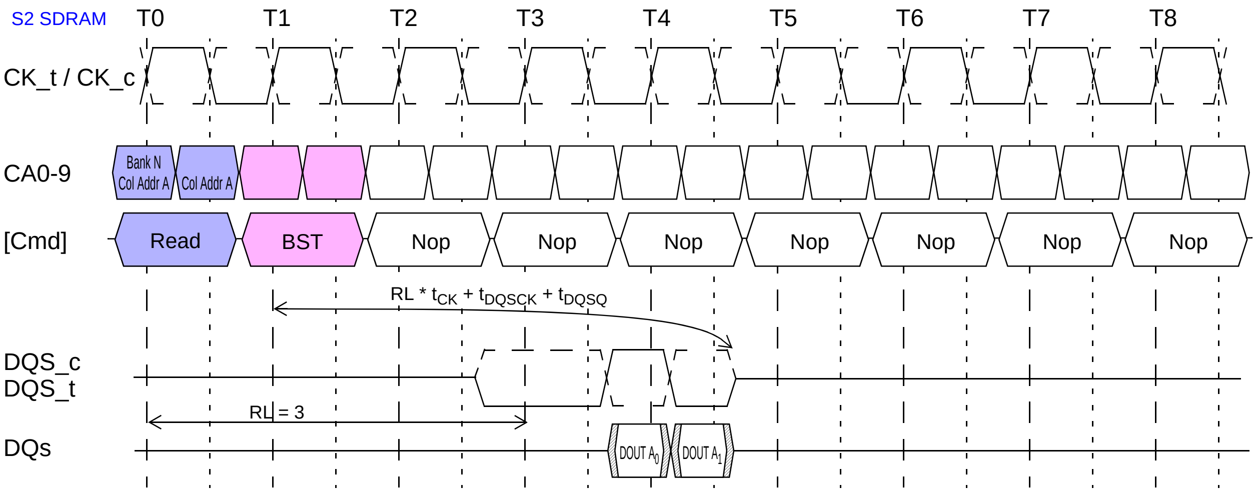


Figure 51 — LPDDR2-S2: Read burst truncated by BST: RL = 3, BL = 4

NOTE 1 The BST command truncates an ongoing read burst RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Burst Terminate command is issued.

NOTE 2 Additional BST commands are not allowed after T1 and may not be issued until after the next Read or Write command.

For LPDDR2-S4 and LPDDR2-N devices, the 4-bit prefetch architecture allows the BST command to be issued on an even number of clock cycles after a Write or Read command. Therefore, the effective burst length of a Read or Write command truncated by a BST command is an integer multiple of 4.

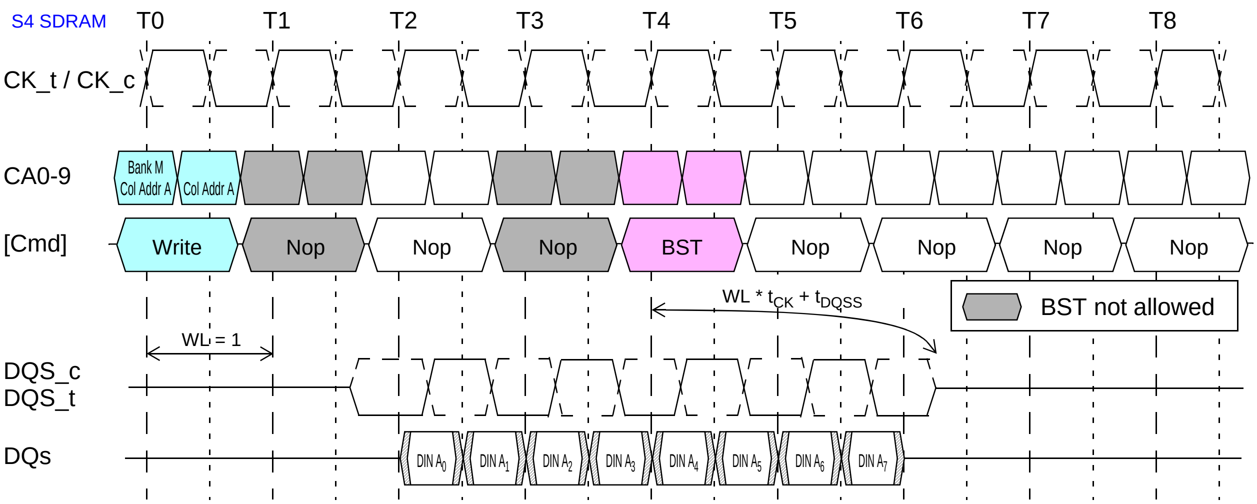


Figure 52 — LPDDR2-S4: Burst Write truncated by BST: WL = 1, BL = 16

NOTE 1 The BST command truncates an ongoing write burst WL * t_{CK} + t_{DQSS} after the rising edge of the clock where the Burst Terminate command is issued.

NOTE 2 For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Write command.

NOTE 3 Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

5.6 Burst Terminate (cont'd)

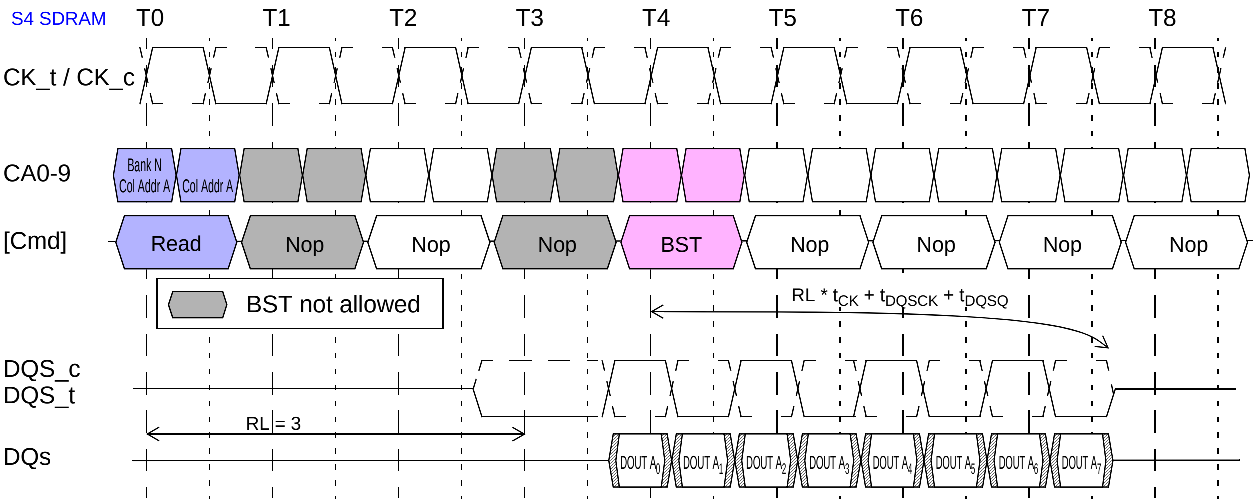


Figure 53 — LPDDR2-S4: Burst Read truncated by BST: RL=3, BL = 16

NOTE 1 The BST command truncates an ongoing read burst RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Burst Terminate command is issued.

NOTE 2 For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Read command.

NOTE 3 Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

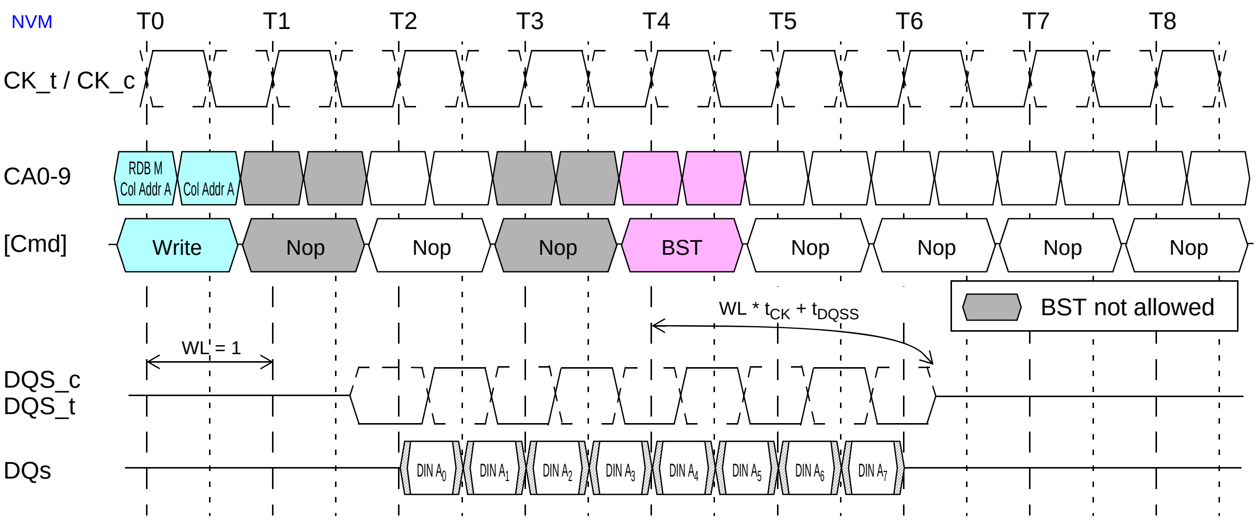


Figure 54 — LPDDR2-N: Burst Write truncated by BST: WL = 1, BL = 16

NOTE 1 The BST command truncates an ongoing write burst WL * t_{CK} + t_{DQSS} after the rising edge of the clock where the Burst Terminate command is issued.

NOTE 2 For LPDDR2-N devices, BST can only be issued an even number of clock cycles after the Write command.

NOTE 3 Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

5.6 Burst Terminate (cont'd)

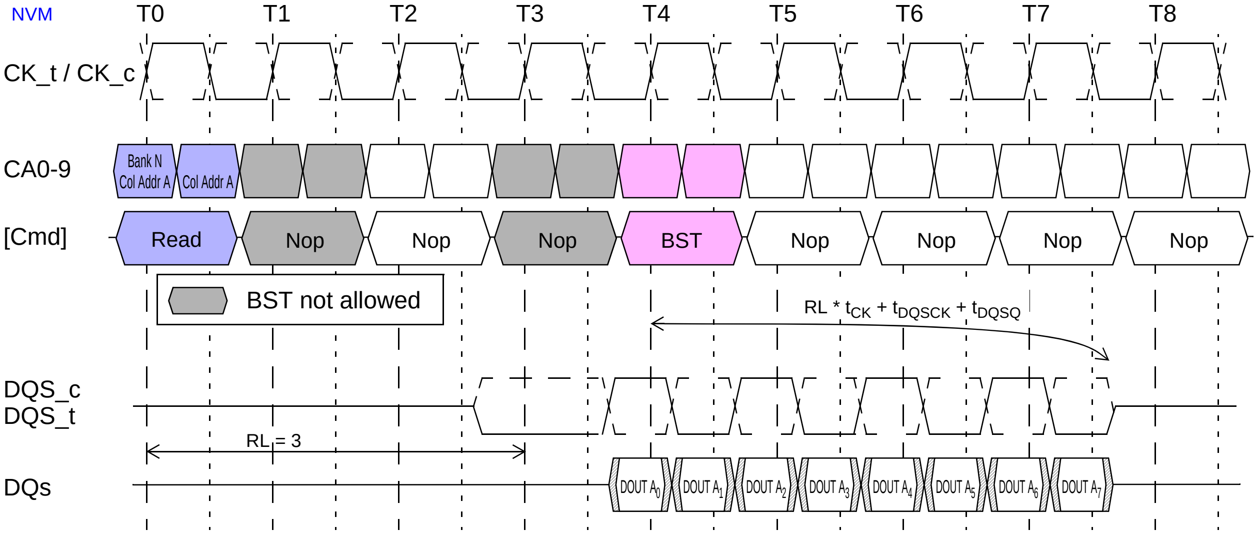


Figure 55 — LPDDR2-N: Burst Read truncated by BST: RL=3, BL = 16

NOTE 1 The BST command truncates an ongoing read burst RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Burst Terminate command is issued.

NOTE 2 For LPDDR2-N devices, BST can only be issued an even number of clock cycles after the Read command.

NOTE 3 Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

5.7 Write Data Mask

One write data mask (DM) pin for each data byte (DQ) will be supported on LPDDR2 devices, consistent with the implementation on LPDDR SDRAMs. Each data mask (DM) may mask its respective data byte (DQ) for any given cycle of the burst. Data mask has identical timings on write operations as the data bits, though used as input only, is internally loaded identically to data bits to insure matched system timing.

See Table 51 on page 102 for Write to Precharge timings for LPDDR2-S4 and Table 52 on page 103 for Write to Precharge timings for LPDDR2-S2.

SDRAM

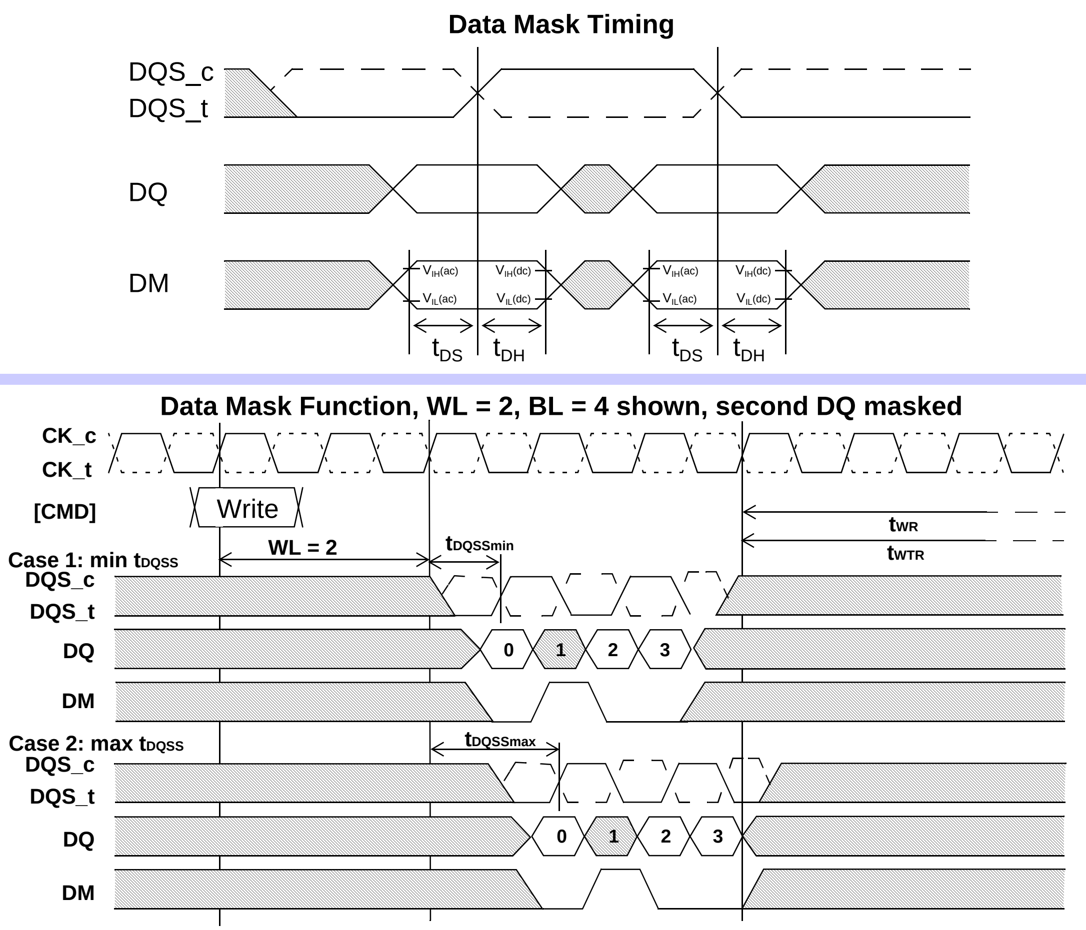
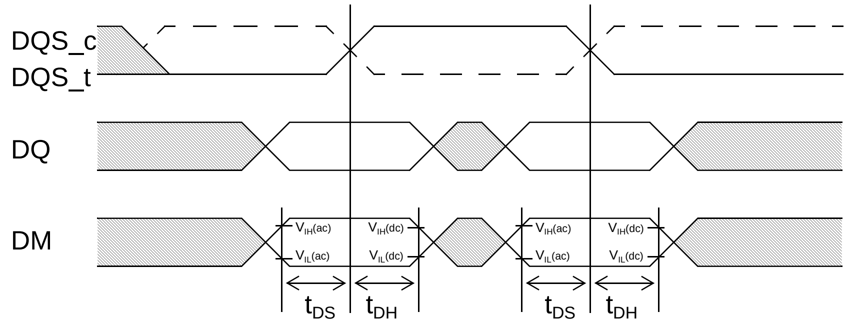


Figure 56 — LPDDR2-SX: Write data mask

5.7 Write Data Mask (cont'd)

NVM

Data Mask Timing



Data Mask Function, WL = 2, BL = 4 shown, second DQ masked

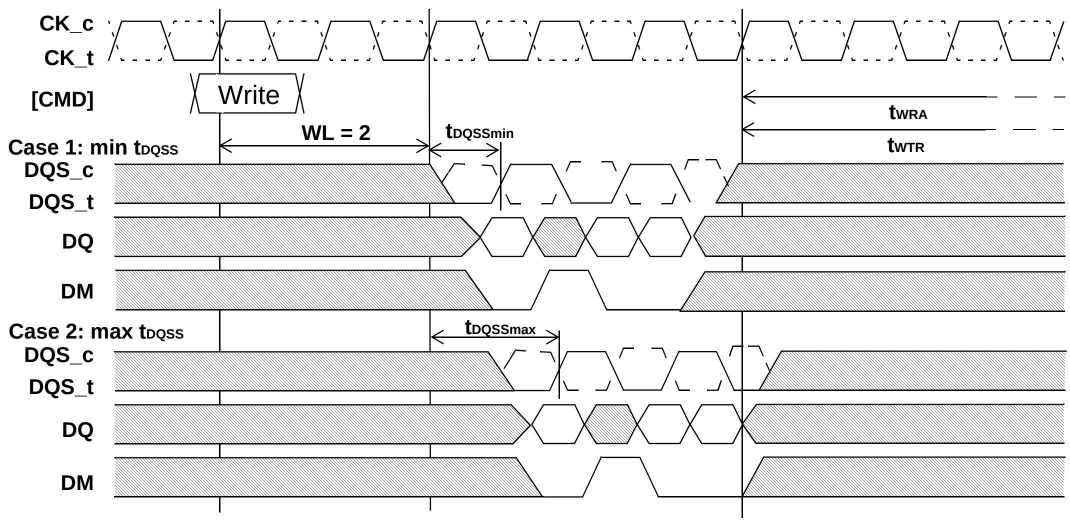


Figure 57 — LPDDR2-N: Write data mask

5.8 LPDDR2-N: Preactive operation

The Preactive command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of clock. After issuing a Preactive command, the target Row Buffer will return to the Idle state once the minimum Preactive latency (t_{RP}) is satisfied and any ongoing Read or Write operation is complete. The Preactive command addresses one Row Address Buffer (RAB). Each RAB is coupled with one specific Row Data Buffer (RDB) selected by BA0 - BA2. An {RAB, RDB} pair is referred to as a Row Buffer (RB).

The Preactive command is used to load the upper part of a row address into one RAB selected by BA0 - BA2. The address subset stored in an RAB will later be combined with the lower portion of the row address sent with the Activate command to load one row of the memory array or Overlay Window content into an RDB. Note that the row size of the NVM device may differ from the row size for an SDRAM.

Devices may have four or eight RABs. Each RAB is not restricted to any portion of the device address space, therefore the controller may use any RAB for any partial row address, including storing the same partial row address value in multiple RABs concurrently. Each RAB is persistent until a MRW Reset command is issued or power loss occurs, or until a new Preactive command is issued to that RAB. Therefore, Preactive is optional when the desired RAB already holds the desired partial row-address value.

The Preactive command does not invoke internal sensing. Therefore, after issuing a Preactive command to any RAB and then satisfying t_{RP}, the memory controller shall issue an Activate command to the corresponding RB before issuing a Read or Write command to the respective RDB.

All RABs shall be reset to 0x0000 by the memory during the initialization procedure.

Table 49 — Row Address Buffer selection for Preactive by BA inputs

BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Selected RAB (4-RB devices)	Selected RAB (8-RB devices)
0	0	0	RAB 0	RAB 0
0	0	1	RAB 1	RAB 1
0	1	0	RAB 2	RAB 2
0	1	1	RAB 3	RAB 3
1	0	0	RAB 0	RAB 4
1	0	1	RAB 1	RAB 5
1	1	0	RAB 2	RAB 6
1	1	1	RAB 3	RAB 7

5.8.1 LPDDR2-N: Burst Read operation followed by Activate or Preactive

For LPDDR2-N devices, a Read burst may be followed by a Preactive or Activate command to the same Row Buffer pair. An Activate command to the same Row Buffer pair may not be issued earlier than BL/2 cycles after the Read command. BL is the complete burst length selected in the Mode Registers. A Preactive command may be issued at any time following a Read command. Following the Preactive or Activate command, a subsequent command to the same Row Buffer cannot be issued until t_{RP} (for Preactive) or t_{RCD} (for Activate) is met. Read bursts are not impacted by Preactive or Activate commands to different Row Buffer pairs.

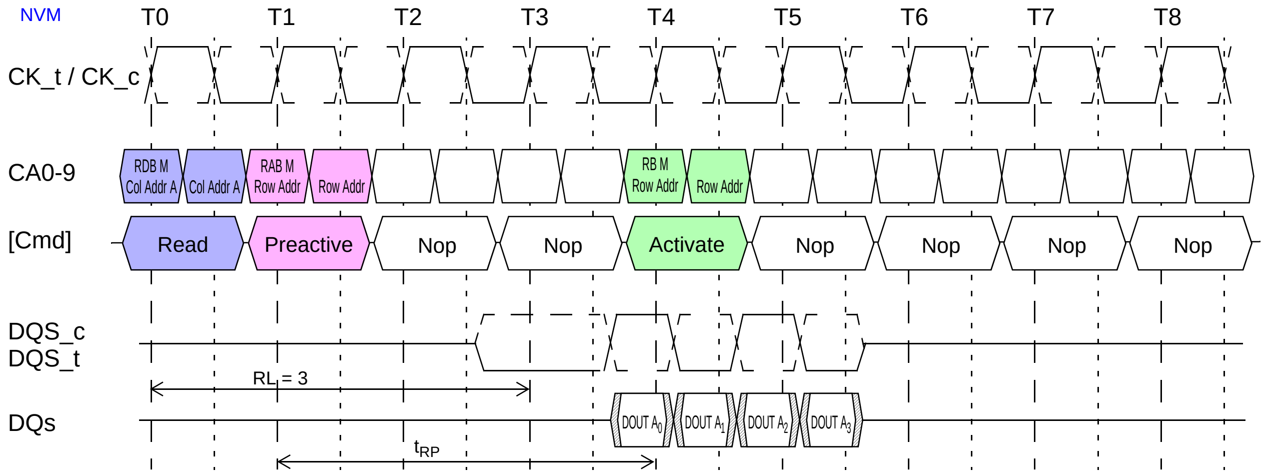


Figure 58 — LPDDR2-N: Burst read operation followed by Preactive: RL = 3, BL = 4

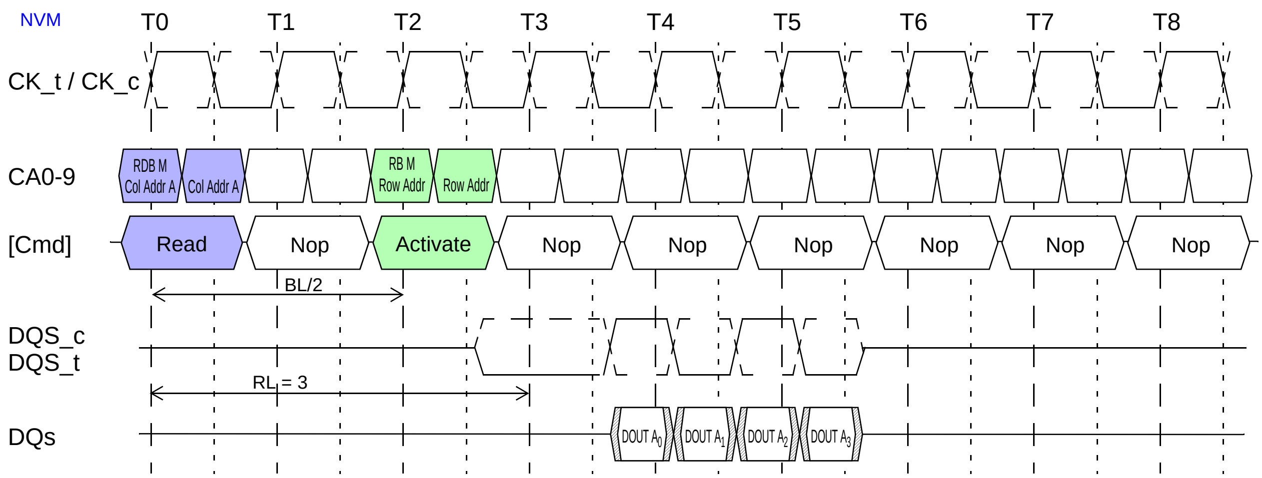


Figure 59 — LPDDR2-N: Burst read operation followed by Activate: RL = 3, BL = 4

5.8.2 LPDDR2-N: Burst Write operation followed by Activate or Preactive

A Preactive command may be issued at any time after a Write command. An Activate command to the same RDB may be issued t_{WRA} after the completion of the last burst write cycle. No Activate command to the same RDB should be issued prior to the t_{WRA} delay.

Minimum Write to Activate command spacing to the same Row Buffer equals WL + BL/2 + 1 + RU(t_{WRA}/t_{CK}) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For an truncated burst, BL is the effective burst length.

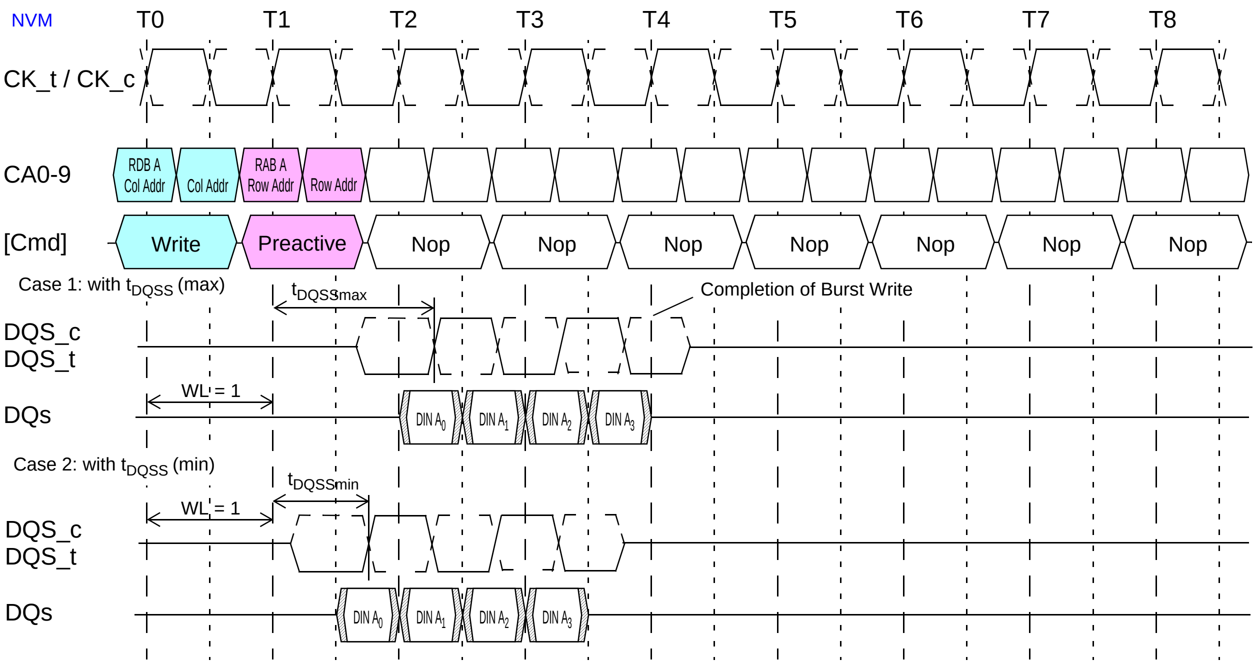


Figure 60 — LPDDR2-N: Burst write followed by Preactive: WL = 1, BL = 4

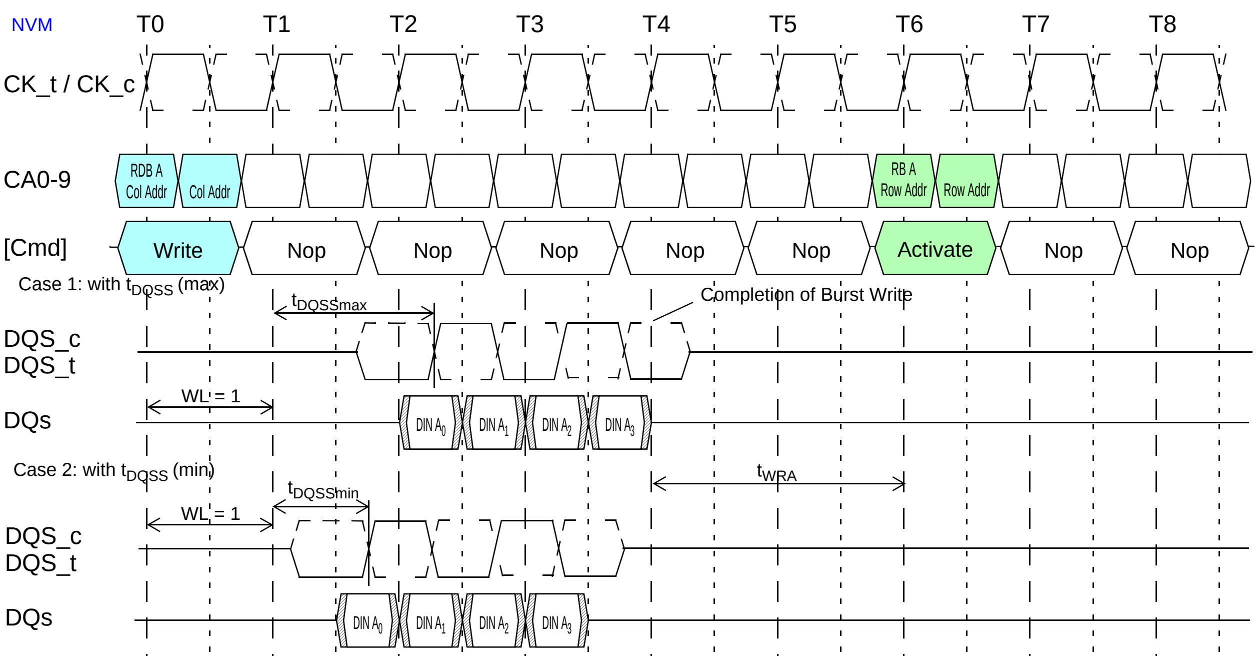


Figure 61 — LPDDR2-N: Burst write followed by Activate: WL = 1, BL = 4

5.8.3 LPDDR2-N: Auto Precharge (AP) bit

The AP bit (CA0f) is ignored during READ and WRITE commands.

5.9 LPDDR2-SX: Precharge operation

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices, the AB flag, and the bank address bits, BA0 and BA1, are used to determine which bank(s) to precharge. For 8-bank devices, the AB flag, and the bank address bits, BA0, BA1, and BA2, are used to determine which bank(s) to precharge. The bank(s) will be available for a subsequent row access t_{RPab} after an All-Bank Precharge command is issued and t_{RPpb} after a Single-Bank Precharge command is issued.

In order to ensure that 8-bank devices do not exceed the instantaneous current supplying capability of 4-bank devices, the Row Precharge time (t_{RP}) for an All-Bank Precharge for 8-bank devices (t_{RPab}) will be longer than the Row Precharge time for a Single-Bank Precharge (t_{RPpb}). For 4-bank devices, the Row Precharge time (t_{RP}) for an All-Bank Precharge (t_{RPab}) is equal to the Row Precharge time for a Single-Bank Precharge (t_{RPpb}).

Figure 19 on page 70 shows Activate to Precharge timing.

Table 50 — Bank selection for Precharge by address bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 4-bank device	Precharged Bank(s) 8-bank device
0	0	0	0	Bank 0 only	Bank 0 only
0	0	0	1	Bank 1 only	Bank 1 only
0	0	1	0	Bank 2 only	Bank 2 only
0	0	1	1	Bank 3 only	Bank 3 only
0	1	0	0	Bank 0 only	Bank 4 only
0	1	0	1	Bank 1 only	Bank 5 only
0	1	1	0	Bank 2 only	Bank 6 only
0	1	1	1	Bank 3 only	Bank 7 only
1	DON'T CARE	DON'T CARE	DON'T CARE	All Banks	All Banks

5.9.1 LPDDR2-SX: Burst Read operation followed by Precharge

For the earliest possible precharge, the precharge command may be issued BL/2 clock cycles after a Read command. A new bank active (command) may be issued to the same bank after the Row Precharge time (t_{RP}). A precharge command cannot be issued until after t_{RAS} is satisfied.

For LPDDR2-S4 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read command. For LPDDR2-S2 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 2-bit prefetch of a Read command.This time is called t_{RTP} (Read to Precharge).

For LPDDR2-S2 devices, t_{RTP} begins BL/2 - 1 clock cycles after the Read command. For LPDDR2-S4 devices, t_{RTP} begins BL/2 - 2 clock cycles after the Read command. If the burst is truncated by a BST command, the effective “BL” shall be used to calculate when t_{RTP} begins.

See Table 51 on page 102 for Read to Precharge timings for LPDDR2-S4 and Table 52 on page 103 for Read to Precharge timings for LPDDR2-S2.

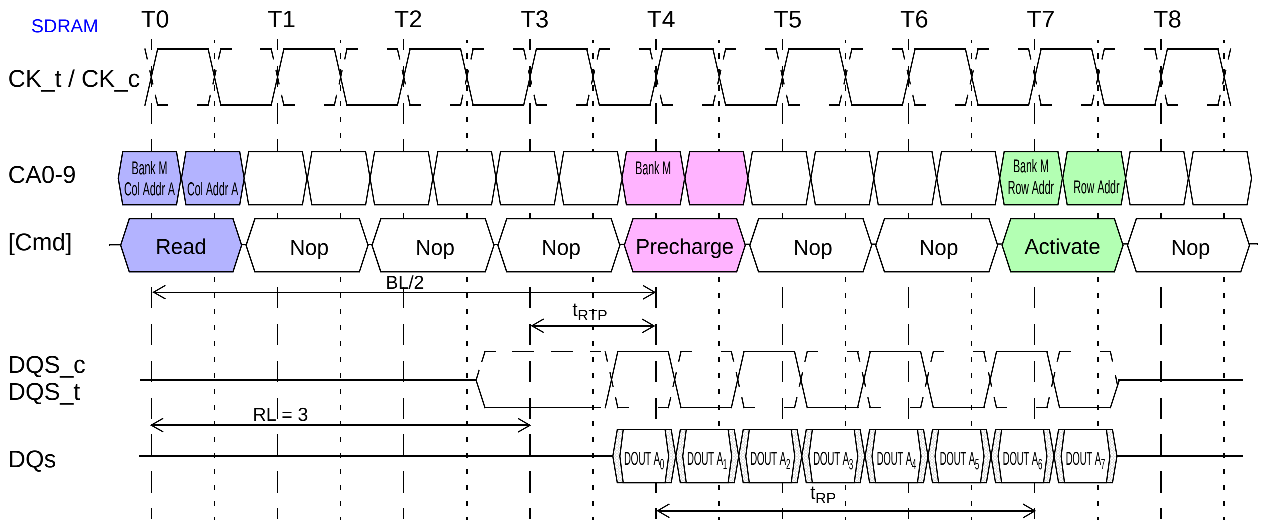


Figure 62 — LPDDR2-S2: Burst read followed by Precharge: RL = 3, BL = 8, t_{RTP}(min) <= t_{CK}

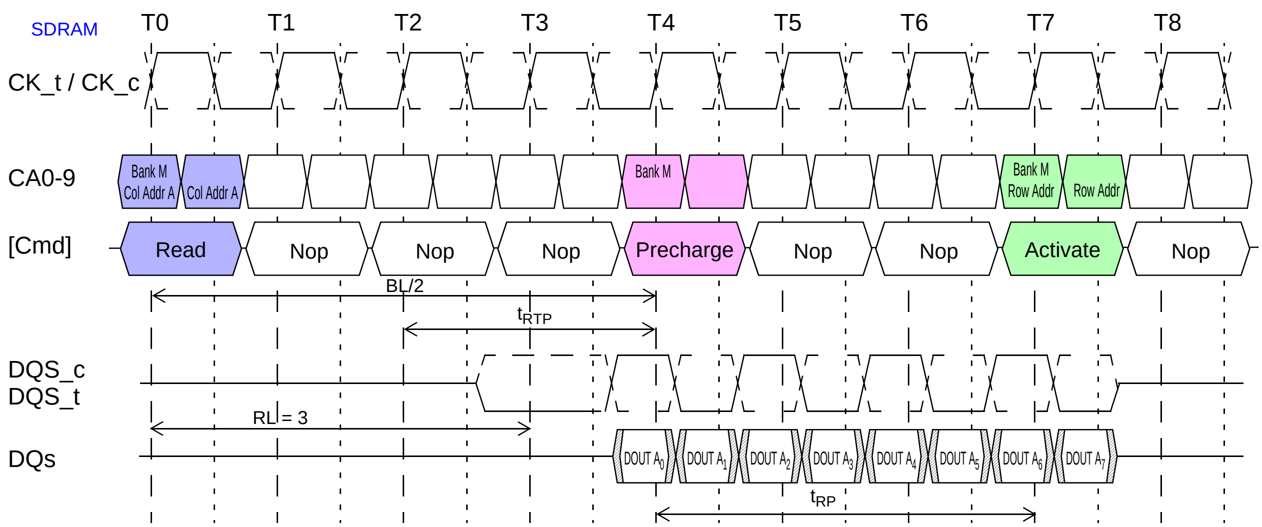


Figure 63 — LPDDR2-S4: Burst read followed by Precharge: RL = 3, BL = 8, RU(t_{RTP}(min)/t_{CK}) = 2

5.9.1 LPDDR2-SX: Burst Read operation followed by Precharge 9cont’d)

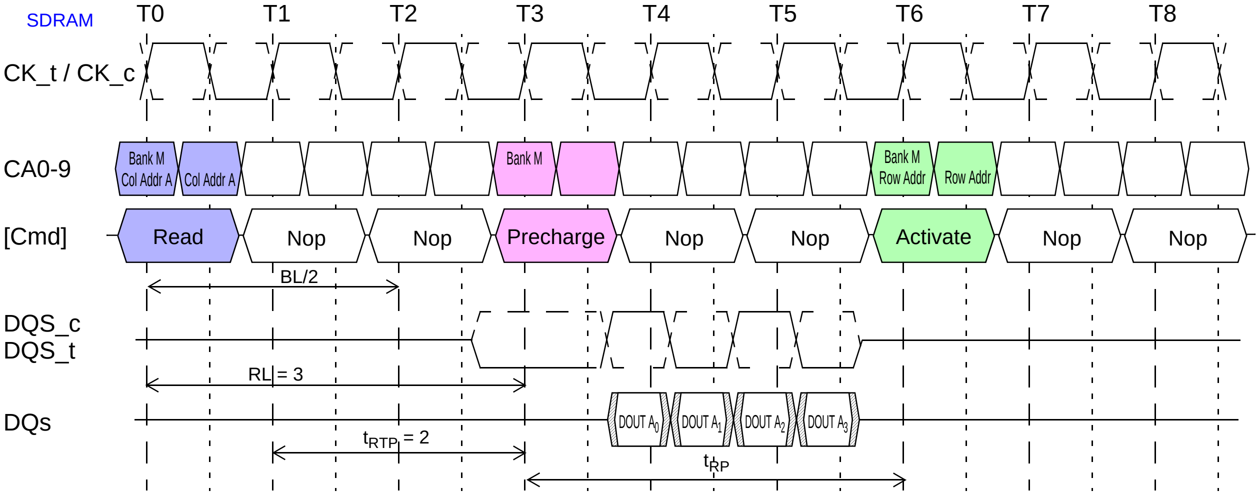


Figure 64 — LPDDR2-S2: Burst read followed by Precharge: RL = 3, BL = 4, RU(t_{RTP}(min)/t_{CK}) = 2

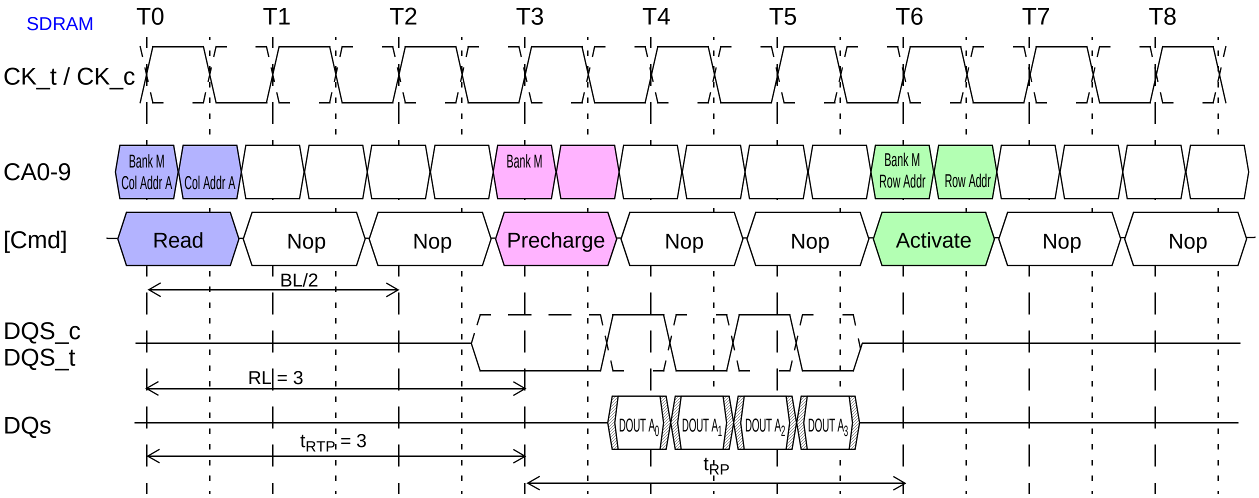


Figure 65 — LPDDR2-S4: Burst read followed by Precharge: RL = 3, BL = 4, RU(t_{RTP}(min)/t_{CK}) = 3

5.9.2 LPDDR2-SX: Burst Write followed by Precharge

For write cycles, a delay must be satisfied from the time of the last valid burst input data until the Precharge command may be issued. This delay is known as the write recovery time (t_{WR}) referenced from the completion of the burst write to the precharge command. No Precharge command to the same bank should be issued prior to the t_{WR} delay.

LPDDR2-S2 devices write data to the array in prefetch pairs (prefetch = 2) and LPDDR2-S4 devices write data to the array in prefetch quadruples (prefetch = 4). The beginning of an internal write operation may only begin after a prefetch group has been latched completely. Therefore, the write recovery time (t_{WR}) starts at different boundaries for LPDDR2-S2 and LPDDR2-S4 devices.

For LPDDR2-S2 devices, minimum Write to Precharge command spacing to the same bank is WL + RU(BL/2) + 1 + RU(t_{WR}/t_{CK}) clock cycles. For LPDDR2-S4 devices, minimum Write to Precharge command spacing to the same bank is WL + BL/2 + 1 + RU(t_{WR}/t_{CK}) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For an truncated burst, BL is the effective burst length.

See Table 51 on page 102 for Write to Precharge timings for LPDDR2-S4 and Table 52 on page 103 for Write to Precharge timings for LPDDR2-S2.

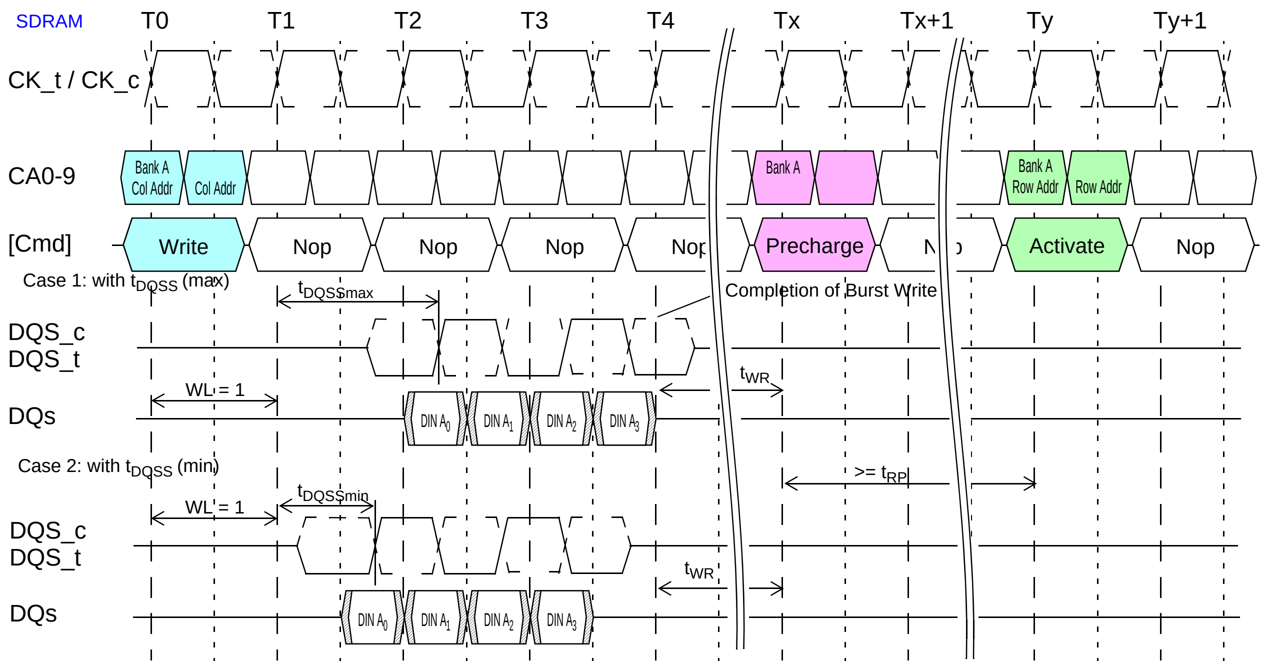


Figure 66 — LPDDR2-SX: Burst write followed by precharge: WL = 1, BL = 4

5.9.3 LPDDR2-SX: Auto Precharge operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the LPDDR2 SDRAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle.

If AP is LOW when the Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency) thus improving system performance for random data access.

5.9.3.1 LPDDR2-SX: Burst Read with Auto-Precharge

If AP (CA0f) is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged.

LPDDR2-S2 devices start an Auto-Precharge operation on the rising edge of the clock BL/2 - 1 + RU(t_{RTP}/t_{CK}) clock cycles later than the Read with AP command. Refer to Table 52 on page 103 for equations related to Auto-Precharge for LPDDR2-S2.

LPDDR2-S4 devices start an Auto-Precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 + RU(t_{RTP}/t_{CK}) clock cycles later than the Read with AP command, whichever is greater. Refer to Table 51 on page 102 for equations related to Auto-Precharge for LPDDR2-S4.

A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied simultaneously.

The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto precharge begins.

The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

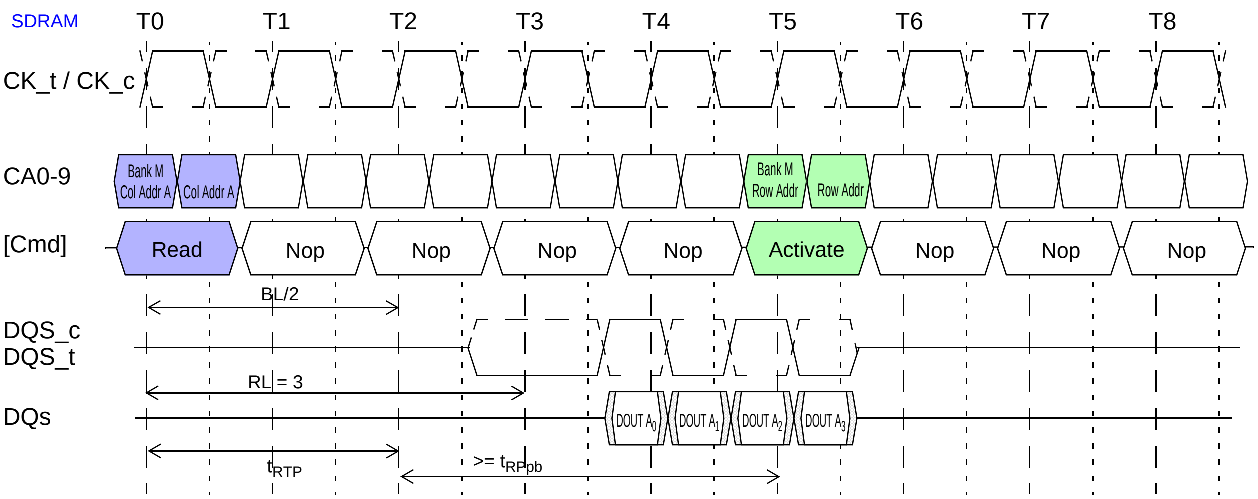


Figure 67 — LPDDR2-S4: Burst read with Auto-Precharge: RL = 3, BL = 4, RU(t_{RTP}(min)/t_{CK}) = 2

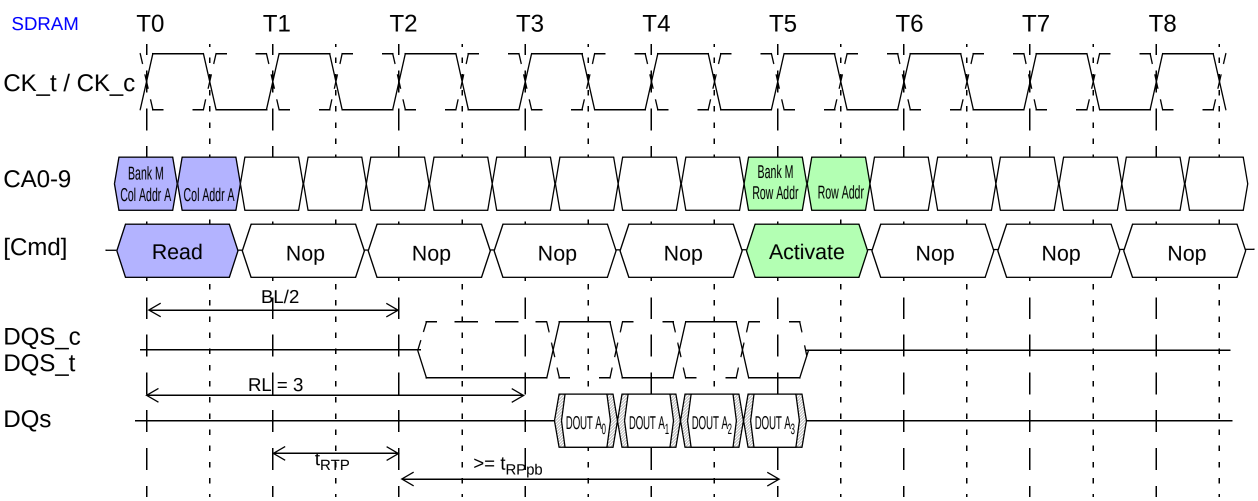


Figure 68 — LPDDR2-S2: Burst read with Auto-Precharge: RL = 3, BL = 4, RU(t_{RTP}(min)/t_{CK}) = 1

5.9.3.2 LPDDR2-SX: Burst write with Auto-Precharge

If AP (CA0f) is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The LPDDR2 SDRAM starts an Auto Precharge operation on the rising edge which is t_{WR} cycles after the completion of the burst write.

A new bank activate (command) may be issued to the same bank if both of the following two conditions are satisfied.

The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto precharge begins.

The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

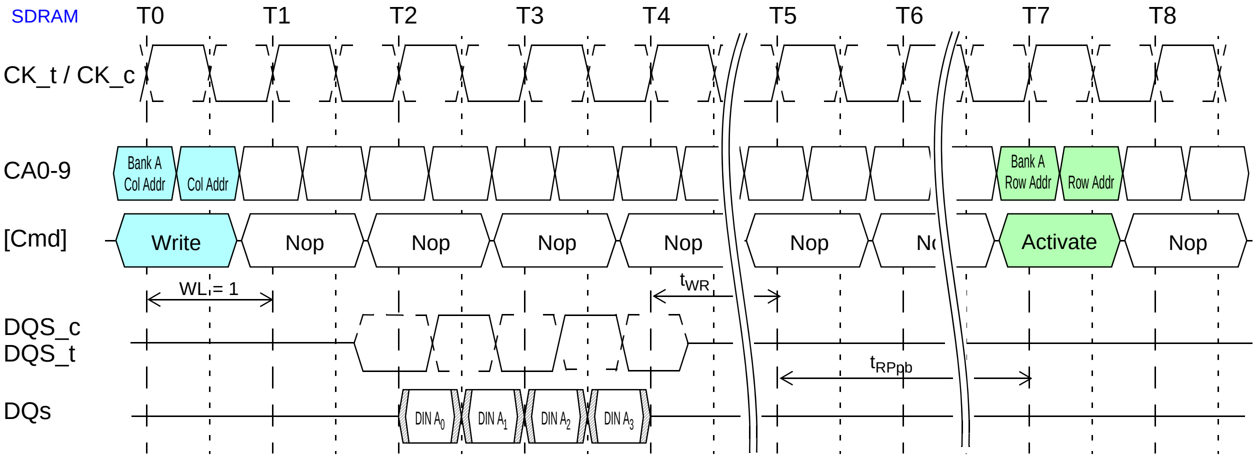


Figure 69 — LPDDR2-SX: Burst write w/Auto Precharge: WL = 1, BL = 4

5.9.3.2 LPDDR2-SX: Burst write with Auto-Precharge (cont'd)

Table 51 — LPDDR-S4: Precharge & Auto Precharge clarification

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Notes
Read	Precharge (to same Bank as Read)	BL/2 + max(2, RU(t_{RTP}/t_{CK})) - 2	clks	1
	Precharge All	BL/2 + max(2, RU(t_{RTP}/t_{CK})) - 2	clks	1
BST (for Reads)	Precharge (to same Bank as Read)	1	clks	1
	Precharge All	1	clks	1
Read w/AP	Precharge (to same Bank as Read w/AP)	BL/2 + max(2, RU(t_{RTP}/t_{CK})) - 2	clks	1,2
	Precharge All	BL/2 + max(2, RU(t_{RTP}/t_{CK})) - 2	clks	1
	Activate (to same Bank as Read w/AP)	BL/2 + max(2, RU(t_{RTP}/t_{CK})) - 2 + RU(t_{RPpb}/t_{CK})	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU(tDQSCKmax/tCK) - WL + 1	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	BL/2	clks	3
Write	Precharge (to same Bank as Write)	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	clks	1
	Precharge All	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	clks	1
BST (for Writes)	Precharge (to same Bank as Write)	WL + RU(t_{WR}/t_{CK}) + 1	clks	1
	Precharge All	WL + RU(t_{WR}/t_{CK}) + 1	clks	1
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	clks	1
	Precharge All	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	clks	1
	Activate (to same Bank as Write w/AP)	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1 + RU(t_{RPpb}/t_{CK})	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	BL/2	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU(t_{WTR}/t_{CK}) + 1	clks	3
Precharge	Precharge (to same Bank as Precharge)	1	clks	1
	Precharge All	1	clks	1
Precharge All	Precharge	1	clks	1
	Precharge All	1	clks	1

NOTE 1 For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after t_{RP} depending on the latest precharge command issued to that bank.

NOTE 2 Any command issued during the minimum delay time as specified in Table 51 is illegal.

NOTE 3 After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write w/AP may not be interrupted or truncated.

5.9.3.2 LPDDR2-SX: Burst write with Auto-Precharge (cont'd)

Table 52 — LPDDR-S2: Precharge & Auto Precharge clarification

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Notes
Read	Precharge (to same Bank as Read)	$BL/2 + RU(t_{RTP}/t_{CK}) - 1$	clks	1
	Precharge All	$BL/2 + RU(t_{RTP}/t_{CK}) - 1$	clks	1
BST (for Reads)	Precharge (to same Bank as Read)	1	clks	1
	Precharge All	1	clks	1
Read w/AP	Precharge (to same Bank as Read w/AP)	$BL/2 + RU(t_{RTP}/t_{CK}) - 1$	clks	1
	Precharge All	$BL/2 + RU(t_{RTP}/t_{CK}) - 1$	clks	1
	Activate (to same Bank as Read w/AP)	$BL/2 + RU(t_{RTP}/t_{CK}) - 1$ $+ RU(t_{RPpb}/t_{CK})$	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU(tDQSCKmax/tCK) - WL + 1	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	BL/2	clks	3
Write	Precharge (to same Bank as Write)	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	clks	1
	Precharge All	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	clks	1
BST (for Writes)	Precharge (to same Bank as Write)	$WL + RU(t_{WR}/t_{CK}) + 1$	clks	1
	Precharge All	$WL + RU(t_{WR}/t_{CK}) + 1$	clks	1
Write w/AP	Precharge (to same Bank as Write w/AP)	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	clks	1
	Precharge All	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	clks	1
	Activate (to same Bank as Write w/AP)	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$ $+ RU(t_{RPpb}/t_{CK})$	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	BL/2	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	$WL + BL/2 + RU(t_{WTR}/t_{CK}) + 1$	clks	3
Precharge	Precharge (to same Bank as Precharge)	1	clks	1
	Precharge All	1	clks	1
Precharge All	Precharge	1	clks	1
	Precharge All	1	clks	1

NOTE 1 For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after t_{RP} depending on the latest precharge command issued to that bank.

NOTE 2 Any command issued during the minimum delay time as specified in Table 52 is illegal.

NOTE 3 After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write w/AP may not be interrupted or truncated.

5.10 LPDDR2-SX: Refresh command

The Refresh command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of clock. Per Bank Refresh is initiated by having CA3 LOW at the rising edge of clock and All Bank Refresh is initiated by having CA3 HIGH at the rising edge of clock. Per Bank Refresh is only allowed in devices with 8 banks.

A Per Bank Refresh command, REFpb performs a refresh operation to the bank which is scheduled by the bank counter in the memory device. The bank sequence of Per Bank Refresh is fixed to be a sequential round-robin: "0-1-2-3-4-5-6-7-0-1-...". The bank count is synchronized between the controller and the SDRAM upon issuing a RESET command or at every exit from self refresh, by resetting bank count to zero. The bank addressing for the Per Bank Refresh count is the same as established in the single-bank Precharge command (see Table 50 on page 96, "Bank selection for Precharge by address bits").

A bank must be idle before it can be refreshed. It is the responsibility of the controller to track the bank being refreshed by the Per Bank Refresh command.

As shown in Table 53 on page 105, the REFpb command may not be issued to the memory until the following conditions are met:

a) t_{RFCab} has been satisified after the prior REFab command

b) t_{RFCpb} has been satisfied after the prior REFpb command

c) t_{RP} has been satisified after the prior Precharge command to that given bank

t_{RRD} has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than affected by the REFpb command).

The target bank is inaccessable during the Per Bank Refresh cycle time (t_{RFCpb}), however other banks within the device are accessable and may be addressed during the Per Bank Refresh cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in active state or accessed by a read or a write command.

When the Per Bank refresh cycle has completed, the affected bank will be in the Idle state.

As shown in Table 53 on page 105, after issuing REFpb:

a) t_{RFCpb} must be satisified before issuing a REFab command

b) t_{RFCpb} must be satisfied before issuing an ACTIVATE command to the same bank

c) t_{RRD} must be satisified before issuing an ACTIVATE command to a different bank

d) t_{RFCpb} must be satisified before issuing another REFpb command

An All Bank Refresh command, REFab performs a refresh operation to all banks. All banks have to be in Idle state when REFab is issued (for instance, by Precharge all-bank command). REFab also synchronizes the bank count between the controller and the SDRAM to zero.

As shown in Table 53 on page 105, the REFab command may not be issued to the memory until the following conditions have been met:

a) t_{RFCab} has been satisified after the prior REFab command

b) t_{RFCpb} has been satisified after the prior REFpb command

c) t_{RP} has been satisified after prior Precharge commands

When the All Bank refresh cycle has completed, all banks will be in the Idle state.

As shown in Table 53 on page 105, after issuing REFab:

a) the t_{RFCab} latency must be satisfied before issuing an ACTIVATE command

b) the t_{RFCab} latency must be satisfied before issuing a REFab or REFpb command.

5.10 LPDDR2-SX: Refresh command (cont'd)

Table 53 — Command Scheduling Separations related to Refresh

Symbol	minimum delay from	to		Notes
t_{RFCab}	REFab	REFab		
		Activate cmd to *any* bank .		
		REFpb		
t_{RFCpb}	REFpb	REFab		
		Activate cmd to *same* bank as REFpb		
		REFpb		
t_{RRD}	REFpb	Activate cmd to *different* bank than REFpb		
	Activate	REFpb affecting an idle bank (*different* bank than Activate)		1
		Activate cmd to *different* bank than prior Activate		
NOTE 1 A bank must be in the Idle state before it is refreshed. Therefore, after Activate, REFab is not allowed and REFpb is allowed only if it affects a bank which is in the Idle state.				

5.10.1 LPDDR2 SDRAM Refresh Requirements

(1) Minimum number of Refresh commands:
The LPDDR2 SDRAM requires a minimum number of R Refresh (REFab) commands within *any* rolling Refresh Window (t_{REFW} = 32 ms @ MR4[2:0] = "011" or Tcase $\leq$ 85 °C). See Table 101 on page 180 and Table 102 on page 180 for actual numbers per density. The resulting average refresh interval (t_{REFI}) is given in Table 102 on page 180 and Table 101 on page 180.

See Mode Register 4 on page 28 for t_{REFW} and t_{REFI} refresh multipliers at different MR4 settings.

For LPDDR2-SDRAM devices supporting Per-Bank-Refresh, a REFab command may be replaced by a full cycle of eight REFpb commands.

(2) Burst Refresh limitation:
To limit maximum current consumption, a maximum of 8 REFab commands may be issued in any rolling t_{REFBW} (t_{REFBW} = 4 x 8 x t_{RFCab}). This condition does not apply if REFpb commands are used.

(3) Refresh Requirements and Self-Refresh:
If any time within a refresh window is spent in Self-Refresh Mode, the number of required Refresh commands in this particular window is reduced to:

$\mathbf{R^* = R - RU\{t_{SRF} / t_{REFI}\} = R - RU\{R * t_{SRF} / t_{REFW}\};}$ where RU stands for the round-up function.

5.10.1 LPDDR2 SDRAM Refresh Requirements (cont'd)

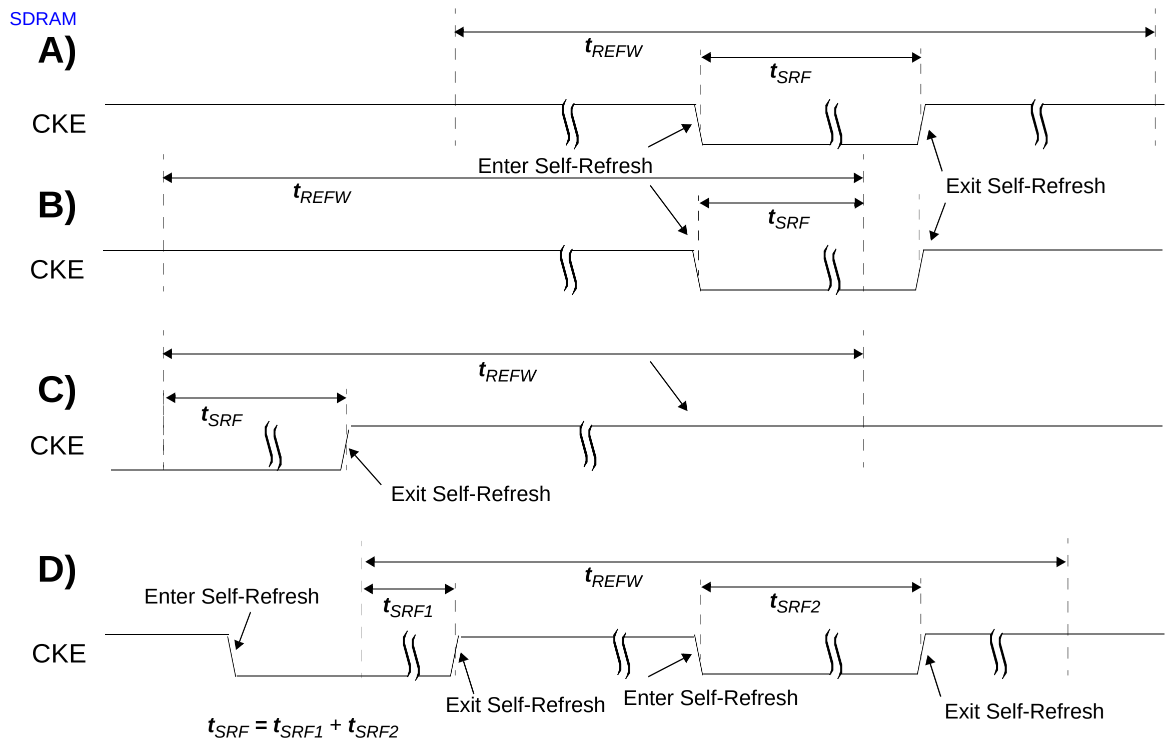


Figure 70 — LPDDR2-SX: Definition of t_{SRF}

Several examples on how to t_{SRF} is caclulated:

A: with the time spent in Self-Refresh Mode fully enclosed in the Refresh Window (t_{REF}),

B: at Self-Refresh entry

C: at Self-Refresh exit

D: with several different invervals spent in Self Refresh during one t_{REFW} interval

In contrast to JESD79 and JESD79-2 and JESD79-3 compliant SDRAM devices, LPDDR2-SX devices allow significant flexibiliy in scheduling REFRESH commends, as long as the boundary conditions above are met.

In the most straight forward case a REFRESH command should be scheduled every t_{REFI}. In this case Self-Refresh may be entered at any time.

The users may choose to deviate from this regular refresh pattern e.g., to enable a period where no refreshes are required. In the extreme (e.g., LPDDR2-S4 1Gb) the user may choose to issue a refresh burst of 4096 REFRESH commands with the maximum allowable rate (limited by t_{REFBW}) followed by a long time without any REFRESH commands, until the refresh window is complete, then repeating this sequence. The achieveable time without REFRESH commands is given by t_{REFW} - (R / 8) * t_{REFBW} = t_{REFW} - R * 4 * t_{RFCab}. (e.g., for a LPDDR2-S4 1Gb device @ Tcase <= 85°C this can be up to 32 ms - 4096 * 4 * 130 ns ~ 30 ms).

While both - the regular and the burst/pause - patterns can satisfy the refresh requirements per rolling refresh interval, if they are repeated in every subsequent 32 ms window, extreme care must be taken when transitioning from one pattern to another to satisfy the refresh requirement in *every* rolling refresh window during the transition. Figure 72 on page 108 shows an example of an allowable transition from a burst pattern to a regular, distributed pattern. If this transition happens directly after the burst refresh phase, all rolling t_{REFW} intervalls will have at least the required number of refreshes. Figure 73 on page 109 shows an example of a non-allowable transition. In this case the regular refresh pattern starts after the completion of the pause-phase of the burst/pause refresh pattern. For several rolling t_{REFW} intervals the minimmun number of REFRESH commands is not satisfied. The understanding of the pattern transition is extremly relevant (even if in normal operation only one pattern is employed), as in Self-Refresh-Mode a regular, distributed refresh pattern has to be assumed, which is reflected in the equation for R* above. Therefore it is recommended to enter Self-Refresh-Mode ONLY directly after the burst-phase of a burst/pause refresh pattern as indicated in Figure 74 on page 109 and begin with the burst phase upon exit from Self-Refresh.

5.10.1 LPDDR2 SDRAM Refresh Requirements (cont'd)

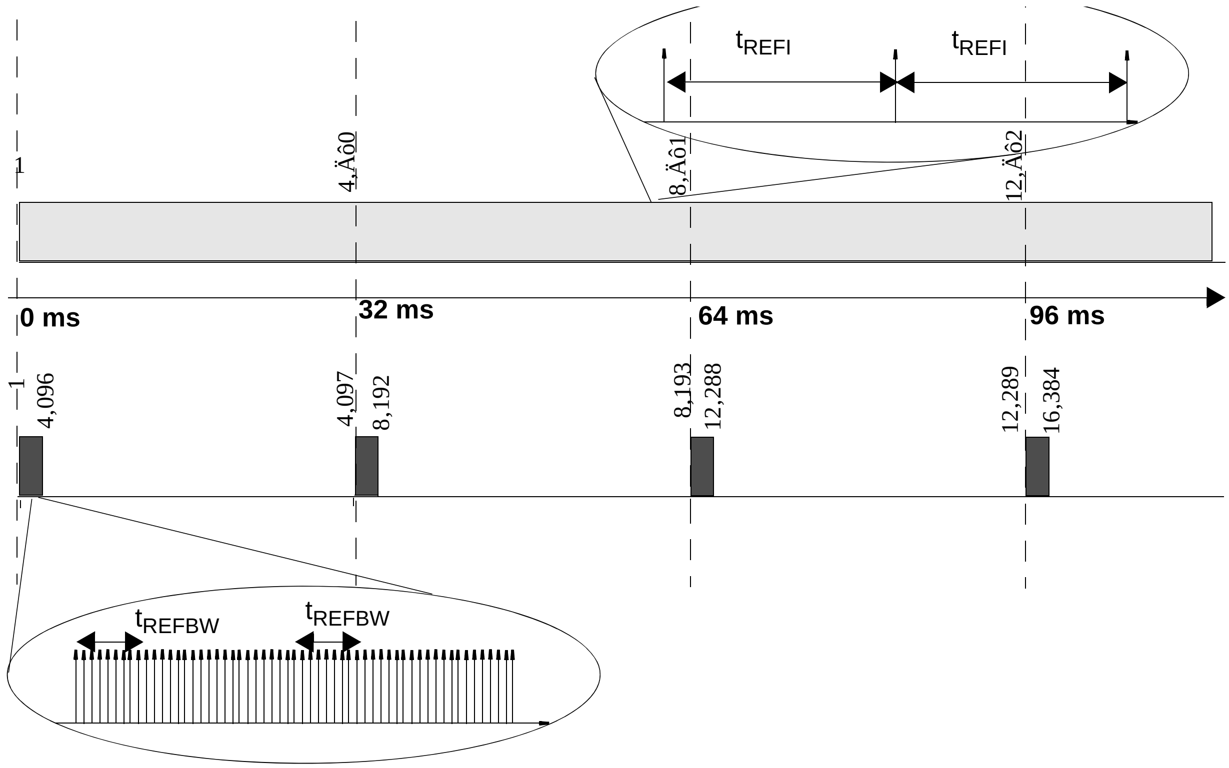


Figure 71 — LPDDR2-SX: Regular, Distributed Refresh Pattern vs. Repetitive Burst Refresh with Subsequent Refresh Pause

NOTE 1 For a (e.g.) LPDDR2-S4 1 Gb device @ Tcase less than or equal to 85C the distributed refresh pattern would have one REFRESH command per 7.8 us; the burst refresh pattern would have an average of one refresh command per 0.52 us followed by ~30 ms without any REFRESH command.

5.10.1 LPDDR2 SDRAM Refresh Requirements (cont'd)

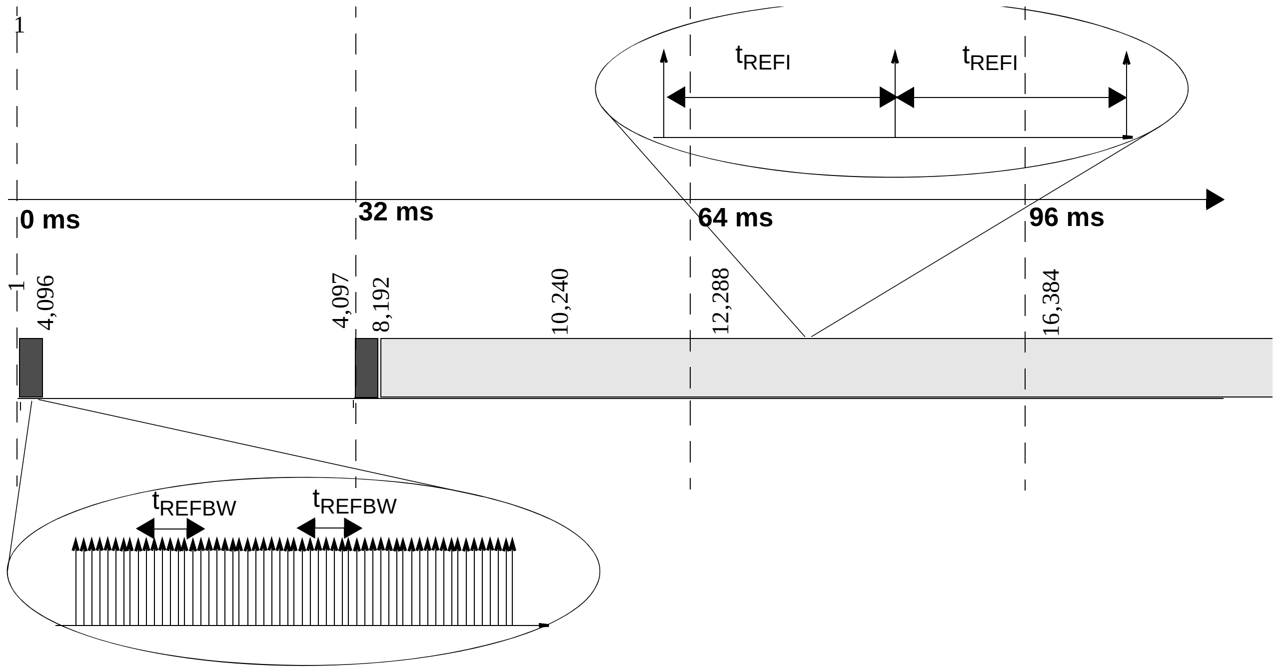


Figure 72 — LPDDR2-SX: Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern

NOTE 1 For a (e.g.) LPDDR2-S4 1 Gb device @ Tcase less than or equal to 85 C the distributed refresh pattern would have one REFRESH command per 7.8 us; the burst refresh pattern would have an average of one refresh command per 0.52 us followed by ~30 ms without any REFRESH command.

5.10.1 LPDDR2 SDRAM Refresh Requirements (cont'd)

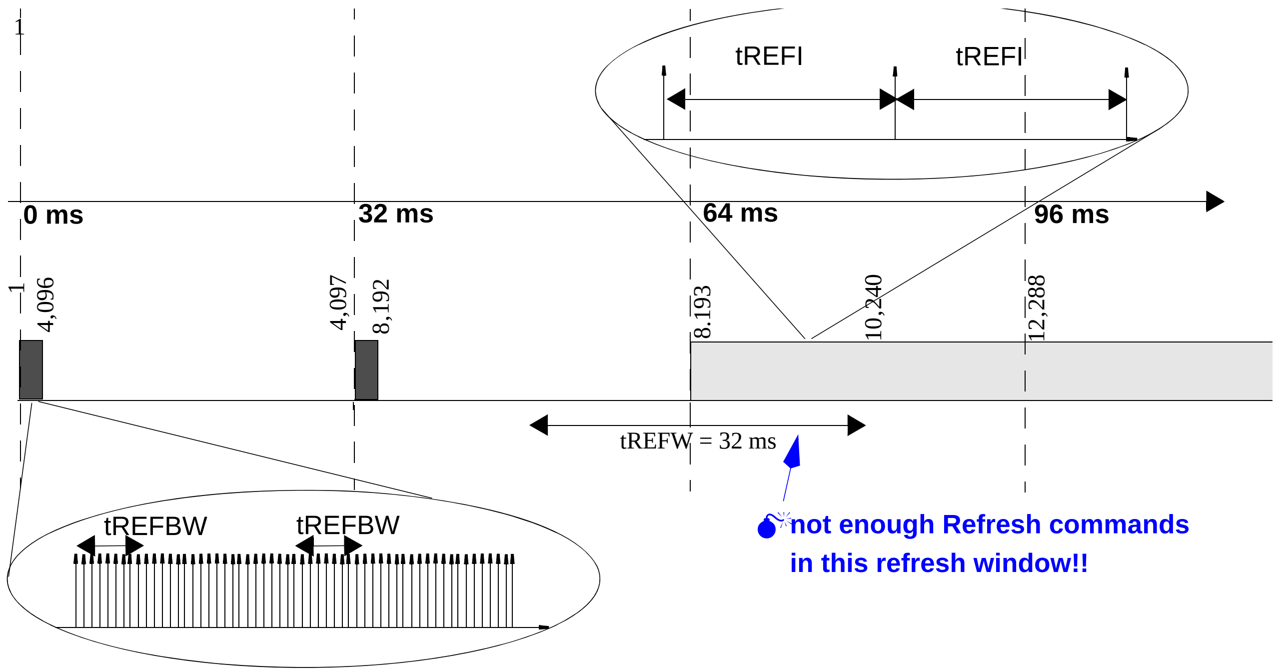


Figure 73 — LPDDR2-SX: NOT-Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern

NOTE 1 Only ~2048 REFRESH commands (<R!!) in the indicated tREFW win-

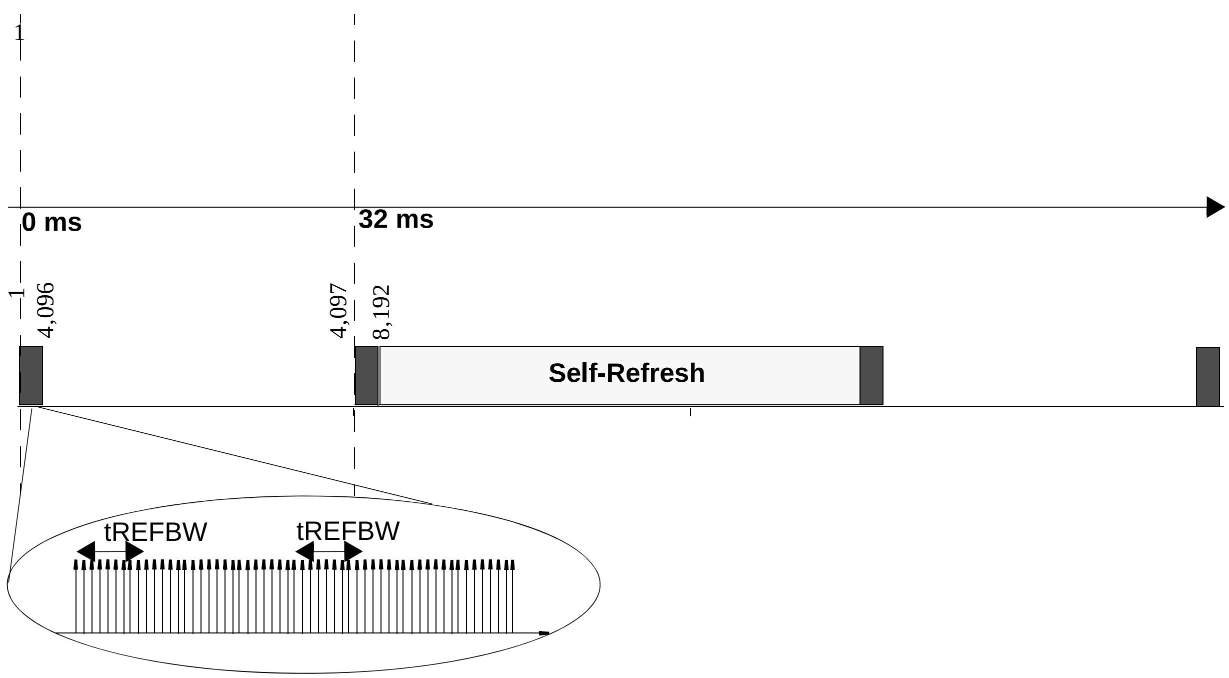


Figure 74 — LPDDR2-SX: Recommended Self-refresh entry and exit in conjunction with a Burst/Pause Refresh patterns.

5.10.1 LPDDR2 SDRAM Refresh Requirements (cont'd)

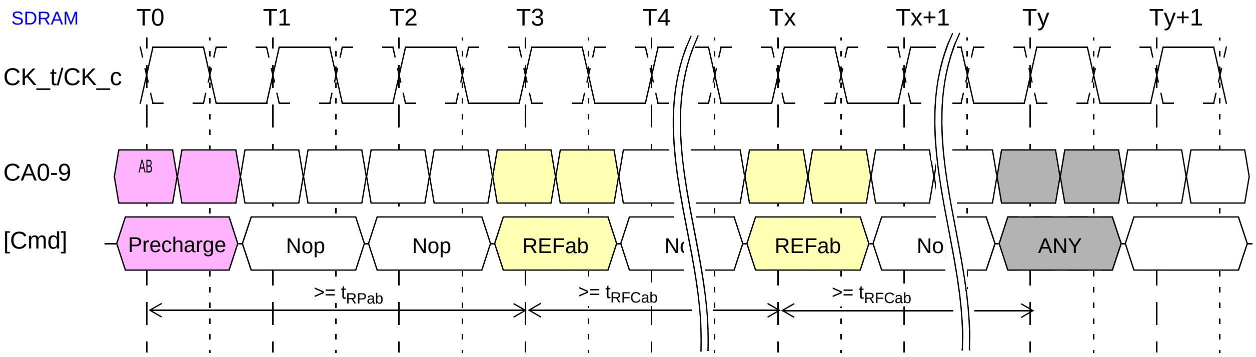
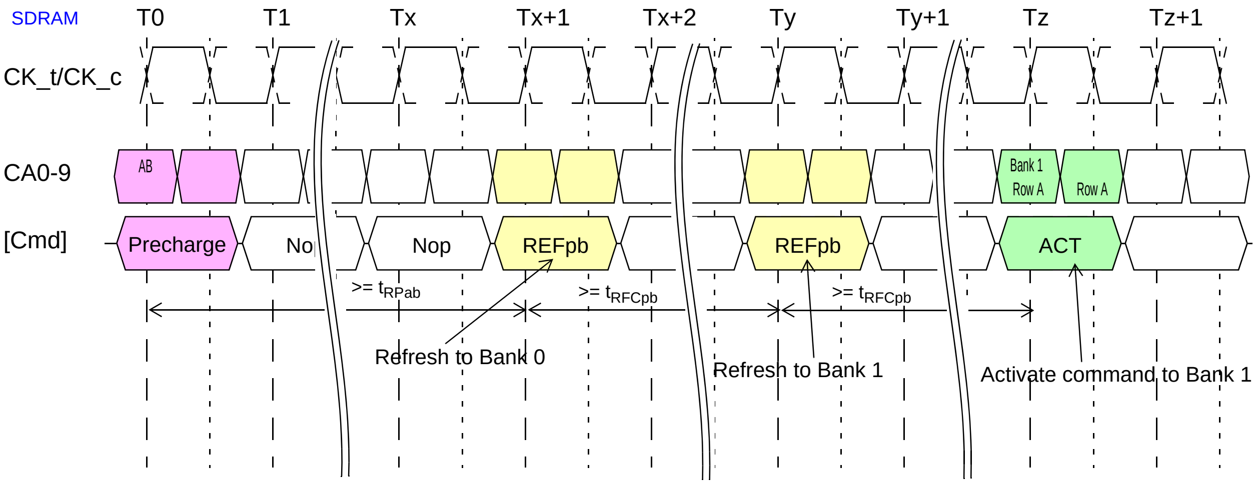


Figure 75 — LPDDR2-SX: All Bank Refresh Operation



NOTE 1 In the beginning of this example, the REFpb bank is pointing to Bank 0.

NOTE 2 Operations to other banks than the bank being refreshed are allowed during the t_{RFCpb} period.

Figure 76 — LPDDR2-SX: Per Bank Refresh Operation

5.11 LPDDR2-SX: Self Refresh operation

The Self Refresh command can be used to retain data in the LPDDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the LPDDR2 SDRAM retains data without external clocking. The LPDDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR2-SX devices can operate in Self Refresh in both the Standard or Extended Temperature Ranges. LPDDR2-SX devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher at high temperatures. See “LPDDR2 IDD Specification Parameters and Operating Conditions” on page 172 for details.

Once the LPDDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pins (VDD1, VDD2, and VDDCA) must be at valid levels. VDDQ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, VDDQ must be within specified limits. VrefDQ and VrefCA may be at any level within minimum and maximum levels (see “Absolute Maximum DC Ratings” on page 146). However prior to exiting Self-Refresh, VrefDQ and VrefCA must be within specified limits (see “Recommended DC Operating Conditions” on page 147). The SDRAM initiates a minimum of one all-bank refresh command internally within t_{CKESR} period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the LPDDR2 SDRAM must remain in Self Refresh mode is t_{CKESR}. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minmum of 2 clock cycles prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least t_{XSR} must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period t_{XSR} for proper operation except for self refresh re-entry. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval t_{XSR}.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.

5.11 LPDDR2-SX: Self Refresh operation (cont'd)

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section "LPDDR2 SDRAM Refresh Requirements" on page 105, since no refresh operations are performed in power-down mode.

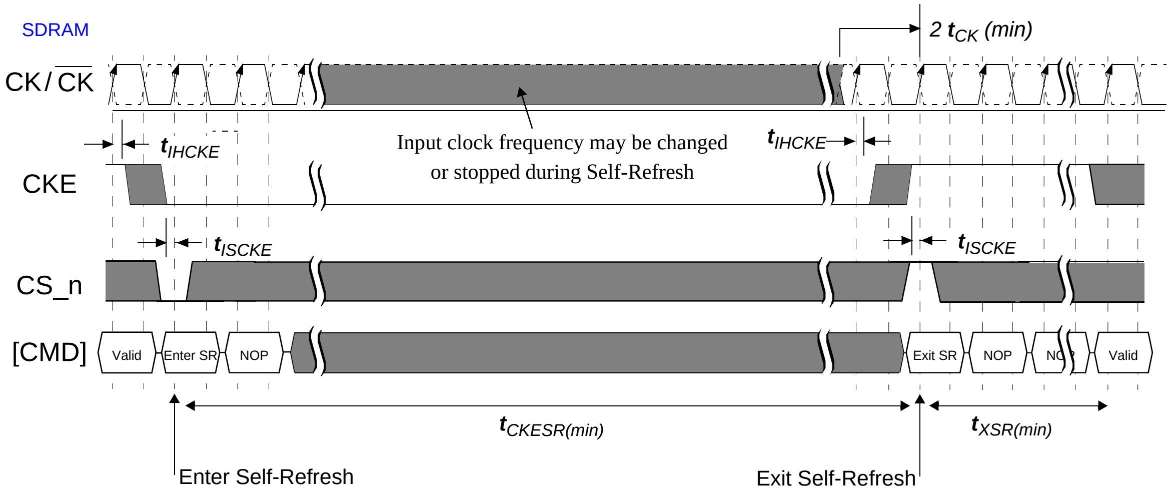


Figure 77 — LPDDR2-SX: Self-Refresh Operation

NOTE 1 Input clock frequency may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 5 clocks (t_{INIT2}) of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

NOTE 2 Device must be in the "All banks idle" state prior to entering Self Refresh mode.

NOTE 3 t_{XSR} begins at the rising edge of the clock after CKE is driven HIGH.

NOTE 4 A valid command may be issued only after t_{XSR} is satisfied. NOPs shall be issued during t_{XSR}.

5.11.1 LPDDR2-S2: Partial Array Self-Refresh: Bank Masking

LPDDR2-S2 SDRAM keeps the same PASR mapping of LPDDR SDRAM (JESD209). The choice of partial array to be refreshed in self refresh mode allows to reduce the range into lower numbered banks. MR16 has to be properly programmed to choose the PASR range (See Mode Register 16 as described on page 31). The PASR range becomes effective when the device goes into self refresh mode and determines which bank or banks to be refreshed.

Table 54 — Bank Masking in LPDDR2-S2 4-Bank devices (64mb-2Gb)

PASR Choice	Bank 0	Bank 1	Bank 2	Bank 3
Full Array				
1/2 Array			No Self-Refresh	
1/4 Array		No Self-Refresh		

Table 55 — Bank Masking in LPDDR2-S2 8-Bank devices (4Gb-8Gb)

PASR Choice	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Full Array								
1/2 Array					No Self-Refresh			
1/4 Array			No Self-Refresh					
1/8 Array		No Self-Refresh						

5.11.2 LPDDR2-S4: Partial Array Self-Refresh: Bank Masking

LPDDR2-S4 SDRAM has 4 or 8 banks. For LPDDR2-S4 devices, 64Mb to 512Mb LPDDR2 SDRAM has 4 banks, while 1Gb and higher density has 8. Each bank of LPDDR2 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16 as described on page 31.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to entire bank is not blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, “unmasked”. When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is decribed in the following chapter.

5.11.3 LPDDR2-S4: Partial Array Self-Refresh: Segment Masking

Segment masking scheme may be used in lieu of or in combination with bank masking scheme in LPDDR2-S4 SDRAM. The number of segments differ by the density and the setting of each segment mask bit is applied across all the banks. For segment masking bit assignments, see Mode Register 17 as described on page 31.

For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, “masked”. Programming of segment mask bits is similar to the one of bank mask bits. LPDDR2 SDRAM whose density is 64Mb, 128Mb, 256Mb, or 512Mb does not support segment masking. Only bank masking scheme is available. For 1Gb and larger densities, 8 segments are used as listed in Mode Register 17 as described on page 31. One mode register unit is used for the programming of segment mask bits up to 8 bits. One more mode register unit may be reserved for future use. These 2 mode register units are noted as “not used” for low-density LPDDR2-S4 SDRAM and a programming of mask bits has no effect on the device operation.

Table 56 — Example of Bank and Segment Masking use in LPDDR2-S4 devices

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0		M						M
Segment 1	0		M						M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0		M						M
Segment 4	0		M						M
Segment 5	0		M						M
Segment 6	0		M						M
Segment 7	1	M	M	M	M	M	M	M	M

NOTE 1 This table illustrates an example of an 8-bank LPDDR2-S4 device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

5.12 Mode Register Read Command

The Mode Register Read command is used to read configuration and status data from mode registers for both NVM and SDRAM. The Mode Register Read (MRR) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The mode register contents are available on the first data beat of DQ0-DQ7, RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in "DQ Calibration" on page 117. All DQS shall be toggled for the duration of the Mode Register Read burst. The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (t_{MRR}) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS shall be toggled.

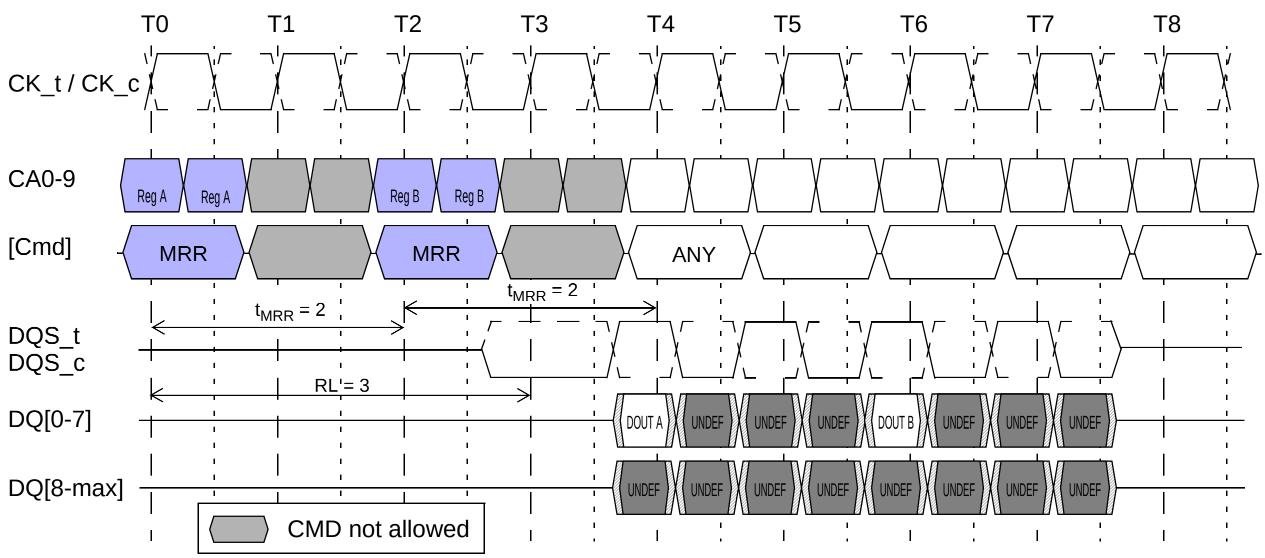


Figure 78 — Mode Register Read timing example: RL = 3, t_{MRR} = 2

NOTE 1 Mode Register Read has a burst length of four.
NOTE 2 Mode Register Read operation shall not be interrupted.
NOTE 3 Mode Register data is valid only on DQ[0-7] on the first beat. Subsequent beats contain valid, but undefined data. DQ[8-max] contain valid, but undefined data for the duration of the MRR burst.
NOTE 4 The Mode Register Command period is t_{MRR}. No command (other than Nop) is allowed during this period.
NOTE 5 Mode Register Reads to DQ Calibration registers MR32 and MR40 are described in the section on DQ Calibration.

The MRR command shall not be issued earlier than BL/2 clock cycles after a prior Read command and WL + 1 + BL/2 + RU(t_{WTR}/t_{CK}) clock cycles after a prior Write command, because read-bursts and write-bursts shall not be truncated by MRR. Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as "BL."

5.12 Mode Register Read Command (cont'd)

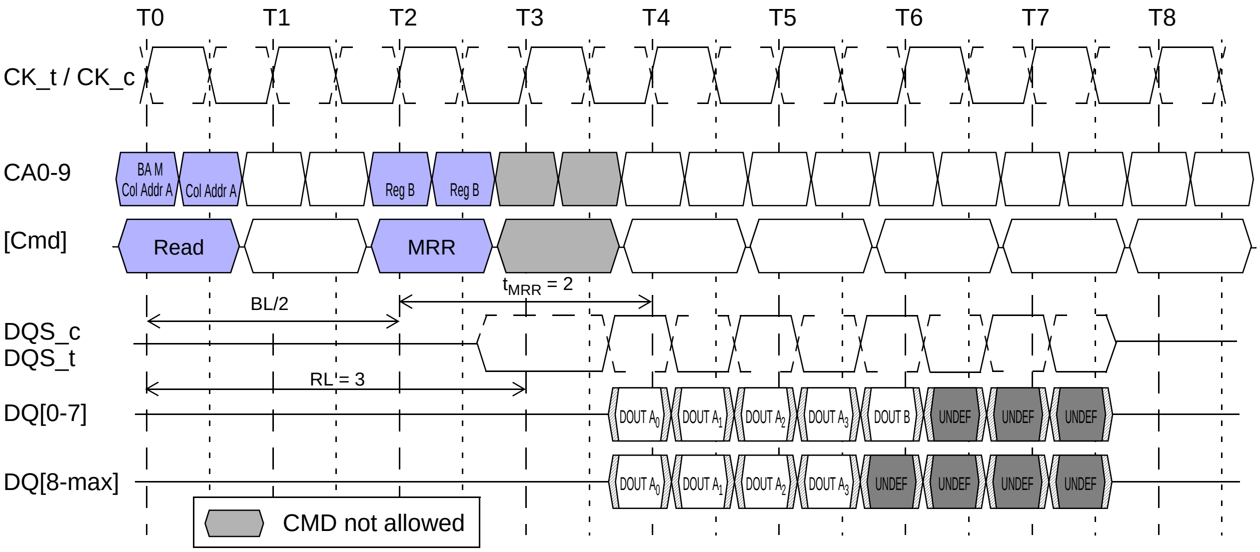


Figure 79 — LPDDR2: Read to MRR timing example: RL = 3, t_{MRR} = 2

NOTE 1: The minimum number of clocks from the burst read command to the Mode Register Read command is BL/2.

NOTE 2: The Mode Register Read Command period is t_{MRR}. No command (other than Nop) is allowed during this

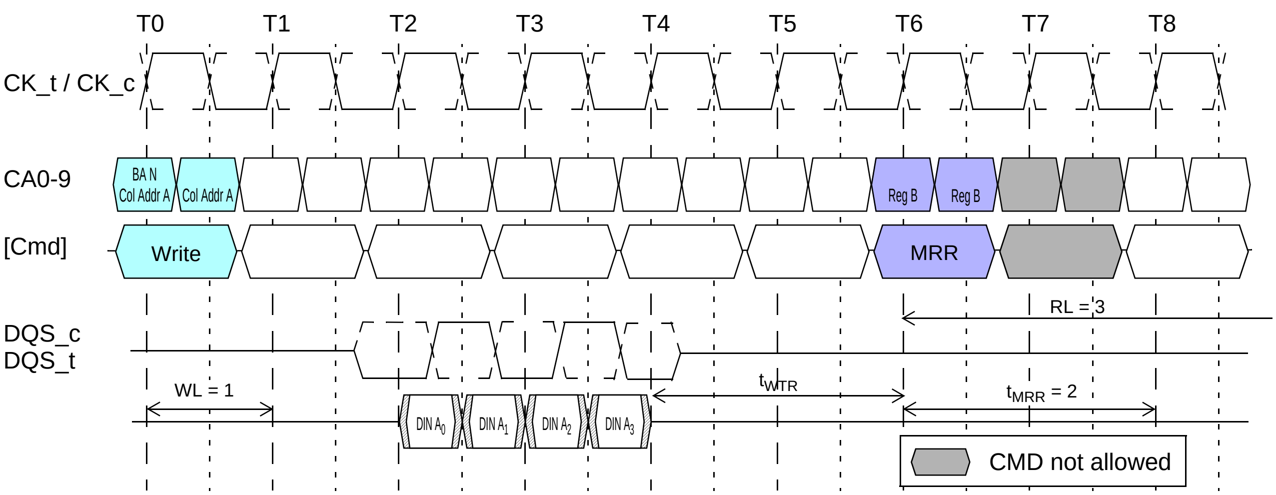


Figure 80 — LPDDR2: Burst Write Followed by MRR: RL = 3, WL = 1, BL = 4

NOTE 1 The minimum number of clock cycles from the burst write command to the Mode Register Read command is [WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})].

NOTE 2 The Mode Register Read Command period is t_{MRR}. No command (other than Nop) is allowed during this period.

5.12.1 Temperature Sensor

LPDDR2-SX and LPDDR2-N devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate (SDRAM), determine whether AC timing de-rating is required in the Extended Temperature Range (SDRAM and NVM), and/or monitor the operating temperature (SDRAM and NVM). Either the temperature sensor or the device TOPER (See “Operating Temperature Range” on page 148) may be used to determine whether operating temperature requirements are being met.

Temperature sensor data may be read from MR4 using the Mode Register Read protocol.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification (See “Operating Temperature Range” on page 148) that applies for the Standard or Extended Temperature Ranges. For example, TCASE may be above 85° C when MR4[2:0] equals 011B.

To assure proper operation using the temperature sensor, applications should consider the following factors:

TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2° C.

ReadInterval is the time period between MR4 reads from the system.

TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.

SysRespDelay is the maximum time between a read of MR4 and the response by the system.

LPDDR2 devices shall allow for a 2° C temperature margin between the point at which the device temperature enters the Extended Temperature Range and point at which the controller re-configures the system accordingly.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$TempGradient \times (ReadInterval + tTSI + SysRespDelay) \le 2C$$

Table 57 — Temperature Sensor

Parameter	Symbol	Max/Min	Value	Unit	Notes
System Temperature Gradient	TempGradient	Max	System Dependent	°C/s	
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	
Temperature Sensor Interval	tTSI	Max	16	ms	
System Response Delay	SysRespDelay	Max	System Dependent	ms	
Device Temperature Margin	TempMargin	Max	2	°C	

For example, if TempGradient is 10°C/s and the SysRespDelay is 1 ms:

$$\frac{10C}{s} \times (ReadInterval + 16ms + 1ms) \le 2C$$

In this case, ReadInterval shall be no greater than 183 ms.

5.12.1 Temperature Sensor (cont'd)

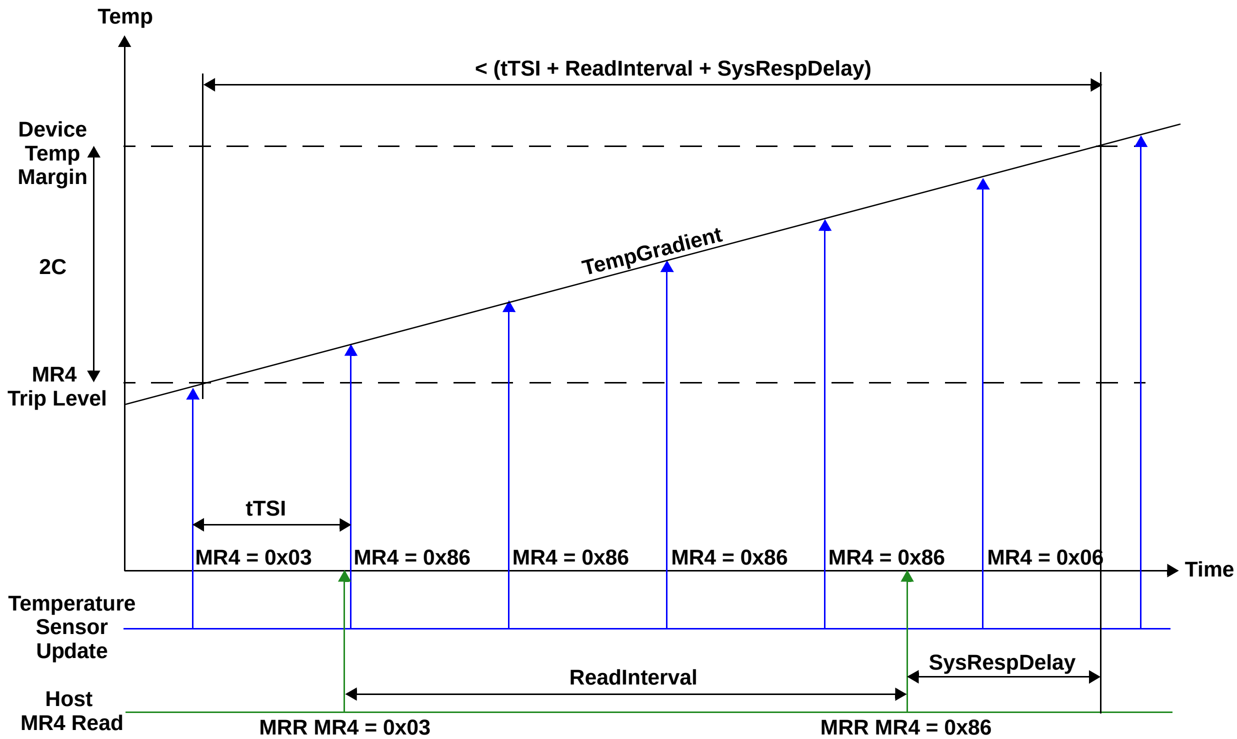


Figure 81 — Temp Sensor Timing

5.12.2 DQ Calibration

LPDDR2-SX and LPDDR2-N devices feature a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern "A") or MR40 (Pattern "B") will return the specified pattern on DQ[0] for x8 devices, DQ[0] and DQ[8] for x16 devices, and DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices. For x8 devices, DQ[7:1] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For x16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst.

For LPDDR2-SX devices, MRR DQ Calibration commands may only occur in the Idle state.

Table 58 — Data Calibration Pattern Description

	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
Pattern "A" (MR32)	1	0	1	0
Pattern "B" (MR40)	0	0	1	1

5.12.2 DQ Calibration (cont'd)

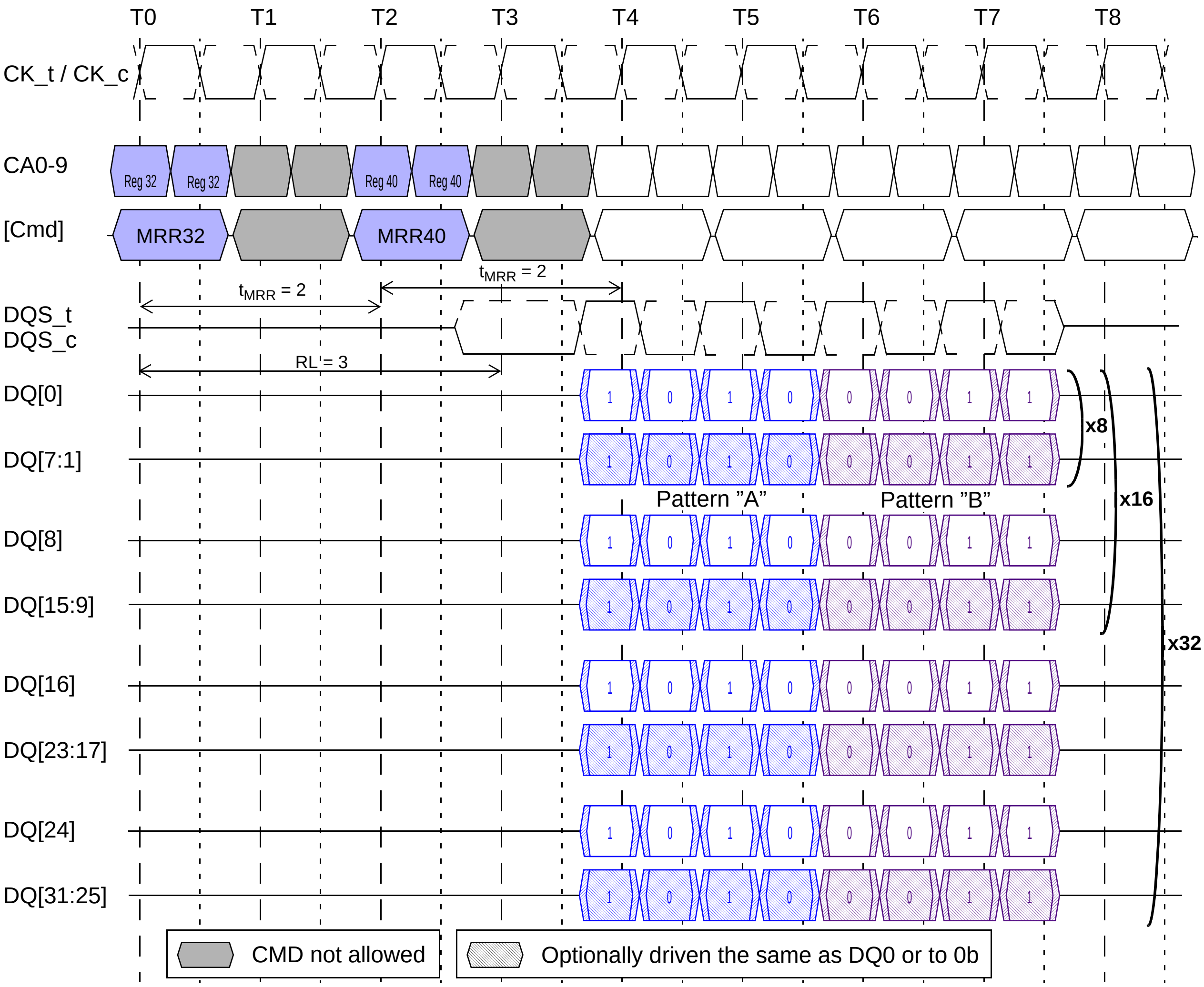


Figure 82 — MR32 and MR40 DQ Calibration timing example: RL = 3, t_{MRR} = 2

NOTE 1 Mode Register Read has a burst length of four.
NOTE 2 Mode Register Read operation shall not be interrupted.
NOTE 3 Mode Register Reads to MR32 and MR40 drive valid data on DQ[0] during the entire burst. For x16 devices, DQ[8] shall drive the same information as DQ[0] during the burst. For x32 devices, DQ[8], DQ[16], and DQ[24] shall drive the same information as DQ[0] during the burst.
NOTE 4 For x8 devices, DQ[7:1] may optionally drive the same information as DQ[0] or they may drive 0b during the burst. For x16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or they may drive 0b during the burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or they may drive 0b during the burst.
NOTE 5 The Mode Register Command period is t_{MRR}. No command (other than Nop) is allowed during this period

5.13 Mode Register Write Command

The Mode Register Write command is used to write configuration data to mode registers for both NVM and SDRAM. The Mode Register Write (MRW) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by t_{MRW}. Mode Register Writes to read-only registers shall have no impact on the functionality of the device.

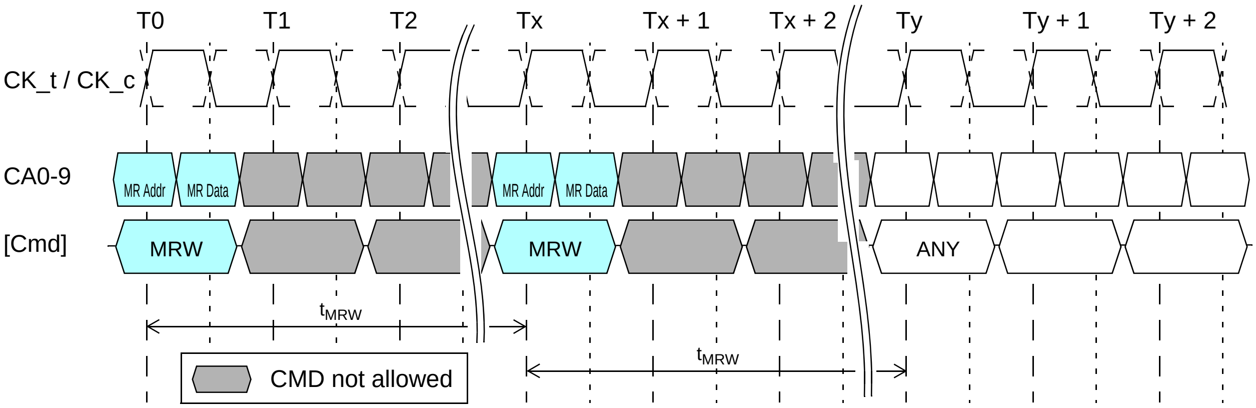


Figure 83 — Mode Register Write timing example: RL = 3, t_{MRW} = 5

NOTE 1 The Mode Register Write Command period is t_{MRW}. No command (other than Nop) is allowed during this period.
NOTE 2 At time Ty, the device is in the idle state.

5.13.1 LPDDR2-SX: Mode Register Write

For LPDDR2-S devices, the MRW may only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in the idle precharge state is to issue a Precharge-All command.

5.13.2 LPDDR2-N: Mode Register Write

For LPDDR2-N devices, the MRW may be issued from the Row Active or Idle states. If the MRW command is issued from the Row Active state, all row buffer contents are invalidated and the device returns to the Idle state.

The minimum time from the burst read command to the MRW command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum Read to MRW latency is RL + RU(t_{DQSCK}max/t_{CK}) + BL/2 clock cycles. The minimum time from the burst write command to the MRW command is defined by the Write Latency (WL) and the Burst Length (BL). Minimum Write to MRW latency is WL + 1 + BL/2 + RU(t_{WTR}/t_{CK}) clock cycles. Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL.”

5.13.2 LPDDR2-N: Mode Register Write (cont'd)

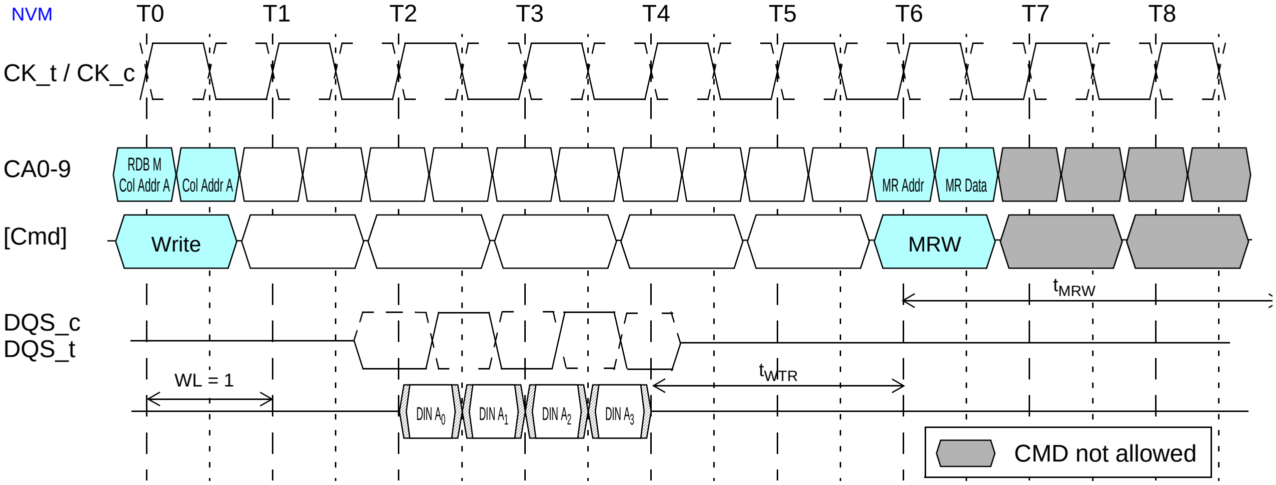


Figure 84 — LPDDR2-N: Burst Write Followed by MRW: WL = 1, BL = 4

NOTE 1 The minimum number of clock cycles from the burst write command to the Mode Register Write command is [WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})].

NOTE 2 The Mode Register Write Command period is t_{MRW}. No command (other than Nop) is allowed during this period.

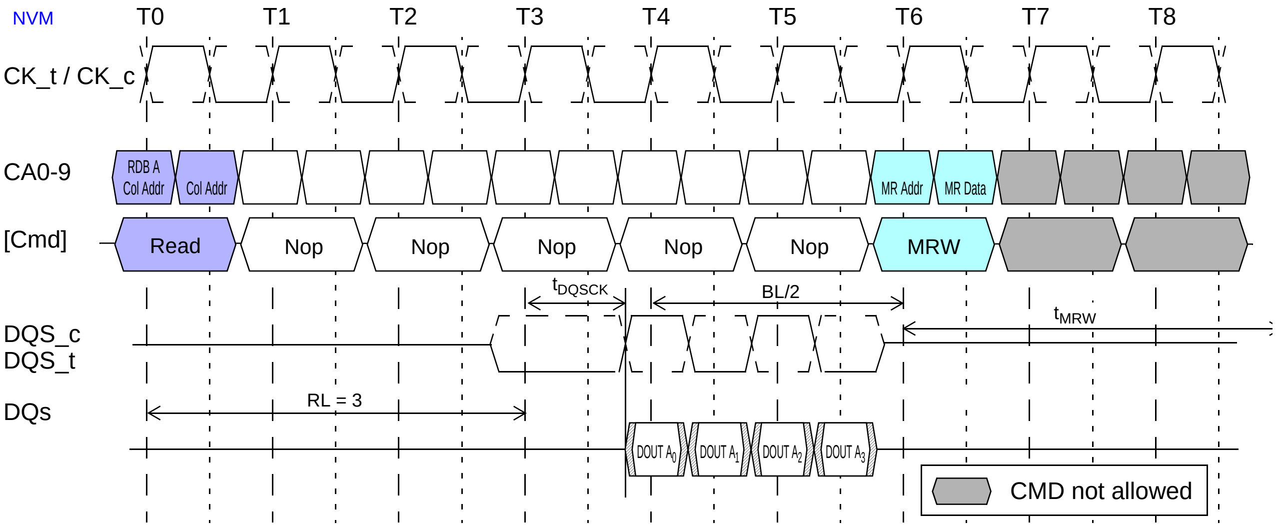


Figure 85 — LPDDR2-N: Burst Read followed by MRW: RL = 3, BL = 4

NOTE 1 The minimum number of clock cycles from the burst read command to the Mode Register Write command is [RL + RU(t_{DQSCK}/t_{CK}) + BL/2].

NOTE 2 The Mode Register Write Command period is t_{MRW}. No command (other than Nop) is allowed during this period.

5.13.2 LPDDR2-N: Mode Register Write (cont'd)

Table 59 — Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State		Command	Intermediate State		Next State	
SDRAM	NVM		SDRAM	NVM	SDRAM	NVM
All Banks Idle	All RBs idle	MRR	Mode Register Reading (All Banks Idle)	Mode Register Reading (All RBs Idle)	All Banks Idle	All RBs Idle
		MRW	Mode Register Writing (All Banks Idle)	Mode Register Writing (All RBs Idle)	All Banks Idle	All RBs Idle
		MRW (RESET)	Resetting (Device Auto-Init)	Device Auto-Init (Resetting)	All Banks Idle	All RBs Idle
Bank(s) Active	RB(s) Active	MRR	Mode Register Reading (Bank(s) Active)	Mode Register Reading (RB(s) Active)	Bank(s) Active	RB(s) Active
		MRW	Not Allowed	Mode Register Writing (RB(s) Active)	Not Allowed	All RBs Idle
		MRW (RESET)	Not Allowed	Device Auto-Init (Resetting)	Not Allowed	All RBs Idle

5.13.3 Mode Register Write Reset (MRW Reset)

Any MRW command issued to MRW63 initiates an MRW Reset. The MRW Reset command brings the device to the Device Auto-Initialization (Resetting) State in the Power-On Initialization sequence (step 3 in section 3.4.1). The MRW Reset command may be issued from the Idle state for LPDDR2-SX devices and the Idle or Active states for LPDDR2-N devices. This command resets all Mode Registers to their default values. In addition, for LPDDR2-N devices, this command ends all embedded operations and resets all Overlay Window registers to their default values. No commands other than NOP may be issued to the LPDDR2 device during the MRW Reset period ($\mathbf{t}_{INIT4}$). After MRW Reset, boot timings must be observed until the device initialization sequence is complete and the device is in the Idle state. Array data for LPDDR2-SX devices are undefined after the MRW Reset command.

For the timing diagram related to MRW Reset, refer to Figure 6 on page 21.

5.13.4 Mode Register Write ZQ Calibration Command

The MRW command is also used to initiate the ZQ Calibration command. The ZQ Calibration command is used to calibrate the LPDDR2 ouput drivers (RON) over process, temperature, and voltage. LPDDR2-S2 devices do not support ZQ Calibration and the ZQ Calibration command shall be ignored by these devices. LPDDR2-S4 and LPDDR2-N devices support ZQ Calibration.

There are four ZQ Calibration commands and related timings, tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT corresponds to the initialization calibration, tZQRESET for resetting ZQ setting to default, tZQCL is for long calibration, and tZQCS is for short calibration. See Mode Register 10 on page 30 for description on the command codes for the different ZQ Calibration commands.

The Initialization ZQ Calibration (ZQINIT) shall be performed for LPDDR2-S4 and LPDDR2-N devices. This Initialization Calibration achieves a RON accuracy of +/-15%. After initialization, the ZQ Long Calibration may be used to re-calibrate the system to a RON accuracy of +/-15%. A ZQ Short Calibration may be used periodically to compensate for temperature and voltage drift in the system.

The ZQReset Command resets the RON calibration to a default accuracy of +/-30% across process, voltage, and temperature. This command is used to ensure RON accuracy to +/-30% when ZQCS and ZQCL are not used.

One ZQCS command can effectively correct a minimum of 1.5% (ZQCorrection) of RON impedance error within tZQCS for all speed bins assuming the maximum sensitivities specified in the ‘Output Driver Voltage and Temperature Sensitivity’. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the LPDDR2 is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where TSens = max(dRONdT) and VSens = max(dRONdV) define the LPDDR2 temperature and voltage sensitivities.

For example, if TSens = 0.75% / ^{o}C, VSens = 0.20% / mV, Tdriftrate = 1 ^{o}C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

For LPDDR2-S4 devices, a ZQ Calibration command may only be issued when the device is in Idle state with all banks precharged. For LPDDR2-N devices, a ZQ Calibration command may only be issued when the device is in the Idle or Active states.

No other activities can be performed on the LPDDR2 data bus during the calibration period (tZQINIT, tZQCL, tZQCS). The quiet time on the LPDDR2 data bus helps to accurately calibrate RON. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ Resistor, only one device may be calibrating at any given time. After calibration is achieved, the LPDDR2 device shall disable the ZQ ball’s current consumption path to reduce power.

In systems that share the ZQ resistor between devices, the controller must not allow overlap of tZQINIT, tZQCS, or tZQCL between the devices. ZQ Reset overlap is allowed. If the ZQ resistor is absent from the system, ZQ shall be connected permanently to VDDCA. In this case, the LPDDR2 device shall ignore ZQ calibration commands and the device will use the default calibration settings (See “Output Driver DC Electrical Characteristics without ZQ Calibration” on page 165)

5.13.4 Mode Register Write ZQ Calibration Command (cont'd)

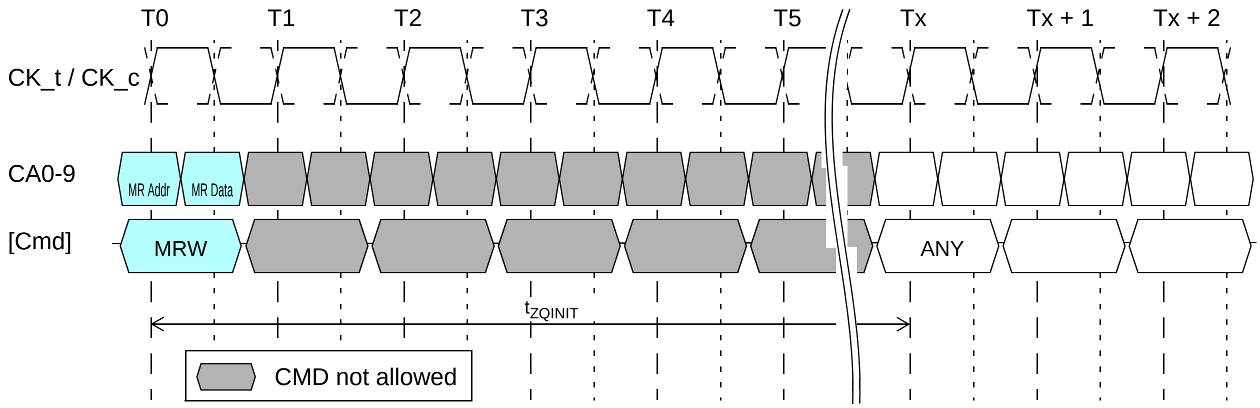


Figure 86 — ZQ Calibration Initialization timing example

NOTE 1: The ZQ Calibration Initialization period is t_{ZQINIT}. No command (other than Nop) is allowed during this period.
NOTE 2: CKE must be continuously registered HIGH during the calibration period.
NOTE 3: All devices connected to the DQ bus should be high impedance during the calibration process.

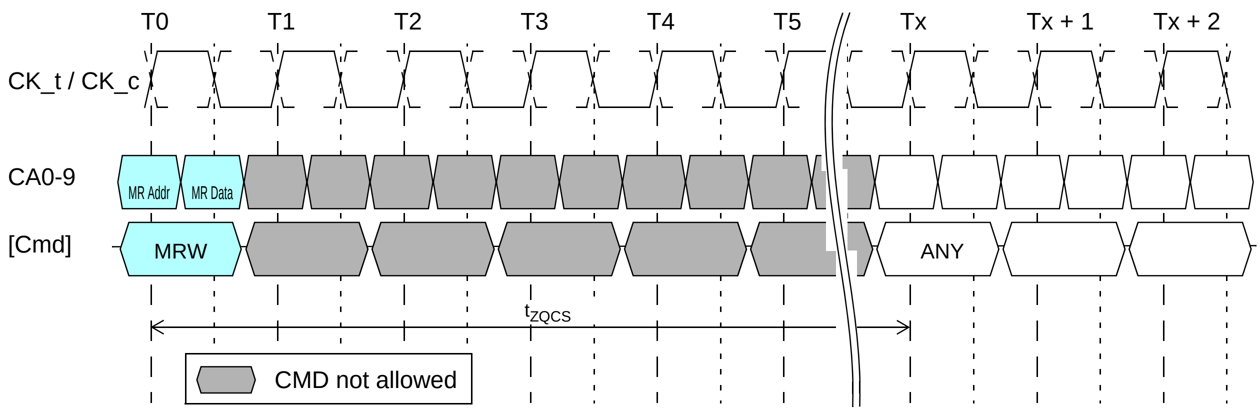


Figure 87 — ZQ Calibration Short timing example

NOTE 1: The ZQ Calibration Short period is t_{ZQCS}. No command (other than Nop) is allowed during this period.
NOTE 2: CKE must be continuously registered HIGH during the calibration period.
NOTE 3: All devices connected to the DQ bus should be high impedance during the calibration process.

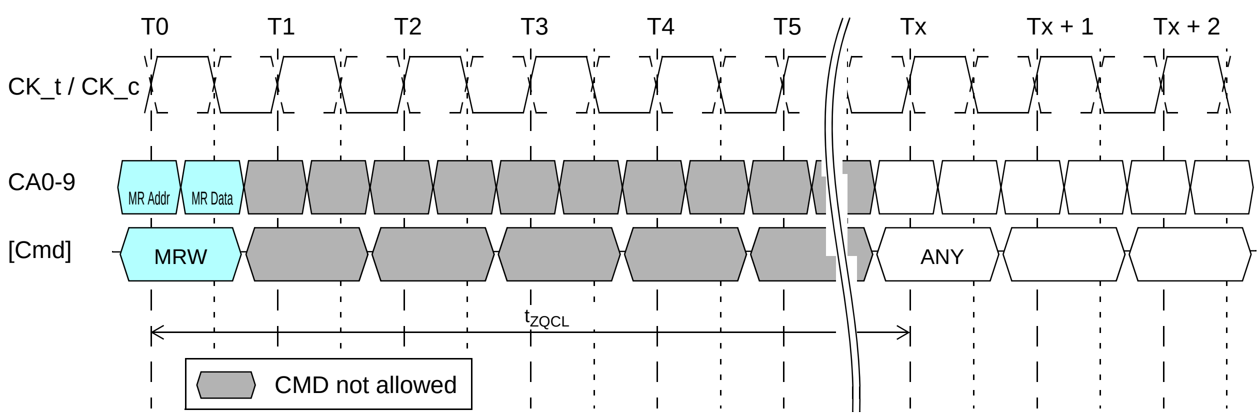


Figure 88 — ZQ Calibration Long timing example

NOTE 1 The ZQ Calibration Long period is t_{ZQCL}. No command (other than Nop) is allowed during this period.
NOTE 2 CKE must be continuously registered HIGH during the calibration period.
NOTE 3 All devices connected to the DQ bus should be high impedance during the calibration process.

5.13.4 Mode Register Write ZQ Calibration Command (cont'd)

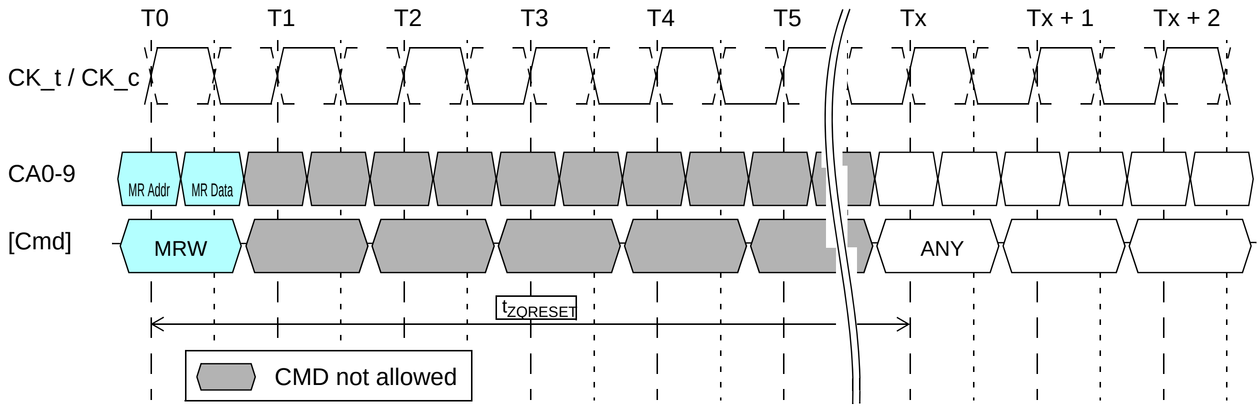


Figure 89 — ZQ Calibration Reset timing example

NOTE 1 The ZQ Calibration Reset period is $t_{ZQRESET}$. No command (other than Nop) is allowed during this peri
NOTE 2 CKE must be continuously registered HIGH during the calibration period.
NOTE 3 All devices connected to the DQ bus should be high impedance during the calibration process.

5.13.4.1 ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ Calibration function, a 240 Ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each LPDDR2 device or one resistor can be shared between multiple LPDDR2 devices if the ZQ calibration timings for each LPDDR2 device do not overlap. The total capacitive loading on the ZQ pin must be limited (See "Input/output capacitance" on page 168).

5.14 Power-down

For LPDDR2 SDRAM, power-down is synchronously entered when CKE is registered LOW and CS_n HIGH at the rising edge of clock. For LPDDR2 NVM, power-down is synchronously entered when CKE is registered LOW at the rising edge of clock. CKE must be registered HIGH in the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. CKE is allowed to go LOW while any of other operations such as row activation, preactive, precharge, autoprecharge, or refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power down.

For LPDDR2 SDRAM, if power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

For LPDDR2 NVM, if power-down occurs when all row buffers are idle, this mode is referred to as idle power-down; if power-down occurs when any row buffer is in the active state, this mode is referred to as active power-down.

Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, and CKE. In power-down mode, CKE must be maintained LOW while all other input signals are “Don’t Care”. CKE LOW must be maintained until t_{CKE} has been satisfied. V_{REF} must be maintained at a valid level during power down.

VDDQ may be turned off during power down. If VDDQ is turned off, then VREFDQ must also be turned off. Prior to exiting power down, both VDDQ and VREFDQ must be within their respective min/max operating ranges (See “Recommended DC Operating Conditions” on page 147).

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section “LPDDR2 SDRAM Refresh Requirements” on page 105, as no refresh operations are performed in power-down mode.

The power-down state is exited when CKE is registered HIGH. The controller shall drive CS_n HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until t_{CKE} has been satisfied. A valid, executable command can be applied with power-down exit latency, t_{XP} after CKE goes HIGH. Power-down exit latency is defined in the timing parameter table of this standard.

SDRAM

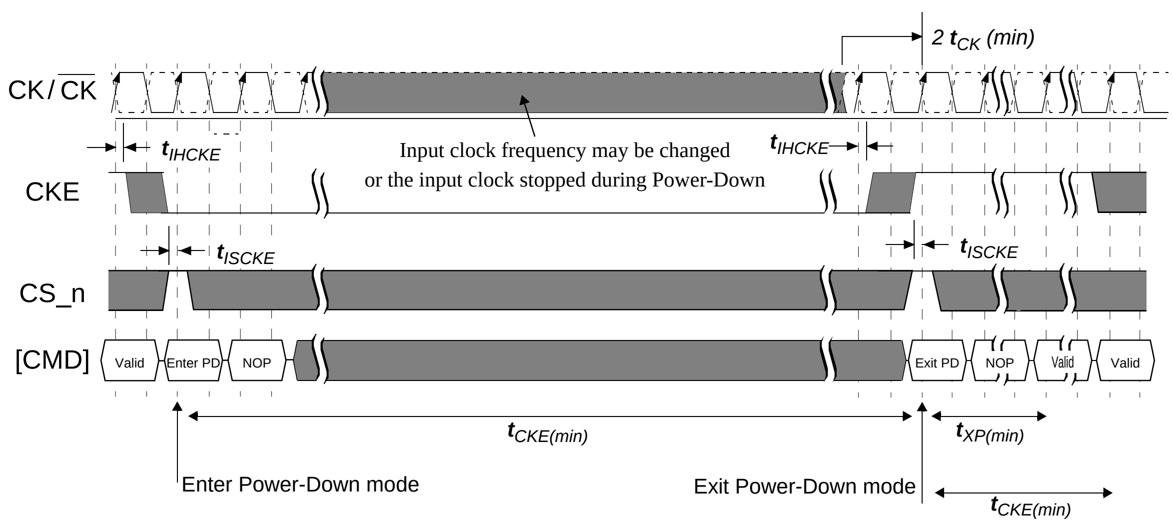


Figure 90 — LPDDR2-SX: Basic power down entry and exit timing diagram

NOTE 1 Input clock frequency may be changed or the input clock stopped during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minmum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

5.14 Power-down (cont'd)

NVM

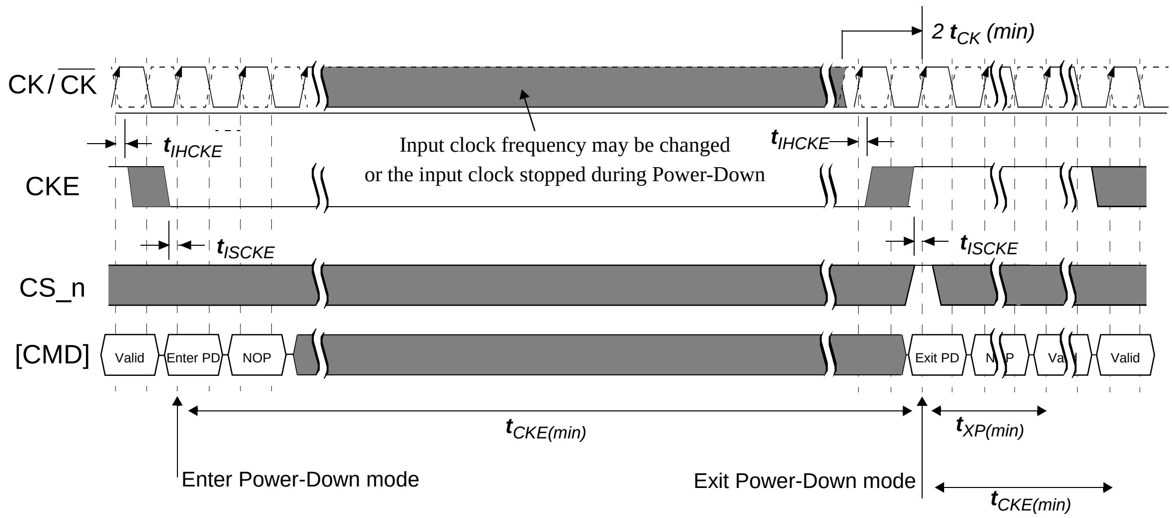


Figure 91 — LPDDR2-N: Basic power down entry and exit timing diagram

NOTE 1 Input clock frequency may be changed or the input clock stopped during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minmum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

NOTE 2 CS_n is "do not care" for entry into power-down for NVM.

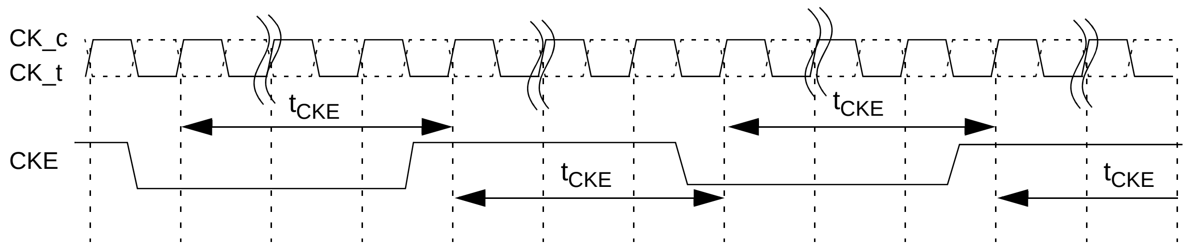
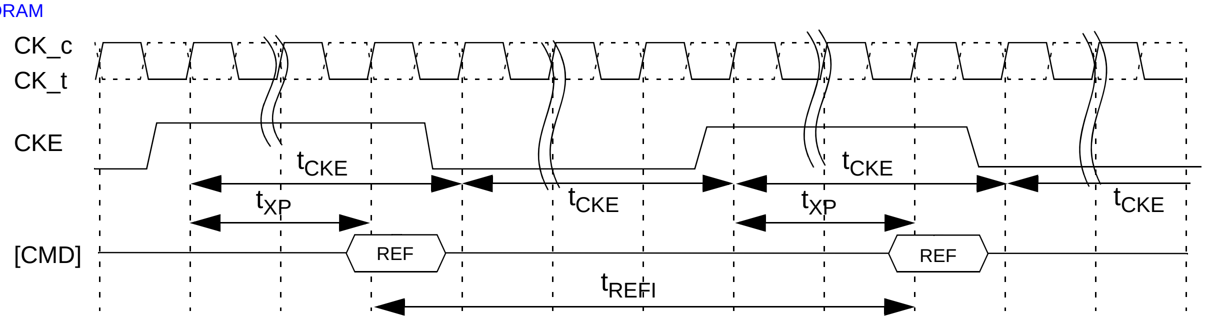


Figure 92 — Example of CKE intensive environment

SDRAM



NOTE 1 The pattern shown above can repeat over a long period of time. With this pattern, LPDDR2 SDRAM guarantees all AC and DC timing & voltage specifications with temperature and voltage drift

Figure 93 — REF to REF timing with CKE intensive environment for LPDDR2 SDRAM

5.14 Power-down (cont'd)

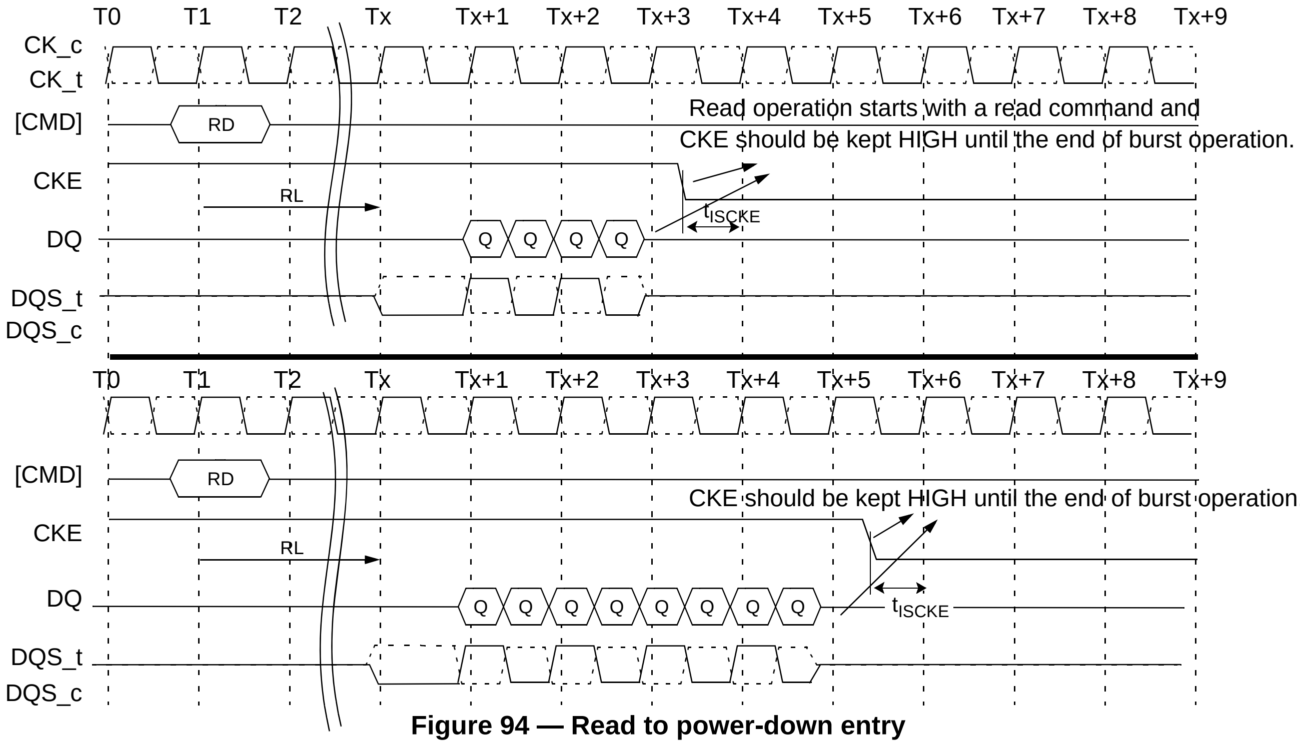


Figure 94 — Read to power-down entry

NOTE 1 CKE may be registered LOW RL + RU($t_{DQSCK(MAX)}/t_{CK}$) + BL/2 + 1 clock cycles after the clock on which the Read command is registered.

SDRAM

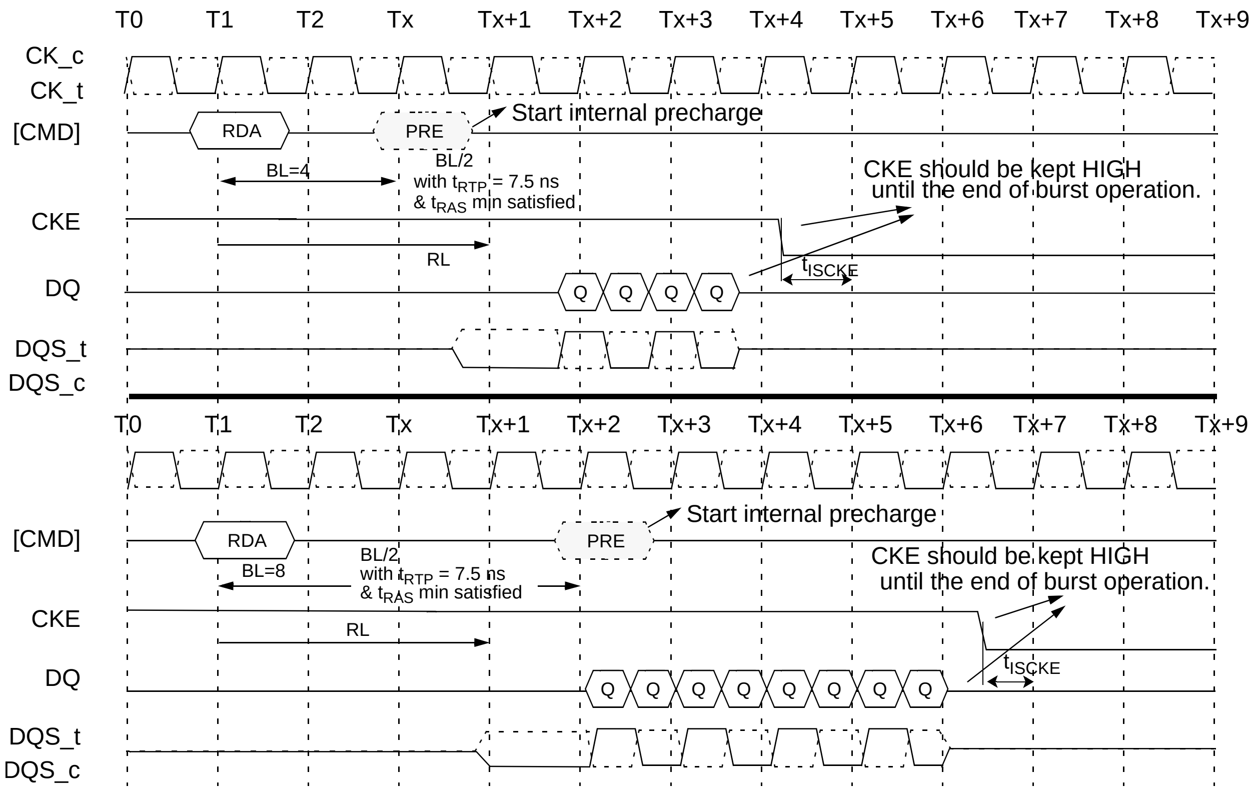


Figure 95 — LPDDR2 SDRAM Read with autoprecharge to power-down entry

NOTE 1 CKE may be registered LOW RL + RU(t_{DQSCK}/t_{CK})+ BL/2 + 1 clock cycles after the clock on which the Read command is registered.

5.14 Power-down (cont'd)

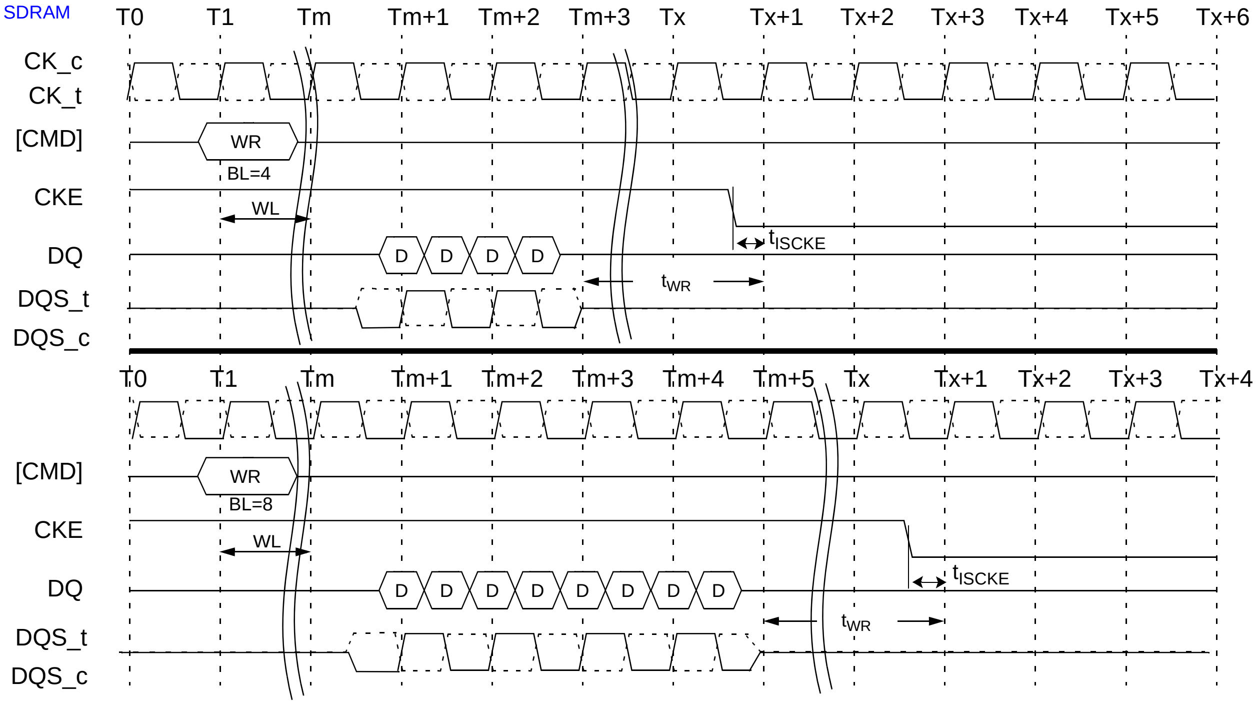


Figure 96 — Write to power-down entry

NOTE 1 CKE may be registered LOW WL + 1 + BL/2 + RU(t_{WR}/t_{CK})clock cycles after the clock on which the Write command is registered.

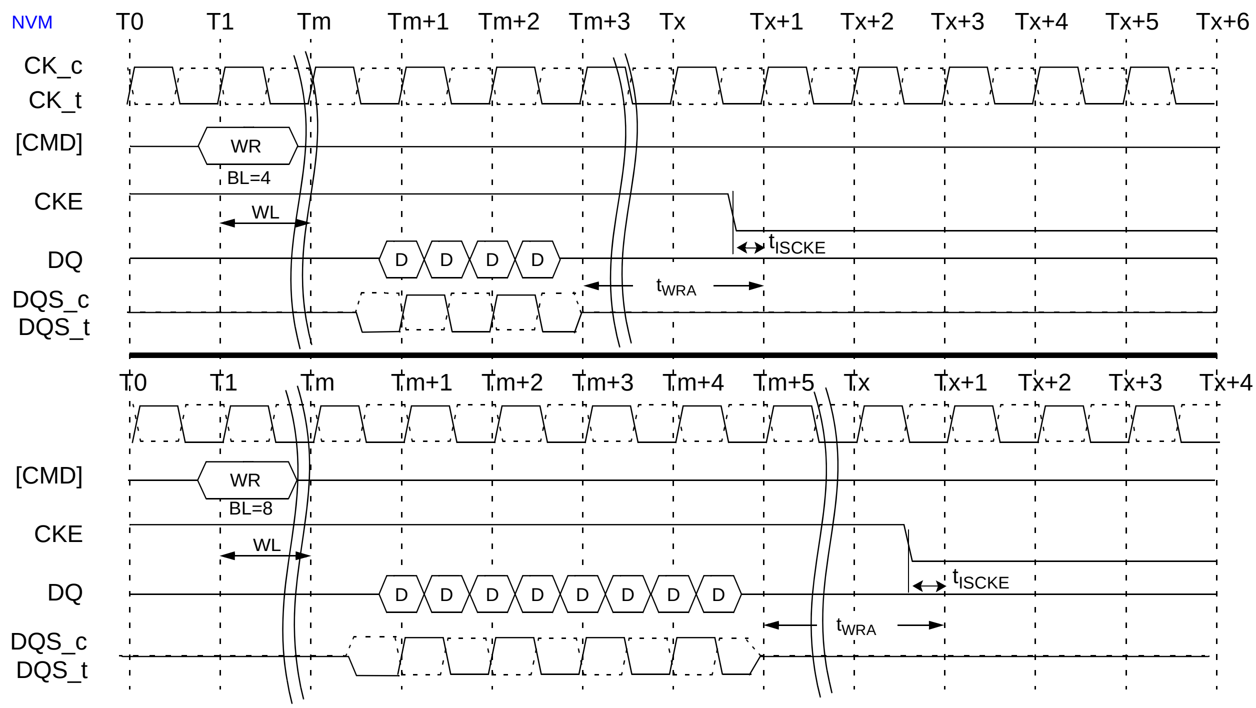


Figure 97 — Write to power-down entry

NOTE 1 CKE may be registered LOW WL + 1 + BL/2 + RU(t_{WRA}/t_{CK})clock cycles after the clock on which the Write command is registered.

5.14 Power-down (cont'd)

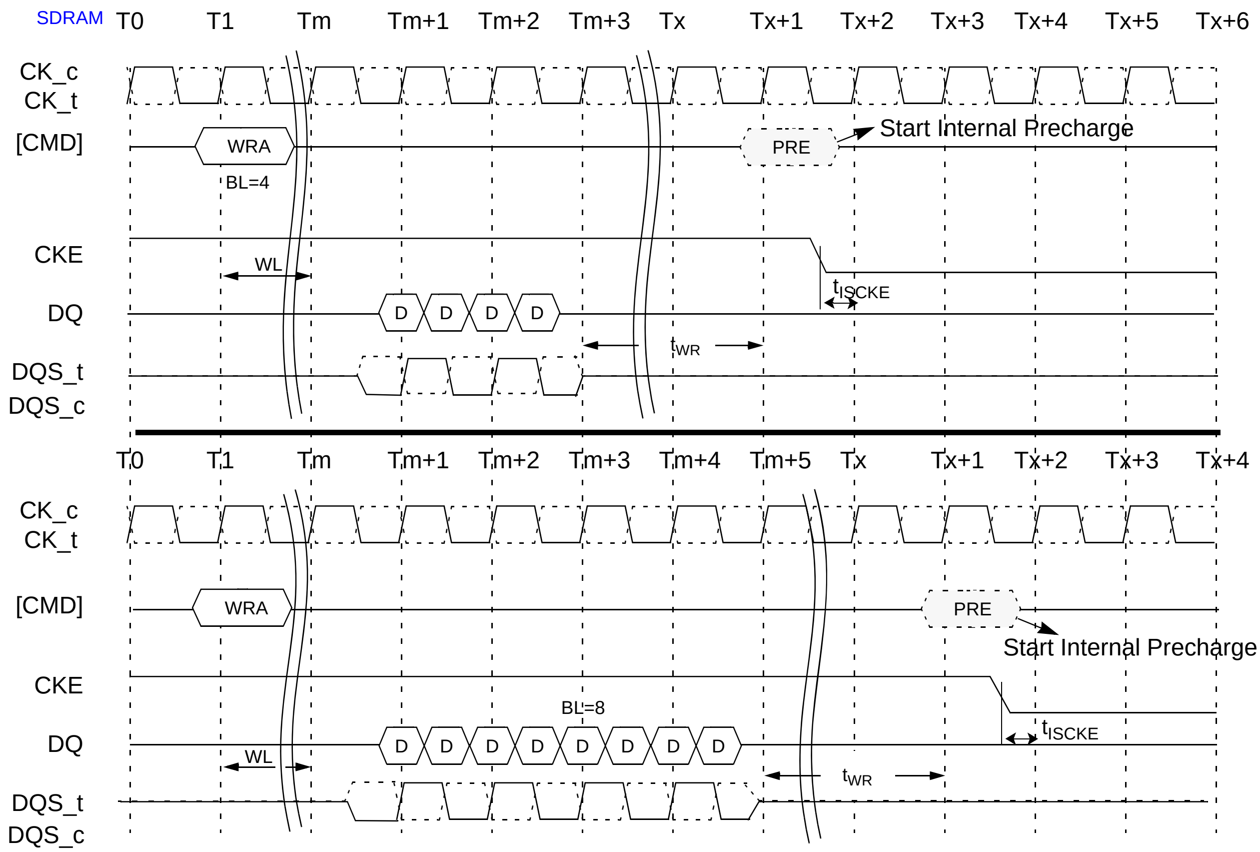


Figure 98 — LPDDR2-SX: Write with autoprecharge to power-down entry

NOTE 1 CKE may be registered LOW WL + 1 + BL/2 + RU(t_{WR}/t_{CK}) + 1 clock cycles after the Write command is registered.

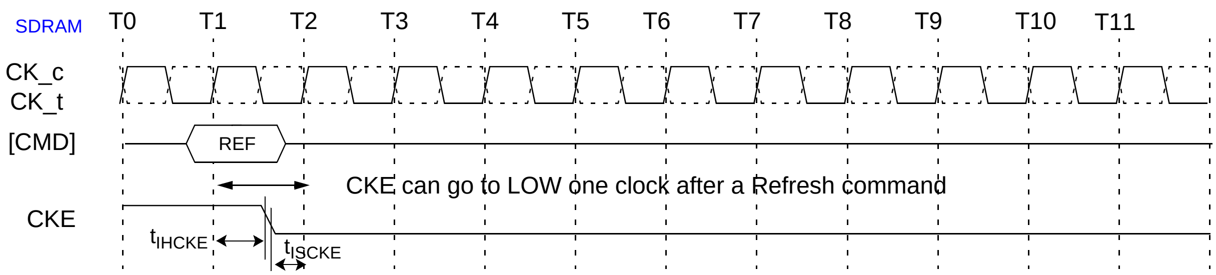


Figure 99 — LPDDR2-SX: Refresh command to power-down entry

NOTE 1 CKE may go LOW t_{IHCKE} after the clock on which the Refresh command is registered.

5.14 Power-down (cont'd)

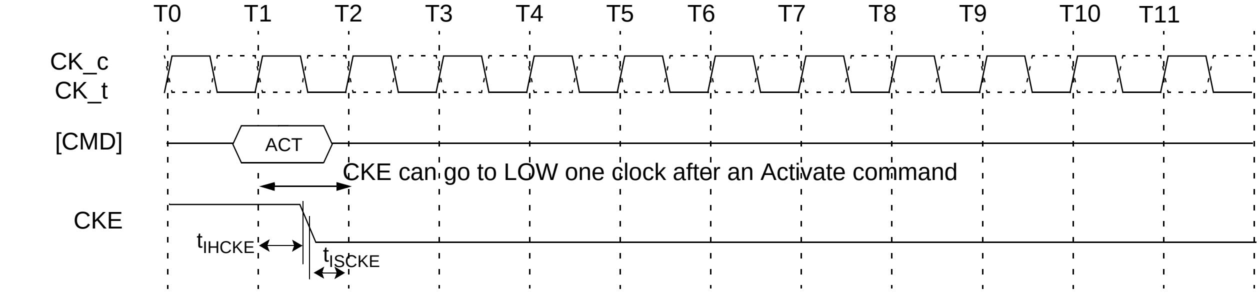


Figure 100 — Activate command to power-down entry

NOTE 1 CKE may go LOW t_{IHCKE} after the clock on which the Activate command is registered.

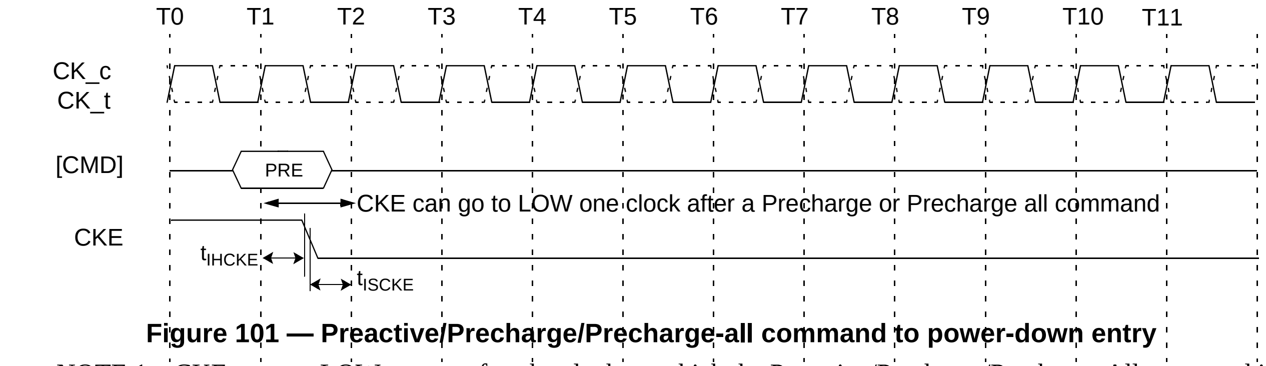


Figure 101 — Preactive/Precharge/Precharge-all command to power-down entry

NOTE 1 CKE may go LOW t_{IHCKE} after the clock on which the Preactive/Precharge/Precharge-All command is registered.

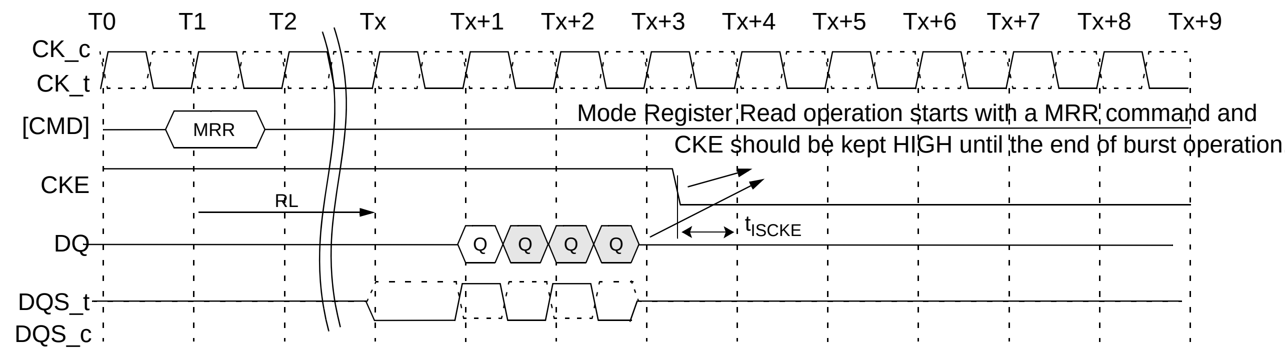


Figure 102 — Mode Register Read to power-down entry

NOTE 1 CKE may be registered LOW RL + RU(t_{DQSCK}/t_{CK})+ BL/2 + 1 clock cycles after the clock on which the Mode Register Read command is registered.

5.14 Power-down (cont'd)

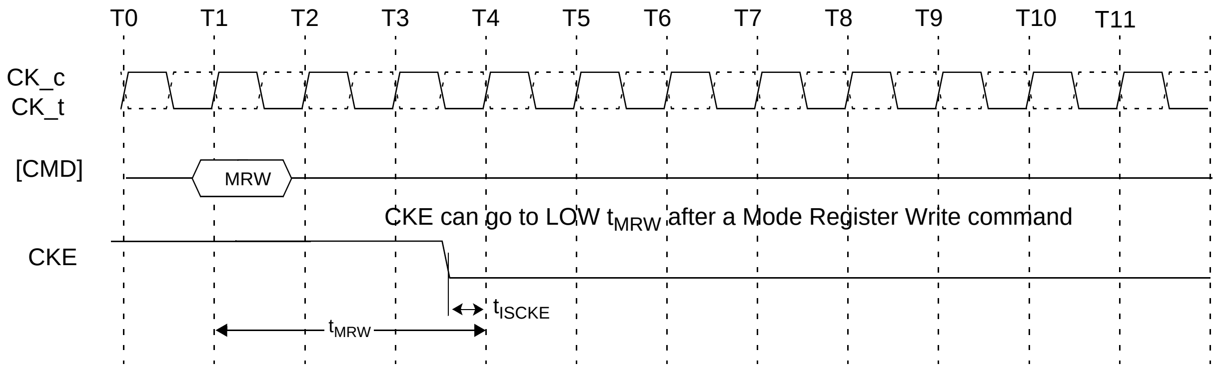


Figure 103 — MRW command to power-down entry

NOTE 1 CKE may be registered LOW t_{MRW} after the clock on which the Mode Register Write command is

5.15 LPDDR2-SX: Deep Power-Down

Deep Power-Down is entered when CKE is registered LOW with CS_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. CKE is allowed to go LOW while any of other operations such as row activation, precharge, autoprecharge, or Refresh is in progress, but deep power-down IDD spec will not be applied until finishing those operations.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. All power supplies must be within specified limits prior to exiting Deep Power-Down. VrefDQ and VrefCA may be at any level within minimum and maximum levels (see “Absolute Maximum DC Ratings” on page 146). However prior to exiting Deep Power-Down, Vref must be within specified limits (See “Recommended DC Operating Conditions” on page 147).

The contents of the SDRAM may be lost upon entry into Deep Power-Down mode.

The Deep Power-Down state is exited when CKE is registered HIGH, while meeting t_{ISCKE} with a stable clock input. The SDRAM must be fully re-initialized as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence.

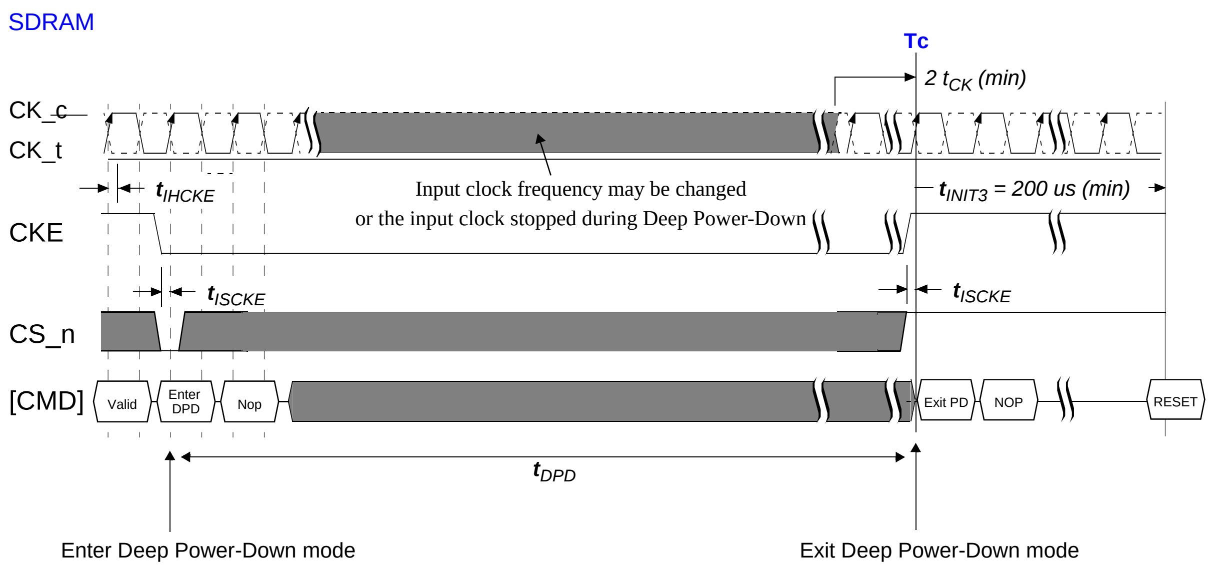


Figure 104 — LPDDR2-SX: Deep power down entry and exit timing diagram

NOTE 1 Initialization sequence may start at any time after Tc.

NOTE 2 t_{INIT2}, t_{INIT3}, and Tc refer to timings in the LPDDR2 initialization sequence. For more detail, see “Power-up, Initialization, and Power-Off” on page 19.

NOTE 3 Input clock frequency may be changed or the input clock stopped during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minmum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

5.16 Input clock stop and frequency change

LPDDR2 devices support input clock frequency change during CKE LOW under the following conditions:

- $t_{CK(MIN)}$ and $t_{CK(MAX)}$ are met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate, Preactive, or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions (t_{RCD}, t_{RP}) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE LOW under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Preactive, or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions (t_{RCD}, t_{RP}) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR2 devices support input clock frequency change during CKE HIGH under the following conditions:

- $t_{CK(MIN)}$ and $t_{CK(MAX)}$ are met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- Any Activate, Read, Write, Preactive, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions (t_{RCD}, t_{WR}, t_{WRA}, t_{RP}, t_{MRW}, t_{MRR}, etc.) have been met prior to changing the frequency;
- CS_n shall be held HIGH during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- The LPDDR2 device is ready for normal operation after the clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2tCK + tXP.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE HIGH under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- CS_n shall be held HIGH during clock clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Read, Write, Preactive, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions (t_{RCD}, t_{WR}, t_{WRA}, t_{RP}, t_{MRW}, t_{MRR}, etc.) have been met prior to stopping the clock;
- The LPDDR2 device is ready for normal operation after the clock is restarted and satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2tCK + tXP.

5.17 No Operation command

The purpose of the No Operation command (NOP) is to prevent the LPDDR2 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. CS_n HIGH at the clock rising edge N.

2. CS_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

5.18 Truth tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

5.18.1 Command Truth Table

Table 60 — Command Truth Table

		SDR Command Pins			DDR CA pins (10)										
SDRAM Command	NVM Command	CKE CK_t(n-1)	CKE CK_t(n)	CS_N	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK EDGE
MRW	MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
					MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
					MA6	MA7	X								↓
Refresh (per bank)[11]	-	H	H	L	L	L	H	L	X						↑
					X										↓
Refresh (all bank)	-	H	H	L	L	L	H	H	X						↑
					X										↓
Enter Self Refresh	Enter Power Down	H	L	L	L	L	H	X							↑
					X										↓
Activate (bank)	Activate (row buffer)	H	H	L	L	H	R8/a15	R9/a16	R10/a17	R11/a18	R12/a19	BA0	BA1	BA2	↑
					R0/a5	R1/a6	R2/a7	R3/a8	R4/a9	R5/a10	R6/a11	R7/a12	R13/a13	R14/a14	↓
Write (bank)	Write (RDB)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
					AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Read (bank)	Read (RDB)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
					AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Precharge (bank)	Preactive (RAB)	H	H	L	H	H	L	H	AB/a30	X/a31	X/a32	BA0	BA1	BA2	↑
					X/a20	X/a21	X/a22	X/a23	X/a24	X/a25	X/a26	X/a27	X/a28	X/a29	↓
BST	BST	H	H	L	H	H	L	L	X						↑
					X										↓
Enter Deep Power Down	Enter Power Down	H	L	L	H	H	L	X							↑
					X										↓
NOP	NOP	H	H	L	H	H	H	X							↑
					X										↓
Maintain PD, SREF, DPD (NOP)	Maintain PD, SREF, DPD (NOP)	L	L	L	H	H	H	X							↑
					X										↓
NOP	NOP	H	H	H	X										↑
					X										↓
Maintain PD, SREF, DPD (NOP)	Maintain PD, SREF, DPD (NOP)	L	L	H	X										↑
					X										↓
Enter Power Down	Enter Power Down	H	L	H	X										↑
					X										↓
Exit PD, SREF, DPD	Exit Power Down	L	H	H	X										↑
					X										↓

5.18.1 Command Truth Table (cont'd)

Notes to Table 60

NOTE 1 All LPDDR2 commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.

NOTE 2 For LPDDR2 SDRAM, Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For LPDDR2 NVM, BA0, BA1, BA2 determine a row buffer.

NOTE 3 AP is significant only to SDRAM. AP is do-not-care for NVM.

NOTE 4 AP "high" during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.

NOTE 5 "X" means "H or L (but a defined logic level)"

NOTE 6 Self refresh exit and Deep Power Down exit are asynchronous.

NOTE 7 VREF must be between 0 and VDDQ during Self Refresh and Deep Power Down operation.

NOTE 8 CAxr refers to command/address bit "x" on the rising edge of clock.

NOTE 9 CAxf refers to command/address bit "x" on the falling edge of clock.

NOTE 10 CS_n and CKE are sampled at the rising edge of clock.

NOTE 11 Per Bank Refresh is only allowed in devices with 8 banks.

NOTE 12 The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

5.19 LPDDR2-SDRAM Truth Tables

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the Banks.

Table 61 — LPDDR2-SX: CKE Table

Device Current State*3	CKE_{n-1} *1	CKE_n *1	CS_n*2	Command n*4	Operation n*4	Device Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6, 9
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6, 9
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6, 9, 12
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7, 10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	
	H	L	L	Enter Self-Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Deep Power Down	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
	H	H	Refer to the Command Truth Table				

NOTE 1 “CKE_n” is the logic state of CKE at clock rising edge n; “CKE_{n-1}” was the state of CKE at the previous clock edge.
NOTE 2 “CS_n” is the logic state of CS_n at the clock rising edge n;
NOTE 3 “Current state” is the state of the LPDDR2 device immediately prior to clock edge n.
NOTE 4 “Command n” is the command registered at clock edge N, and “Operation n” is a result of “Command n”.
NOTE 5 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
NOTE 6 Power Down exit time (t_{XP}) should elapse before a command other than NOP is issued.
NOTE 7 Self-Refresh exit time (t_{XSR}) should elapse before a command other than NOP is issued.
NOTE 8 The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
NOTE 9 The clock must toggle at least twice during the t_{XP} period.
NOTE 10 The clock must toggle at least twice during the t_{XSR} time.
NOTE 11 'X' means ‘Don’t care’.
NOTE 12 Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.

5.19 LPDDR2-SDRAM Truth Tables (cont'd)

Table 62 — Current State Bank n - Command to Bank n

Current State	Command	Operation	Next State	NOTES
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing(All Bank)	7
	MRW	Load value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	7, 8
	Precharge	Deactivate row in bank or banks	Precharging	9, 15
Row Active	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10, 11
	Write	Select column, and start write burst	Writing	10, 11, 12
	BST	Read burst terminate	Active	13
Writing	Write	Select column, and start new write burst	Writing	10, 11
	Read	Select column, and start read burst	Reading	10, 11, 14
	BST	Write burst terminate	Active	13
Power On	Reset	Begin Device Auto-Initialization	Resetting	7, 9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE 1 The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Power Down.

NOTE 2 All states and sequences not shown are illegal or reserved.

NOTE 3 Current State Definitions:

Idle: The bank or banks have been precharged, and tRP has been met.

Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accessesare in progress.

Reading: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

Writing: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

NOTE 4 The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and Table 2, and according to Table 3.

Precharging: starts with the registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

Row Activating: starts with registration of an Activate command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'Active' state.

Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.

Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

5.19 LPDDR2-SDRAM Truth Tables (cont'd)

Notes (cont'd) to Table 62

NOTE 5 The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.

Refreshing (Per Bank): starts with registration of an Refresh (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.

Refreshing (All Bank): starts with registration of an Refresh (All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.

Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.

Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.

Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.

MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.

Precharging All: starts with the registration of a Precharge-All command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

NOTE 6 Bank-specific; requires that the bank is idle and no bursts are in progress.

NOTE 7 Not bank-specific; requires that all banks are idle and no bursts are in progress.

NOTE 8 Not bank-specific reset command is achieved through Mode Register Write command.

NOTE 9 This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.

NOTE 10 A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.

NOTE 11 The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.

NOTE 12 A Write command may be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.

NOTE 13 Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank.

NOTE 14 A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.

NOTE 15 If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

5.19 LPDDR2-SDRAM Truth Tables (cont'd)

Table 63 — Current State Bank n - Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	NOTES
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	7
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	10, 11, 13
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8, 14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8, 16
	Write	Select column, and start write burst to Bank m	Writing	8
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15
	Write	Select column, and start write burst to Bank m	Writing	8, 14, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15, 16
	Write	Select column, and start write burst to Bank m	Writing	8, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Power On	Reset	Begin Device Auto-Initialization	Resetting	12, 17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE 1 The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.

NOTE 2 All states and sequences not shown are illegal or reserved.

NOTE 3 Current State Definitions:

Idle: the bank has been precharged, and tRP has been met.

Active: a row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

Reading: a Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

Writing: a Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

NOTE 4 Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.

NOTE 5 A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.

5.19 LPDDR2-SDRAM Truth Tables (cont'd)

Notes (cont'd) to Table 63

NOTE 6 The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:

Idle MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Idle state.

Resetting MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Resetting state.

Active MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Active state.

MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Idle state.

NOTE 7 t_{RRD} must be met between Activate command to Bank n and a subsequent Activate command to Bank m.

NOTE 8 Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.

NOTE 9 This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for pre-charging.

NOTE 10 MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when t_{RCD} is met.)

NOTE 11 MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when t_{RP} is met.

NOTE 12 Not bank-specific; requires that all banks are idle and no bursts are in progress.

NOTE 13 The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon t_{RCD} and t_{RP} respectively.

NOTE 14 A Write command may be applied after the completion of the Read burst, otherwise a BST must be issued to end the Read prior to asserting a Write command.

NOTE 15 Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions in Table 51 on page 102 and Table 52 on page 103 are followed.

NOTE 16 A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.

NOTE 17 Reset command is achieved through Mode Register Write command.

NOTE 18 BST is allowed only if a Read or Write burst is ongoing.

5.20 LPDDR2-N: Truth Tables

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the Row Buffers.

Table 64 on page 142 describes Power Down transitions for a LPDDR2-NVM. If the Enter Power Down command is issued when all Row Buffers are Idle the device goes into the Idle Power Down state. However, if the Enter Power Down command is issued when one or more Row Buffers are Active, the device goes into the Active Power Down state. CKE shall be held low to maintain the Power Down state. When CKE is driven high with CS_n high the device exits the Power Down State. For additional details on entering and exiting power down, please refer to section “Power-down” on page 125.

Table 64 — LPDDR2-N: CKE Table

<table>
<tr><th colspan="2">Row Buffer Current State*3</th><th>Device Current State*4</th><th>CKE$_{n-1}$*1</th><th>CKE$_n$*1</th><th>CS_n*2</th><th>Command n*5</th><th>Operation n*5</th><th>Row Buffer Next State</th><th>Device Next State</th><th>Notes</th></tr>
<tr><td>All</td><td>Resetting</td><td>Resetting</td><td>H</td><td>L</td><td>X</td><td>ENTER POWER DOWN</td><td>Enter in Resetting Power Down</td><td>Resetting Power Down</td><td>Resetting Power Down</td><td>10</td></tr>
<tr><td>All</td><td>Idle</td><td>Idle</td><td>H</td><td>L</td><td>X</td><td>ENTER POWER DOWN</td><td>Enter in Idle Power Down</td><td>Idle Power Down</td><td>Idle Power Down</td><td>10</td></tr>
<tr><td>RB$_j$</td><td>Active</td><td rowspan="2">Not Power Down</td><td rowspan="2">H</td><td rowspan="2">L</td><td rowspan="2">X</td><td rowspan="2">ENTER POWER DOWN</td><td rowspan="2">Enter in Active Power Down</td><td>Active Power Down</td><td rowspan="2">Active Power Down</td><td rowspan="2">10,11</td></tr>
<tr><td>RB$_k$</td><td>Idle</td><td>Idle Power Down</td></tr>
<tr><td>All</td><td>Resetting Power Down</td><td>Resetting Power Down</td><td>L</td><td>L</td><td>X</td><td>X</td><td>Maintain Resetting Power Down</td><td>Resetting Power Down</td><td>Resetting Power Down</td><td>9</td></tr>
<tr><td>All</td><td>Idle Power Down</td><td>Idle Power Down</td><td>L</td><td>L</td><td>X</td><td>X</td><td>Maintain Idle Power Down</td><td>Idle Power Down</td><td>Idle Power Down</td><td>9</td></tr>
<tr><td>RB$_j$</td><td>Active Power Down</td><td rowspan="2">Active Power Down</td><td rowspan="2">L</td><td rowspan="2">L</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">Maintain Active Power Down</td><td>Active Power Down</td><td rowspan="2">Active Power Down</td><td rowspan="2">9,11</td></tr>
<tr><td>RB$_k$</td><td>Idle Power Down</td><td>Idle Power Down</td></tr>
<tr><td>All</td><td>Resetting Power Down</td><td>Resetting Power Down</td><td>L</td><td>H</td><td>H</td><td>EXIT POWER DOWN</td><td>Exit Resetting Power Down</td><td>Resetting</td><td>Resetting</td><td>7,8</td></tr>
<tr><td>All</td><td>Idle Power Down</td><td>Idle Power Down</td><td>L</td><td>H</td><td>H</td><td>EXIT POWER DOWN</td><td>Exit Idle Power Down</td><td>Idle</td><td>Idle</td><td>7,8</td></tr>
<tr><td>RB$_j$</td><td>Active Power Down</td><td rowspan="2">Active Power Down</td><td rowspan="2">L</td><td rowspan="2">H</td><td rowspan="2">H</td><td rowspan="2">EXIT POWER DOWN</td><td rowspan="2">Exit Active Power Down</td><td>Active</td><td rowspan="2">Not Power Down</td><td rowspan="2">7,8,11</td></tr>
<tr><td>RB$_k$</td><td>Idle Power Down</td><td>Idle</td></tr>
</table>

NOTE 1 “CKE$_n$” is the logic state of CKE at clock rising edge n; “CKE$_{n-1}$” was the state of CKE at the previous clock rising edge.

NOTE 2 “CS_n” is the logic state of CS_n at clock rising edge n;

NOTE 3 “Row Buffer Current State” is the state of a particular Row Buffer immediately prior to clock cycle n.

NOTE 4 “Device Current State” is the state of LPDDR2-NVM immediately prior to clock cycle n.

NOTE 5 “Command n” is the command registered at clock cycle n, and “Operation n” is the result of “Command n”.

NOTE 6 All states and sequences not shown are illegal or reserved, unless explicitly described elsewhere in this standard.

NOTE 7 Power Down exit time (t_{XP}) should elapse before a command other than NOP is issued.

NOTE 8 The clock must toggle at least twice during the t_{XP} period.

NOTE 9 Clock frequency may be reduced, and/or the clock may be stopped, during ‘Idle Power Down’, ‘Resetting Power Down’, or ‘Active Power Down’ states.

NOTE 10 Power Down may not be entered while Read, Write, Mode Register Read, Mode Register Write, or Preactive operations are in progress. A Power Down command shall be followed by a NOP command.

NOTE 11 RB$_j$ and RB$_k$ refer to different Row Buffer pairs, (j) and (k).

5.20 LPDDR2-N: Truth Tables (cont'd)

Table 65 on page 143 shows the transition from the current state to the next state of a given Row Buffer due to command issued on the same Row Buffer.

Only allowed commands are shown, all other commands are illegal or reserved for the given Row Buffer state.

For the state definition refer to section LPDDR2-NVM state diagram.

Table 65 — Current State Row Buffer n - Command to Row Buffer n

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current State	
Idle	PREACTIVE	Load RAB	Preactivating	
	ACTIVATE	Select RAB & RDB, and activate RDB	Active	
	MRW	Load value to Mode Register	MR Writing	
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	6
Active	PREACTIVE	Load RAB	Preactivating	
	ACTIVATE	Select RAB & RDB, and activate RDB	Active	7
	READ	Select RDB & column, and start read burst	Reading	
	WRITE	Select RDB & column, and start write burst	Writing	
	MRW	Load value to Mode Register	MR Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	6
Reading	READ	Select RDB & column, and start new read burst	Reading	
	BST	Read burst terminate	Active	4
Writing	BST	Write burst terminate	Active	4
	WRITE	Select RDB & column, and start new write burst	Writing	
Power On	Reset	Begin Device Auto-Initialization	Resetting	6
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE 1 The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XP} has been met if the previous state was Power Down.

NOTE 2 The following states must not be interrupted by a command issued to the same Row Buffer. NOP commands or allowable commands to other Row Buffer should be issued on any clock cycle occurring during these states.

Preactivating: starts with the registration of a Preactive command and ends when t_{RP} is met. The Row Buffer will return to the Idle state once t_{RP} is satisfied and any ongoing Read or Write operation is complete.

Row Activating: starts with registration of an Activate command and ends when t_{RCD} is met. Once t_{RCD} is met, the Row Buffer will be in the Row Active state.

NOTE 3 The following states must not be interrupted by any executable command; NOP commands must be applied to each clock cycle during these states.

Idle MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the Row Buffer will be in the Idle state.
Resetting MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the Row Buffer will be in the Resetting state.
Active MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the Row Buffer will be in the Active state.
MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the Row Buffer will be in the Idle state.

NOTE 4 BURST TERMINATE command affects the read/write burst started by the most recent READ/WRITE command.
NOTE 5 Reset command is achieved through MODE REG. WRITE command. Reset command sets all Row Address Buffers to 0x0000.
NOTE 6 t_{RC} must be met between Activate command to Row Buffer n and subsequent Activate command to Row Buffer n.

5.20 LPDDR2-N: Truth Tables (cont'd)

Given the state of a Row Buffer (n), Table 66 on page 144 shows allowed commands to another Row Buffer (m), and the corresponding next state. Only allowed commands are shown, all other commands are illegal or reserved for the given Row Buffer state, unless explicitly described elsewhere in this standard.

For the state definition refer to section LPDDR2-NVM state diagram.

Table 66 — Current State Row Buffer n - Command to Row Buffer m

Current State of Row Buffer n	Command for Row Buffer m	Operation	Next State for Row Buffer m	Notes
Any	NOP	Continue previous operation	Current State of Row Buffer m	
Idle	Any	Any command allowed to Row Buffer m	-	9
Row Activating, Active, or Preactivating	ACTIVATE	Select RABm & RDBm, and activate row in RDB m	Active	6
	READ	Select RDBm & column, and start read burst from RDBm	Reading	
	BST	Read or Write burst terminate an ongoing Read/Write from/to Row Buffer m	Active	3,9
	WRITE	Select RDBm & column, and start write burst to RDBm	Writing	
	PREACTIVE	Load RABm	Preactivating	
	MRW	Load value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	7, 8
	Reset	Begin Device Auto-Initialization	Resetting	5
Reading	READ	Select RDBm & column, and start read burst from RDBm	Reading	
	ACTIVATE	Select RABm & RDBm, and activate row in RDB m	Active	
	PREACTIVE	Load RABm	Preactivating	
Writing	WRITE	Select RDBm & column, and start write burst to RDBm	Writing	
	ACTIVATE	Select RABm & RDBm, and activate row in RDB m	Active	
	PREACTIVE	Load RABm	Preactivating	
Power On	Reset	Begin Device Auto-Initialization	Resetting	5
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE 1 The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XP} has been met if the previous state was Power Down.

NOTE 2 The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:

Idle MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the Row Buffer will be in the Idle state.

Resetting MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the Row Buffer will be in the Resetting state.

Active MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the Row Buffer will be in the Active state.

MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, all Row Buffers will be in the Idle state.

NOTE 3 BURST TERMINATE command affects the read/write burst started by the most recent READ/WRITE command.

NOTE 4 Reset command is achieved through MODE REGISTER WRITE command. Reset command sets all Row Address Buffers to 0x0000.

NOTE 5 t_{RRD} must be met between Activate command to Row Buffer n and a subsequent Activate command to Row Buffer m.

NOTE 6 MRR is allowed during the Row Activating state and MRW is prohibited during the Row Activating state. (Row Activating starts with registration of an Activate command and ends when t_{RCD} is met.)

NOTE 7 The next state for Row Buffer m depends on the current state of Row Buffer m (Idle, Row Activating, or Active). Note that the state may be in transition when a MRR is issued. Therefore, if Row Buffer m is in the Row Activating state, the next state may be Active dependent upon tRCD.

NOTE 8 BST is allowed only if a Read or Write burst is ongoing.

5.21 Data Mask Truth Table

Table 67 on page 145 provides the data mask truth table.

Table 67 — DM truth table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

NOTE 1 Used to mask write data, provided coincident with the corresponding data.

6 Absolute Maximum Ratings

6.1 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 68 — Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	2
VDD2 supply voltage relative to VSS	VDD2 (1.35V)	-0.4	1.8	V	2
	VDD2 (1.2V)	-0.4	1.6	V	2
VDDCA supply voltage relative to VSSCA	VDDCA	-0.4	1.6	V	2,4
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	2,3
VACC supply voltage relative to VSS	VACC	-0.4	11.5	V	
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	T_{STG}	-55	125	°C	5

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

NOTE 2 See “Power-Ramp” section in “Power-up, Initialization, and Power-Off” on page 19 for relationships between power supplies.

NOTE 3 VREFDQ ≤ 0.6 x VDDQ; however, VREFDQ may be ≥ VDDQ provided that VREFDQ ≤ 300mV.

NOTE 4 VREFCA ≤ 0.6 x VDDCA; however, VREFCA may be ≥ VDDCA provided that VREFCA ≤ 300mV.

NOTE 5 Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

7 AC & DC Operating Conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

7.1 Recommended DC Operating Conditions

Table 69 — Recommended LPDDR2-S2 DC Operating Conditions

Symbol	LPDDR2-S2A			LPDDR2-S2B			DRAM	Unit
	Min	Typ	Max	Min	Typ	Max		
VDD1	1.70	1.80	1.95	1.70	1.80	1.95	Core Power1	V
VDD2	N/A	N/A	N/A	1.14	1.20	1.3	Core Power2	V
VDDCA	1.14	1.20	1.3	1.14	1.20	1.3	Input Buffer Power	V
VDDQ	1.14	1.20	1.3	1.14	1.20	1.3	I/O Buffer Power	V

NOTE 1 When VDD2 is used, VDD1 uses significantly less current than VDD2
N/A(Not available)

Table 70 — Recommended LPDDR2-S4 DC Operating Conditions

Symbol	LPDDR2-S4A			LPDDR2-S4B			DRAM	Unit
	Min	Typ	Max	Min	Typ	Max		
VDD1	1.70	1.80	1.95	1.70	1.80	1.95	Core Power1	V
VDD2	1.28	1.35	1.42	1.14	1.20	1.3	Core Power2	V
VDDCA	1.14	1.20	1.3	1.14	1.20	1.3	Input Buffer Power	V
VDDQ	1.14	1.20	1.3	1.14	1.20	1.3	I/O Buffer Power	V

NOTE 1 VDD1 uses significantly less power than VDD2

Table 71 — Recommended LPDDR2-N DC Operating Conditions

Symbol	Voltage LPDDR2-N-A			LPDDR2-N-B			NVMem	Unit
	Min	Typ	Max	Min	Typ	Max		
VDD1	1.7	1.8	1.95	1.7	1.8	1.95	Core Power	V
VDD2	N/A	N/A	N/A	1.14	1.2	1.3	Core Power 2	V
VDDCA	1.14	1.2	1.3	1.14	1.2	1.3	Input Buffer Power	V
VDDQ	1.14	1.2	1.3	1.14	1.2	1.3	I/O Buffer Power	V
VACC	-0.4	0.0	0.4	-0.4	0.0	0.4	Lockout Voltage	V
	1.7	1.8	1.95	1.7	1.8	1.95	Normal Operation	V
	8.5	9	9.5	8.5	9	9.5	Acceleration Power	V

NOTE 1 When VACC is in the lockout voltage range, program and erase functions are disabled and will not be executed. The lockout voltage range provides hardware program and erase protection for the LPDDR2-NVM array.

NOTE 2 The maximum time for the device to be in the Acceleration Power range for VACC is 80 hours.

7.2 Input Leakage Current

Table 72 — Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current For CA, CKE, CS_n, CK_t, CK_c Any input 0V $\leq$ VIN $\leq$ VDDCA (All other pins not under test = 0V)	I_L	-2	2	uA	2
V_{REF} supply leakage current V_{REFDQ} = VDDQ/2 or V_{REFCA} = VDDCA/2 (All other pins not under test = 0V)	I_{VREF}	-1	1	uA	1

NOTE 1 The minimum limit requirement is for testing purposes. The leakage current on V_{REFCA} and V_{REFDQ} pins should be minimal.

NOTE 2 Although DM is for input only, the DM leakage shall match the DQ and DQS_t/DQS_c output leakage specification.

7.3 Operating Temperature Range

Table 73 — Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	T_{OPER}	-25	85	°C
Extended		85	105	°C

NOTE 1 Operating Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 2 Some applications require operation of LPDDR2 in the maximum temperature conditons in the Extended Temperature Range between 85 °C and 105 °C case temperature. For LPDDR2 devices, some derating is neccessary to operate in this range. See MR4 on page 30.

NOTE 3 Either the device case temperature rating or the temperature sensor (See “Temperature Sensor” on page 116) may be used to set an appropriate refresh rate (SDRAM), determine the need for AC timing de-rating (SDRAM and NVM) and/or monitor the operating temperature (SDRAM and NVM). When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Extended Temperature Ranges. For example, TCASE may be above 85 °C when the temperature sensor indicates a temperature of less than 85 °C.

8 AC and DC Input Measurement Levels

8.1 AC and DC Logic Input Levels for Single-Ended Signals

8.1.1 AC and DC Input Levels for Single-Ended CA and CS_n Signals

Table 74 — Single-Ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
V_{IHCA}(AC)	AC input logic high	Vref + 0.220	Note 2	Vref + 0.300	Note 2	V	1, 2
V_{ILCA}(AC)	AC input logic low	Note 2	Vref - 0.220	Note 2	Vref - 0.300	V	1, 2
V_{IHCA}(DC)	DC input logic high	Vref + 0.130	VDDCA	Vref + 0.200	VDDCA	V	1
V_{ILCA}(DC)	DC input logic low	VSSCA	Vref - 0.130	VSSCA	Vref - 0.200	V	1
V_{RefCA}(DC)	Reference Voltage for CA and CS_n inputs	0.49 * VDDCA	0.51 * VDDCA	0.49 * VDDCA	0.51 * VDDCA	V	3, 4

NOTE 1 For CA and CS_n input only pins. Vref = VrefCA(DC).
NOTE 2 See “Overshoot and Undershoot Specifications” on page 161
NOTE 3 The ac peak noise on V_{RefCA} may not allow V_{RefCA} to deviate from $V_{RefCA(DC)}$ by more than +/-1% VDDCA (for reference: approx. +/- 12 mV).
NOTE 4 For reference: approx. VDDCA/2 +/- 12 mV.

8.1.2 AC and DC Input Levels for CKE

Table 75 — Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCKE}	CKE Input High Level	0.8 * VDDCA	Note 1	V	1
V_{ILCKE}	CKE Input Low Level	Note 1	0.2 * VDDCA	V	1

Note 1 See “Overshoot and Undershoot Specifications” on page 161

8.1.3 AC and DC Input Levels for Single-Ended Data Signals

Table 76 — Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
V_{IHDQ}(AC)	AC input logic high	Vref + 0.220	Note 2	Vref + 0.300	Note 2	V	1, 2, 5
V_{ILDQ}(AC)	AC input logic low	Note 2	Vref - 0.220	Note 2	Vref - 0.300	V	1, 2, 5
V_{IHDQ}(DC)	DC input logic high	Vref + 0.130	VDDQ	Vref + 0.200	VDDQ	V	1
V_{ILDQ}(DC)	DC input logic low	VSSQ	Vref - 0.130	VSSQ	Vref - 0.200	V	1
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDDQ	0.51 * VDDQ	0.49 * VDDQ	0.51 * VDDQ	V	3, 4

NOTE 1 For DQ input only pins. Vref = VrefDQ(DC).
NOTE 2 See “Overshoot and Undershoot Specifications” on page 161
NOTE 3 The ac peak noise on V_{RefDQ} may not allow V_{RefDQ} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% VDDQ (for reference: approx. +/- 12 mV).
NOTE 4 For reference: approx. VDDQ/2 +/- 12 mV.

8.2 Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{RefCA} and V_{RefDQ} are illustrated in Figure 105. It shows a valid reference voltage $V_{Ref}(t)$ as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise). VDD stands for VDDCA for V_{RefCA} and VDDQ for V_{RefDQ}. V_{Ref}(DC) is the linear average of $V_{Ref}(t)$ over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VDDQ or VDDCA also over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 74. Furthermore $V_{Ref}(t)$ may temporarily deviate from $V_{Ref(DC)}$ by no more than +/- 1% VDD. Vref(t) cannot track noise on VDDQ or VDDCA if this would send Vref outside these specifications.

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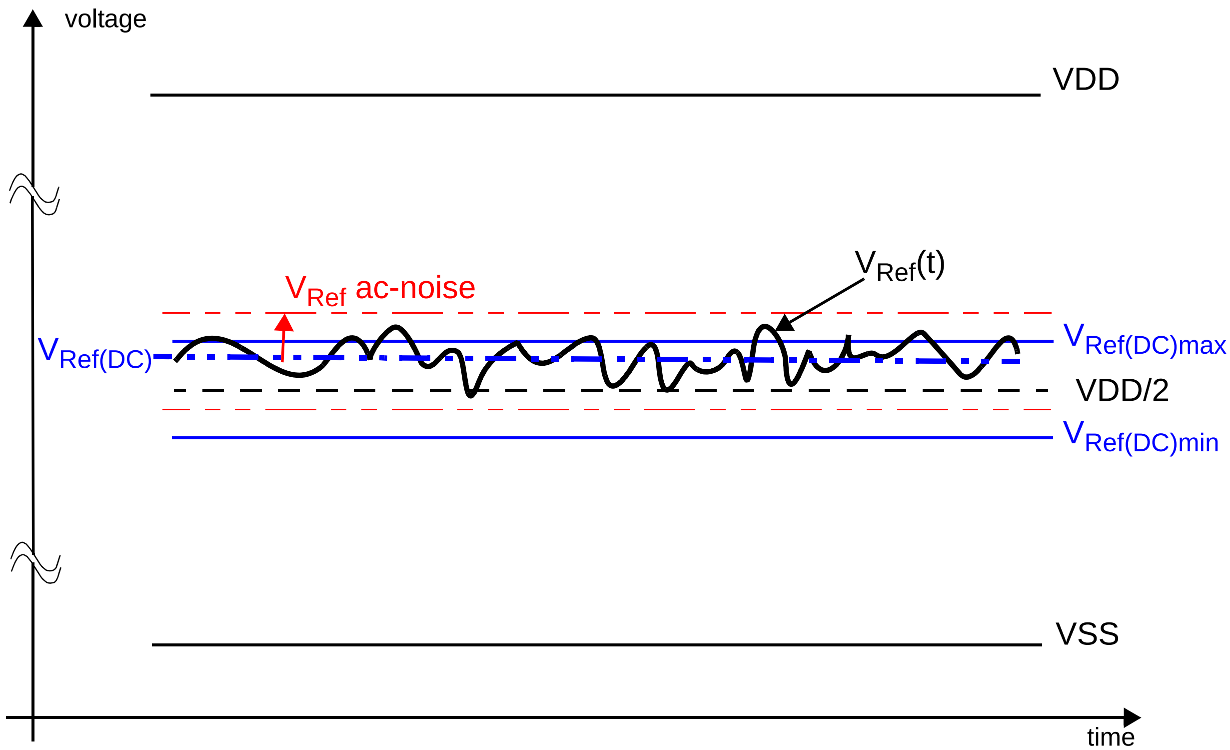


Figure 105 — Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$ and $V_{IL(DC)}$ are dependent on V_{Ref}.

"V_{Ref} " shall be understood as $V_{Ref(DC)}$, as defined in Figure 105.

This clarifies that dc-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. Devices will function correctly with appropriate timing deratings with V_{REF} outside these specified levels so long as V_{REF} is maintained between 0.44 x V_{DDQ} (or V_{DDCA}) and 0.56 x V_{DDQ} (or V_{DDCA}) and so long as the controller achieves the required single-ended AC and DC input levels from instantaneous V_{REF} (see the Single-Ended AC and DC Input Levels for CA and CS_n Inputs Table on page 149 and Single-Ended AC and DC Input Levels for DQ and DM on page 171.) Therefore, system timing and voltage budgets need to account for V_{REF} deviations outside of this range.

This also clarifies that the LPDDR2 setup/hold specification and derating values need to include time and voltage associated with V_{Ref} ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit (+/-1% of VDD) are included in LPDDR2 timings and their associated deratings.

8.3 Input Signal

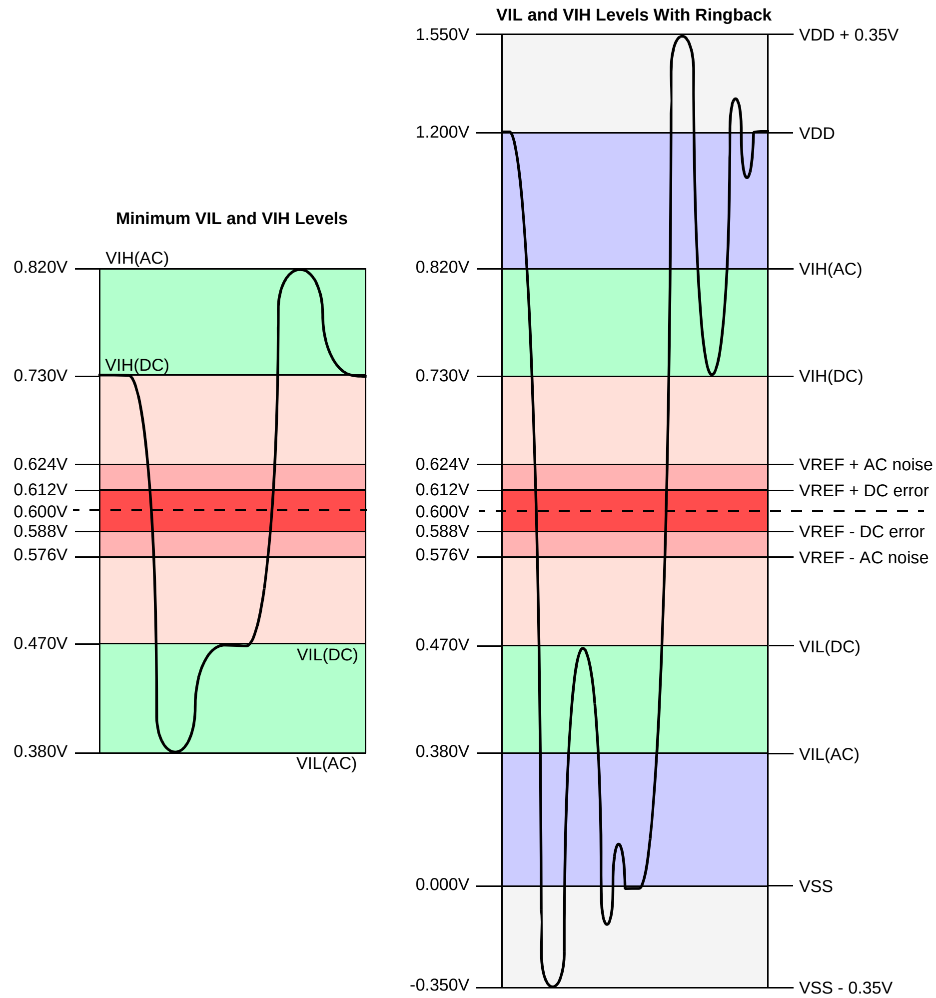


Figure 106 — LPDDR2-466 to LPDDR2-1066 Input Signal

NOTE 1 Numbers reflect nominal values.

NOTE 2 For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDDCA. For DQ, DM/DNV, DQS_t, and DQS_c, VDD stands for VDDQ.

NOTE 3 For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSSCA. For DQ, DM/DNV, DQS_t, and DQS_c, VSS stands for VSSQ.

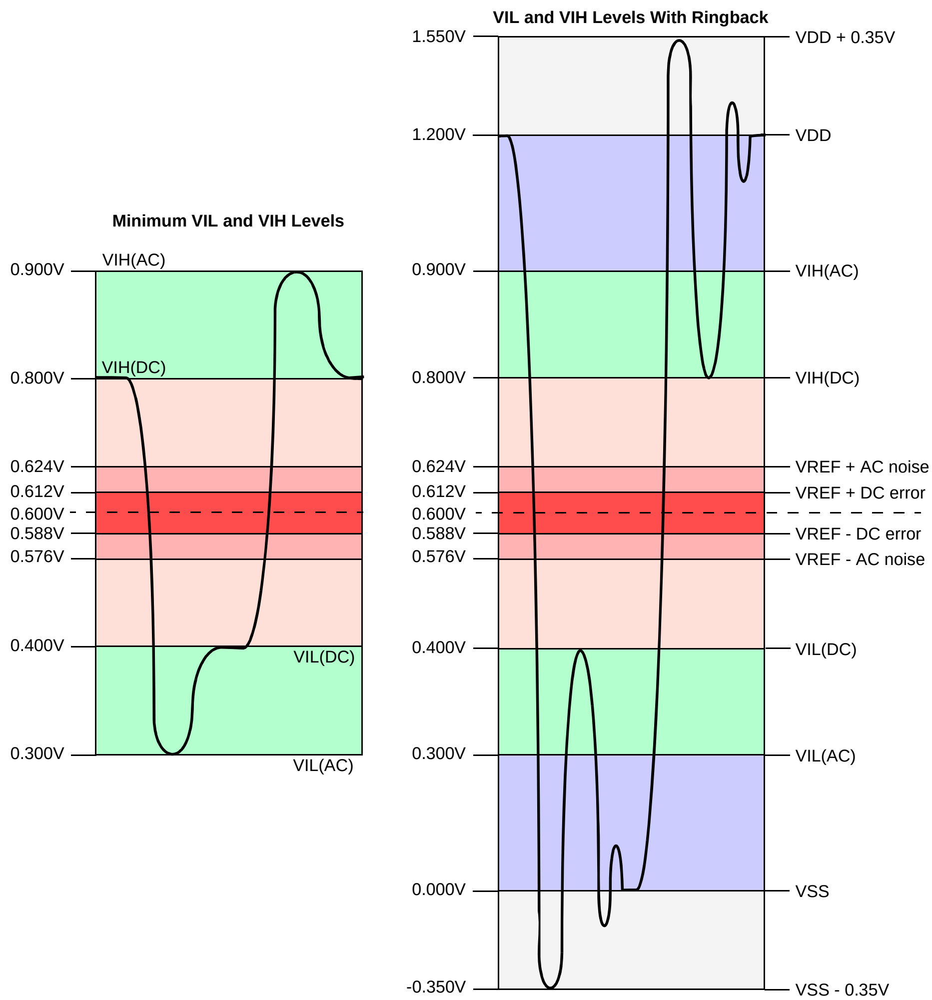


Figure 107 — LPDDR2-200 to LPDDR2-400 Input Signal

NOTE 1 Numbers reflect nominal values

NOTE 2 For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDDCA. For DQ, DM/DNV, DQS_t, a DQS_c, VDD stands for VDDQ.

NOTE 3 For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSSCA. For DQ, DM/DNV, DQS_t, an DQS_c, VSS stands for VSSQ.

8.4 AC and DC Logic Input Levels for Differential Signals

8.4.1 Differential signal definition

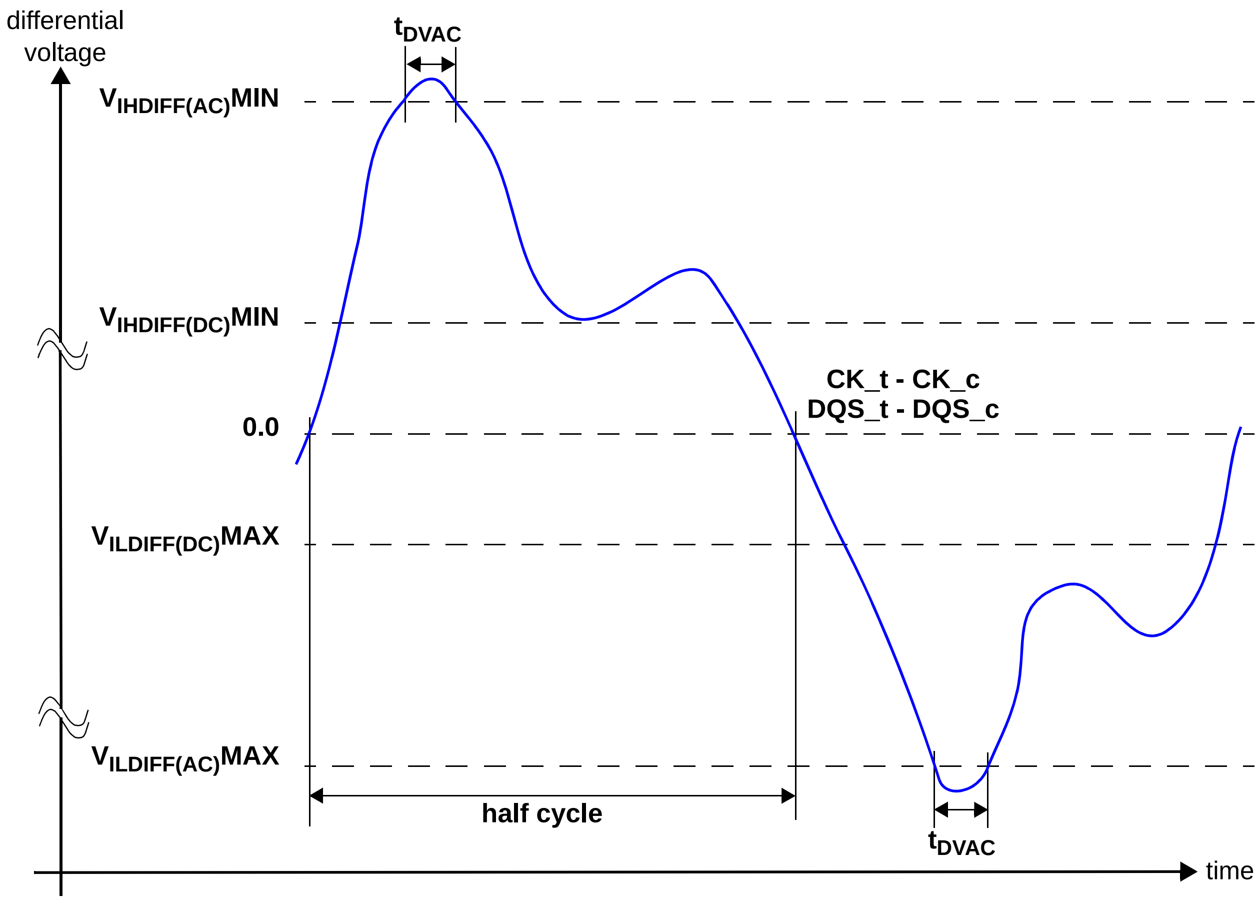


Figure 108 — Definition of differential ac-swing and "time above ac-level" t_{DVAC}

8.4.2 Differential swing requirements for clock (CK_t - CK_c) and strobe (DQS_t - DQS_c)

Table 77 — Differential AC and DC Input Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IHdiff(dc)}$	Differential input high	2 x (VIH(dc) - Vref)	note 3	2 x (VIH(dc) - Vref)	note 3	V	1
$V_{ILdiff(dc)}$	Differential input logic low	Note 3	2 x (Vref - VIL(dc))	Note 3	2 x (Vref - VIL(dc))	V	1
$V_{IHdiff(ac)}$	Differential input high ac	2 x (VIH(ac) - Vref)	Note 3	2 x (VIH(ac) - Vref)	Note 3	V	2
$V_{ILdiff(ac)}$	Differential input low ac	note 3	2 x (Vref - VIL(ac))	note 3	2 x (Vref - VIL(ac))	V	2

NOTE 1 Used to define a differential signal slew-rate.

NOTE 2 For CK_t - CK_c use VIH/VIL(ac) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

NOTE 3 These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 161.

NOTE 4 For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC).

8.4.2 Differential swing requirements for clock (CK_t - CK_c) and strobe (DQS_t - DQS_c) (cont'd)

Table 78 — Allowed time before ringback (tDVAC) for CK_t - CK_c and DQS_t - DQS_c

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(ac)| = 440mV	tDVAC [ps] @ |VIH/Ldiff(ac)| = 600mV
	min	min
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

8.4.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle.

DQS_t, DQS_c shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle preceeding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

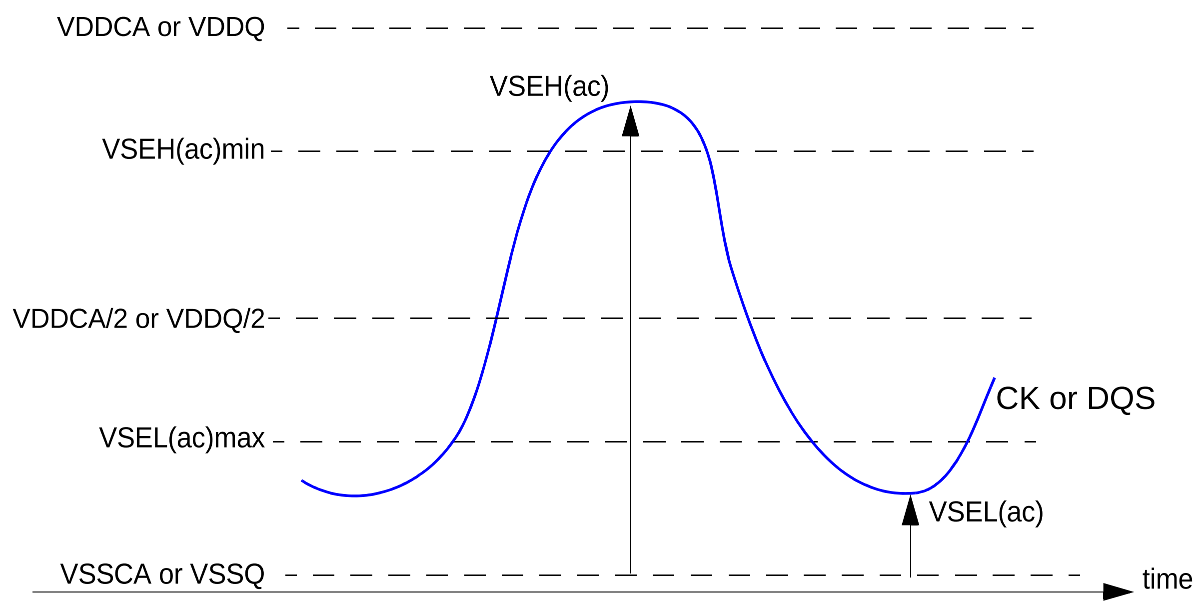


Figure 109 — Single-ended requirement for differential signals.

Note that while CA and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS and VDDCA/2 for CK; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL(ac)max, VSEH(ac)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

The signal ended requirements for CK and DQS are found in tables 74 and 76, respectively.

Table 79 — Single-ended levels for CK_t, DQS_t, CK_c, DQS_c

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
VSEH(AC)	Single-ended high-level for strobes	(VDDQ / 2) + 0.220	note 3	(VDDQ / 2) + 0.300	note 3	V	1, 2
	Single-ended high-level for CK_t, CK_c	(VDDCA / 2) + 0.220	note 3	(VDDCA / 2) + 0.300	note 3	V	1, 2
VSEL(AC)	Single-ended low-level for strobes	note 3	(VDDDQ / 2) - 0.220	note 3	(VDDQ / 2) - 0.300	V	1, 2
	Single-ended low-level for CK_t, CK_c	note 3	(VDDCA / 2) - 0.220	note 3	(VDDCA / 2) - 0.300	V	1, 2

NOTE 1 For CK_t, CK_c use VSEH/VSEL(ac) of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use VIH/VIL(ac) of DQs.

NOTE 2 VIH(ac)/VIL(ac) for DQs is based on VREFDQ; VSEH(ac)/VSEL(ac) for CA is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here

NOTE 3 These values are not defined, ho\wever the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 161

8.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements in Table 79. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

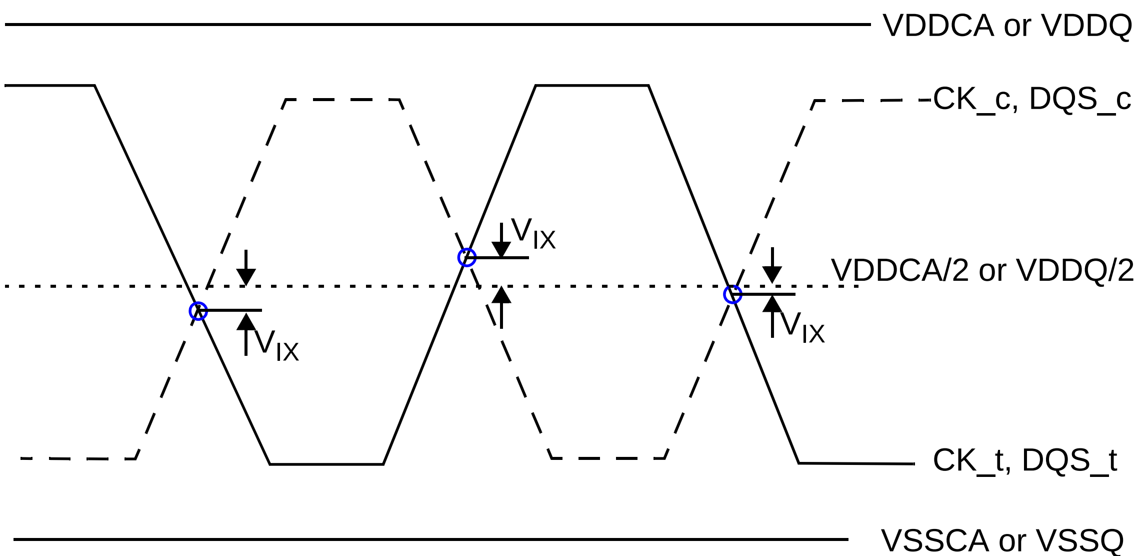


Figure 110 — Vix Definition

Table 80 — Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200		Unit	Notes
		Min	Max		
V_{IXCA}	Differential Input Cross Point Voltage relative to VDDCA/2 for CK_t, CK_c	- 120	120	mV	1,2
V_{IXDQ}	Differential Input Cross Point Voltage relative to VDDQ/2 for DQS_t, DQS_c	- 120	120	mV	1,2

NOTE 1 The typical value of VIX(AC) is expected to be about 0.5 × VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
NOTE 2 For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC).

8.6 Slew Rate Definitions for Single-Ended Input Signals

See “CA and CS_n Setup, Hold and Derating” on page 190 for single-ended slew rate definitions for address and command signals.

See “Data Setup, Hold and Slew Rate Derating” on page 196 for single-ended slew rate definitions for data signals.

8.7 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in Table 81 and Figure 111.

Table 81 — Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK_t - CK_c and DQS_t - DQS_c).	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTRdiff
Differential input slew rate for falling edge (CK_t - CK_c and DQS_t - DQS_c).	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTFdiff
NOTE 1 The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds.			

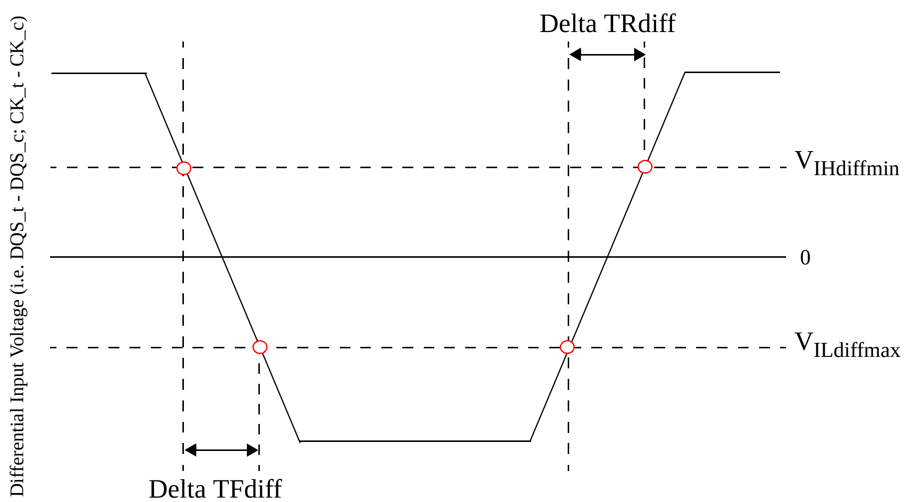


Figure 111 — Differential Input Slew Rate Definition for DQS_t, DQS_c and CK_t, CK_c

9 AC and DC Output Measurement Levels

9.1 Single Ended AC and DC Output Levels

Table 82 shows the output levels used for measurements of single ended signals.

Table 82 — Single-ended AC and DC Output Levels

Symbol	Parameter		LPDDR2-1066 to LPDDR2-200	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)		0.9 x V_{DDQ}	V	1
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)		0.1 x V_{DDQ}	V	2
$V_{OH(AC)}$	AC output high measurement level (for output slew rate)		V_{REFDQ} + 0.12	V	
$V_{OL(AC)}$	AC output low measurement level (for output slew rate)		V_{REFDQ} - 0.12	V	
I_{OZ}	Output Leakage current (DQ, DM, DQS_t, DQS_c) (DQ, DQS_t, DQS_c are disabled; 0V ≤ VOUT ≤ VDDQ	Min	-5	uA	
		Max	5	uA	
MM_{PUPD}	Delta RON between pull-up and pull-down for DQ/DM	Min	-15	%	
		Max	15	%	

NOTE 1 IOH = -0.1mA.
NOTE 2 IOL = 0.1mA.

9.2 Differential AC and DC Output Levels

Table 83 shows the output levels used for measurements of differential signals (DQS_t, DQS_c).

Table 83 — Differential AC and DC Output Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.25 x V_{DDQ}	V	
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	- 0.25 x V_{DDQ}	V	

9.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 84 and Figure 112.

Table 84 — Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTFse
Note: Output slew rate is verified by design and characterization, and may not be subject to production test.			

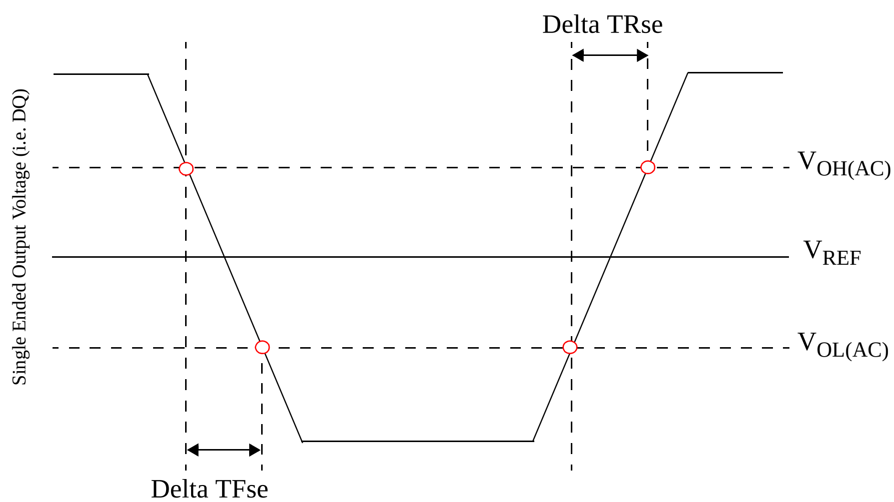


Figure 112 — Single Ended Output Slew Rate Definition

Table 85 — Output Slew Rate (single-ended)

Parameter	Symbol	LPDDR2-1066 to LPDDR2-200		Units
		Min	Max	
Single-ended Output Slew Rate (RON = 40Ω +/- 30%)	SRQse	1.5	3.5	V/ns
Single-ended Output Slew Rate (RON = 60Ω +/- 30%)	SRQse	1.0	2.5	V/ns
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4	

Description: SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

NOTE 1 Measured with output reference load.
NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
NOTE 3 The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
NOTE 4 Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

9.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 86 and Figure 113.

Table 86 — Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / DeltaTFdiff
NOTE 1 Output slew rate is verified by design and characterization, and may not be subject to production test.			

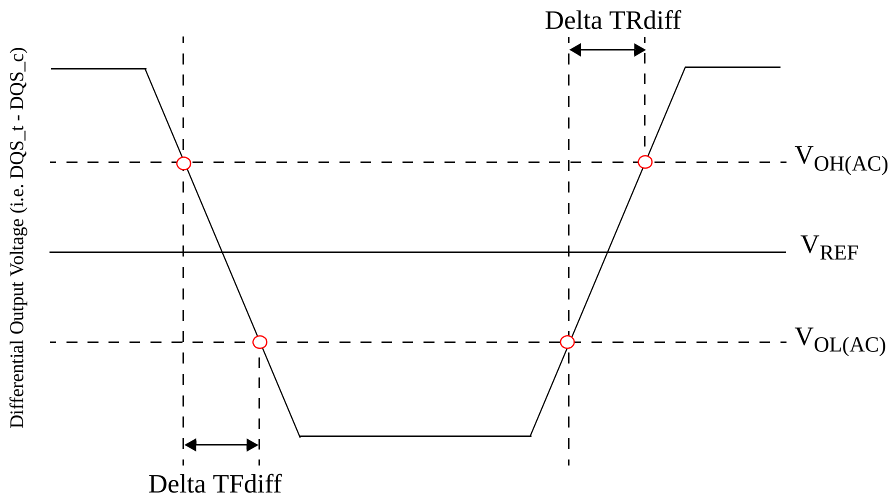


Figure 113 — Differential Output Slew Rate Definition

Table 87 — Differential Output Slew Rate

Parameter	Symbol	LPDDR2-1066 to LPDDR2-200		Units
		Min	Max	
Differential Output Slew Rate (RON = 40Ω +/- 30%)	SRQdiff	3.0	7.0	V/ns
Differential Output Slew Rate (RON = 60Ω +/- 30%)	SRQdiff	2.0	5.0	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

NOTE 1 Measured with output reference load.
NOTE 2 The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
NOTE 3 Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

9.5 Overshoot and Undershoot Specifications

Table 88 — AC Overshoot/Undershoot Specification

Parameter		1066	933	800	667	533	466	400	333	266	200	Units
Maximum peak amplitude allowed for overshoot area. (See Figure 114)	Max	0.35										V
Maximum peak amplitude allowed for undershoot area. (See Figure 114)	Max	0.35										V
Maximum area above VDD. (See Figure 114)	Max	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns
Maximum area below VSS. (See Figure 114)	Max	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns

(CA0-9, CS_n, CKE, CK_t, CK_c, DQ, DQS_t, DQS_c, DM/DNV)

NOTE 1 For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDDCA. For DQ, DM/DNV, DQS_t, and DQS_c, VDD stands for VDDQ.

NOTE 2 For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSSCA. For DQ, DM/DNV, DQS_t, and DQS_c, VSS stands for VSSQ.

NOTE 3 Values are referenced from actual VDDQ, VDDCA, VSSQ, and VSSCA levels.

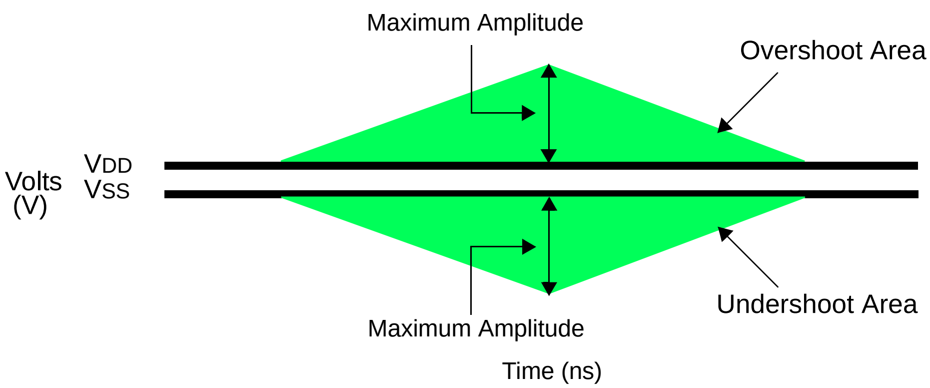


Figure 114 — Overshoot and Undershoot Definition

NOTE 1 For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDDCA. For DQ, DM/DNV, DQS_t, and DQS_c, VDD stands for VDDQ.

NOTE 2 For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSSCA. For DQ, DM/DNV, DQS_t, and DQS_c, VSS stands for VSSQ.

9.6 Output buffer characteristics

9.6.1 HSUL_12 Driver Output Timing Reference Load

These ‘Timing Reference Loads’ are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

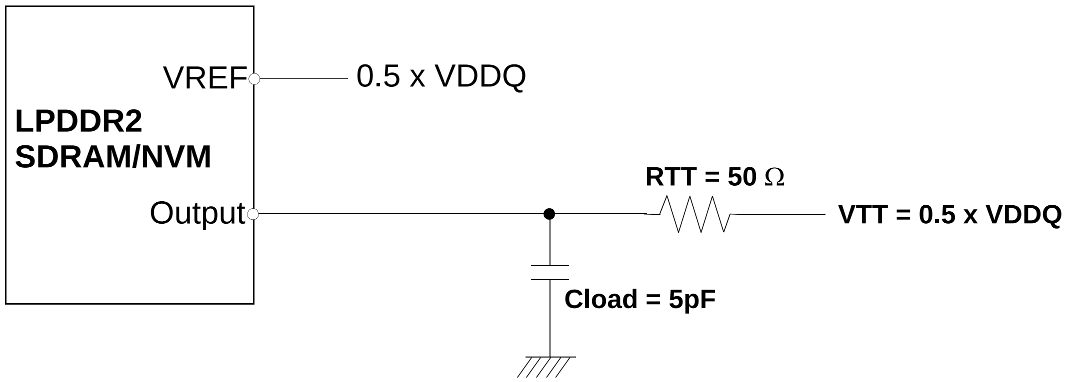


Figure 115 — HSUL_12 Driver Output Reference Load for Timing and Slew Rate

NOTE 1: All output timing parameter values (like t_{DQSCK}, t_{DQSQ}, t_{QHS}, t_{HZ}, t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

9.7 RON_{PU} and RON_{PD} Resistor Definition

$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

NOTE 1: This is under the condition that RON_{PD} is turned off

$$RONPD = \frac{Vout}{ABS(Iout)}$$

NOTE 1: This is under the condition that RON_{PU} is turned off

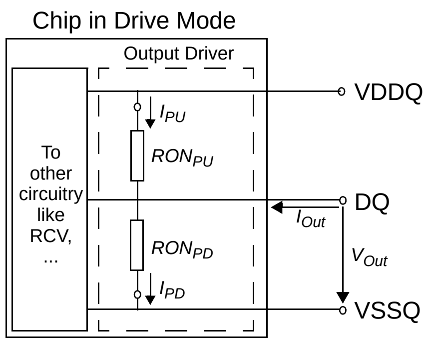


Figure 116 — Output Driver: Definition of Voltages and Currents

9.7.1 RON_{PU} and RON_{PD} Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω.

Table 89 — Output Driver DC Electrical Characteristics with ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
	RON34PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
40.0Ω	RON40PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
	RON40PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
48.0Ω	RON48PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
	RON48PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
60.0Ω	RON60PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
	RON60PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
80.0Ω	RON80PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
	RON80PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
Mismatch between pull-up and pull-down	MM_{PUPD}		-15.00		+15.00	%	1,2,3,4,5

NOTE 1 Across entire operating temperature range, after calibration.

NOTE 2 RZQ = 240Ω.

NOTE 3 The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

NOTE 4 Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ.

NOTE 5 Measurement definition for mismatch between pull-up and pull-down, MMPUPD: Measure RON_{PU} and RON_{PD}, both at 0.5 x VDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

For example, with MMPUPD(max) = 15% and RONPD = 0.85, RONPU must be less than 1.0.

9.7.2 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table 90 — Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Notes
RONPD	0.5 x VDDQ	$85 - (dRONdT \times \lvert\Delta T\rvert) - (dRONdV \times \lvert\Delta V\rvert)$	$115 + (dRONdT \times \lvert\Delta T\rvert) + (dRONdV \times \lvert\Delta V\rvert)$	%	1,2
RONPU					

NOTE 1 $\Delta T = T - T$ (@ calibration), $\Delta V = V - V$ (@ calibration)

NOTE 2 dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Table 91 — Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	MIn	Max	Unit	Notes
dRONdT	RON Temperature Sensitivity	0.00	0.75	% / C	
dRONdV	RON Voltage Sensitivity	0.00	0.20	% / mV	

9.7.3 RON_{PU} and RON_{PD} Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

Table 92 — Output Driver DC Electrical Characteristics without ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	0.70	1.00	1.30	RZQ/7	1,2
	RON34PU	0.5 x VDDQ	0.70	1.00	1.30	RZQ/7	1,2
40.0Ω	RON40PD	0.5 x VDDQ	0.70	1.00	1.30	RZQ/6	1,2
	RON40PU	0.5 x VDDQ	0.70	1.00	1.30	RZQ/6	1,2
48.0Ω	RON48PD	0.5 x VDDQ	0.70	1.00	1.30	RZQ/5	1,2
	RON48PU	0.5 x VDDQ	0.70	1.00	1.30	RZQ/5	1,2
60.0Ω	RON60PD	0.5 x VDDQ	0.70	1.00	1.30	RZQ/4	1,2
	RON60PU	0.5 x VDDQ	0.70	1.00	1.30	RZQ/4	1,2
80.0Ω	RON80PD	0.5 x VDDQ	0.70	1.00	1.30	RZQ/3	1,2
	RON80PU	0.5 x VDDQ	0.70	1.00	1.30	RZQ/3	1,2

NOTE 1 Across entire operating temperature range, without calibration.
NOTE 2 RZQ = 240Ω.

9.7.4 RZQ I-V Curve

Table 93 — RZQ I-V Curve

Voltage[V]	RON = 240Ω (RZQ)							
	Pull-Down				Pull-Up			
	Current [mA] / RON [Ohms]				Current [mA] / RON [Ohms]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	-0.19	-0.32	-0.21	-0.26
0.10	0.38	0.64	0.40	0.53	-0.38	-0.64	-0.40	-0.53
0.15	0.56	0.94	0.60	0.78	-0.56	-0.94	-0.60	-0.78
0.20	0.74	1.26	0.79	1.04	-0.74	-1.26	-0.79	-1.04
0.25	0.92	1.57	0.98	1.29	-0.92	-1.57	-0.98	-1.29
0.30	1.08	1.86	1.17	1.53	-1.08	-1.86	-1.17	-1.53
0.35	1.25	2.17	1.35	1.79	-1.25	-2.17	-1.35	-1.79
0.40	1.40	2.46	1.52	2.03	-1.40	-2.46	-1.52	-2.03
0.45	1.54	2.74	1.69	2.26	-1.54	-2.74	-1.69	-2.26
0.50	1.68	3.02	1.86	2.49	-1.68	-3.02	-1.86	-2.49
0.55	1.81	3.30	2.02	2.72	-1.81	-3.30	-2.02	-2.72
0.60	1.92	3.57	2.17	2.94	-1.92	-3.57	-2.17	-2.94
0.65	2.02	3.83	2.32	3.15	-2.02	-3.83	-2.32	-3.15
0.70	2.11	4.08	2.46	3.36	-2.11	-4.08	-2.46	-3.36
0.75	2.19	4.31	2.58	3.55	-2.19	-4.31	-2.58	-3.55
0.80	2.25	4.54	2.70	3.74	-2.25	-4.54	-2.70	-3.74
0.85	2.30	4.74	2.81	3.91	-2.30	-4.74	-2.81	-3.91
0.90	2.34	4.92	2.89	4.05	-2.34	-4.92	-2.89	-4.05
0.95	2.37	5.08	2.97	4.23	-2.37	-5.08	-2.97	-4.23
1.00	2.41	5.20	3.04	4.33	-2.41	-5.20	-3.04	-4.33
1.05	2.43	5.31	3.09	4.44	-2.43	-5.31	-3.09	-4.44
1.10	2.46	5.41	3.14	4.52	-2.46	-5.41	-3.14	-4.52
1.15	2.48	5.48	3.19	4.59	-2.48	-5.48	-3.19	-4.59
1.20	2.50	5.55	3.23	4.65	-2.50	-5.55	-3.23	-4.65

9.7.4 RZQ I-V Curve (cont'd)

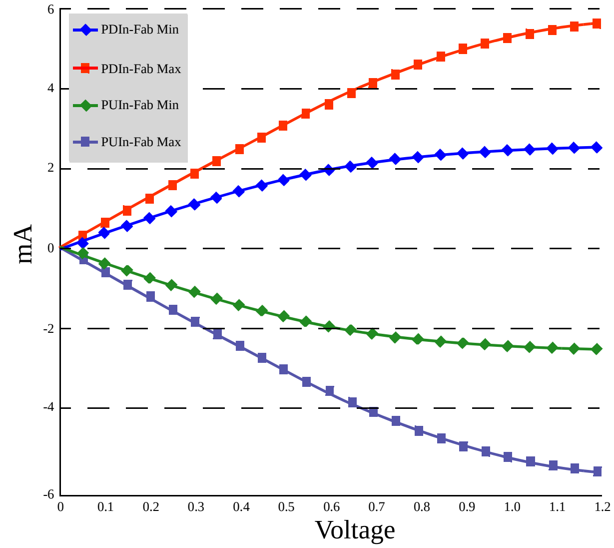


Figure 117 — RON 240 Ohms
IV Curve after ZQReset

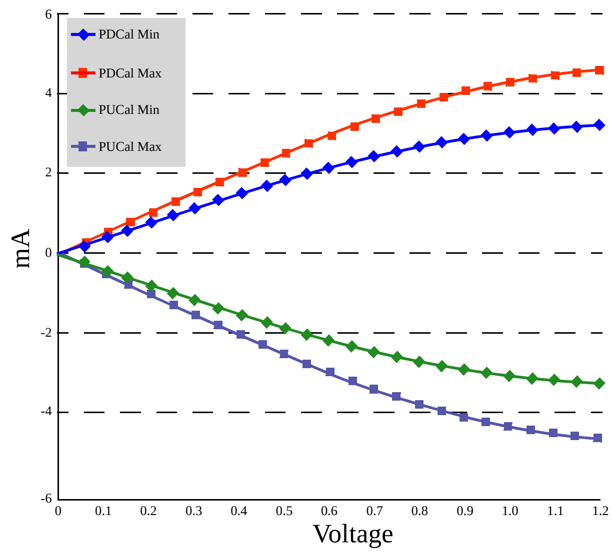


Figure 118 — RON = 240 Ohms
IV Curve after calibration

10 Input/Output Capacitance

10.1 Input/Output Capacitance

Table 94 — Input/output capacitance

Parameter	Symbol		LPDDR2 1066-466	LPDDR2 400-200	Units	Notes
Input capacitance, CK_t and CK_c	CCK	Min	1.0		pF	1,2
		Max	2.0		pF	1,2
Input capacitance delta, CK_t and CK_c	CDCK	Min	0		pF	1,2,3
		Max	0.20	0.25	pF	1,2,3
Input capacitance, all other input-only pins	CI	Min	1.0		pF	1,2,4
		Max	2.0		pF	1,2,4
Input capacitance delta, all other input-only pins	CDI	Min	-0.40	-0.50	pF	1,2,5
		Max	0.40	0.50	pF	1,2,5
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	Min	1.25		pF	1,2,6,7
		Max	2.5		pF	1,2,6,7
Input/output capacitance delta, DQS_t, DQS_c	CDDQS	Min	0		pF	1,2,7,8
		Max	0.25	0.30	pF	1,2,7,8
Input/output capacitance delta, DQ, DM	CDIO	Min	-0.5	-0.6	pF	1,2,7,9
		Max	0.5	0.6	pF	1,2,7,9
Input/output capacitance ZQ Pin	CZQ	Min	0		pF	1,2
		Max	2.5		pF	1,2
Package Input capacitance, CK_t and CK_c	CPKGCK	Min			pF	2,10
		Max			pF	2,10
Package Input capacitance delta, CK_t and CK_c	CDPKGCK	Min			pF	2,10,11
		Max			pF	2,10,11
Package Input capacitance, all other input-only pins	CPKGI	Min			pF	2,10,12
		Max			pF	2,10,12
Package Input capacitance delta, all other input-only pins	CDPKGI	Min			pF	2,10,13
		Max			pF	2,10,13
Package Input/output capacitance, DQ, DM, DQS_t, DQS_c	CPKGIO	Min			pF	2,10,5
		Max			pF	2,10,5
Package Input/output capacitance delta, DQS_t, DQS_c	CDPKGDQS	Min			pF	2,10,14
		Max			pF	2,10,14
Package Input/output capacitance delta, DQ, DM	CDPKGIO	Min			pF	2,10,15
		Max			pF	2,10,15
Package Input/output capacitance, ZQ Pin	CDPKZQ	Min			pF	2,10
		Max			pF	2,10,16

(T_{OPER}; V_{DDQ} = 1.14-1.3V; V_{DDCA} = 1.14-1.3V; V_{DD1} = 1.7-1.95V, LPDDR2-S4A V_{DD2} = 1.28-1.42V, LPDDR2-S2B, LPDDR2-N-B V_{DD2} = 1.14-1.3V)

10.1 Input/Output Capacitance (cont'd)

Notes to Table 94

NOTE 1 This parameter applies to die device only (does not include package capacitance).

NOTE 2 This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating.

NOTE 3 Absolute value of CCK_t - CCK_c.

NOTE 4 CI applies to CS_n, CKE, CA0-CA9.

NOTE 5 CDI = CI - 0.5 * (CCK_t + CCK_c)

NOTE 6 DM loading matches DQ and DQS.

NOTE 7 MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ohm typical)

NOTE 8 Absolute value of CDQS_t and CDQS_c.

NOTE 9 CDIO = CIO - 0.5 * (CDQS_t + CDQS_c) in byte-lane.

NOTE 10 This parameter applies to package only (does not include die capacitance). This value is vendor specific.

NOTE 11 Absolute value of CPKGCK_t and CPKGCK_c.

NOTE 12 CPKGI applies to CS_n, CKE, CA9-CA0.

NOTE 13 CDPKGI = CPKGI - 0.5 * (CPKGDQS_t + CPKGDQS_c).

NOTE 14 Absolute value of CPKGDQS_t and CPKGDQS_c.

NOTE 15 CDPKGIO = CPKGIO - 0.5 * (CPKGDQS_t + CPKGDQS_c) in byte lane.

NOTE 16 Maximum external load capacitance on ZQ pin, including packaging, board, pin, resistor, and other LPDDR2 devices: 5 pF.

11 IDD Specification Parameters and Test Conditions

11.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:

LOW: $V_{IN} \leq V_{IL(DC)}$ MAX

HIGH: $V_{IN} \geq V_{IH(DC)}$ MIN

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See tables 95 and 96.

Table 95 — Definition of Switching for CA Input Signals

Switching for CA								
	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)
Cycle	N		N+1		N+2		N+3	
CS_n	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

NOTE 1 CS_n must always be driven HIGH.

NOTE 2 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.

NOTE 3 The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.

11.1 IDD Measurement Conditions (cont'd)

Table 96 — Definition of Switching for IDD4R

Clock	CKE	CS_n	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLHLH	L
Rising	HIGH	LOW	N + 2	Read_Rising	HLH	HLHLHLH	H
Falling	HIGH	LOW	N + 2	Read_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

NOTE 1 Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
NOTE 2 The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4R.

Table 97 — Definition of Switching for IDD4W

Clock	CKE	CS_n	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Write_Rising	HLL	LHLHLHL	L
Falling	HIGH	LOW	N	Write_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLHLH	L
Rising	HIGH	LOW	N + 2	Write_Rising	HLL	HLHLHLH	H
Falling	HIGH	LOW	N + 2	Write_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

NOTE 1 Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
NOTE 2 Data masking (DM) must always be driven LOW.
NOTE 3 The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.

11.2 IDD Specifications

IDD values are for the entire operating voltage range and the standard and extended temperature ranges, unless otherwise noted.

Table 98 — LPDDR2 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Units	Notes
Operating one bank active-precharge current (SDRAM): **Operating one RB active current (NVM):** $t_{CK} = t_{CKmin}$; $t_{RC} = t_{RCmin}$; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD0_1$	VDD1	mA	4
	$IDD0_2$	VDD2	mA	4
	$IDD0_{IN}$	VDDCA VDDQ	mA	4,5
Idle power-down standby current: $t_{CK} = t_{CKmin}$; CKE is LOW; CS_n is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2P_1$	VDD1	mA	4
	$IDD2P_2$	VDD2	mA	4
	$IDD2P_{IN}$	VDDCA VDDQ	mA	4,5
Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is LOW; CS_n is HIGH; All banks/RBs idle; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD2PS_1$	VDD1	mA	4
	$IDD2PS_2$	VDD2	mA	4
	$IDD2PS_{IN}$	VDDCA VDDQ	mA	4,5
Idle non power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS_n is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2N_1$	VDD1	mA	4
	$IDD2N_2$	VDD2	mA	4
	$IDD2N_{IN}$	VDDCA VDDQ	mA	4,5
Active power-down standby current: $t_{CK} = t_{CKmin}$; CKE is LOW; CS_n is HIGH; One bank/RB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3P_1$	VDD1	mA	4
	$IDD3P_2$	VDD2	mA	4
	$IDD3P_{IN}$	VDDCA VDDQ	mA	4,5
Active power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is LOW; CS_n is HIGH; One bank/RB active; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD3PS_1$	VDD1	mA	4
	$IDD3PS_2$	VDD2	mA	4
	$IDD3PS_{IN}$	VDDCA VDDQ	mA	4,5
Active non power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS_n is HIGH; One bank/RB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3N_1$	VDD1	mA	4
	$IDD3N_2$	VDD2	mA	4
	$IDD3N_{IN}$	VDDCA VDDQ	mA	4,5

Parameter/Condition	Symbol	Power Supply	Units	Notes
Operating burst read current: $t_{CK} = t_{CKmin}$; CS_n is HIGH between valid commands; One bank/RB active; BL = 4; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4R_1$	VDD1	mA	4
	$IDD4R_2$	VDD2	mA	4
	$IDD4R_{IN}$	VDDCA	mA	4
	$IDD4R_Q$	VDDQ	mA	4,8
Operating burst write current: $t_{CK} = t_{CKmin}$; CS_n is HIGH between valid commands; One bank/RB active; BL = 4; WL = WLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4W_1$	VDD1	mA	4
	$IDD4W_2$	VDD2	mA	4
	$IDD4W_{IN}$	VDDCA VDDQ	mA	4,5
All Bank Refresh Burst current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{RFCabmin}$; Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5_1$	VDD1	mA	1,4
	$IDD5_2$	VDD2	mA	1,4
	$IDD5_{IN}$	VDDCA VDDQ	mA	1,4,5
All Bank Refresh Average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5AB_1$	VDD1	mA	1,4
	$IDD5AB_2$	VDD2	mA	1,4
	$IDD5AB_{IN}$	VDDCA VDDQ	mA	1,4,5
Per Bank Refresh Average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}/8$; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5PB_1$	VDD1	mA	1,2,4
	$IDD5PB_2$	VDD2	mA	1,2,4
	$IDD5PB_{IN}$	VDDCA VDDQ	mA	1,2,4,5
Self refresh current (Standard Temperature Range): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; Maximum 1x Self-Refresh Rate;	$IDD6_1$	VDD1	mA	1,3,4,11,12
	$IDD6_2$	VDD2	mA	1,3,4,11,12
	$IDD6_{IN}$	VDDCA VDDQ	mA	1,3,4,5,11,12
Self refresh current (Extended Temperature Range): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;	$IDD6ET_1$	VDD1	mA	1,3,4,11,13
	$IDD6ET_2$	VDD2	mA	1,3,4,11,13
	$IDD6ET_{IN}$	VDDCA VDDQ	mA	1,3,4,5,11,13
Deep Power-Down current: CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;	$IDD8_1$	VDD1	uA	1,4
	$IDD8_2$	VDD2	uA	1,4
	$IDD8_{IN}$	VDDCA VDDQ	uA	1,4,5

Parameter/Condition	Symbol	Power Supply	Units	Notes
LPDDR2-N Program current: CK_t =LOW, CK_c =HIGH; CKE is LOW; RBs active or idle; CKE is HIGH; CS_n is HIGH; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDDN_{P1}$	VDD1	mA	4,7
	$IDDN_{P2}$	VDD2	mA	4,7
LPDDR2-N Erase current: CK_t =LOW, CK_c =HIGH; CKE is LOW; RBs active or idle; CKE is HIGH; CS_n is HIGH; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDDN_{E1}$	VDD1	mA	4,6,7
	$IDDN_{E2}$	VDD2	mA	4,6,7

NOTE 1 Refresh currents and Deep Power Down currents are not relevant for NVM devices.

NOTE 2 Per Bank Refresh only applicable for LPDDR2-S4 devices of 1Gb or higher densities and LPDDR2-S2 devices of 4Gb and higher densities.

NOTE 3 This is the general definition that applies to full array Self Refresh. Refer to IDD6 Partial Array Self-Refresh Current on page 174 for details of Partial Array Self Refresh IDD6 specification.

NOTE 4 IDD values published are the maximum of the distribution of the arithmetic mean.

NOTE 5 Measured currents are the summation of VDDQ and VDDCA.

NOTE 6 Some LPDDR2-N devices do not support the erase function.

NOTE 7 To calculate total current consumption, the currents of all active operations must be considered.

NOTE 8 Guaranteed by design with output reference load and RON = 40Ohm.

NOTE 9 Currents related to VDD2 do not apply to LPDDR2-N-A and LPDDR2-S2A devices.

NOTE 10 IDD current specifications are tested after the device is properly initialized.

NOTE 11 In addition, supplier data sheets may include additional Self Refresh IDD values for temperature subranges within the Standard or Extended Temperature Ranges.

NOTE 12 1x Self-Refresh Rate is the rate at which the LPDDR2-SX device is refreshed internally during Self-Refresh before going into the Extended Temperature range.

NOTE 13 IDD6ET is a typical value, is sampled only and is not tested.

Table 99 — IDD6 Partial Array Self-Refresh Current

Parameter		LPDDR2-S2		LPDDR2-S4		Unit
		64Mb-2Gb	4Gb-8Gb	64Mb-512Mb	1Gb-8Gb	
IDD6 Partial Array Self-Refresh Current	Full Array	-	-	-	-	uA
	1/2 Array	-	-	-	-	uA
	1/4 Array	-	-	-	-	uA
	1/8 Array	NA	-	NA	-	uA

NOTE 1 LPDDR2-S2 SDRAM uses the same PASR scheme & IDD6 current value categorization as LPDDR (JESD209).

NOTE 2 LPDDR2-S4 SDRAM uses the same IDD6 current value categorization as LPDDR2-S2 SDRAM. Some LPDDR2-S4 SDRAM densities support both bank-masking & segment-masking. The IDD6 currents are measured using bank-masking only.

NOTE 3 IDD values published are the maximum of the distribution of the arithmetic mean.

12 Electrical Characteristics and AC Timing

12.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR2 device.

12.1.1 Definition for t_{CK}(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j\right) / N$$
$$where \qquad N = 200$$

Unit ‘tCK(avg)’ represents the actual clock average tCK(avg) of the input clock under operation. Unit ‘nCK’ represents one clock cycle of the input clock, counting the actual clock edges.
tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

12.1.2 Definition for t_{CK}(abs)

t_{CK}(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.
t_{CK}(abs) is not subject to production test.

12.1.3 Definition for t_{CH}(avg) and t_{CL}(avg)

t_{CH}(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j\right) / (N \times tCK(avg))$$
$$where \qquad N = 200$$

t_{CL}(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j\right) / (N \times tCK(avg))$$
$$where \qquad N = 200$$

12.1.4 Definition for t_{JIT}(per)

t_{JIT}(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).
t_{JIT}(per) = Min/max of {tCK_i - tCK(avg) where i = 1 to 200}.
t_{JIT}(per),act is the actual clock jitter for a given system.
t_{JIT}(per),allowed is the specified allowed clock period jitter.
t_{JIT}(per) is not subject to production test.

12.1.5 Definition for t_{JIT}(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

t_{JIT}(cc) = Max of $|\{tCK_{i+1} - tCK_i\}|$.
t_{JIT}(cc) defines the cycle to cycle jitter.
t_{JIT}(cc) is not subject to production test.

12.1.6 Definition for t_{ERR}(nper)

t_{ERR}(nper) is defined as the cumulative error across n multiple consecutive cycles from tCK(avg).

t_{ERR}(nper),act is the actual clock jitter over n cycles for a given system.
t_{ERR}(nper),allowed is the specified allowed clock period jitter over n cycles.
t_{ERR}(nper) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCK_j\right) - n \times tCK(avg)$$

t_{ERR}(nper),min can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68LN(n)) \times tJIT(per), min$$

t_{ERR}(nper),max can be calculated by the formula shown below:

$$tERR(nper), max = (1 + 0.68LN(n)) \times tJIT(per), max$$

Using these equations, t_{ERR}(nper) tables can be generated for each t_{JIT}(per),act value.

12.1.7 Definition for duty cycle jitter t_{JIT}(duty)

t_{JIT}(duty) is defined with tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH(avg). tCL jitter is the largest deviation of any single tCL from tCL(avg).

t_{JIT}(duty) = Min/max of {tJIT(CH), tJIT(CL)}

where,

t_{JIT}(CH) = {tCHi- tCH(avg) where i=1 to 200}

t_{JIT}(CL) = {tCLi- tCL(avg) where i=1 to 200}

12.1.8 Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Table 100 — Definition for tCK(abs), tCH(abs), and tCL(abs)

Parameter	Symbol	Min	Unit
Absolute Clock Period	t_{CK}(abs)	tCK(avg),min + tJIT(per),min	ps
Absolute Clock HIGH Pulse Width	t_{CH}(abs)	tCH(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)
Absolute Clock LOW Pulse Width	t_{CL}(abs)	tCL(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)

NOTE 1 tCK(avg),min is expressed is ps for this table.

NOTE 2 tJIT(duty),min is a negative value.

12.2 Period Clock Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in Table 103 on page 181 and how to determine cycle time de-rating and clock cycle de-rating.

12.2.1 Clock period jitter effects on core timing parameters (tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR2 device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

12.2.1.1 Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter (tCORE).

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

12.2.1.2 Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter (tCORE).

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

12.2.2 Clock jitter effects on Command/Address timing parameters (tIS, tIH, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb)

These parameters are measured from a command/address signal (CKE, CS, CA0 - CA9) transition edge to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

12.2.3 Clock jitter effects on Read timing parameters

12.2.3.1 tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}\right)$$

For example,

if the measured jitter into a LPDDR2-800 device has tCK(avg) = 2500 ps, tJIT(per),act,min = -172 ps and tJIT(per),act,max = + 193 ps, then

tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 0.9 - (193 - 100)/2500= .8628 tCK(avg)

12.2.3.2 tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0–31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per).

12.2.3.3 tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min. Therefore tQSH(abs)min and tQSL(abs)min can be specified with tCH(abs)min and tCL(abs)min.

tQSH(abs)min = tCH(abs)min – 0.05

tQSL(abs)min = tCL(abs)min – 0.05

These parameters determine absolute Data-Valid window at the LPDDR2 device pin.

Absolute min data-valid window @ LPDDR2 device pin =

min { (tQSH(abs)min * tCK(avg)min – tDQSQmax – tQHSmax) , (tQSL(abs)min * tCK(avg)min – tDQSQmax – tQHSmax) }

This minimum data-valid window shall be met at the target frequency regardless of clock jitter.

12.2.3.4 tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.

tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

12.2.4 Clock jitter effects on Write timing parameters

12.2.4.1 tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

12.2.4.2 tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

12.2.4.3 tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act,min - tJIT(per),allowed,min}{tCK(avg)}$$

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}$$

For example,

if the measured jitter into a LPDDR2-800 device has tCK(avg)= 2500 ps, tJIT(per),act,min= -172 ps and tJIT(per),act,max= + 193 ps, then

tDQSS,(min,derated) = 0.75 +(tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-172 + 100)/2500 = .7788 tCK(avg)

and

tDQSS,(max,derated) = 1.25 + (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (193 - 100)/2500 = 1.2128 tCK(avg)

12.3 LPDDR2-SX Refresh Requirements by Device Density

Table 101 — LPDDR2-S2 Refresh Requirement Parameters (per density)

Parameter		Symbol	64 Mb	128 Mb	256 Mb	512 Mb	1 Gb	2 Gb	4 Gb	8 Gb	Unit
Number of Banks			4						8		
Refresh Window Tcase ≤ 85°C		t_{REFW}	32								ms
Refresh Window 85°C < Tcase ≤ 105°C		t_{REFW}	8								ms
Required number of REFRESH commands (min)		R	2,048	2,048	4,096	4,096	4096	8,192	8,192	8,192	
average time between REFRESH commands (for reference only) Tcase ≤ 85°C	REFab	t_{REFI}	15.6	15.6	7.8	7.8	7.8	3.9	3.9	3.9	us
	REFpb	t_{REFIpb}	(REFpb not allowed below 4Gb)						0.4875	0.4875	us
Refresh Cycle time		t_{RFCab}	90	90	90	90	130	130	130	210	ns
Per Bank Refresh Cycle time		t_{RFCpb}	NA						60	90	ns
Burst Refresh Window = 4 x 8 x t_{RFCab}		t_{REFBW}	2.88	2.88	2.88	2.88	4.16	4.16	4.16	6.72	us

Table 102 — LPDDR2-S4 Refresh Requirement Parameters (per density)

Parameter		Symbol	64 Mb	128 Mb	256 Mb	512 Mb	1 Gb	2 Gb	4 Gb	8 Gb	Unit
Number of Banks			4				8				
Refresh Window Tcase ≤ 85°C		t_{REFW}	32								ms
Refresh Window 85°C < Tcase ≤ 105°C		t_{REFW}	8								ms
Required number of REFRESH commands (min)		R	2,048	2,048	4,096	4,096	4,096	8,192	8,192	8,192	
average time between REFRESH commands (for reference only) Tcase ≤ 85°C	REFab	t_{REFI}	15.6	15.6	7.8	7.8	7.8	3.9	3.9	3.9	us
	REFpb	t_{REFIpb}	(REFpb not allowed below 1 Gb.)				0.975	0.4875	0.4875	0.4875	us
Refresh Cycle time		t_{RFCab}	90	90	90	90	130	130	130	210	ns
Per Bank Refresh Cycle time		t_{RFCpb}	NA				60	60	60	90	ns
Burst Refresh Window = 4 x 8 x t_{RFCab}		t_{REFBW}	2.88	2.88	2.88	2.88	4.16	4.16	4.16	6.72	us

12.4 AC Timings

Table 103 — LPDDR2 AC Timing Table[*9]

Parameter	Symbol	min max	min t_{CK}	LPDDR2										Unit
				1066	933	800	667	533	466[*5]	400	333	266[*5]	200[*5]	
Max. Frequency[*4]		~		533	466	400	333	266	233	200	166	133	100	MHz
Clock Timing														
Clock cycle time	t_{CK}	min		1.875	2.15	2.5	3	3.75	4.3	5	6	7.5	10	ns
		max		100										ns
Clock high-level width	t_{CH}	min		0.45										t_{CK}
		max		0.55										
Clock low-level width	t_{CL}	min		0.45										t_{CK}
		max		0.55										
Clock half period	t_{HP}	=		min {t_{CH}, t_{CL}}										t_{CK}
Average Clock Period	t_{CK}(avg)	min		1.875	2.15	2.5	3	3.75	4.3	5	6	7.5	10	ns
		max		100										
Average high pulse width	t_{CH}(avg)	min		0.45										t_{CK}(avg)
		max		0.55										
Average low pulse width	t_{CL}(avg)	min		0.45										t_{CK}(avg)
		max		0.55										
Absolute Clock Period	t_{CK}(abs)	min		t_{CK}(avg)min + t_{JIT}(per),min										ps
Absolute clock HIGH pulse width (with allowed jitter)	t_{CH}(abs), allowed	min		0.43										t_{CK}(avg)
Absolute clock LOW pulse width (with allowed jitter)	t_{CL}(abs), allowed	min		0.43										t_{CK}(avg)
Clock Period Jitter (with allowed jitter)	t_{JIT}(per), allowed	min		-90	-95	-100	-110	-120	-130	-140	-150	-180	-250	ps
		max		90	95	100	110	120	130	140	150	180	250	
Cumulative error across 2 cycles	t_{ERR}(2per), allowed	min		-132	-140	-147	-162	-177	-191	-206	-221	-265	-368	ps
		max		132	140	147	162	177	191	206	221	265	368	
Cumulative error across 3 cycles	t_{ERR}(3per), allowed	min		-157	-166	-175	-192	-210	-227	-245	-262	-314	-437	ps
		max		157	166	175	192	210	227	245	262	314	437	
Cumulative error across 4 cycles	t_{ERR}(4per), allowed	min		-175	-185	-194	-214	-233	-253	-272	-291	-350	-486	ps
		max		175	185	194	214	233	253	272	291	350	486	
Cumulative error across 5 cycles	t_{ERR}(5per), allowed	min		-188	-199	-209	-230	-251	-272	-293	-314	-377	-524	ps
		max		188	199	209	230	251	272	293	314	377	524	
Cumulative error across 6 cycles	t_{ERR}(6per), allowed	min		-200	-211	-222	-244	-266	-288	-311	-333	-399	-555	ps
		max		200	211	222	244	266	288	311	333	399	555	

Table 103 — LPDDR2 AC Timing Table[*9]

Parameter	Symbol	min max	min t_{CK}	LPDDR2										Unit
				1066	933	800	667	533	466[*5]	400	333	266[*5]	200[*5]	
Cumulative error across 7 cycles	t_{ERR}(7per), allowed	min		-209	-221	-232	-256	-279	-302	-325	-348	-418	-581	ps
		max		209	221	232	256	279	302	325	348	418	581	
Cumulative error across 8 cycles	t_{ERR}(8per), allowed	min		-217	-229	-241	-256	-290	-314	-338	-362	-435	-604	ps
		max		217	229	241	256	290	314	338	362	435	604	
Cumulative error across 9 cycles	t_{ERR}(9per), allowed	min		-224	-237	-249	-274	-299	-324	-349	-374	-449	-624	ps
		max		224	237	249	274	299	324	349	374	449	624	
Cumulative error across 10 cycles	t_{ERR}(10per), allowed	min		-231	-244	-257	-282	-308	-334	-359	-385	-462	-641	ps
		max		231	244	257	282	308	334	359	385	462	641	
Cumulative error across 11 cycles	t_{ERR}(11per), allowed	min		-237	-250	-263	-289	-316	-342	-368	-395	-474	-658	ps
		max		237	250	263	289	316	342	368	395	474	658	
Cumulative error across 12 cycles	t_{ERR}(12per), allowed	min		-242	-256	-269	-296	-323	-350	-377	-403	-484	-672	ps
		max		242	256	269	296	323	350	377	403	484	672	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	t_{ERR}(nper), allowed	min		t_{ERR}(nper),allowed,min = (1 + 0.68ln(n)) * t_{JIT}(per),allowed,min										ps
		max		t_{ERR}(nper),allowed,max = (1 + 0.68ln(n)) * t_{JIT}(per),allowed,max										

Table 103 — LPDDR2 AC Timing Table[*9]

Parameter	Symbol	min max	min t_{CK}	LPDDR2 1066	933	800	667	533	466[*5]	400	333	266[*5]	200[*5]	Unit
ZQ Calibration Parameters														
Initialization Calibration Time	t_{ZQINIT}	max		1										us
Long Calibration Time	t_{ZQCL}	max		360										ns
Short Calibration Time	t_{ZQCS}	max		90										ns
Calibration Reset Time	$t_{ZQRESET}$	max	3	50										ns
Read Parameters[*14]														
DQS output access time from CK_t/CK_c	t_{DQSCK}	min		2500										ps
		max		5500										
DQSCK Delta Short[*18]	$t_{DQSCKDS}$	max		330	380	450	540	670	770	900	1080	1350	1800	ps
DQSCK Delta Medium[*19]	$t_{DQSCKDM}$	max		680	780	900	1050	1350	1550	1800	1900	2000	2100	ps
DQSCK Delta Long[*20]	$t_{DQSCKDL}$	max		920	1050	1200	1400	1800	2100	2400	-	-	-	ps
DQS - DQ skew	t_{DQSQ}	max		200	220	240	280	340	370	400	500	600	700	ps
Data hold skew factor	t_{QHS}	max		230	260	280	340	400	450	480	600	750	1000	ps
DQS Output High Pulse Width	t_{QSH}	min		t_{CH} - 0.05										t_{CK}
DQS Output Low Pulse Width	t_{QSL}	min		t_{CL} - 0.05										t_{CK}
Data Half Period	t_{QHP}	min		min(t_{QSH}, t_{QSL})										t_{CK}
DQ / DQS output hold time from DQS	t_{QH}	min		t_{QHP} - t_{QHS}										ps
Read preamble[*15,*16]	t_{RPRE}	min		0.9										t_{CK}
Read postamble[*15,*17]	t_{RPST}	min		t_{CL} - 0.05										t_{CK}
DQS low-Z from clock[*15]	$t_{LZ(DQS)}$	min		$t_{DQSCK(MIN)}$ - 300										ps
DQ low-Z from clock[*15]	$t_{LZ(DQ)}$	min		$t_{DQSCK(MIN)}$ - (1.4 * $t_{QHS(MAX)}$)										ps
DQS high-Z from clock[*15]	$t_{HZ(DQS)}$	max		$t_{DQSCK(MAX)}$ - 100										ps
DQ high-Z from clock[*15]	$t_{HZ(DQ)}$	max		$t_{DQSCK(MAX)}$ + (1.4 * $t_{DQSQ(MAX)}$)										ps

Table 103 — LPDDR2 AC Timing Table[*9]

Parameter	Symbol	min max	min t_{CK}	LPDDR2										Unit
				1066	933	800	667	533	466[*5]	400	333	266[*5]	200[*5]	
Write Parameters[*14]														
DQ and DM input hold time (Vref based)	t_{DH}	min		210	235	270	350	430	450	480	600	750	1000	ps
DQ and DM input setup time (Vref based)	t_{DS}	min		210	235	270	350	430	450	480	600	750	1000	ps
DQ and DM input pulse width	t_{DIPW}	min		0.35										t_{CK}
Write command to 1st DQS latching transition	t_{DQSS}	min		0.75										t_{CK}
		max		1.25										
DQS input high-level width	t_{DQSH}	min		0.4										t_{CK}
DQS input low-level width	t_{DQSL}	min		0.4										t_{CK}
DQS falling edge to CK setup time	t_{DSS}	min		0.2										t_{CK}
DQS falling edge hold time from CK	t_{DSH}	min		0.2										t_{CK}
Write postamble	t_{WPST}	min		0.4										t_{CK}
Write preamble	t_{WPRE}	min		0.35										t_{CK}

Table 103 — LPDDR2 AC Timing Table[*9]

Parameter	Symbol	min max	min t_{CK}	LPDDR2										Unit
				1066	933	800	667	533	466[*5]	400	333	266[*5]	200[*5]	
CKE Input Parameters														
CKE min. pulse width (high and low pulse width)	t_{CKE}	min	3	3										t_{CK}
CKE input setup time	t_{ISCKE}*2	min		0.25										t_{CK}
CKE input hold time	t_{IHCKE}*3	min		0.25										t_{CK}
Command Address Input Parameters[*14]														
Address and control input setup time	t_{IS}*1	min		220	250	290	370	460	520	600	740	900	1150	ps
Address and control input hold time	t_{IH}*1	min		220	250	290	370	460	520	600	740	900	1150	ps
Address and control input pulse width	t_{IPW}	min		0.40										t_{CK}
Boot Parameters (10 MHz - 55 MHz)[*8,10,11]														
Clock Cycle Time	t_{CKb}	max	-	100										ns
		min		18										
CKE Input Setup Time	t_{ISCKEb}	min	-	2.5										ns
CKE Input Hold Time	t_{IHCKEb}	min	-	2.5										ns
Address & Control Input Setup Time	t_{ISb}	min	-	1150										ps
Address & Control Input Hold Time	t_{IHb}	min	-	1150										ps
DQS Output Data Access Time from CK_t/CK_c	t_{DQSCKb}	min	-	2.0										ns
		max		10.0										
Data Strobe Edge to Ouput Data Edge t_{DQSQb} - 1.2	t_{DQSQb}	max	-	1.2										ns
Data Hold Skew Factor	t_{QHSb}	max	-	1.2										ns
Mode Register Parameters														
MODE REGISTER Write command period	t_{MRW}	min	5	5										t_{CK}
Mode Register Read command period	t_{MRR}	min	2	2										t_{CK}

Table 103 — LPDDR2 AC Timing Table[*9]

Parameter	Symbol	min max	min t_{CK}	LPDDR2 1066	933	800	667	533	466[*5]	400	333	266[*5]	200[*5]	Unit
LPDDR2 SDRAM Core Parameters[*12]														
Read Latency	RL	min	3	8	7	6	5	4		3	3			t_{CK}
Write Latency	WL	min	1	4	4	3	2	2		1	1			t_{CK}
ACTIVE to ACTIVE command period	t_{RC}	min		$t_{RAS} + t_{RPab}$ (with all-bank Precharge) $t_{RAS} + t_{RPpb}$ (with per-bank Precharge)										ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	t_{CKESR}	min	3	15						15				ns
Self refresh exit to next valid command delay	t_{XSR}	min	2	t_{RFCab} + 10										ns
Exit power down to next valid command delay	t_{XP}	min	2	7.5						7.5				ns
LPDDR2-S4 CAS to CAS delay	t_{CCD}	min	2	2						2				t_{CK}
LPDDR2-S2 CAS to CAS delay	t_{CCD}	min	1	1						1				t_{CK}
Internal Read to Precharge command delay	t_{RTP}	min	2	7.5						7.5				ns
RAS to CAS Delay	t_{RCD}	Fast	3	15						15				ns
		Typ	3	18						18				ns
		Slow	3	24						24				ns
Row Precharge Time (single bank)	t_{RPpb}	Fast	3	15						15				ns
		Typ	3	18						18				ns
		Slow	3	24						24				ns
Row Precharge Time (all banks)	t_{RPab} 4-bank	Fast	3	15						15				ns
		Typ	3	18						18				ns
		Slow	3	24						24				ns
Row Precharge Time (all banks)	t_{RPab} 8-bank	Fast	3	18						18				ns
		Typ	3	21						21				ns
		Slow	3	27						27				ns
Row Active Time	t_{RAS}	min	3	42						42				ns
		max	-	70						70				us
Write Recovery Time	t_{WR}	min	3	15						15				ns
Internal Write to Read Command Delay	t_{WTR}	min	2	7.5						10				ns
Active bank A to Active bank B	t_{RRD}	min	2	10						10				ns
Four Bank Activate Window	t_{FAW}	min	8	50						50	60			ns
Minimum Deep Power Down Time	t_{DPD}	min		500						500				us

Table 103 — LPDDR2 AC Timing Table[*9]

Parameter	Symbol	min max	min t_{CK}	LPDDR2										Unit
				1066	933	800	667	533	466[*5]	400	333	266[*5]	200[*5]	
LPDDR2 NVM Core Parameters[*12]														
Read Latency	RL	min	3	8	7	6	5	4		3				t_{CK}
Write Latency	WL	min	1	4		3	2			1				t_{CK}
Activate to Read/Write command period (min)	t_{RCDMIN}	min		15										ns
		max		255										ns
Activate to Read/Write command period	t_{RCD}[*6, *21]	min	5	t_{RCDMIN}										ns
Activate to Activate command period (different Row Buffer)	t_{RRD}[*7, *21]	min	5	t_{RCDMIN}										ns
Activate to Activate command period (same Row Buffer)	t_{RC}[*21]	min	5	t_{RCDMIN}										ns
CAS to CAS delay	t_{CCD}	min	2	2										t_{CK}
Write recovery time before Activate	t_{WRA}	min	3	15										ns
Internal write to read command delay	t_{WTR}	min	2	7.5					10					ns
Preactive to Activate command period	t_{RP}	min	3	3										t_{CK}
Activate to Preactive command period	t_{RAS}[*21]	min	5	t_{RCDMIN}										ns
Exit power down to next valid command delay	t_{XP}	min	2	10										ns

Table 103 — LPDDR2 AC Timing Table*9

Parameter	Symbol	min max	min t_{CK}	LPDDR2										Unit
				1066	933	800	667	533	466*5	400	333	266*5	200*5	
LPDDR2 Temperature De-Rating														
t_{DQSCK} De-Rating	t_{DQSCK} (Derated)	max		5620	6000									ps
Core Timings Temperature De-Rating for SDRAM	t_{RCD} (Derated)	min		t_{RCD} + 1.875										ns
	t_{RC} (Derated)	min		t_{RC} + 1.875										ns
	t_{RAS} (Derated)	min		t_{RAS} + 1.875										ns
	t_{RP} (Derated)	min		t_{RP} + 1.875										ns
	t_{RRD} (Derated)	min		t_{RRD} + 1.875										ns
Core Timings Temperature De-Rating for NVM*22	t_{RCD} (Derated)	min		t_{RCD} + $t_{NVMDERATING}$										ns
	t_{RC} (Derated)	min		t_{RC} + $t_{NVMDERATING}$										ns
	t_{RAS} (Derated)	min		t_{RAS} + $t_{NVMDERATING}$										ns
	t_{RRD} (Derated)	min		t_{RRD} + $t_{NVMDERATING}$										ns

NOTE 1 Input set-up/hold time for signal(CA0 ~ 9, CS_n)

NOTE 2 CKE input setup time is measured from CKE reaching high/low voltage level to CK_t/CK_c crossing.

NOTE 3 CKE input hold time is measured from CK_t/CK_c crossing to CKE reaching high/low voltage level .

NOTE 4 Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.

NOTE 5 The speed bins 466, 266, and 200 are for NVM only.

NOTE 6 For NVM, t_{RCDMIN} defines the minimum tRCD value. Vendors may choose a minimum tRCD value within the range of t_{RCDMIN}.

NOTE 7 For NVM, vendors may choose a value for tRRD that is less than or equal to the tRCD value.

NOTE 8 To guarantee device operation before the LPDDR2 device is configured a number of AC boot timing parameters are defined in the Table 103 on page 181 . Boot parameter symbols have the letter **b** appended, e.g. tCK during boot is $t_{CK\mathbf{b}}$.

NOTE 9 Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.

NOTE 10 The SDRAM/NVM will set some Mode register default values upon receiving a RESET (MRW) command as specified in "Mode Register Definition" on page 23.

NOTE 11 The output skew parameters are measured with Ron default settings into the reference load.

NOTE 12 The min tCK column applies only when tCK is greater than 6ns for LPDDR2-SX devices and 10ns for LPDDR2-N devices.

NOTE 13 All AC timings assume an input slew rate of 1V/ns.

NOTE 14 Read, Write, and Input Setup and Hold values are referenced to Vref.

NOTE 15 For low-to-high and high-to-low transitions, the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure 119 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

12.4 AC Timings (cont'd)

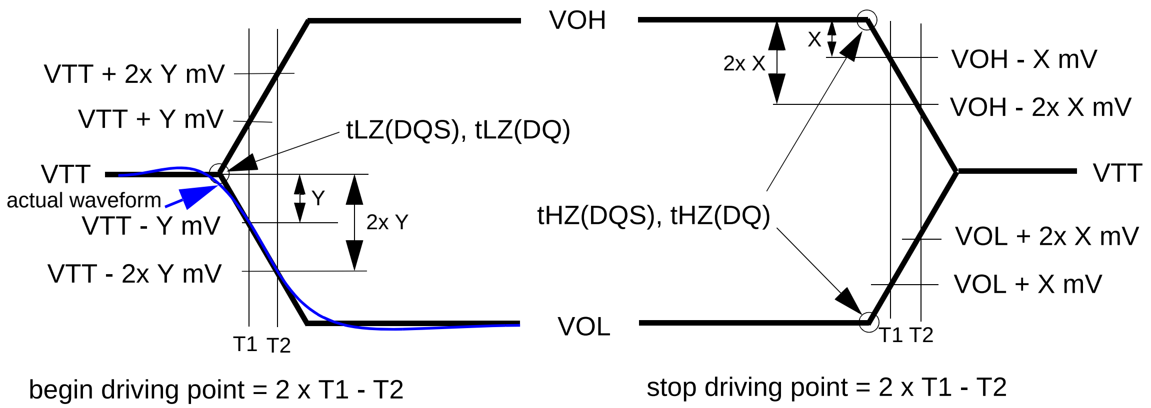


Figure 119 — HSUL_12 Driver Output Reference Load for Timing and Slew Rate

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS_t-DQS_c.

NOTE 16 Measured from the start driving of DQS_t - DQS_c to the start driving the first rising strobe edge.

NOTE 17 Measured from the from start driving the last falling strobe edge to the stop driving DQS_t - DQS_c.

NOTE 18 tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a contiguous sequence of bursts within a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.

NOTE 19 tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 1.6us rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.

NOTE 20 tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.

NOTE 21 Min tCK of 5 clocks is valid when the Overlay Window is disabled. Refer to vendor datasheets for min tCK when the Overlay Window is enabled.

NOTE 22 For LPDDR2-NVM De-rating, the de-rating value found in MR20 OP5:OP4 ($\mathbf{t}_{NVMDERATING}$) shall be used to de-rate the following parameters: tRCD, tRRD, tRAS, and tRC.

12.5 CA and CS_n Setup, Hold and Derating

For all input signals (CA and CS_n) the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see Table 104) to the ΔtIS and ΔtIH derating value (see Table 105 and Table 106) respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure Figure 120). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 122).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of $V_{REF(dc)}$. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 121). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 123).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 107).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in Table 105, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 104 — CA and CS_n Setup and Hold Base-Values for 1V/ns

unit [ps]	LPDDR2						reference
	1066	933	800	667	533	466	
tIS(base)	0	30	70	150	240	300	$V_{IH/L(ac)}$ = VREF(dc) +/-220mV
tIH(base)	90	120	160	240	330	390	$V_{IH/L(dc)}$ = VREF(dc) +/-130mV

unit [ps]	LPDDR2				reference
	400	333	266	200	
tIS(base)	300	440	600	850	$V_{IH/L(ac)}$ = VREF(dc) +/-300mV
tIH(base)	400	540	700	950	$V_{IH/L(dc)}$ = VREF(dc) +/-200mV

NOTE 1 ac/dc referenced for 1V/ns CA and CS_n slew rate and 2V/ns differential CK_t-CK_c slew rate.

12.5 CA and CS_n Setup, Hold and Derating (cont'd)

Table 105 — Derating values LPDDR2 tIS/tIH - ac/dc based AC220

ΔtIS, ΔtIH derating in [ps] AC/DC based AC220 Threshold -> VIH(ac)=VREF(dc)+220mV, VIL(ac)=VREF(dc)-220mV DC100 Threshold -> VIH(dc)=VREF(dc)+130mV, VIL(dc)=VREF(dc)-130mV																	
		CK_t,CK_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

NOTE 1 Cell contents shaded in red are defined as 'not supported'.

Table 106 — Derating values LPDDR2 tIS/tIH - ac/dc based - AC300

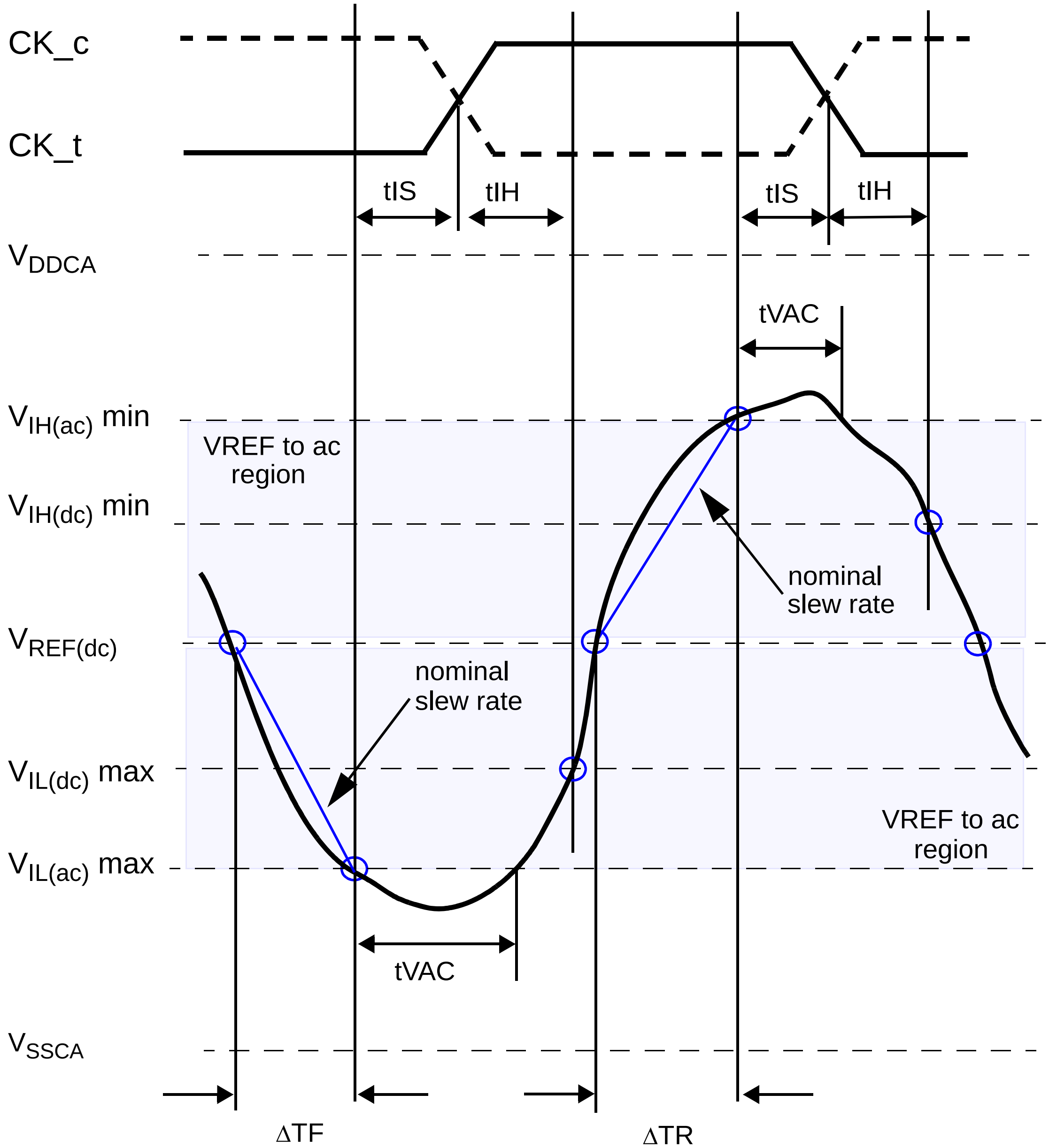
ΔtIS, ΔtIH derating in [ps] AC/DC based AC300 Threshold -> VIH(ac)=VREF(dc)+300mV, VIL(ac)=VREF(dc)-300mV DC200 Threshold -> VIH(dc)=VREF(dc)+200mV, VIL(dc)=VREF(dc)-200mV																	
		CK_t,CK_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

NOTE 1 Cell contents shaded in red are defined as 'not supported'.

Table 107 — Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate [V/ns]	t_{VAC} @ 300mV [ps]		t_{VAC} @ 220mV [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
< 0.5	0	-	150	-

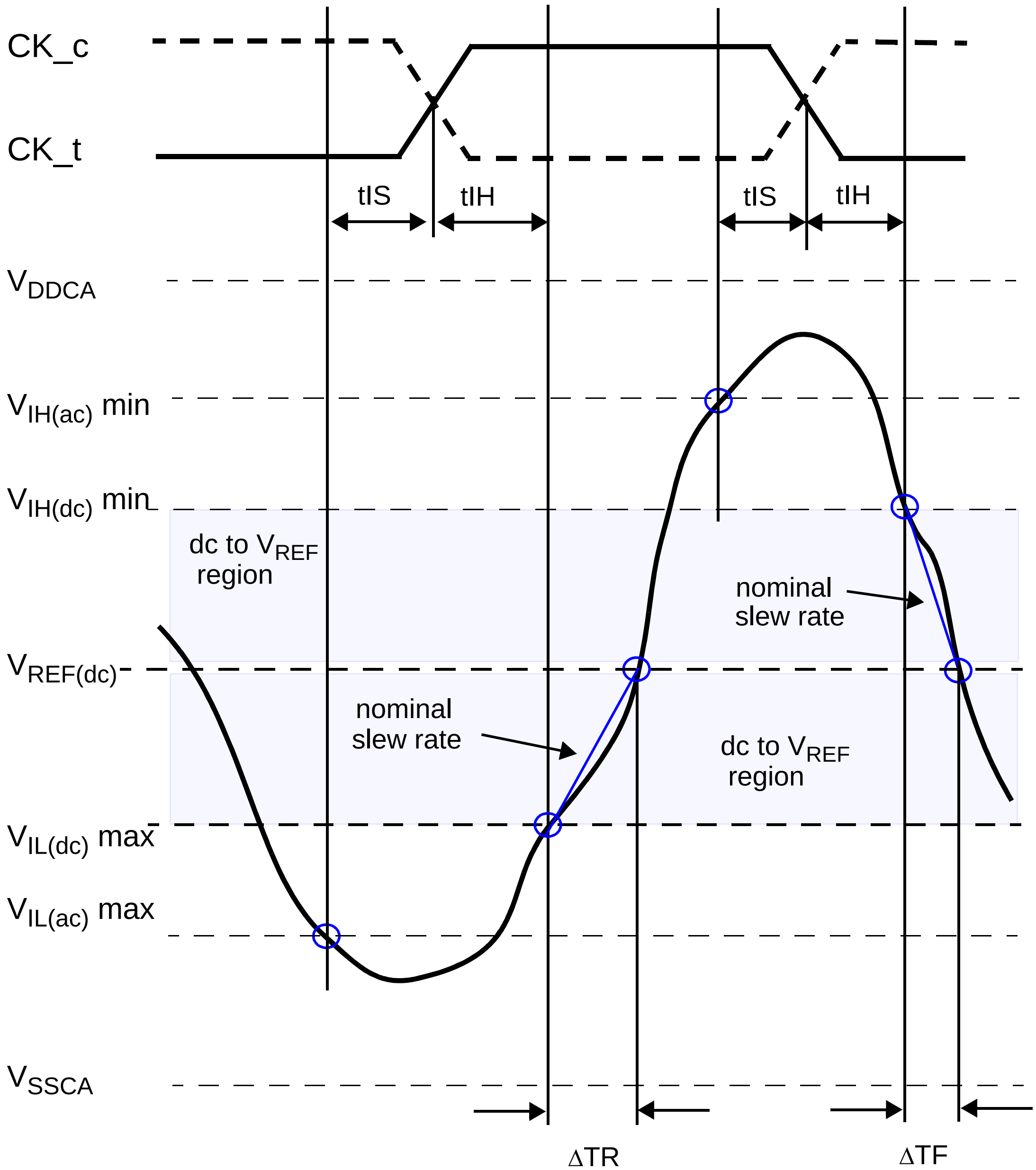
12.5 CA and CS_n Setup, Hold and Derating (cont'd)



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}\text{max}}{\Delta TF} \qquad \text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}\text{min} - V_{REF(dc)}}{\Delta TR}$$

Figure 120 — Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} for CA and CS_n with respect to clock.

12.5 CA and CS_n Setup, Hold and Derating (cont'd)



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{\Delta TR} \qquad \text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{\Delta TF}$$

Figure 121 — Illustration of nominal slew rate for hold time t_{IH} for CA and CS_n with respect to clock

12.5 CA and CS_n Setup, Hold and Derating (cont'd)

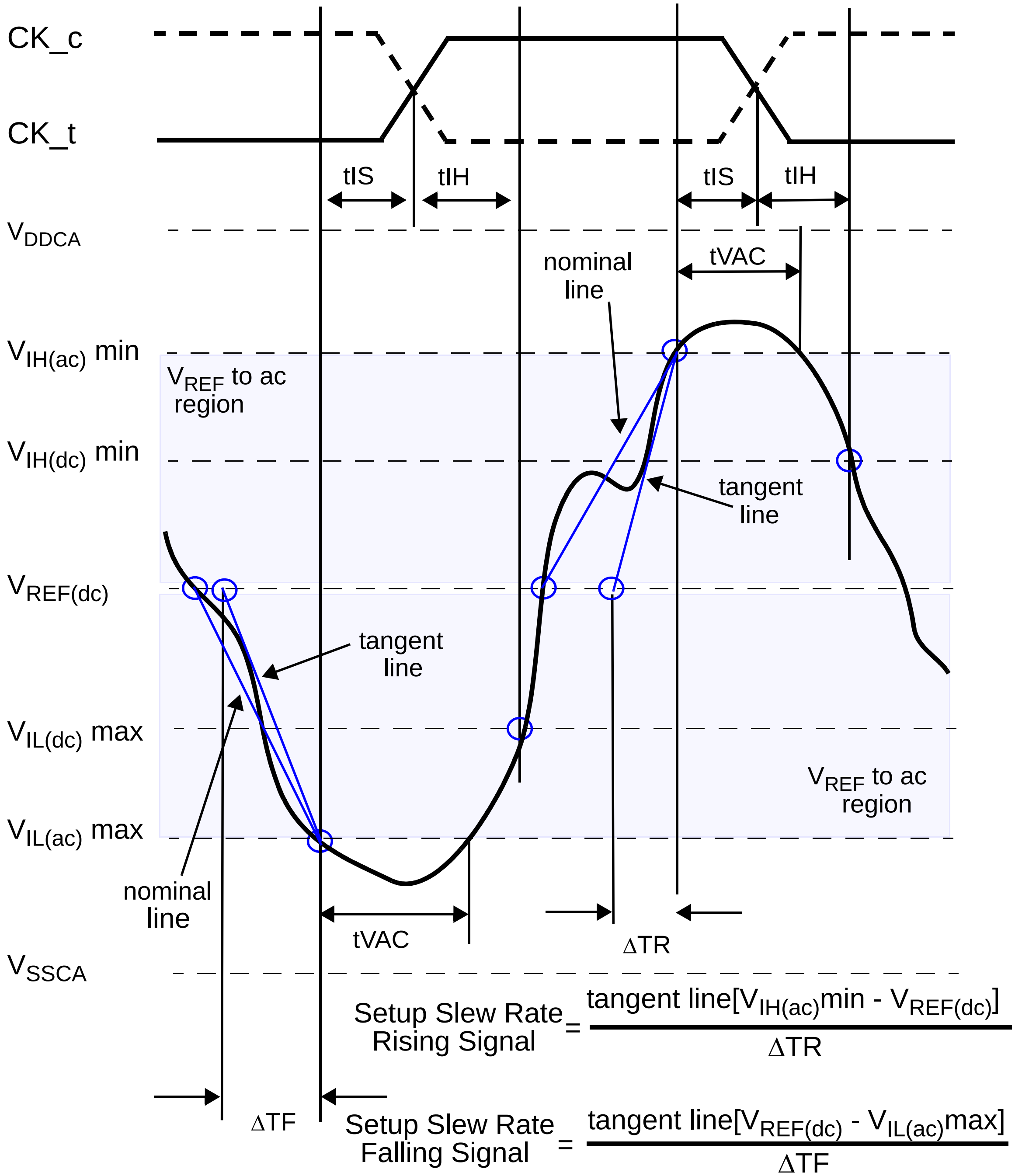
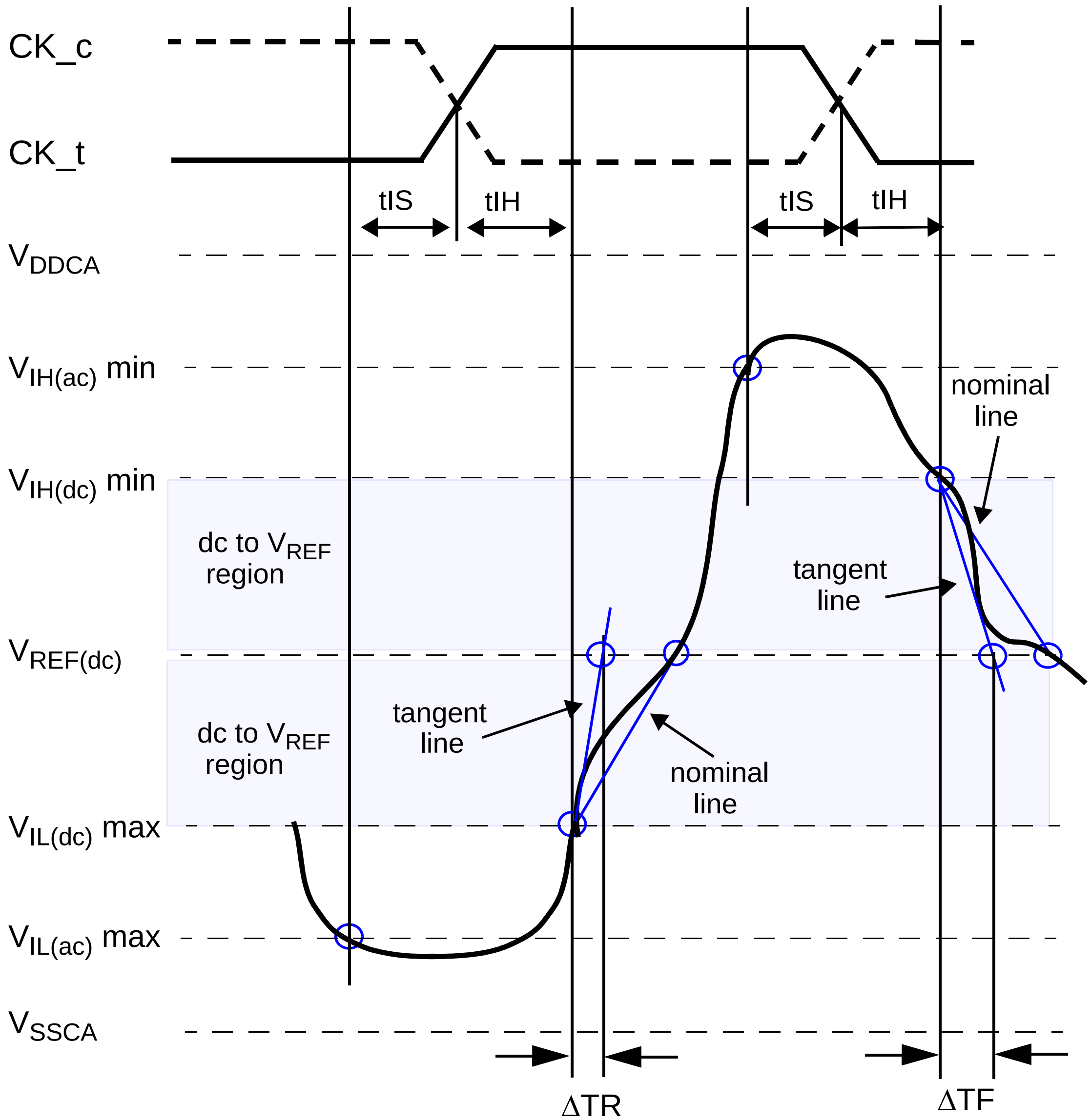


Figure 122 — Illustration of tangent line for setup time t_{IS} for CA and CS_n with respect to clock

12.5 CA and CS_n Setup, Hold and Derating (cont'd)



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(dc)} - V_{IL(dc)}\text{max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH(dc)}\text{min} - V_{REF(dc)}]}{\Delta TF}$$

Figure 123 — Illustration of tangent line for for hold time t_{IH} for CA and CS_n with respect to clock

12.6 Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 108) to the ΔtDS and ΔtDH (see Table 109 and Table 110) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max (see Figure 124). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 126).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)}$max and the first crossing of $V_{REF(dc)}$. Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)}$min and the first crossing of $V_{REF(dc)}$ (see Figure 125). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 127).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 111).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

Table 108 — Data Setup and Hold Base-Values

[ps]	LPDDR2						reference
	1066	933	800	667	533	466	
tDS(base)	-10	15	50	130	210	230	$V_{IH/L(ac)}$ = VREF(dc) +/- 220mV
tDH(base)	80	105	140	220	300	320	$V_{IH/L(dc)}$ = VREF(dc) +/- 130mV

unit [ps]	LPDDR2				reference
	400	333	266	200	
tDS(base)	180	300	450	700	$V_{IH/L(ac)}$ = VREF(dc) +/-300mV
tDH(base)	280	400	550	800	$V_{IH/L(dc)}$ = VREF(dc) +/-200mV

NOTE 1 ac/dc referenced for 1V/ns DQ, DM slew rate and 2V/ns differential DQS_t-DQS_c slew rate.

12.6 Data Setup, Hold and Slew Rate Derating (cont'd)

Table 109 — Derating values LPDDR2 tDS/tDH - ac/dc based AC220

ΔtDS, ΔDH derating in [ps] AC/DC based AC220 Threshold -> VIH(ac)=VREF(dc)+220mV, VIL(ac)=VREF(dc)-220mV DC130 Threshold -> VIH(dc)=VREF(dc)+130mV, VIL(dc)=VREF(dc)-130mV																	
		DQS_t, DQS_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ,DM Slew rate V/ns	2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
	1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
	0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
	0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
	0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
	0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

NOTE 1 Cell contents shaded in red are defined as 'not supported'.

Table 110 — Derating values LPDDR2 tDS/tDH - ac/dc based AC300

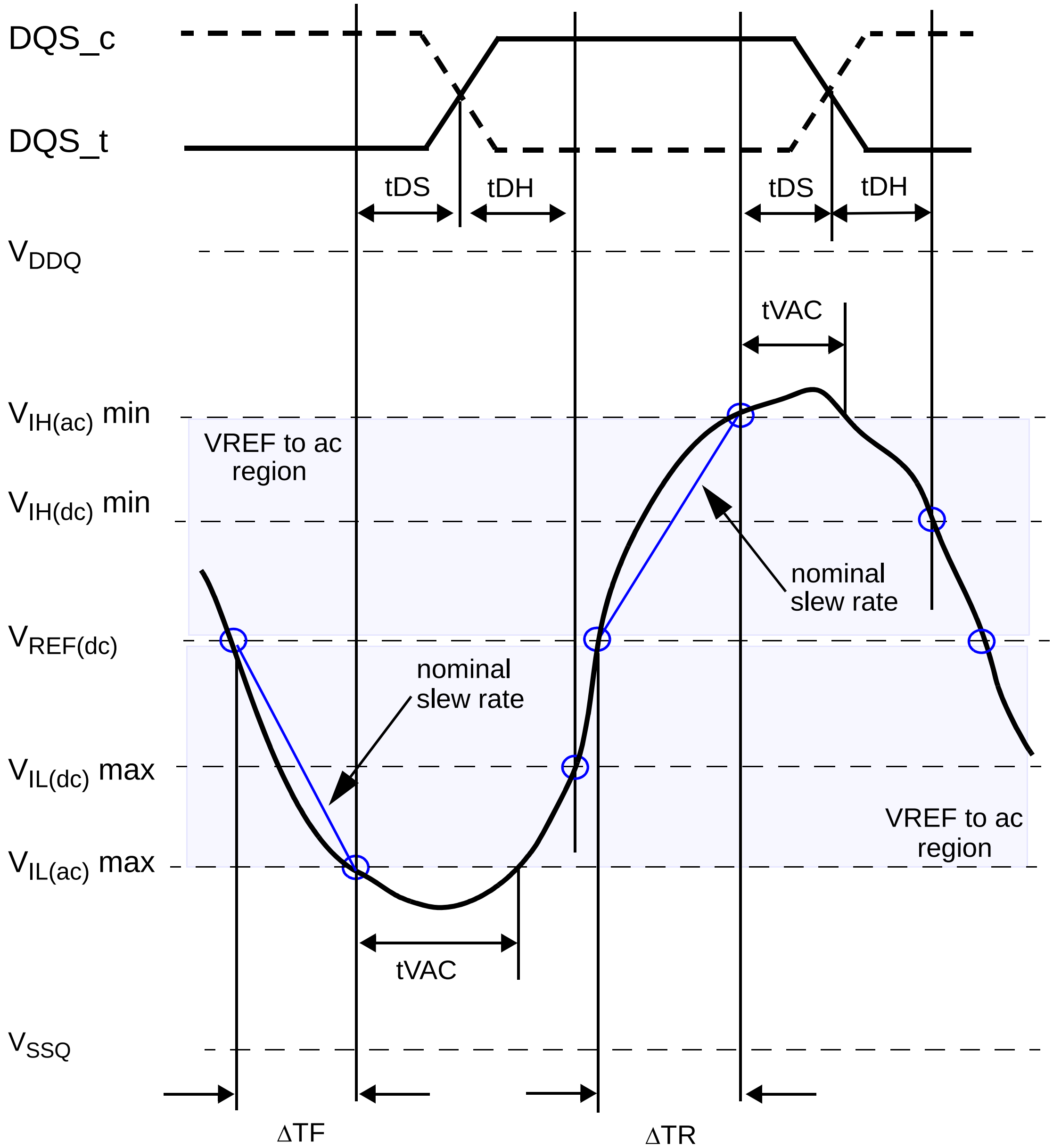
ΔtDS, ΔDH derating in [ps] AC/DC based AC300 Threshold -> VIH(ac)=VREF(dc)+300mV, VIL(ac)=VREF(dc)-300mV DC200 Threshold -> VIH(dc)=VREF(dc)+200mV, VIL(dc)=VREF(dc)-200mV																	
		DQS_t, DQS_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ,DM Slew rate V/ns	2.0	150	100	150	100	150	100	-	-	-	-	-	-	-	-	-	-
	1.5	100	67	100	67	100	67	116	83	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-4	-8	-4	-8	12	8	28	24	44	40	-	-	-	-
	0.8	-	-	-	-	-12	-20	4	-4	20	12	36	28	52	48	-	-
	0.7	-	-	-	-	-	-	-3	-18	13	-2	29	14	45	34	61	66
	0.6	-	-	-	-	-	-	-	-	2	-21	18	-5	34	15	50	47
	0.5	-	-	-	-	-	-	-	-	-	-	-12	-32	4	-12	20	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-35	-40	-11	-8

NOTE 1 Cell contents shaded in red are defined as 'not supported'.

Table 111 — Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate [V/ns]	t_{VAC} @ 300mV [ps]		t_{VAC} @ 220mV [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
< 0.5	0	-	150	-

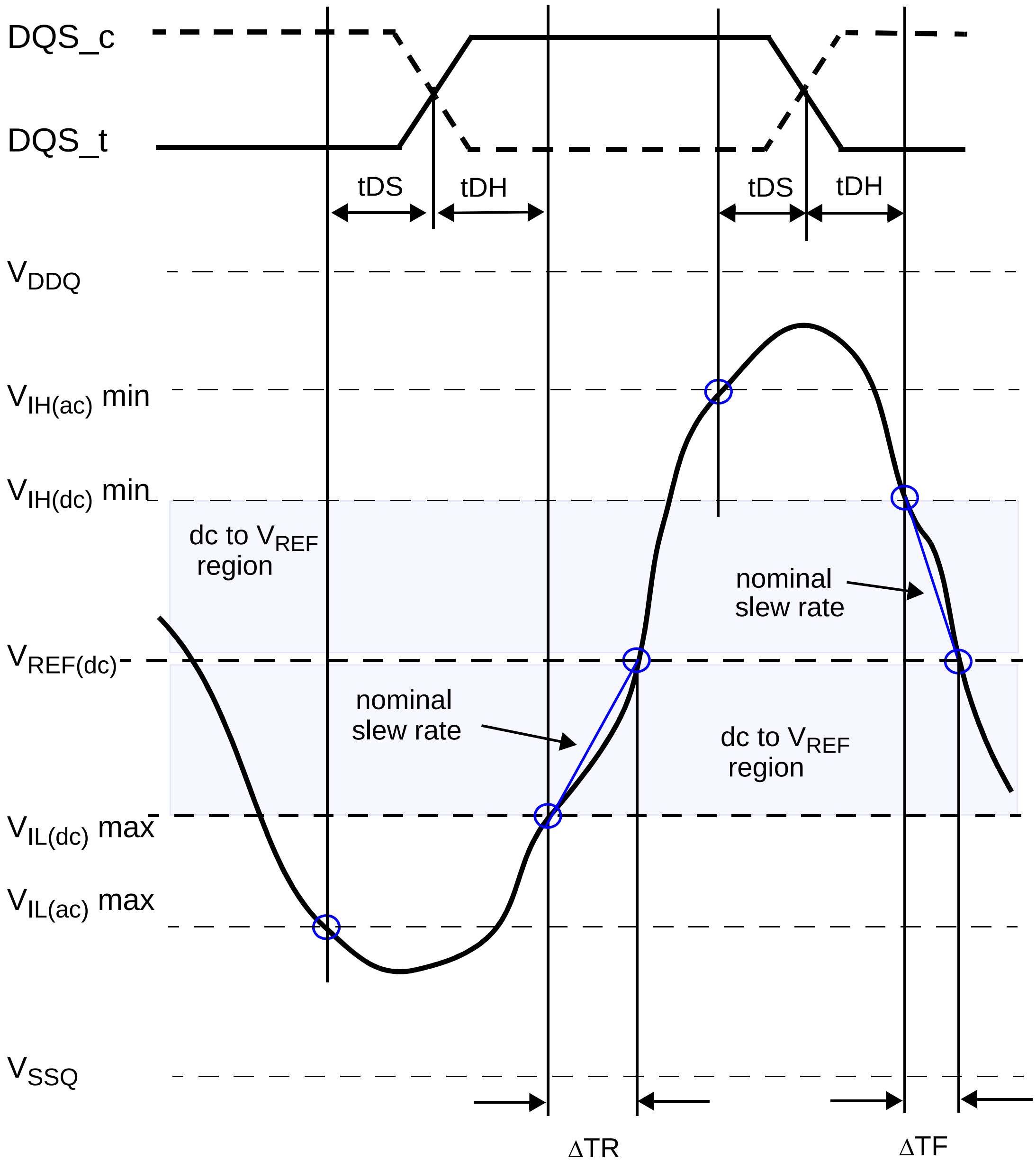
12.6 Data Setup, Hold and Slew Rate Derating (cont'd)



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF} \qquad \text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{\Delta TR}$$

Figure 124 — Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} for DQ with respect to strobe

12.6 Data Setup, Hold and Slew Rate Derating (cont'd)



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{\Delta TR} \qquad \text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{\Delta TF}$$

Figure 125 — Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe

12.6 Data Setup, Hold and Slew Rate Derating (cont'd)

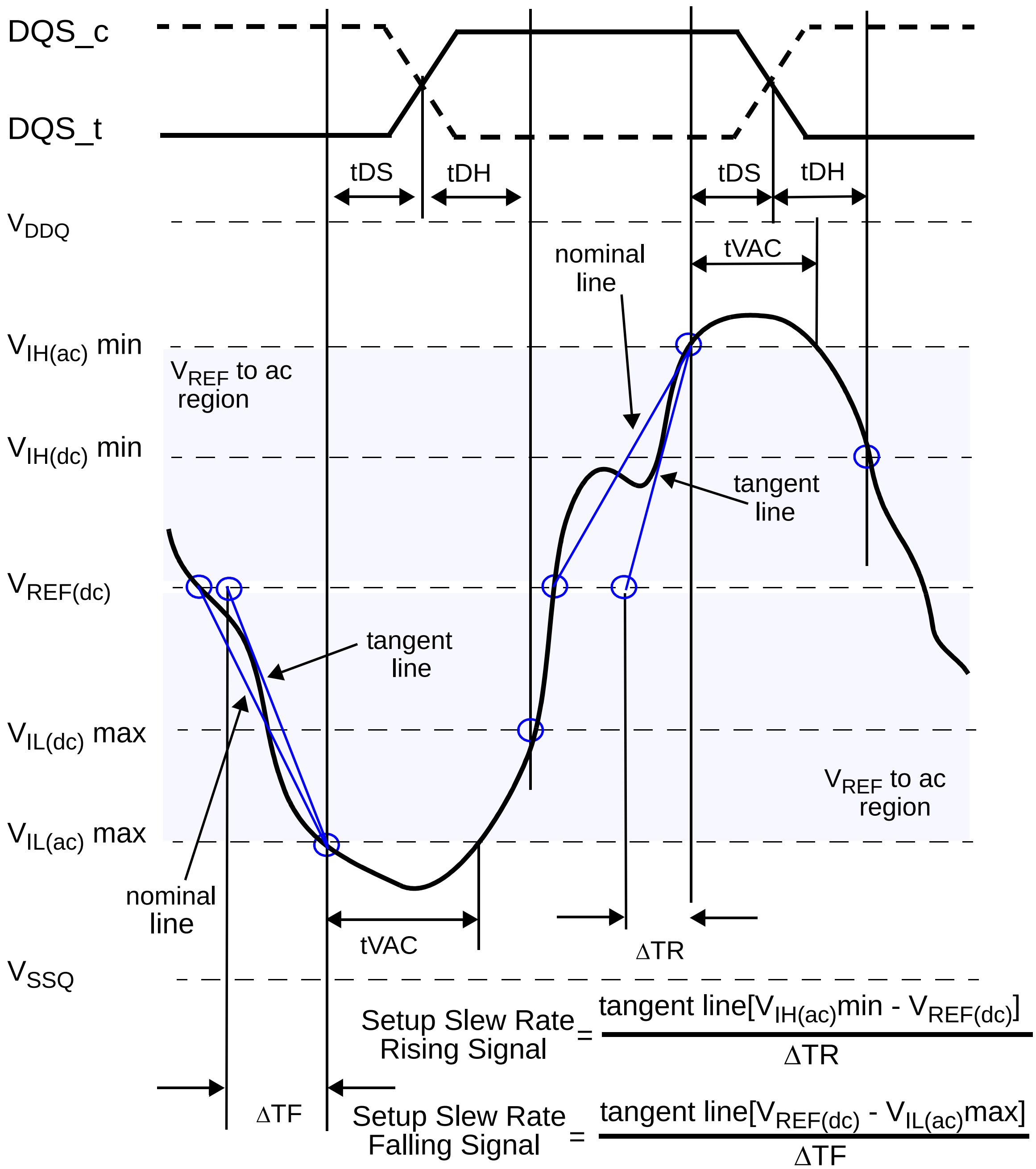
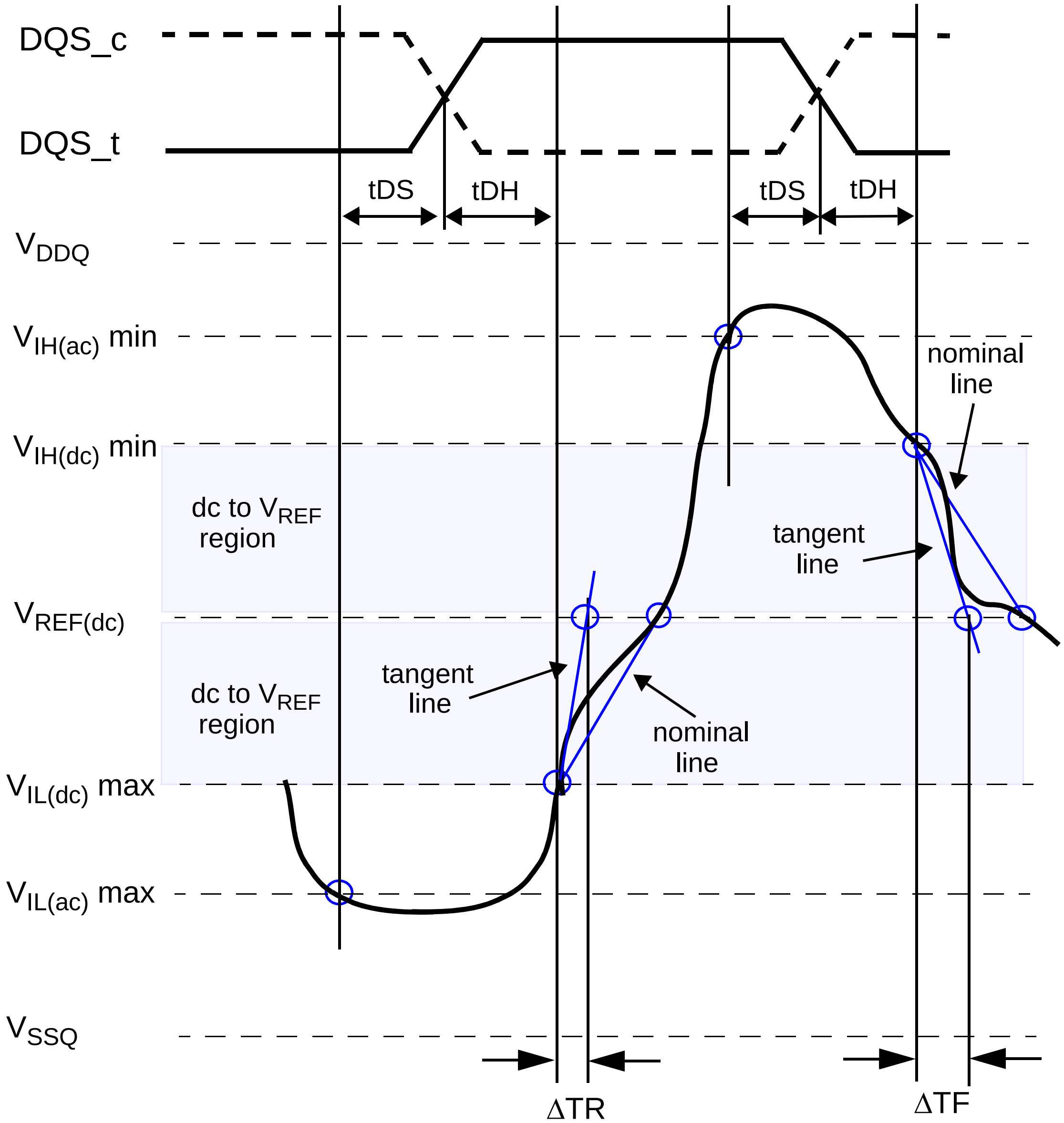


Figure 126 — Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe

12.6 Data Setup, Hold and Slew Rate Derating (cont'd)



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(dc)} - V_{IL(dc)}\text{max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH(dc)}\text{min} - V_{REF(dc)}]}{\Delta TF}$$

Figure 127 — Illustration of tangent line for for hold time t_{DH} for DQ with respect to strobe

Annex A DDR2-NVM Software Application Notes

A.1 Scope

LPDDR-NVM can be produced from a variety of memory array technologies.

The variety of technologies causes variation in software that manages the non-volatile arrays.

This application note shows a program method for a particular NV memory technology as an example of possible implementation.

A.2 Programming operations based on Programming Region

A.2.1 Introduction

This section describes a particular program method that might be implemented in some LPDDR2-NVM devices. The scope of this section is only to provide an example, other technology or product may implement a different program method.
Users should refer to the vendor memory datasheet for complete information.

Some LPDDR2-NVM devices may implement innovative features specially developed to improve the storage flexibility and efficiency of memory arrays.

A.2.2 Programming Modes

Typically, the memory array of an NVM is divided into multiple blocks. Each block can be divided in uniform programming regions.

Each programming region in a block can be configured for one of two programming modes: Control Mode or Object Mode. The programming mode is automatically set based on the data pattern when a region is first programmed. The selection of either Control Mode or Object Mode is done according to the specific needs of the system with consideration given to two types of information:

• Control Mode: Flash File System (FFS) or Header information, including frequently changing code or data. Control Mode allows for multiple programs within a programming region between block erases.

• Object Mode: Large, infrequently changing code or data, such as objects or payloads. Object Mode allows only a single program operation within each programming region between block erases.

By implementing the appropriate programming mode, software can efficiently organize how information is stored in the flash memory array.

Control Mode programming regions and Object Mode programming regions can be intermingled within the same erase block. However, the programming mode of any region within a block can be changed only after erasing the entire block.

A.2.3 Programming Regions

The following table shows the amount of Programming Regions within each block for various block sizes and 512-Byte and 1-KByte Programming region size.

Refer to the device datasheet to discover the actual size of the Programming Region.

Table 112 — Number of Programming Regions

Block Size	Programming Region Size	
	512Byte	1KByte
64KByte	128	64
128KByte	256	128
256KByte	512	256

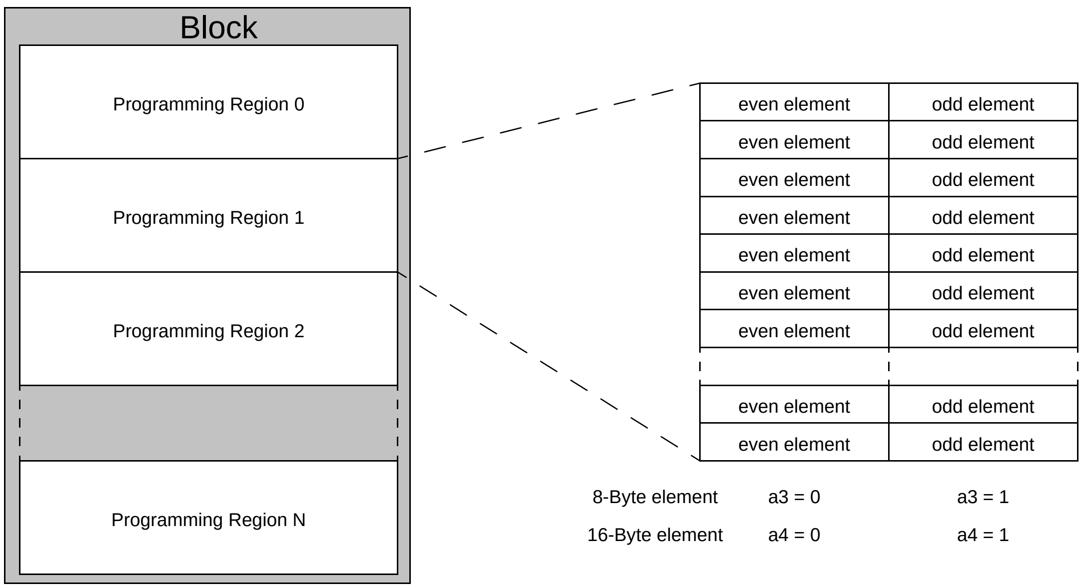
Erase operations have a Block granularity, whereas program operations have a Programming Region granularity.

The user can configure each Programming Region to be programmed either in the Control mode or in the Object mode.

A given Block can contain Programming Regions configured in the Control mode and others configured in the Object mode.

A.2.3 Programming Regions (cont'd)

Special care should be taken when selecting the programming mode for the Programming Regions because once the Programming Regions are configured their program mode cannot be changed until the entire Block is erased.



Each Programming Region is split into elements, and the element size can be either 8 Bytes or 16 Bytes. There are even elements and odd elements as defined in Table 113, where a3 and a4 are byte address bits.

Figure 128 — Programming Regions and elements

Table 113 — Even and Odd elements

Element	8-Byte	16-Byte
Even Element	a3 = 0	a4 = 0
Odd Element	a3 = 1	a4 = 1

A.2.4 Program Modes

There are two program modes, which allow the memory to store different types of data.

A.2.4.1 Control Mode

The Control mode is best suited to the storage of small, dynamic information. Typically such data is contained within one Programming Region and it will be frequently updated and/or new data will be added to it.

Programming Regions are configured in the Control mode by programming data only to the even elements. The odd elements must remain erased, that is they should not contain any zeros (Figure 128, "Programming Regions and elements" on page 203).

In a Programming Region of 1-KByte (512Byte) configured in the Control mode, only 512 Byte (256Byte) of data can be stored, in particular only even elements are writable while odd elements are reserved.

Some LPDDR2-NVM devices will allow to program each byte of the even elements only once. Some others will not have this restriction, therefore each byte might be programmed subsequently several times without erasing the Block.

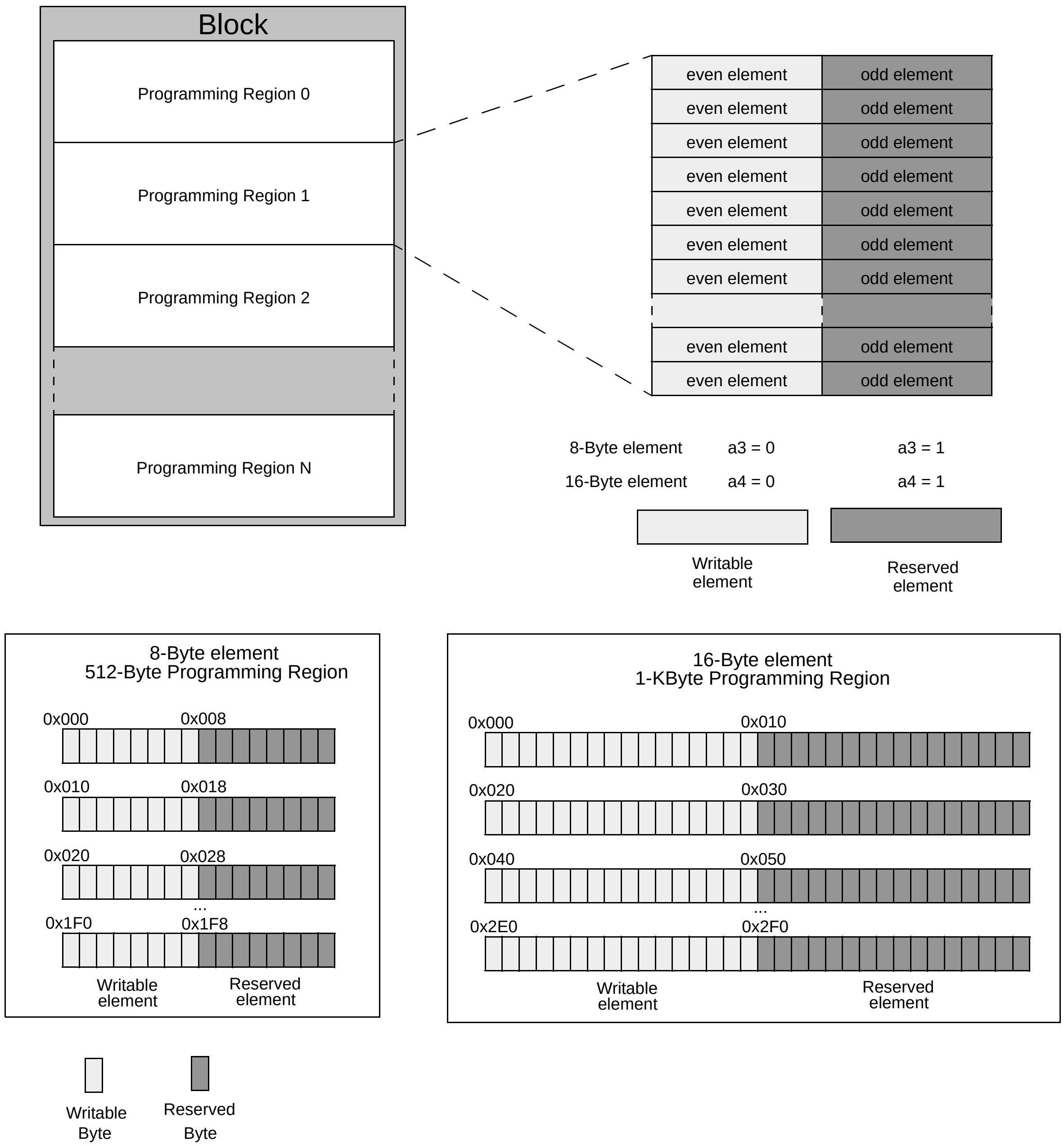
When the Programming Regions are configured in the Control mode, any program command can be used: the Single Word (if supported) or the Buffered Program command.

Once a Programming Region has been configured in the Control mode, if a zero is written to an odd element, the program operation is terminated without programming the array and an error is generated.

The Status Register bits MR22.OP4 (PSB) and MR23.OP1 (CMSB) are set to '1'. (Refer to Status Register description and to Table 114, "Relationships Between Program Commands and Programming modes" on page 206 for details).

A.2.4.1 Control Mode (cont'd)

The program mode of a Programming Region configured in the Control mode can only be changed by first erasing the Block that contains the Programming Region.



NOTE 1 Only the even elements of a Programming Region configured Control Mode are writable.
NOTE 2 Reserved elements return "0xFF" when read.

Figure 129 — Programming Regions Configured in Control Mode

A.2.4.2 Object Mode

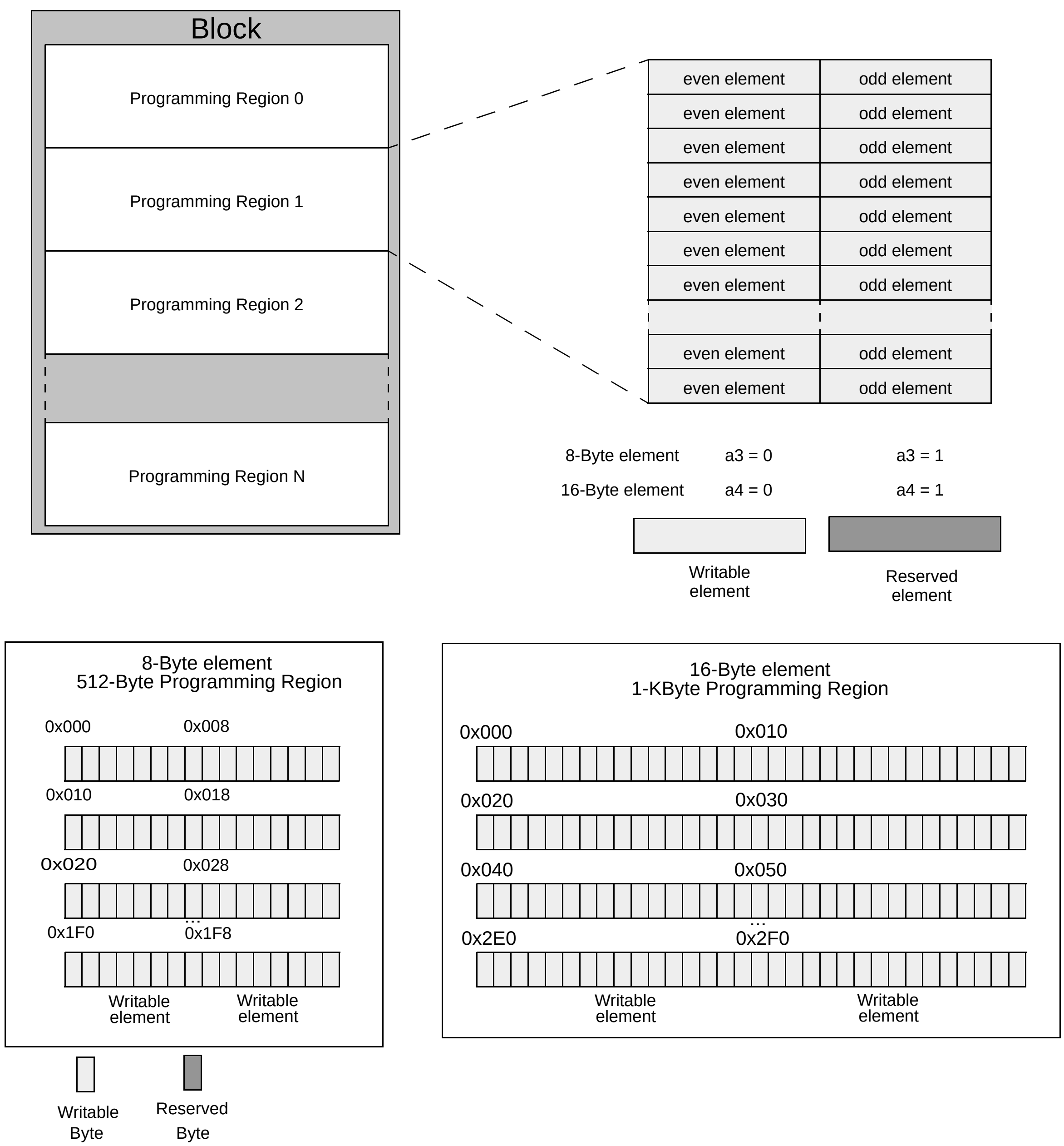
The Object mode is best suited to the storage of large, static information. In a Programming Region of 1-KByte (512-Byte) configured in the Object mode, 1-KByte (512-Byte) of data can be stored.

When a Programming Region is configured in the Object mode, it cannot be reprogrammed nor have new data added without first erasing the entire Block that contains the Programming Region.

Programming Regions are configured in the Object mode simply by programming at least one bit in one of the odd elements.

If the programmed data is smaller than 1-KByte (512Byte), the unused space remains in the erased state (all the bytes set to 0xFF), but can no longer be used to program data. See Figure 128, “Programming Regions and elements” on page 203.

Only the Buffered Program command can be used to establish an Object mode region.



NOTE: All elements of a Programming Region configured Object Mode are writable.

Figure 130 — Programming Regions Configured in Object Mode

A.2.4.3 Programming Region Configuration

Based on the current programming region status, the following table shows the next programming region status after a programming operations.

Table 114 — Relationships Between Program Commands and Programming modes

<table>
<tr><th rowspan="2">Programming Region Status</th><th colspan="4">Next Programming Region Status</th></tr>
<tr><th>Element</th><th colspan="2">Buffered Program</th><th>Single Word Program (3)</th></tr>
<tr><td rowspan="2">Erased</td><td>Even (1)</td><td>Control mode</td><td rowspan="2">Object mode</td><td>Control mode</td></tr>
<tr><td>Odd (2)</td><td>Object mode</td><td>Not allowed (4)</td></tr>
<tr><td rowspan="2">Control Program mode</td><td>Even (1)</td><td colspan="2">Control mode</td><td>Control mode</td></tr>
<tr><td>Odd (2)</td><td colspan="2">Not allowed (5)</td><td>Not allowed(4)</td></tr>
<tr><td rowspan="2">Object Program mode</td><td>Even (1)</td><td>Not allowed (6)</td><td rowspan="2">Not allowed (6)</td><td>Not allowed (6)</td></tr>
<tr><td>Odd (2)</td><td>Not allowed (6)</td><td>Not allowed(4)</td></tr>
</table>

NOTE 1 At least one bit is programmed in an even element

NOTE 2 At least one bit is programmed in an odd element

NOTE 3 If supported

NOTE 4 Program aborted, Status Register error bits MR22.OP4 (PSB), MR23.OP0 (OMSB) and MR23.OP1 (CMSB) are set

NOTE 5 Program aborted, Status Register error bits MR22.OP4 (PSB) MR23.OP1 (CMSB) are set

NOTE 6 Program aborted, subsequent program not allowed, Status Register error bits MR22.OP4 (PSB) MR23.OP0 (OMSB) are set

Figure 131 shows an example of Programming Region configuration. The Programming Region size is 512Byte, the element size is 8Byte, and the Block sizes are 64KByte, 128KByte and 256KByte.

Independently of the Block size, the Programming Region configuration is periodic: the first 124 Programming Regions (62KByte) are configured in Object Mode Region, and the following 4 Programming Regions (2KByte) are configured in Control Mode.

A.2.4.3 Programming Region Configuration (cont'd)

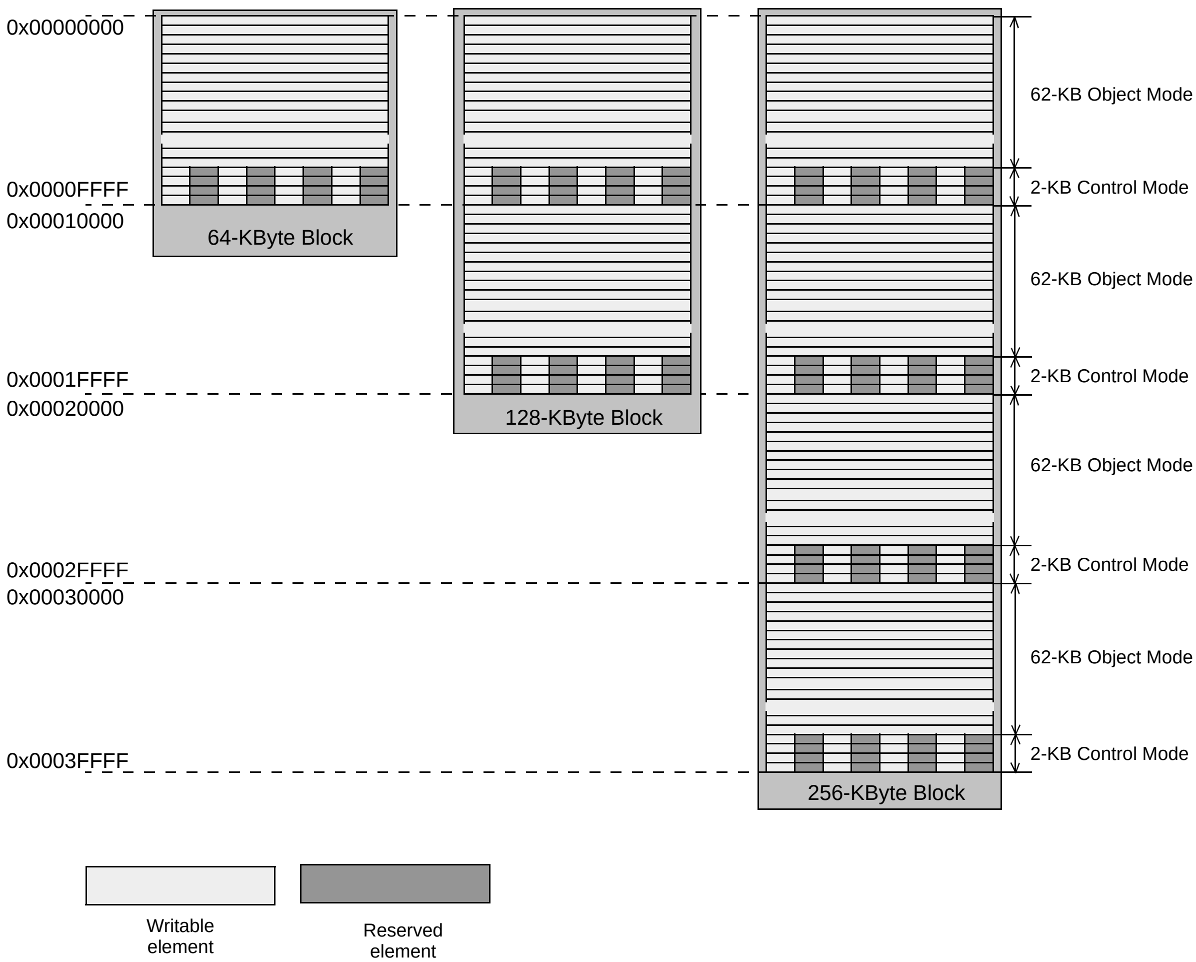


Figure 131 — Control Mode and Program Mode Example

Annex B LPDDR2-NVM Boot Procedure

B.1 Booting From an LPDDR2-NVM Device

Figure 132 illustrates an example LPDDR2 memory subsystem that includes both NVM and SDRAM memories. Chip Select (CSx) and Clock Enable (CKEx) are assigned on a per chip basis, the data bus and the remainder of the command bus are common to both devices. Because LPDDR2 devices (both DRAM and NVM) assign specific functions to the different byte lanes of the data bus and even to specific bits within the bytes, byte and bit swapping shall be avoided. The ZQ input requires connection to a precision 240 ohm resistor that is used to calibrate each device’s output drive strength. The ZQ inputs can use a common 240 ohm resistor or have captive resistors, in this example we use a common resistor.

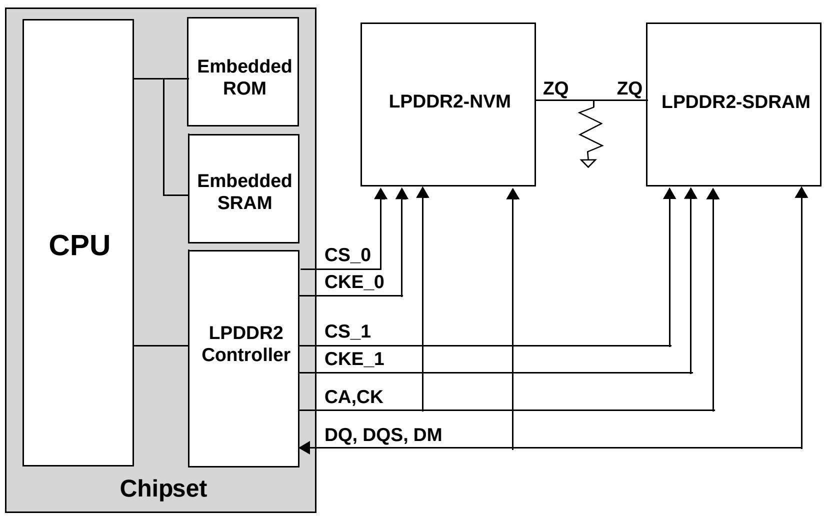


Figure 132 — LPDDR2 based system using both LPDDR2-SDRAM and LPDDR2-NVM

Chipsets implementing an LPDDR2 interface will need to perform a “pre-boot” process prior to accessing the LPDDR2-NVM device. The pre-boot process will perform the LPDDR2-NVM device initialization (as described in Section 3.5.1 - Power Ramp and Device Initialization in the LPDDR2-NVM spec) and configure both the LPDDR2 controller and the external LPDDR2-NVM device properly prior to starting code execution from external memory. The pre-boot process may be performed by executing a code residing in an embedded ROM or it might be implemented using hardware in the memory controller.

B.1 Booting From an LPDDR2-NVM Device (cont'd)

The pre-boot process is composed by the following steps:

1. Memory Controller Preliminary Configuration
   - Configure the memory controller with initial latency settings compatible with the possible LPDDR2-NVM devices that may reside on the LPDDR2 bus
2. Initialization Sequence
   - Apply clock (frequency between 10MHz and 55MHz)
   - Drive CKE High
   - Issue the Reset command and wait until the DAI bit in MR0 transitions to 0. It is recommended that this delay (tINIT5) be accomplished by polling the DAI bit in MR0.
   - Issue a ZQ Initialization Command
3. Search for an LPDDR2-NVM memory
   - Starting from CS0, check the first LPDDR2-NVM device in the bus by reading MR0
4. Memory Controller and LPDDR2-NVM configuration
   - Read MR8 to retrieve the memory type, bus width, density and configure the memory controller accordingly
   - Read MR20 to retrieve Row Data Buffer Size and number of Row Data Buffers, then configure the memory controller accordingly
   - Optionally, set the proper Burst Length value in MR1 of the LPDDR2-NVM
   - Optionally, adjust tRCD memory controller setting according to MR21 and the actual tCKb value.
5. Start to read the boot code from the external LPDDR2-NVM device.

Once the pre-boot process has completed and code execution is passed to the external LPDDR2-NVM memory device the final portion of the memory bus configuration process occurs. During this stage the boot process will optimize timings and finally increase the clock rate to the target value.

6. Specify how frequently the output impedance should be calibrated
7. Set the appropriate output drive strength
8. Adjust the configuration settings in the controller and memories for higher clock rates
9. Bump up the bus operating frequency
10. Perform data training

B.1.1 Power Ramp and Initialization

During power-on the LPDDR2 power supplies are expected to ramp up to the nominal operating voltages within 20ms. At this point CKE should be driven low and the CK_t/CK_c clock signals should begin to toggle. During this early part of the boot process the host chipset is expected to clock the LPDDR2 bus at a frequency between 10MHz and 55MHz. After 100ns and at least five clocks, CKE is driven high to begin internal initialization of the LPDDR2 device. The device is ready to receive the RESET command 200us after CKE is driven high.

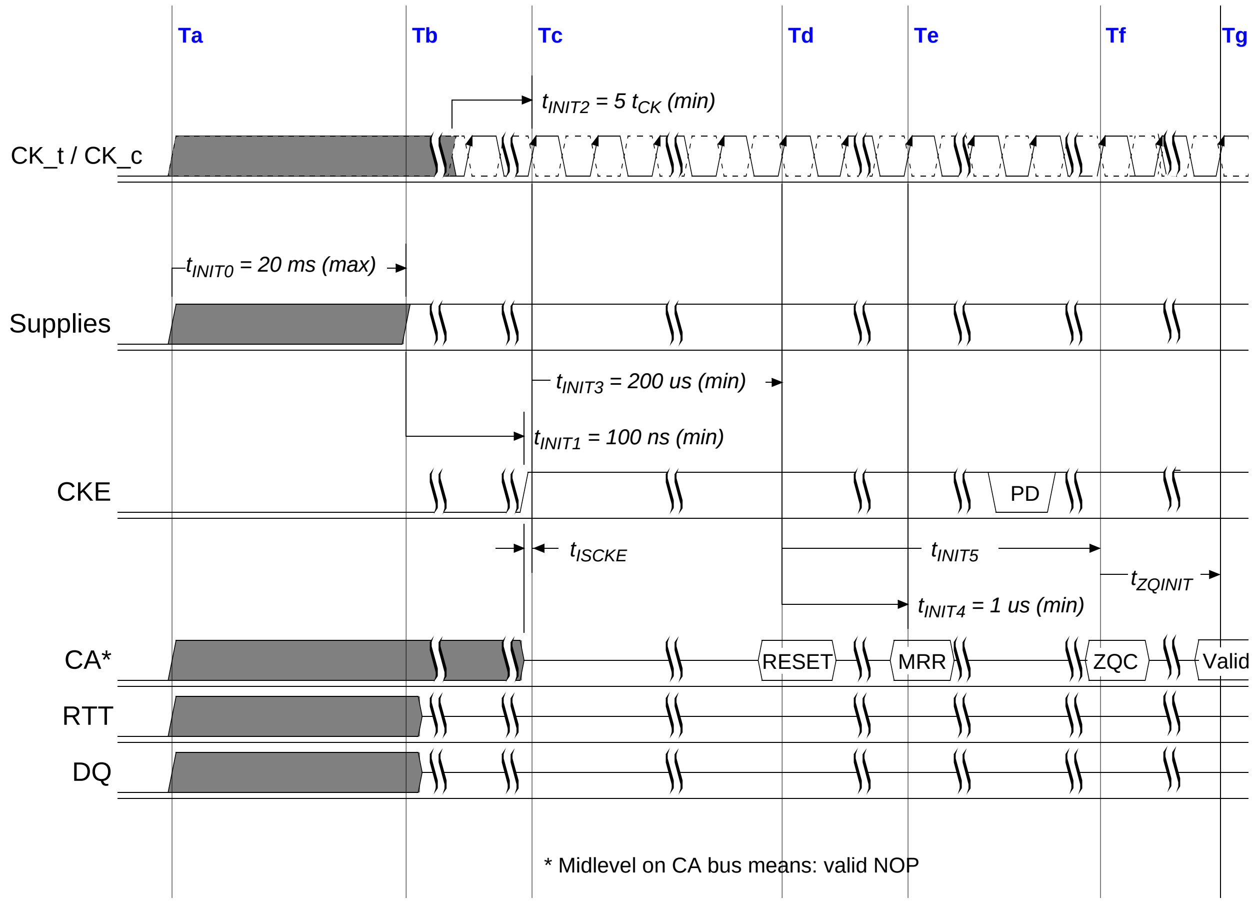


Figure 133 — Power-Up and Initialization (see the LPDDR2-NVM spec for details)

Once the RESET command has been issued the boot process must wait for 1us before continuing. After the 1us tINIT4 time has elapsed the boot process will poll the Device AutoInitialization (DAI) bit in the Device Information Register (MR0). The DAI bit will transition from high to low when the reset operation has completed.

The LPDDR2 devices after RESET assume the following default configuration:

BL=4;

BT= Sequential, Wrap;

RL=3, WL=1;

DS=40Ohm.

It is recommended that the memory controller default configuration should match with the LPDDR2 devices (at least RL, otherwise it would not be possible to read the Mode Registers).

B.1.2 ZQ Initialization

Once reset has completed, the ZQ Initialization command (FFh) is written to the Calibration Mode Register (MR10). During ZQ initialization the on-die output impedance is compared with a 240 ohm precision resistor that is connected between ground and the device's ZQ input. Multiple LPDDR2 devices can share the precision resistor as long as only one of the devices performs calibration at any particular time. Upon completion of the ZQ Initialization the device's output impedance will be within 15% of the nominal value.

At the lower operating frequencies used during the boot process the default drive strength value of 40 ohms is adequate. Adjustment of the drive strength will occur later in the boot process when the clock rate is bumped up prior to normal operation.

B.1.3 Determine the LPDDR2 bus width, memory type, RDB size and density

The boot process then reads the Basic Configuration 4 Mode Register (MR8) from the LPDDR2 device on CS0 to determine the data bus width, memory type and also the device density. When the memory is an NVM, MR20 is read to determine the RDB size. The controller is then configured to operate with the appropriate bus width (x8, x16 or x32). The density value read back from MR8 is used to configure the address space assigned to CS0. The data bus width and the RDB size is relevant system information and is used to ensure proper memory addressing and is mandatory to configure the memory controller accordingly. The embedded ROM can be programmed, or the HW could be used, to step through the remaining LPDDR2 chip selects and configure the host controller according to the information available in the respective mode registers.

B.1.4 Align controller and memory latency settings (RL, WL, tRCD)

Prior to performing standard read and write operations the host controller and target memory must align their Read/Write latencies. The default values for LPDDR2-NVM devices is a three clock read latency and a one clock write latency. These default values are suitable for normal operation for the specified boot frequency (10MHz to 55MHz). If necessary, the memory controller latencies should be adjusted to match those of the LPDDR2-NVM device.

The remaining latency issue needing attention is aligning the host controller with the LPDDR2- NVM tRCD latencies. The value held in the read only tRCD Mode Register (MR21) specifies the minimum tRCD value for the LPDDR2-NVM device. The embedded boot code should configure the LPDDR2 controller latency values to accommodate the tRCD value indicated in MR21.

B.1.5 Determining whether to boot from the LPDDR2 Bus

After the initial latencies have been specified the boot process will determine whether a bootable non-volatile device resides on the LPDDR2 bus. If there is a bootable NVM device on the LPDDR2 bus it will likely reside on the first chip select (CS0). If the device is nonvolatile, program operation will be redirected to the LPDDR2-NVM device on CS0. If the device is volatile (SDRAM), the embedded ROM will continue to search for alternate boot memories.

B.1.6 Continued Boot Out Of the LPDDR2-NVM Device

Once the boot process has passed to the LPDDR2-NVM device, system level characteristics are considered. For the most part this portion of the boot process is used to maximize data throughput by adjusting the output drive strength, clock rate and the data capture point during read operations.

B.1.7 Output Drive Strength

Given various system level considerations, adjustment of the output drive strength away from the default 40 ohm setting may be required. This step is required to optimize driver output impedance to accommodate issues like bus loading (# of devices), PoP/MCP package type, trace length on the PCB and sourcing capabilities of the output driver power supplies.

The I/O Configuration Mode Register (MR3) is used to configure the LPDDR2-NVM output drive strength. Available configuration settings include 34.3, 40 (default), 48, 60 and 80 ohm values (120 ohm value is optional).

B.1.8 Setting the Output Impedance Calibration Interval

During normal operation both operating voltage and temperature drift can cause the output drive strength to change away from the value selected during the boot process. These changes are dealt with by periodically calibrating the output impedance against the 240 ohm precision resistor connected to the ZQ input. Periodic calibration is performed to assure that the selected output impedance remains within the nominal +/-15% spec.

LPDDR2 controllers include a periodic timer that will indicate the length of time between calibration cycles. Once the timer interval has expired the controller will automatically issue a Short Calibration command that will move the output impedance by up to 1.5% toward the ideal setting. The calibration interval is calculated by considering the maximum voltage and temperature drift rates. Given a maximum temperature drift rate of 1.0°C/s and a maximum voltage drift rate of 15mV/s the Short Calibration operation should be performed at least every 400ms. The equation below is the strategy suggested by JEDEC to determine how frequently output impedance should be calibrated.

ZQS_Interval = (ZQS_Correction/((T_Sensitivity*T_DriftRate)+(V_Sensitivity*VDriftRate))

= 1.5%/(((0.75%/°C)*(1.0°C/s))+((0.2%/mV)*(15mV/s)))

= 400ms

If a single 240 ohm ZQ resistor is common to all LPDDR2 devices the ZQS Calibration operation must be performed serially on a per device basis. If each LPDDR2 device has its own ZQ resistor the ZQS Calibration operation must still be performed on a per device basis. See the LPDDR2-NVM spec for further guidance on how to determine the required length of time between ZQS calibration.

B.1.9 Increasing the Clock Rate

At this point in the boot process, preparation to increase the clock rate can begin. This process has three steps. The first step is to alter the memory controller settings to accommodate the latency characteristics of the memory devices on the LPDDR2 bus. The second step is to increase the clock frequency to the target rate. The third and final step is to perform data training to maximize read timing margin.

While the first step (adjusting latency settings) can be executed from code located in the LPDDR2-NVM device, the second (increasing clock rate) and third (data training) steps should not be performed using code executing from a device residing on the LPDDR2 bus. The code used to increase the clock rate and to perform data training should be executed out of embedded memory located in the chipset. The required code could reside in either the embedded ROM or it could be copied temporarily into the chipset’s embedded SRAM for execution. Once these three steps have been performed, program operation will be redirected to the LPDDR2-NVM device with the LPDDR2 bus running at the target frequency.

Configuration of additional devices residing on the LPDDR2 bus can be performed either before or after the clock rate is increased. If additional devices are configured before the clock rate is increased, extensions to the code that manages the LPDDR2-NVM device can be developed. If additional LPDDR2 devices are to be brought on line after the clock rate is increased, the configuration code for the additional devices could be executed out of the LPDDR2-NVM device.

B.1.10 Controller Latency Settings for Higher Clock Rates

The first step toward increasing the clock rate is adjusting the controller settings to account for the memory device’s operational characteristics. The key characteristics include the time required between the Active and Read/Write commands (tRCD) and also the Read/Write Latencies (RL, WL).

The tRCD value can be read from the tRCD Mode Register (MR21). The number of clocks required to meet the tRCD spec given a target operating frequency is then calculated and loaded into the memory controller. This process is repeated for each device sharing the LPDDR2 bus.

Appropriate Read Latency and Write Latency values are then chosen given device characteristics and the target operating frequency. Once determined, the RL/WL values are loaded into the Device Feature 2 Mode Register (MR2). The memory controller is also configured to align with the appropriate RL/WL values for each of the devices on the LPDDR2 bus.

B.1.11 Increasing the Clock Rate

After the latency values have been changed in both the LPDDR2 devices and in the controller the clock rate can be increased to the target operating frequency. Figure 134 describes the timings relevant to changing the clock frequency. In this example, the clock rate is changed while the device is in the Power-Down state. The clock may also be changed when CKE is HIGH. See the LPDDR2 specification for details.

The device must be stable at the new clock frequency for at least two clock cycles before exiting the Power-Down state (two clocks (min), CKE returns high). Once CKE returns high the LPDDR2-NVM device will require 10ns to exit Power-Down (tXP) before accepting the first valid command.

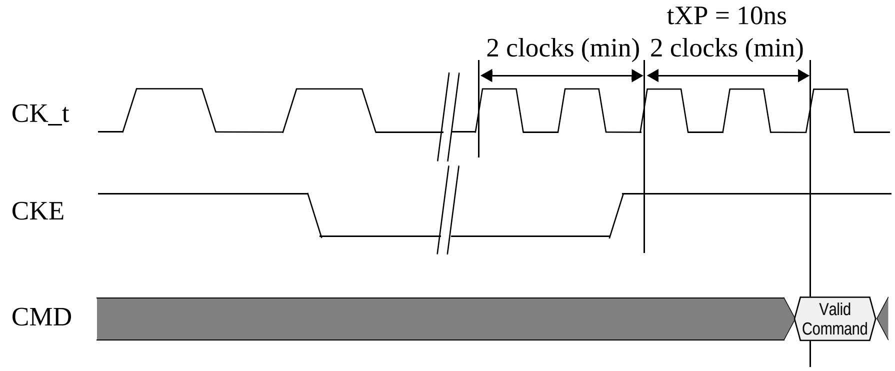


Figure 134 — Clock Rate Change Timings

B.1.12 Data Training

The final step in the boot process is to optimize the controller's read timings. In particular, this step is used to skew the data capture point with respect to the DQS signal generated by the target memory device during a read operation. This offset will be different for each device residing on the memory bus, requiring that an offset be associated with each chip select.

In most implementations the host software will request that the controller perform data training. The controller will then find the optimal read capture point without intervention from the host. Once the controller has completed data training, code execution will be redirected back to the LPDDR2-NVM device at the new clock rate.

B.1.13 Summary

This application note has described how a system can boot from an LPDDR2-NVM device that shares the LPDDR2 bus with an LPDDR2-SDRAM device. Only a few extensions to the chipset's embedded ROM, or dedicated HW, are required to facilitate booting from the LPDDR2 bus. Once code execution has passed from the embedded ROM, or dedicated HW, to the LPDDR2-NVM device the remaining boot code takes into account system level characteristics.

Annex C (informative) Differences between Document Revisions

C.1 Initial Release

Standard Improvement Form   JEDEC ____________

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:
   - [ ] Requirement, clause number ____________
   - [ ] Test method number ____________ Clause number ____________

   The referenced clause number has proven to be:
   - [ ] Unclear
   - [ ] Too Rigid
   - [ ] In Error
   - [ ] Other ____________

2. Recommendations for correction:

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3. Other suggestions for document improvement:

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