JEDEC STANDARD

Low Power Double Data Rate (LPDDR) SDRAM Standard

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February 2009

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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1 Scope

This document defines the Low Power Double Data Rate (LPDDR) SDRAM specification, including features, functionality, AC and DC characteristics, packages, and pin assignments. This scope may be expanded in future to also include other higher density devices.

The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant 64 Mb through 2 Gb for x16 and x32 Low Power Double Data Rate SDRAM devices. System designs based on the required aspects of this specification will be supported by all LPDDR SDRAM vendors providing compliant devices.

This specification was created based on the DDR-I specification (JESD79) and some aspects of the DDR2 specification (JESD79-2) where shared technology suggested commonality provided benefits. Each aspect of the changes for low power operation were considered and balloted. The accumulation of these ballots were then incorporated to prepare this LPDDR SDRAM specification, replacing whole sections and incorporating the changes into Functional Description and Operation. The applicable ballots are summarized in Table 1.

Table 1 — LPDDR Ballots

Item #	Ballot Number	Subject	Spec Coverage
1418.02	JC-42.3-03-183	LPDDR IO levels	Table 12 and notes
1418.04	JC-42.3-03-114	LPDDR addressing table x16	part of Table 2 except tREFI
1418.05	JC-42.3-03-184	LPDDR IDD test condition	Table 13 and notes except IDD6
1418.07	JC-42.3-03-258	AC timing parameters	Table 14 and notes
1418.08	JC-42.3-03-259	Pin capacitance	Table 11 and notes
1418.09	JC-42.3-04-035	LPDDR clock stop mode	Clock stop, pp 46, Figure 43
1418.10	JC-42.3-04-026	Modification of IDD6 definition	Table 13
1418.11	JC-42.3-04-188	LPDDR addressing table x32	part of Table 2, x32, except tREFI
1418.12	JC-42.3-04-147	tREFI for x32 LPDDR	part of Table 2, x32, tREFI only
1452.01	JC-42.3-04-118	LPDDR MRS and EMRS definition	Figure 6 and Figure 7
1452.02	JC-42.3-04-111	LPDDR SDRAM x16 in FBGA-60	Figure 1
1452.03	JC-42.3-04-181	LPDDR SDRAM x32 in FBGA-90	Figure 2
1563.00	JC-42.3-04-037	LPDDR initialization	pp 10; Figure 4 and Figure 5
1563.01	JC-42.3-04-038	LPDDR Deep Power Down mode	pp 45 and Figure 42
1604.01	JC-42.3-04-150A	LPDDR IV Curve	Table 18, Figure 45 and Figure 47
1625.03	JC-42.3-04-392	LPDDR over/undershoot	Table 17 and Figure 44
1718.05	JC-42.6-07-357	LPDDR400 SDRAM AC Parameters	Table 15
1718.08	JC-42.6-07-358	LPDDR400 SDRAM TQ Pad Proposal	Table 3, Figure 5, description page 19, Table 14
1718.13	JC-42.6-07-264	LPDDR SDRAM 60-, 90-Ball BGA Ballouts with A13 ball	Figure 2
1718.14	JC-42.6-07-265	LPDDR SDRAM 60-, 90-Ball BGA Ballouts with additional CS#, CKE	Figure 1 and Figure 2
1718.15	JC-42-6.07-359	LPDDR SDRAM Output Driver Characteristics	Figure 7, Table 16, Table 18, Table 19, and Figure 46.
1718.16	JC-42.3-07-360	LPDDR SDRAM address tables	Table 2

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices

64M = 4M x 16 (1M x 16 x 4 banks), 2M x 32 (512K x 32 x 4 banks)

128M = 8M x 16 (2M x 16 x 4 banks), 4M x 32 (1M x 32 x 4 banks)

256M = 16M x 16 (4M x 16 x 4 banks), 8M x 32 (2M x 32 x 4 banks)

512M = 32M x 16 (8M x 16 x 4 banks), 16M x 32 (4M x 32 x 4 banks)

1G = 64M x 16 (16M x 16 x 4 banks), 32M x 32 (8M x 32 x 4 banks)

2G = 128M x 16 (32M x 16 x 4 banks), 64M x 32 (16M x 32 x 4 banks)

2.1 Features

- Double-data rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- Differential clock inputs (CK and $\overline{CK}$)
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst Length: 2, 4 or 8 (16 is optional)
- Burst Type: Sequential or Interleave
- CAS latency: 3 (2 & 4 are optional)
- Clock Stop capability during idle periods
- Auto Precharge option for each burst access
- Configurable Drive Strength
- Auto Refresh and Self Refresh Modes
- Optional Partial Array Self Refresh and Temperature Compensated Self Refresh
- Deep Power Down Mode
- LV-CMOS compatible inputs
- VDD and VDDQ: 1.8 +/- 0.1 V

2.2 General Description

The LPDDR SDRAM is a high speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. These devices contain the following number of bits:

64 Mb has 67,108,864 bits
128 Mb has 134,217,728 bits
256 Mb has 268,435,456 bits
512 Mb has 536,870,912 bits
1 Gb has 1,073,741,824 bits
2 Gb has 2,147,483,648 bits

The LPDDR SDRAM uses a double data rate architecture to achieve high speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the LPDDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the LPDDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center aligned with data for WRITEs.

The LPDDR SDRAM operates from a differential clock (CK and $\overline{CK}$: the crossing of the CK going high and $\overline{CK}$ going low will be referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered at both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)

2.2 General Description (cont'd)

Read and write accesses to the LPDDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The LPDDR SDRAM provides for programmable read or write bursts of 2, 4 or 8 locations. Some vendors may offer an optional burst length of 16. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of LPDDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation times.

An Auto Refresh mode is provided, along with a power saving Power-down mode. Self Refresh mode may have Temperature Compensated Self Refresh (TCSR) and Partial Array Self Refresh (PASR) options, which allow users to achieve additional power saving. The TCSR and PASR options can be programmed via the extended mode register.

All inputs are LV-CMOS compatible. Devices will have a VDD and VDDQ supply of 1.8 V (nominal).

This datasheet includes all features and functionality required for JEDEC LPDDR SDRAM devices. Certain vendors may elect to offer a superset of this specification by offering improved timings and/or including optional features. Users benefit from knowing that any system design based on the required aspects of the specification are supported by all LPDDR SDRAM vendors; conversely users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

Table 2 — LPDDR SDRAM Addressing Table

Item		64 Mb	128 Mb	256 Mb	512 Mb	1 Gb		2 Gb
Number of banks		4	4	4	4	4		4
Bank Address Pins		BA0, BA1	BA0, BA1	BA0, BA1	BA0, BA1	BA0, BA1		BA0, BA1
Autoprecharge Pin		A10/AP	A10/AP	A10/AP	A10/AP	A10/AP		A10/AP
x16	Row Addresses	A0-A11	A0-A11	A0-A12	A0-A12	A0-A13		A0-A13
	Column Addresses	A0-A8	A0-A8	A0-A8	A0-A9	A0-A9		A0-A9, A11
	t_{REFI} (µs)	15.6	15.6	7.8	7.8	7.8		7.8
x32	Row Addresses	A0-A10	A0-A11	A0-A11	A0-A12	A0-A12	A0-A13	A0-A13
	Column Addresses	A0-A7	A0-A7	A0-A8	A0-A8	A0-A9	A0-A8	A0-A9
	t_{REFI} (µs)	15.6	15.6	15.6	7.8	7.8		7.8

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)
2.2 General Description (cont'd)

2.2.1 Packages

Single-die, one CS# and one CKE:

In the 60-ball x16 package,a maximum SDRAM density of 2Gb can be achieved only with 2-KByte page size and most significant address bit A13.

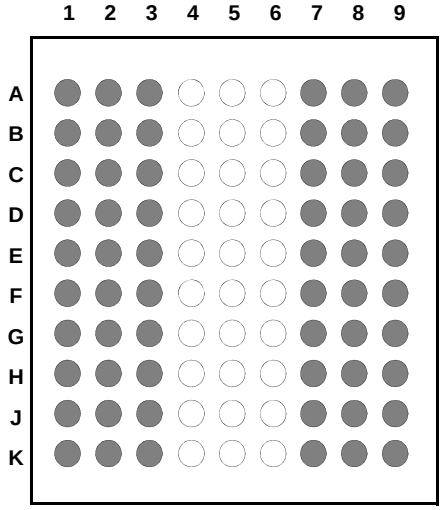
In the 90-ball x32 package, a maximum SDRAM density of 2Gb can be achieved either with 2-KByte page size and most significant address bit A13, or with 4-KByte page size and most significant address bit A12.

Dual-die, two CS# and two CKE:

In the 60-ball x16 package, a maximum SDRAM density of 1Gb can be achieved with most significant address bit A12.

In the 90-ball x32 package, a maximum SDRAM density of 2Gb can be achieved with most significant address bit A12.

Top View
(Balls seen through the package)

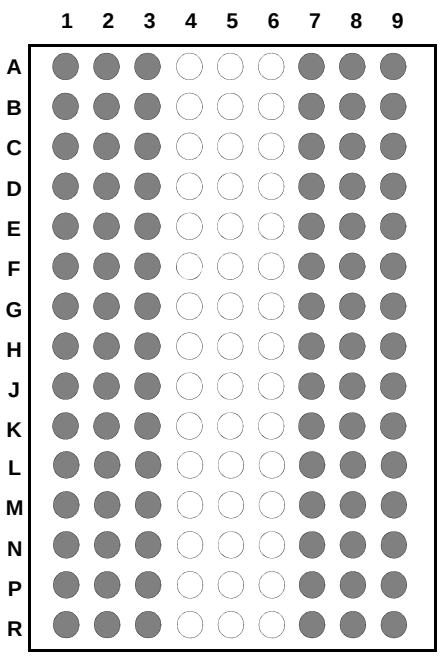


60-Ball (6x10) CSP						
	1	**2**	**3**	**7**	**8**	**9**
A	VSS	DQ15	VSSQ	VDDQ	DQ0	VDD
B	VDDQ	DQ13	DQ14	DQ1	DQ2	VSSQ
C	VSSQ	DQ11	DQ12	DQ3	DQ4	VDDQ
D	VDDQ	DQ9	DQ10	DQ5	DQ6	VSSQ
E	VSSQ	UDQS	DQ8	DQ7	LDQS	VDDQ
F	VSS	UDM	NC,CKE1	A13,NC,CS1	LDM	VDD
G	CKE0	CK	CK	WE	CAS	RAS
H	A9	A11	A12,NC	CS0	BA0	BA1
J	A6	A7	A8	A10/AP	A0	A1
K	VSS	A4	A5	A2	A3	VDD

Figure 1 — Pin Configuration of x16 LPDDR SDRAM IN BGA

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)
2.2 General Description (cont'd)

Top View
(Balls seen through the package)



90-Ball (6x15) CSP						
	1	**2**	**3**	**7**	**8**	**9**
A	VSS	DQ31	VSSQ	VDDQ	DQ16	VDD
B	VDDQ	DQ29	DQ30	DQ17	DQ18	VSSQ
C	VSSQ	DQ27	DQ28	DQ19	DQ20	VDDQ
D	VDDQ	DQ25	DQ26	DQ21	DQ22	VSSQ
E	VSSQ	DQS3	DQ24	DQ23	DQS2	VDDQ
F	VDD	DM3	NC,CKE1	A13,NC,CS1	DM2	VSS
G	CKE0	CK	CK	WE	CAS	RAS
H	A9	A11	A12,NC	CS0	BA0	BA1
J	A6	A7	A8	A10/AP	A0	A1
K	A4	DM1	A5	A2	DM0	A3
L	VSSQ	DQS1	DQ8	DQ7	DQS0	VDDQ
M	VDDQ	DQ9	DQ10	DQ5	DQ6	VSSQ
N	VSSQ	DQ11	DQ12	DQ3	DQ4	VDDQ
P	VDDQ	DQ13	DQ14	DQ1	DQ2	VSSQ
R	VSS	DQ15	VSSQ	VDDQ	DQ0	VDD

Figure 2 — Pin Configuration of x32 LPDDR SDRAM IN BGA

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)

2.2 General Description (cont'd)

Table 3 — Pin Descriptions

Symbol	Type	Description
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK. Input and output data is referenced to the crossing of CK and $\overline{CK}$ (both directions of crossing). Internal clock signals are derived from CK/$\overline{CK}$.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CK, $\overline{CK}$ and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
$\overline{CS}$	Input	Chip Select: $\overline{CS}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM for x16: LDM, UDM for x32: DM0-DM3	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading. For x16 devices, LDM corresponds to the data on DQ0-DQ7, UDM corresponds to the data on DQ8-DQ15. For x32 devices, DM0 corresponds to the data on DQ0-DQ7, DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, and DM3 corresponds to the data on DQ24-DQ31.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [n : 0]	Input	Address Inputs: provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ / WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the opcode during a MODE REGISTER SET command.
DQ for x16: DQ0-DQ15 for x32: DQ0-DQ31	I/O	Data Bus: Input / Output
DQS for x16: LDQS,UDDS for x32: DQS0-DQS3	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. For x16 device, LDQS corresponds to the data on DQ0-DQ7, UDQS corresponds to the data on DQ8-DQ15. For x32 device, DQS0 corresponds to the data on DQ0-DQ7, DQS1 corresponds to the data on DQ8-DQ15, DQS2 corresponds to the data on DQ16-DQ23, and DQS3 corresponds to the data on DQ24-DQ31.
NC	—	No Connect: No internal electrical connection is present
VDDQ	Supply	I/O Power Supply
VSSQ	Supply	I/O Ground
VDD	Supply	Power Supply
VSS	Supply	Ground

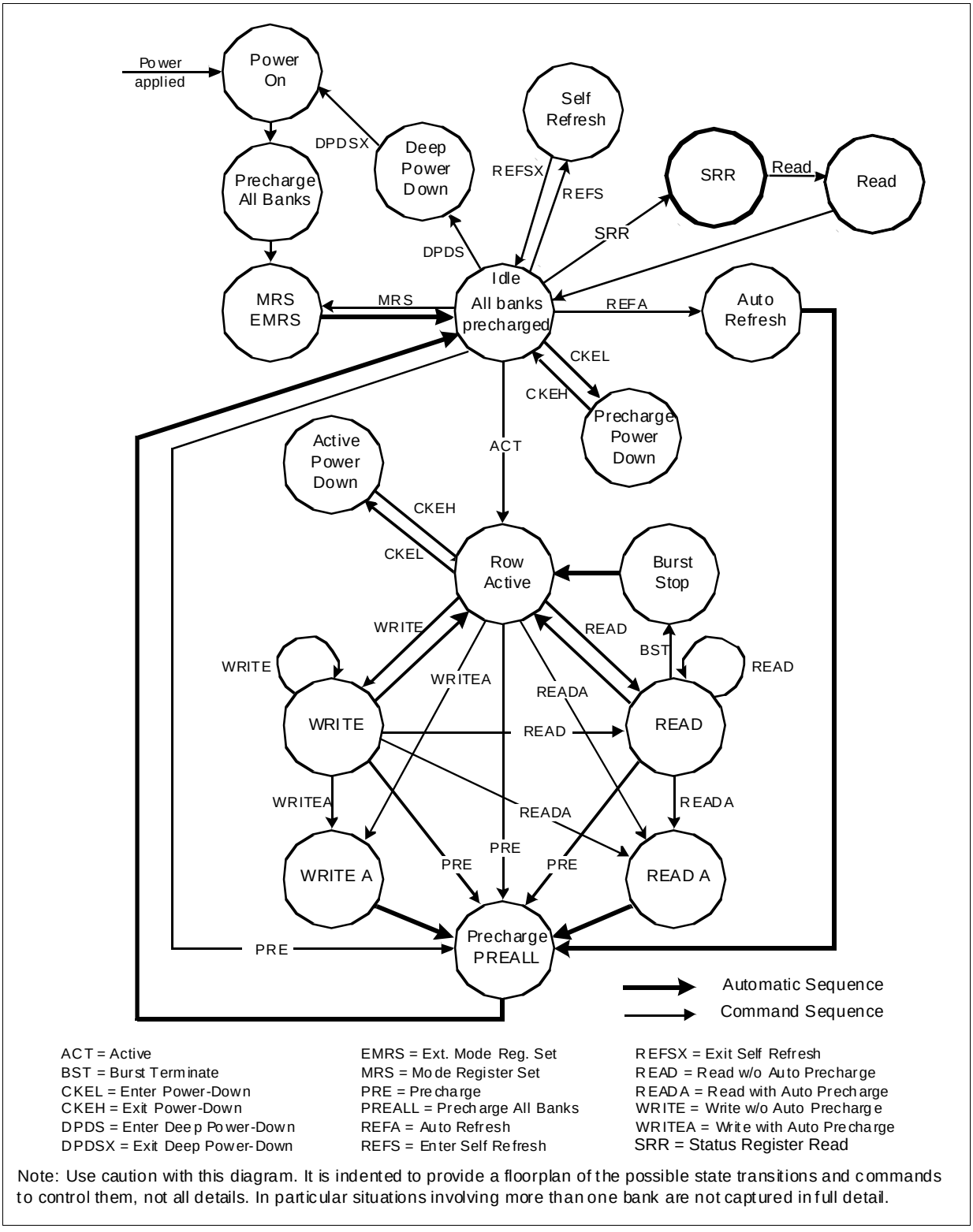
2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)

2.2 General Description (cont'd)

Table 3 — Pin Descriptions

Symbol	Type	Description
TPD (Test Power Down)	Input	Optional pad, Test Power Down or TPD, for test purposes only. TPD LOW is normal operation. Taking TPD HIGH asynchronously will place the die in deep power down mode. The assertion of TPD HIGH must meet all the initialization and sequencing of DPD mode
TQ	Output	Optional. Asynchronous, LVCMOS temperature output. Output logic-HIGH state when device temperature equals or exceeds 85'C. Output logic-LOW state when device temperature is less than 85'C.

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)
2.2 General Description (cont'd)



Note: Use caution with this diagram. It is indented to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular situations involving more than one bank are not captured in full detail.

Figure 3 — Simplified State Diagram

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)

2.3 Terminology Definitions

The following are the definitions of the terms LPDDR200, LPDDR266, LPDDR333, LPDDR370, and LPDDR400 as used in this specification

LPDDR200: A speed grade for LPDDR SDRAM devices. The nominal operating (clock) frequency of such devices is 100 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 100 MHz clock frequency. The corresponding nominal data transfer rate is 200 Million Transfers per Second per pin (MTS).

LPDDR266: A speed grade for LPDDR SDRAM devices. The nominal operating (clock) frequency of such devices is 133 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 133 MHz clock frequency. The corresponding nominal data transfer rate is 266 MTS.

LPDDR333: A speed grade for LPDDR SDRAM devices. The nominal operating (clock) frequency of such devices is 166 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 166 MHz clock frequency. The corresponding nominal data transfer rate is 333 MTS.

LPDDR370: A speed grade for LPDDR SDRAM devices. The nominal operating (clock) frequency of such devices is 185 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 185 MHz clock frequency. The corresponding nominal data transfer rate is 370 MTS.

LPDDR400: A speed grade for LPDDR SDRAM devices. The nominal operating (clock) frequency of such devices is 200 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 200 MHz clock frequency. The corresponding nominal data transfer rate is 400 MTS.

3 Functional Description

The LPDDR SDRAM is a high speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. These devices contain the following number of bits:
64 Mb has 67,108,864 bits
128 Mb has 134,217,728 bits
256 Mb has 268,435,456 bits
512 Mb has 536,870,912 bits
1 Gb has 1,073,741,824 bits
2 Gb has 1,147,483,648 bits

The LPDDR SDRAM uses a double data rate architecture to achieve high speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the LPDDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

3.1 Initialization

LPDDR SDRAMs must be powered up and initialized in a predefined manner. Operations procedures other than those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. The steps to be followed for device initialization are listed below. The Initialization Flow diagram is shown in Figure 4, and the Initialization Flow sequence in Figure 5.

The Mode Register and Extended Mode Register do not have default values. If they are not programmed during the initialization sequence, it may lead to unspecified operation. The clock stop feature is not available until the device has been properly initialized from Steps 1 through 11.

1. Provide power, the device core power (VDD) and the device I/O power (VDDQ) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that VDD and VDDQ are from the same power source. Also assert and hold Clock Enable (CKE) to a LV-CMOS logic high level
2. Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock
3. There must be at least 200 µs of valid clocks before any command may be given to the DRAM. During this time NOP or DESELECT commands must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Provide NOPs or DESELECT commands for at least t_{RP} time.
6. Issue an AUTO REFRESH command followed by NOPs or DESELECT command for at least t_{RFC} time. Issue the second AUTO REFRESH command followed by NOPs or DESELECT command for at least t_{RFC} time. Note as part of the initialization sequence there must be two auto refresh commands issued. The typical flow is to issue them at Step 6, but they may also be issued between steps 10 and 11.
7. Using the MRS command, load the base mode register. Set the desired operating modes.
8. Provide NOPs or DESELECT commands for at least t_{MRD} time.
9. Using the MRS command, program the extended mode register for the desired operating modes. Note the order of the base and extended mode register programming is not important.

3 Functional Description (cont'd)
3.1 Initialization (cont'd)

10. Provide NOP or DESELCT commands for at least t_{MRD} time.
11. The DRAM has been properly initialized and is ready for any valid command.

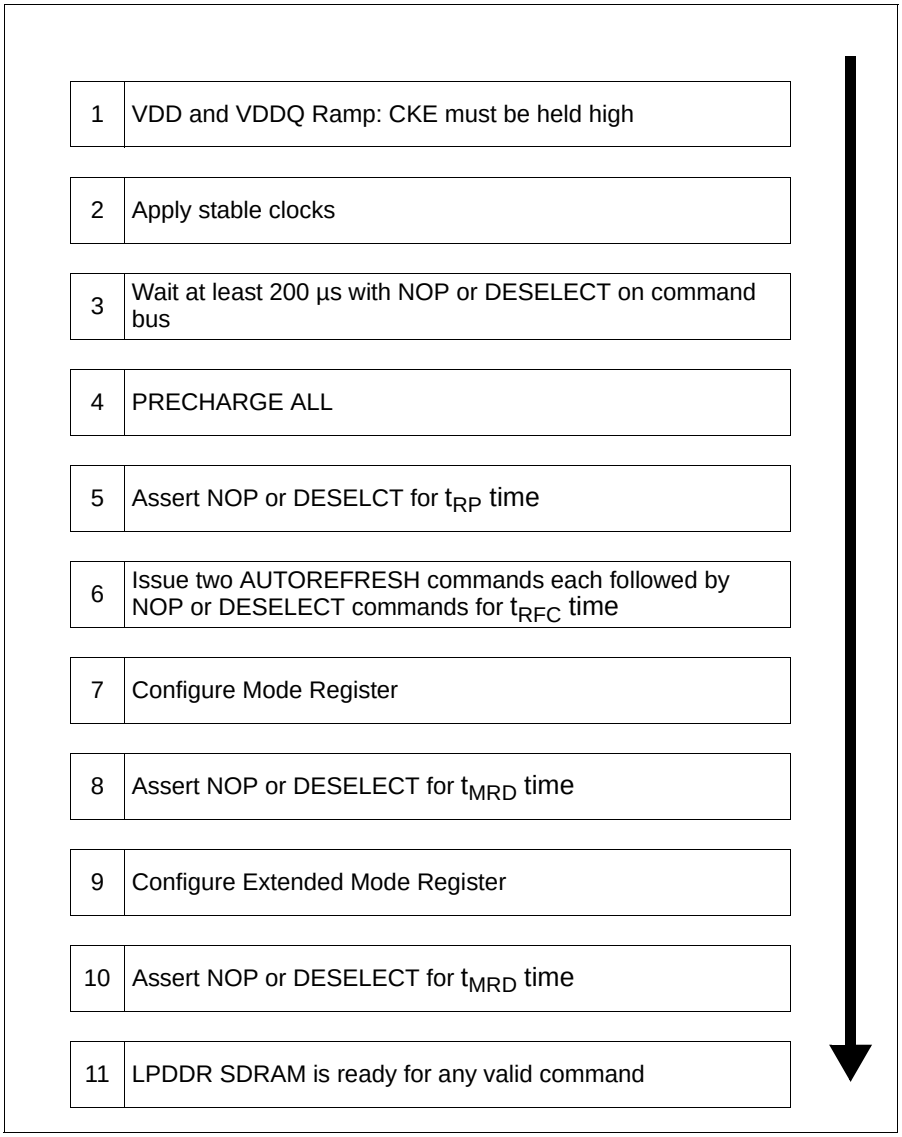


Figure 4 — Initialization Flow Diagram

3 Functional Description (cont'd)
3.1 Initialization (cont'd)

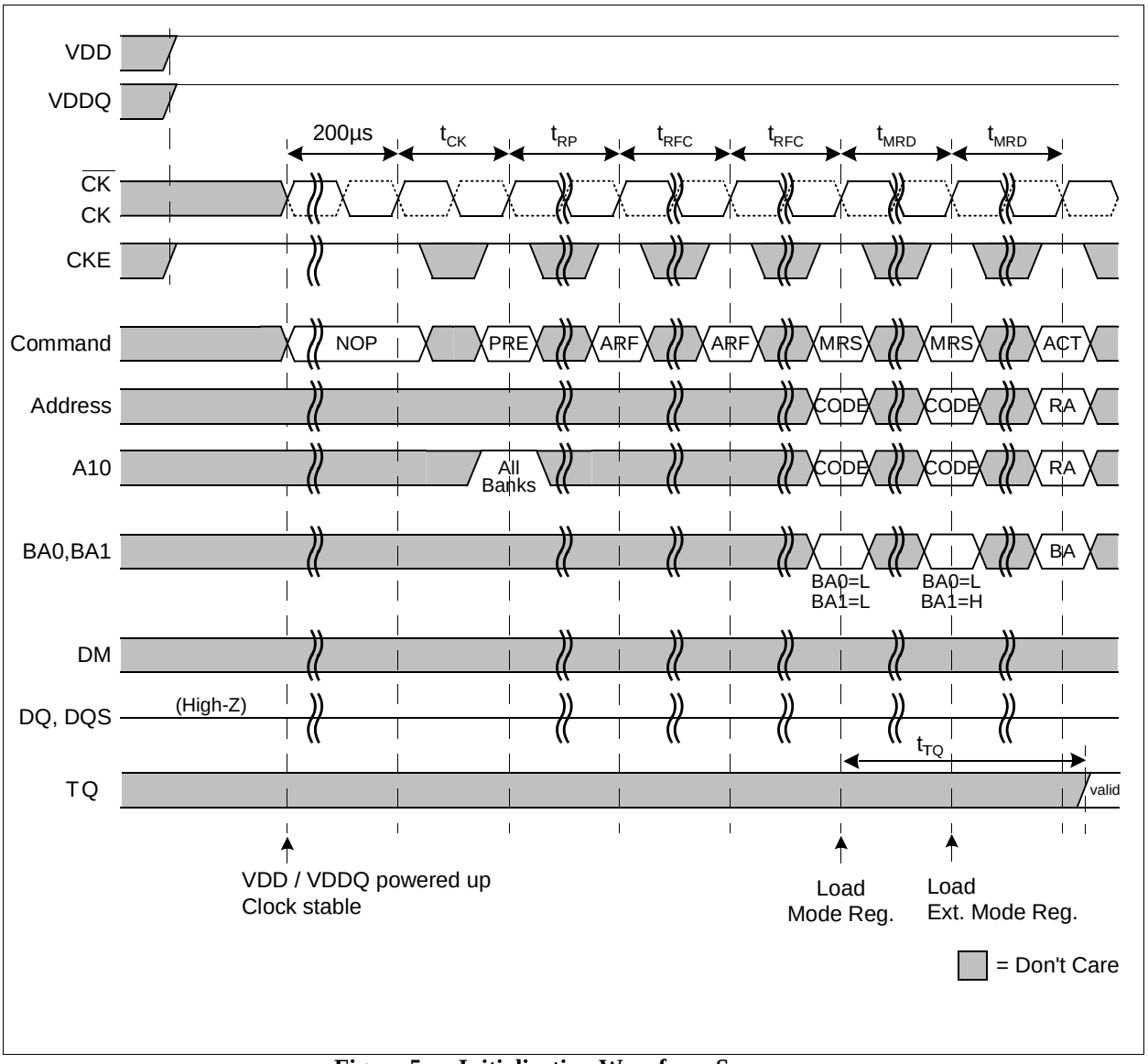


Figure 5 — Initialization Waveform Sequence

3.1.0.1 TQ Signal Initialization

During device initialization the TQ signal output will be invalid until tTQ after the first MRS command. Following tTQ the TQ signal will output logic-HIGH when the device temperature is greater than, or equal to, 85'C, and logic-LOW when the device temperature is less than 85'C. There is no high-impedance state for this output signal.

3 Functional Description (cont'd)

3.2 Register Definition

3.2.1 Mode Register

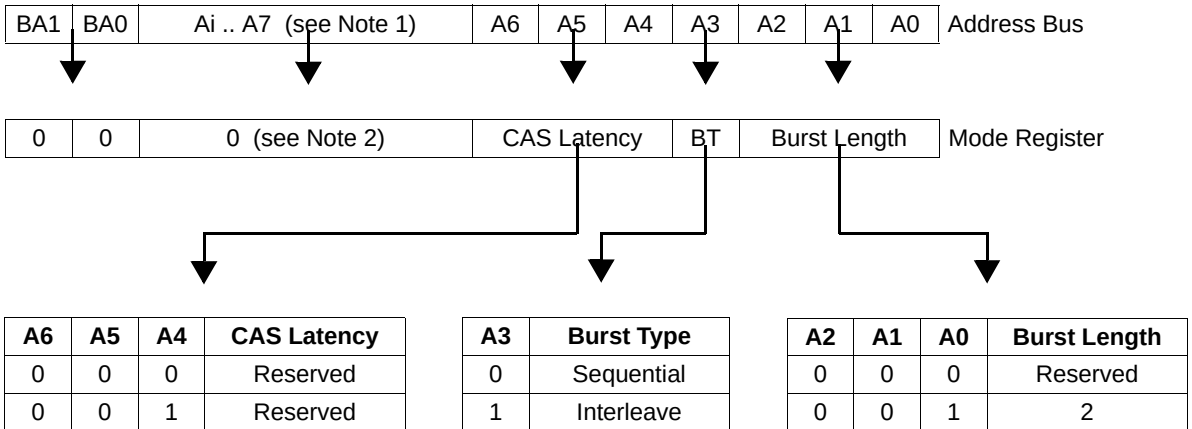
The Mode Register is used to define the specific mode of operation of the LPDDR SDRAM. This definition includes the definition of a burst length, a burst type, a CAS latency as shown in Figure 6.

The Mode Register is programmed via the MODE REGISTER SET command (with BA0=0 and BA1=0) and will retain the stored information until it is reprogrammed, the device goes into Deep Power-Down mode, or the device loses power.

Mode Register bits A0-A2 specify the burst length, A3 the type of burst (sequential or interleave), A4-A6 the CAS latency. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility.

The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.



A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 (optional)
0	1	1	3
1	0	0	4 (optional)
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16 (optional)
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

NOTE:
1. MSB depends on LPDDR SDRAM density.
2. A logic 0 should be programmed to all unused / undefined address bits to ensure future compatibility.

Figure 6 — Mode Register Definition

3.2.1.1 Burst Length

Read and write accesses to the LPDDR SDRAM are burst oriented, with the burst length being set as in Table 6, and the burst order as in Table 4.

The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types. A burst length of 16 is optional and some vendors may choose to implement it.

3 Functional Description (cont'd)
3.2 Register Definition (cont'd)

Table 4 — Burst Definition

BURST LENGTH	STARTING COLUMN ADDRESS				ORDER OF ACCESSES WITHIN A BURST (HEXADECIMAL NOTATION)	
	A3	A2	A1	A0	SEQUENTIAL	INTERLEAVED
2				0	0 - 1	0 - 1
				1	1 - 0	1 - 0
4			0	0	0 - 1 - 2 - 3	0 - 1 - 2 - 3
			0	1	1 - 2 - 3 - 0	1 - 0 - 3 - 2
			1	0	2 - 3 - 0 - 1	2 - 3 - 0 - 1
			1	1	3 - 0 - 1 - 2	3 - 2 - 1 - 0
8		0	0	0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
		0	0	1	1 - 2 - 3 - 4 - 5 - 6 - 7 - 0	1 - 0 - 3 - 2 - 5 - 4 - 7 - 6
		0	1	0	2 - 3 - 4 - 5 - 6 - 7 - 0 - 1	2 - 3 - 0 - 1 - 6 - 7 - 4 - 5
		0	1	1	3 - 4 - 5 - 6 - 7 - 0 - 1 - 2	3 - 2 - 1 - 0 - 7 - 6 - 5 - 4
		1	0	0	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3
		1	0	1	5 - 6 - 7 - 0 - 1 - 2 - 3 - 4	5 - 4 - 7 - 6 - 1 - 0 - 3 - 2
		1	1	0	6 - 7 - 0 - 1 - 2 - 3 - 4 - 5	6 - 7 - 4 - 5 - 2 - 3 - 0 - 1
		1	1	1	7 - 0 - 1 - 2 - 3 - 4 - 5 - 6	7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
16	0	0	0	0	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F
	0	0	0	1	1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-0	1-0-3-2-5-4-7-6-9-8-B-A-D-C-F-E
	0	0	1	0	2-3-4-5-6-7-8-9-A-B-C-D-E-F-0-1	2-3-0-1-6-7-4-5-A-B-8-9-E-F-C-D
	0	0	1	1	3-4-5-6-7-8-9-A-B-C-D-E-F-0-1-2	3-2-1-0-7-6-5-4-B-A-9-8-F-E-D-C
	0	1	0	0	4-5-6-7-8-9-A-B-C-D-E-F-0-1-2-3	4-5-6-7-0-1-2-3-C-D-E-F-8-9-A-B
	0	1	0	1	5-6-7-8-9-A-B-C-D-E-F-0-1-2-3-4	5-4-7-6-1-0-3-2-D-C-F-E-9-8-B-A
	0	1	1	0	6-7-8-9-A-B-C-D-E-F-0-1-2-3-4-5	6-7-4-5-2-3-0-1-E-F-C-D-A-B-8-9
	0	1	1	1	7-8-9-A-B-C-D-E-F-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-F-E-D-C-B-A-9-8
	1	0	0	0	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7
	1	0	0	1	9-A-B-C-D-E-F-0-1-2-3-4-5-6-7-8	9-8-B-A-D-C-F-E-1-0-3-2-5-4-7-6
	1	0	1	0	A-B-C-D-E-F-0-1-2-3-4-5-6-7-8-9	A-B-8-9-E-F-C-D-2-3-0-1-6-7-4-5
	1	0	1	1	B-C-D-E-F-0-1-2-3-4-5-6-7-8-9-A	B-A-9-8-F-E-D-C-3-2-1-0-7-6-5-4
	1	1	0	0	C-D-E-F-0-1-2-3-4-5-6-7-8-9-A-B	C-D-E-F-8-9-A-B-4-5-6-7-0-1-2-3
	1	1	0	1	D-E-F-0-1-2-3-4-5-6-7-8-9-A-B-C	D-C-F-E-9-8-B-A-5-4-7-6-1-0-3-2
	1	1	1	0	E-F-0-1-2-3-4-5-6-7-8-9-A-B-C-D	E-F-C-D-A-B-8-9-6-7-4-5-2-3-0-1
	1	1	1	1	F-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E	F-E-D-C-B-A-9-8-7-6-5-4-3-2-1-0

NOTES:

1. 16-word burst length is optional.
2. For a burst length of two, A1-An selects the two data element block; A0 selects the first access within the block.
3. For a burst length of four, A2-An selects the four data element block; A0-A1 selects the first access within the block.
4. For a burst length of eight, A3-An selects the eight data element block; A0-A2 selects the first access within the block.
5. For the optional burst length of sixteen, A4-An selects the sixteen data element block; A0-A3 selects the first access within the block.
6. Whenever a boundary of the block is reached within a given sequence, the following access wraps within the block.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached.

3 Functional Description (cont'd)
3.2 Register Definition (cont'd)

The block is uniquely selected by A1-An when the burst length is set to two, by A2-An when the burst length is set to 4, by A3-An when the burst length is set to 8 and A4-An when the burst length is set to 16 (where An is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

3.2.1.2 Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 4.

3.2.1.3 Read Latency

The READ latency, or CAS latency, is the delay between the registration of a READ command and the availability of the first piece of output data. The latency should be set to 3 clocks. Some vendors may offer additional options of 2 clocks and/or 4 clocks.

If a READ command is registered at a clock edge n and the latency is 3 clocks, the first data element will be valid at $n + 2t_{CK} + t_{AC}$. If a READ command is registered at a clock edge n and the latency is 2 clocks, the first data element will be valid at $n + t_{CK} + t_{AC}$. Lastly, if a READ command is registered at a clock edge n and the latency is 4 clocks, the first data element will be valid at $n + 3t_{CK} + t_{AC}$.

3.2.2 Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include output drive strength selection, Temperature Compensated Self Refresh (TCSR) and Partial Array Self Refresh (PASR), as shown in Figure 7. The TCSR and PASR functions are optional and some vendors may choose not to implement them. Both TCSR and PASR are effective is in Self Refresh mode only.

The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=1 and BA0=0) and will retain the stored information until it is reprogrammed, the device is put in Deep Power-Down mode, or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Address bits A0-A2 specify PASR, A3-A4 the TCSR, A5-A6 the Drive Strength. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility.

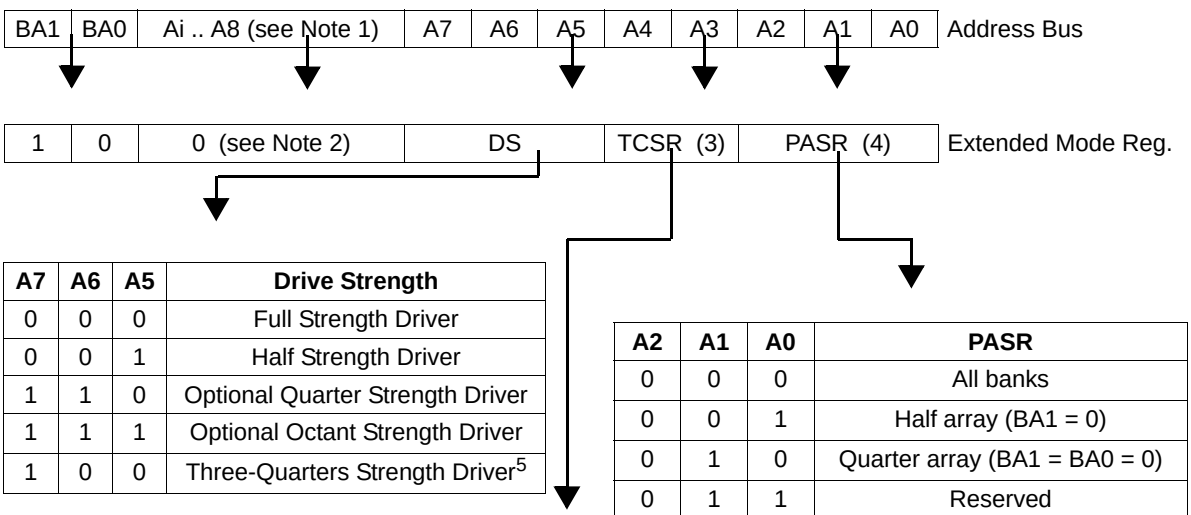
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Address bits A0-A2 specify PASR, A3-A4 the TCSR, A5-A7 the Drive Strength.

A logic 0 should be programmed to all the undefined address bits to ensure future compatibility.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

3 Functional Description (cont'd)
3.2 Register Definition (cont'd)



A7	A6	A5	Drive Strength
0	0	0	Full Strength Driver
0	0	1	Half Strength Driver
1	1	0	Optional Quarter Strength Driver
1	1	1	Optional Octant Strength Driver
1	0	0	Three-Quarters Strength Driver[5]

A4	A3	Max. Temp.
0	0	70 °C
0	1	45 °C
0	0	15 °C
1	1	85 °C

A2	A1	A0	PASR
0	0	0	All banks
0	0	1	Half array (BA1 = 0)
0	1	0	Quarter array (BA1 = BA0 = 0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	1/8 array (optional) (BA1 = BA0 = Row Addr MSB = 0)
1	1	0	1/16 array (optional) (BA1 = BA0 = Row Addr 2 MSB = 0)
1	1	1	Reserved

NOTES:
1. MSB depends on LPDDR SDRAM density.
2. A logic 0 should be programmed to all unused / undefined address bits to ensure future compatibility.
3. TCSR feature is optional; temperatures specified for the TCSR feature are case temperatures.
4. PASR feature is optional.
5. Implementation and availability of Three-Quarters Strength Driver is optional for speed bins LPDDR333 and below.

Figure 7 — Extended Mode Register Definition

3.2.2.1 Partial Array Self Refresh (Optional)

Partial Array Self Refresh (PASR) is an optional feature. With PASR, the self refresh may be restricted to a variable portion of the total array. The whole array (default), 1/2 array, or 1/4 array could be selected. Some vendors may have additional options of 1/8 and 1/16 array refreshed as well. Data outside the defined area will be lost. Address bits A0 to A2 are used to set PASR.

3.2.2.2 Temperature Compensated Self Refresh (Optional)

Temperature Compensated Self Refresh (TCSR) is an optional feature. This function can be used in the LPDDR SDRAM to set refresh rates based on case temperature.This allows the system to control power as a function of temperature. Address bits A3 and A4 are used to set TCSR.

Some vendors may choose to have Internal Temperature Compensated Self Refresh feature, which should automatically adjust the refresh rate based on the device temperature without any register update needed. To maintain backward compatibility, devices having internal TCSR, ignore (don't care) the inputs to address bits A3 and A4 during EMRS programming.

3.2.2.3 Output Drive Strength

The drive strength could be set to full or half or three-quarters strength via address bits A5 and A6 and

A7. The I-V curves for the full drive strength and half drive strength and three-quarters drive strength are included in this document (cf. Table 17 and Table 18, Figure 45 and Figure 46 and Figure 47).

3 Functional Description (cont'd)
3.2 Register Definition (cont'd)

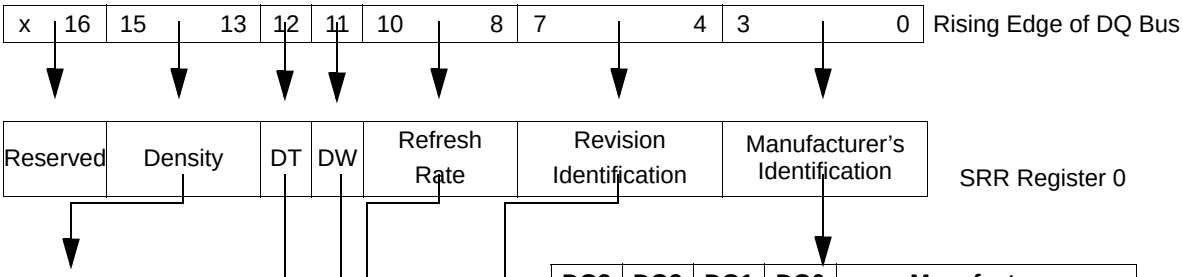
3.2.3 Status Register Read (Optional)

Status Register Read (SRR) is an optional feature. With SRR, a method is defined to read registers from the SDRAM. The encoding for an SRR command is the same as a MRS with BA[1:0] = "01". The address pins (A[n:0]) encode which register is to be read. Currently only one register is defined at A[n:0] = 0. Refer to Figure 1 for the definition of this register. The sequence to perform an SRR command is as follows:

- all reads/writes must be completed
- all banks must be closed
- MRS with BA = 01 is issued (SRR)
- wait tSRR
- Read issued to any bank/page
- CAS latency cycles later the SDRAM returns the registers data as it would a normal read
- The next command to the SDRAM can be issued tSRC after the Read command was issued. (Refer to Figure 8)

The burst length for the SRR read is always fixed to length 2.

3 Functional Description (cont'd)
3.2 Register Definition (cont'd)



DQ15	DQ14	DQ13	Density
0	0	0	128
0	0	1	256
0	1	0	512
0	1	1	1024
1	0	0	1024
1	0	1	Reserved
1	1	0	Reserved
1	1	1	64

DQ12	Device Type
0	LPDDR
1	Reserved

DQ11	DW
0	16 bits
1	32 bits

DQ10	DQ9	DQ8	Refresh Rate
1	1	1	0.25 (see Note 2)
1	1	0	0.25
1	0	1	0.5
1	0	0	1
0	1	1	2
0	1	0	4
0	0	x	4 (see Note 3)

DQ3	DQ2	DQ1	DQ0	Manufacturer
0	0	0	0	Reserved
0	0	0	1	Samsung
0	0	1	0	Infineon
0	0	1	1	Elpida
0	1	0	0	Etron
0	1	0	1	Nanya
0	1	1	0	Hynix
0	1	1	1	Mosel
1	0	0	0	Winbond
1	0	0	1	ESMT
1	0	1	0	NVM (see Note 6)
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Micron

Note 6: Indicates a non-volatile memory.

DQ7:4	Revision ID
	(See Note 1)

Note 1: The manufacturer's revision number starts at '0000' and increments by '0001' each time a change in the manufacturer's specification (AC timings, or feature set), IBIS

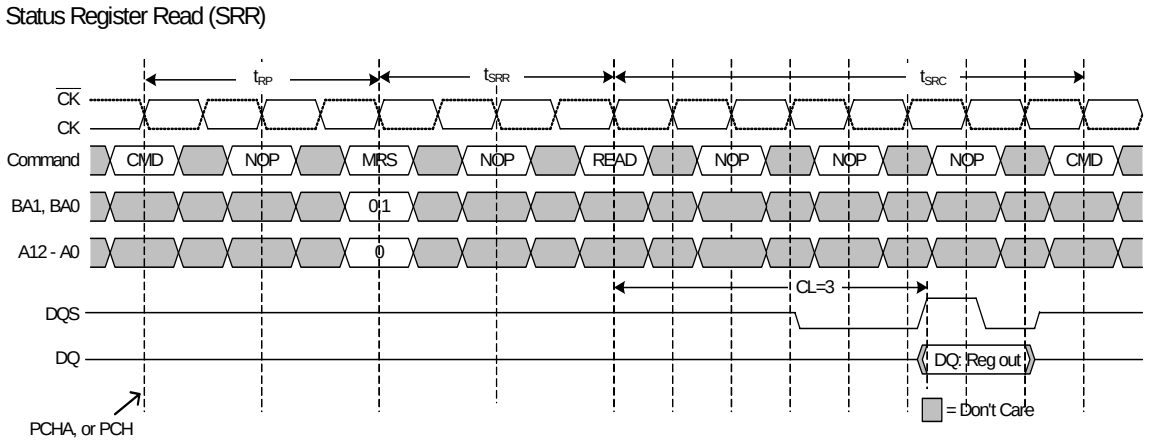
Note 2: High temperature out of range - no refresh rate can guarantee functionality.

Note 3: Low temperature out of range.

Note 4: The refresh rate multiplier is based on the memory's temperature sensor.

Figure 8 — SRR Register (A[n:0] = 0)

3 Functional Description (cont'd)
3.2 Register Definition (cont'd)



Notes:
1) SRR can only be issued after power-up sequence is complete;
2) SRR can only be issued with all banks precharged;
3) SRR CL is unchanged from value in the mode register;
4) SRR BL is fixed at 2;
5) tSRR = 2 (min)
6) tSRC = CL + 1; (min time between read to next valid command)
7) No commands other than NOP and DES are allowed between the SRR and the READ.

Figure 9 — Status Register Read Timing Diagram

3.2.4 Temperature Output Signal (optional)

The LPDDR-SDRAM device may include an optional temperature output signal (TQ). This signal is an asynchronous LVCMOS output which outputs a logic-HIGH when the device temperature is greater than, or equal to, 85'C and a logic-LOW when the device temperature is less than 85'C. There is no high-impedance state output from this signal. The TQ output signal activates even during clock stop, power down, and self refresh modes. The signal is not valid during initialization (see See "Initialization" on page 10.) and becomes valid after t_{TQ} following the first MRS command. When TQ output is logic-HIGH, tREF is specified to be 16ms. Additionally, AC parameters shall be de-rated to 20% and DC parameters shall not be guaranteed.

4 Commands

All commands (address and control signals) are registered on the positive edge of clock (crossing of CK going high and CK going low). Figure 10 shows basic timing parameters for all commands.

Table 5, Table 6 and Table 7 provide a quick reference of available commands.

Table 8 and Table 9 provide the current state / next state information. This is followed by a verbal description of each command.

Table 5 — Truth Table - Commands [Notes 1-11]

NAME (FUNCTION)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10/AP	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	X	X	2
ACTIVE (select bank and activate row)	L	L	H	H	Valid	Row	Row	
READ (select bank and column and start read burst)	L	H	L	H	Valid	L	Col	
READ with AP (read burst with Auto Precharge)	L	H	L	H	Valid	H	Col	3
WRITE (select bank and column and start write burst)	L	H	L	L	Valid	L	Col	
WRITE with AP (write burst with Auto Precharge)	L	H	L	L	Valid	H	Col	3
BURST TERMINATE or enter DEEP POWER DOWN	L	H	H	L	X	X	X	4, 5
PRECHARGE (deactivate row in selected bank)	L	L	H	L	Valid	L	X	6
PRECHARGE ALL (deactivate rows in all banks)	L	L	H	L	X	H	X	6
AUTO REFRESH or enter SELF REFRESH	L	L	L	H	X	X	X	7,8,9
MODE REGISTER SET	L	L	L	L	Valid	Op-code		10

NOTES:

1. All states and sequences not shown are illegal or reserved.
2. DESELECT and NOP are functionally interchangeable.
3. Autoprecharge is non-persistent. A10 High enables Auto Precharge, while A10 Low disables Autoprecharge
4. Burst Terminate applies to only Read bursts with Auto Precharge disabled. This command is undefined and should not be used for Read with Auto Precharge enabled, and for Write bursts.
5. This command is BURST TERMINATE if CKE is High and DEEP POWER DOWN entry if CKE is Low.
6. If A10 is Low, bank address determines which bank is to be precharged. If A10 is High, all banks are precharged and BA0-BA1 are don't care.
7. This command is AUTO REFRESH if CKE is High, and SELF REFRESH if CKE is low.
8. All address inputs and I/O are 'don't care' except for CKE. Internal refresh counters control bank and row addressing.
9. All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.
10. BA0 and BA1 value select between MRS and EMRS.
11. CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER-DOWN.

Table 6 — Truth Table - DM Operations

FUNCTION	DM	DQ	NOTES
Write Enable	L	Valid	1
Write Inhibit	H	X	1

NOTE 1 Used to mask write data, provided coincident with the corresponding data.

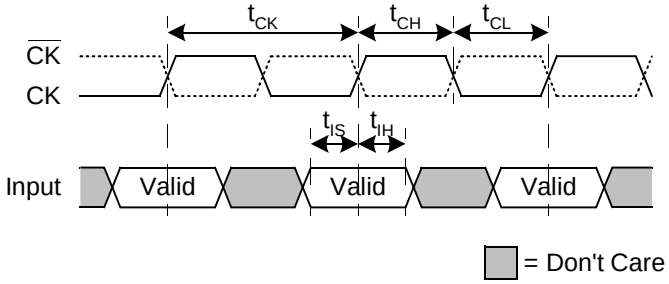
4 Commands (cont'd)

Table 7 — Truth Table - CKE [Notes 1 - 10]

CKE n-1	CKE n	Current State	COMMAND n	ACTION n	NOTES
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	L	Deep Power Down	X	Maintain Deep Power Down	
L	H	Power Down	NOP or DESELECT	Exit Power Down	5, 6, 9
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	5, 7, 10
L	H	Deep Power Down	NOP or DESELECT	Exit Deep Power Down	5, 8
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	5
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	5
H	L	All Banks Idle	AUTO REFRESH	Self Refresh entry	
H	L	All Banks Idle	BURST TERMINATE	Enter Deep Power Down	
H	H	See the other Truth Tables			

NOTES:

1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of LPDDR immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is the result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT and NOP are functionally interchangeable.
6. Power Down exit time (t_{XP}) should elapse before a command other than NOP or DESELECT is issued.
7. SELF REFRESH exit time (t_{XSR}) should elapse before a command other than NOP or DESELECT is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9. The clock must toggle at least once during the t_{XP} period.
10. The clock must toggle at least once during the t_{XSR} time.



NOTE: Input = A0 - An, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$;
An = Address bus MSB

Figure 10 — Basic Timing Parameters for Commands

4 Commands (cont'd)

Table 8 — Truth Table - Current State Bank n - Command to Bank n [Notes 1 - 13]

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND / ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	
	L	H	H	H	No Operation (NOP / continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	10
	L	L	L	L	MODE REGISTER SET	10
Row Active	L	H	L	H	READ (select column & start read burst)	
	L	H	L	L	WRITE (select column & start write burst)	
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	4
Read (Auto Precharge Disabled)	L	H	L	H	READ (select column & start new read burst)	5, 6
	L	H	L	L	WRITE (select column & start write burst)	5, 6,13
	L	L	H	L	PRECHARGE (truncate read burst, start precharge)	
	L	H	H	L	BURST TERMINATE	11
Write (Auto Precharge Disabled)	L	H	L	H	READ (select column & start read burst)	5, 6,12
	L	H	L	L	WRITE (select column & start new write burst)	5, 6
	L	L	H	L	PRECHARGE (truncate write burst, start precharge)	12

NOTES:

1. The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
5. A command other than NOP should not be issued to the same bank while a READ or WRITE burst with Auto Precharge is enabled.
6. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
7. Current State Definitions:

   Idle: The bank has been precharged, and t_{RP} has been met.

   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

   Write: a WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
8. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 8, and according to Table 9.

   Precharging: starts with the registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.

   Row Activating: starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the 'row active' state.

   Read with AP Enabled: starts with the registration of the READ command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} has been met, the bank will be in the idle state.

   Write with AP Enabled: starts with registration of a WRITE command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
9. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied to each positive clock edge during these states.

   Refreshing: starts with registration of an AUTO REFRESH command and ends when t_{RFC} is met. Once t_{RFC} is met, the device will be in an 'all banks idle' state.

   Accessing Mode Register: starts with registration of a MODE REGISTER SET command and ends when t_{MRD} has been met. Once t_{MRD} is met, the device will be in an 'all banks idle' state.

   Precharging All: starts with the registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
10. Not bank-specific; requires that all banks are idle and no bursts are in progress.

4 Commands (cont'd)

Table 8, Notes (cont'd)

11. Not bank-specific. BURST TERMINATE affects the most recent read burst, regardless of bank.
12. Requires appropriate DM masking.
13. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ prior to asserting a WRITE command.

4 Commands (cont'd)

Table 9 — Truth Table - Current State Bank n - Command to Bank m [Notes 1 - 10]

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND / ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	
	L	H	H	H	No Operation (NOP / continue previous operation)	
Idle	X	X	X	X	Any command allowed to bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start read burst)	8
	L	H	L	L	WRITE (select column & start write burst)	8
	L	L	H	L	PRECHARGE	
Read (Auto Precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start new read burst)	8
	L	H	L	L	WRITE (select column & start write burst)	8,10
	L	L	H	L	PRECHARGE	
Write (Auto Precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start read burst)	8,9
	L	H	L	L	WRITE (select column & start new write burst)	8
	L	L	H	L	PRECHARGE	
Read with Auto Precharge	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start new read burst)	5, 8
	L	H	L	L	WRITE (select column & start write burst)	5, 8, 10
	L	L	H	L	PRECHARGE	
Write with Auto Precharge	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start read burst)	5, 8
	L	H	L	L	WRITE (select column & start new write burst)	5, 8
	L	L	H	L	PRECHARGE	

NOTES:

1. The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. Current State Definitions:

   Idle: the bank has been precharged, and t_{RP} has been met.

   Row Active: a row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.

   Read: a READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

   Write: a WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
5. Read with AP enabled and Write with AP enabled: the Read with Auto Precharge enabled or Write with Auto Precharge enabled states can be broken into two parts: the access period and the precharge period. For Read with AP, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst. For Write with AP, the precharge period begins when t_{WR} ends, with t_{WR} measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the Read with AP enabled or Write with AP enabled states, ACTIVE, PRECHARGE, READ, and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other banks may be applied. In either case, all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).
6. AUTO REFRESH, SELF REFRESH, and MODE REGISTER SET commands may only be issued when all bank are idle.
7. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.

4 Commands (cont'd)

Table 9, Notes (cont'd)

8. READs or WRITEs listed in the Command column include READs and WRITEs with Auto Precharge enabled and READs and WRITEs with Auto Precharge disabled.
9. Requires appropriate DM masking.
10. A WRITE command may be applied after the completion of data output, otherwise a BURST TERMINATE command must be issued to end the READ prior to asserting a WRITE command.

5 Operation

5.1 Deselect

The DESELECT function ($\overline{CS}$ = High) prevents new commands from being executed by the LPDDR SDRAM. The LPDDR SDRAM is effectively deselected. Operations already in progress are not affected.

5.2 No Operation

The NO OPERATION (NOP) command (see Figure 11) is used to perform a NOP to a LPDDR SDRAM that is selected ($\overline{CS}$ = Low). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

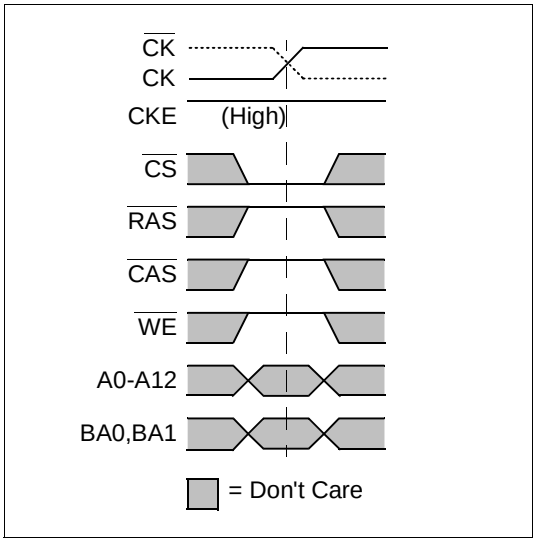


Figure 11 — NOP Command

5.3 Mode Register Set

The Mode Register and the Extended Mode Register are loaded via the address inputs. See Mode Register (Figure 6) and the Extended Mode Register (Figure 7) descriptions for further details.

The MODE REGISTER SET command (see Figure 12) can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until t_{MRD} (see Figure 13) is met.

5 Operation (cont'd)
5.3 Mode Register Set (cont'd)

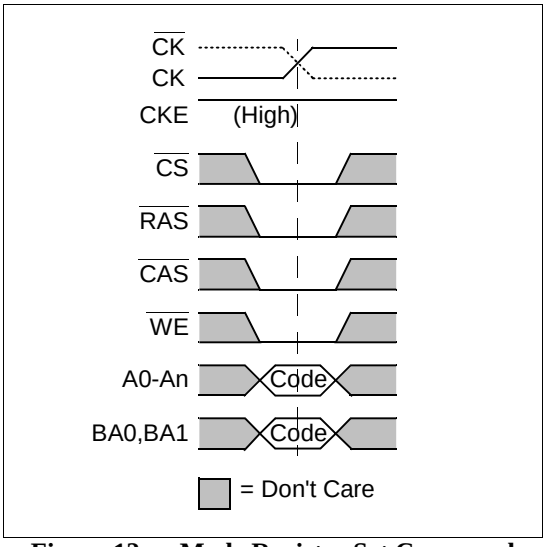


Figure 12 — Mode Register Set Command

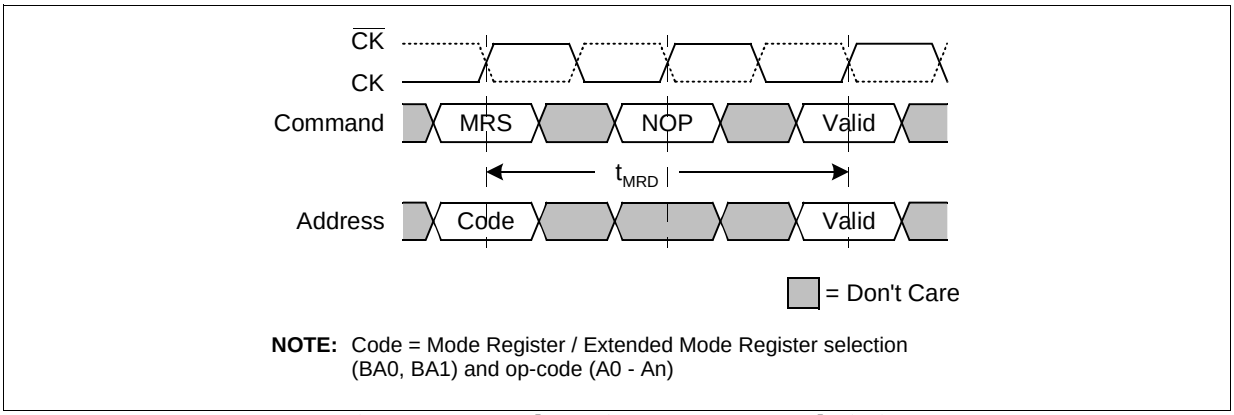


Figure 13 — Mode Register Set Command Timing

5.4 Active

Before any READ or WRITE commands can be issued to a bank in the LPDDR SDRAM, a row in that bank must be opened. This is accomplished by the ACTIVE command (see Figure 14): BA0 and BA1 select the bank, and the address inputs select the row to be activated. More than one bank can be active at any time.

Once a row is open, a READ or WRITE command could be issued to that row, subject to the t_{RCD} specification.

A subsequent ACTIVE command to another row in the same bank can only be issued after the previous row has been closed. The minimum time interval between two successive ACTIVE commands on the same bank is defined by t_{RC}.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between two successive ACTIVE commands on different banks is defined by t_{RRD}. Figure 15 shows the t_{RCD} and t_{RRD} definition.

The row remains active until a PRECHARGE command (or READ or WRITE command with Auto Precharge) is issued to the bank.

A PRECHARGE command (or READ or WRITE command with Auto Precharge) must be issued before opening a different row in the same bank.

5 Operation (cont'd)
5.4 Active (cont'd)

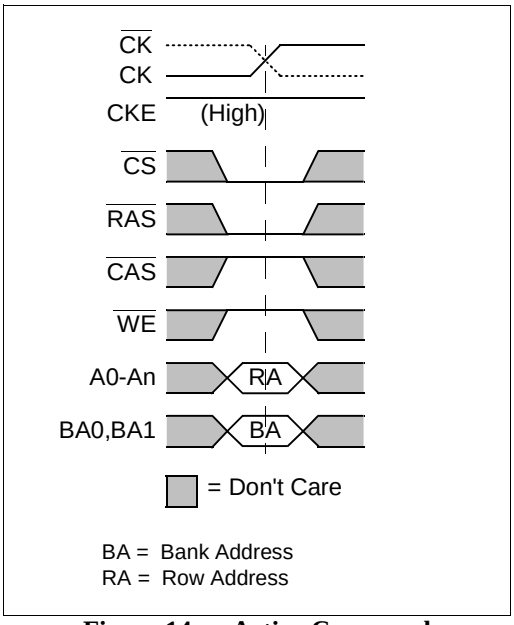


Figure 14 — Active Command

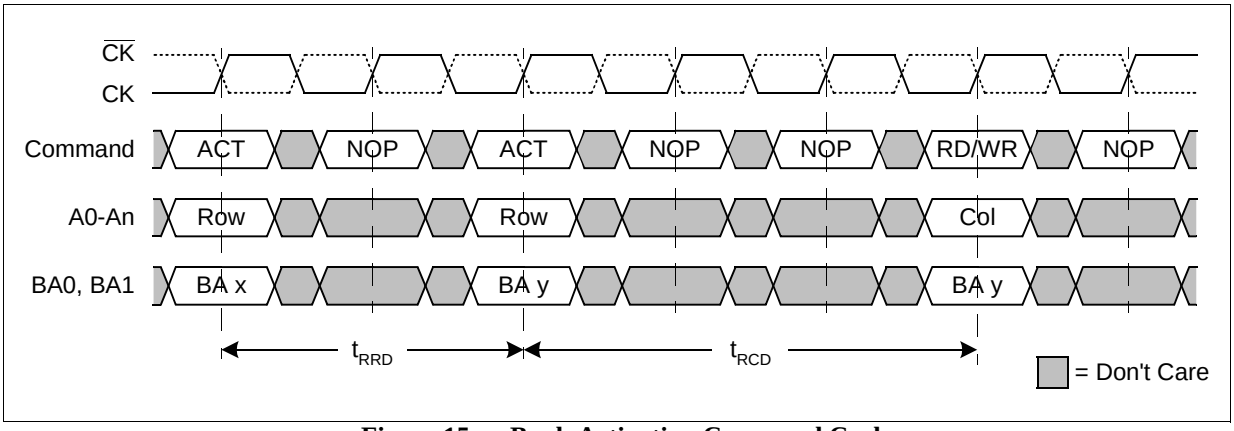


Figure 15 — Bank Activation Command Cycle

5.5 Read

The READ command (see Figure 16) is used to initiate a burst read access to an active row, with a burst length as set in the Mode Register. BA0 and BA1 select the bank, and the address inputs select the starting column location. The value of A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed will be precharged at the end of the read burst; if Auto Precharge is not selected, the row will remain open for subsequent accesses.

The basic Read timing parameters for DQs are shown in Figure 17; they apply to all Read operations.

During Read bursts, DQS is driven by the LPDDR SDRAM along with the output data. The initial Low state of the DQS is known as the read preamble; the Low state coincident with last data-out element is known as the read postamble. The first data-out element is edge aligned with the first rising edge of DQS and the successive data-out elements are edge aligned to successive edges of DQS. This is shown in Figure 18 with a CAS latency of 2 and 3.

Upon completion of a read burst, assuming no other READ command has been initiated, the DQs will go to High-Z.

5 Operation (cont'd)
5.5 Read (cont'd)

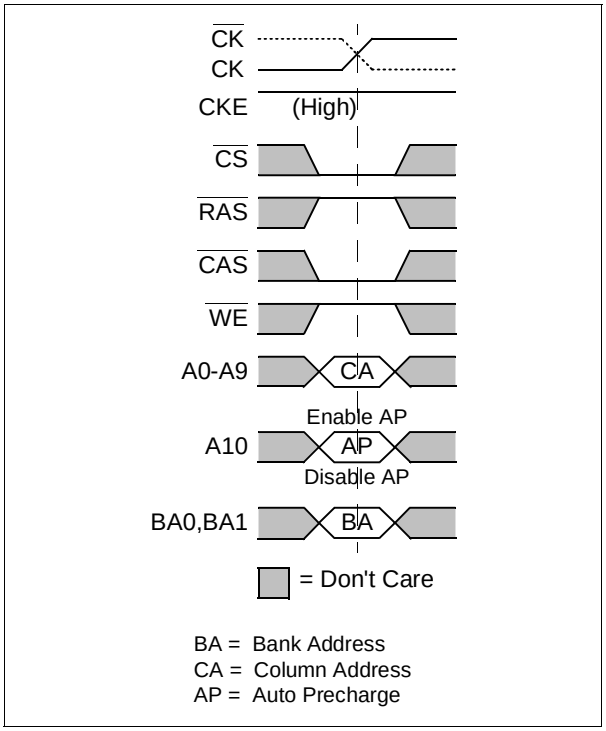


Figure 16 — Read Command

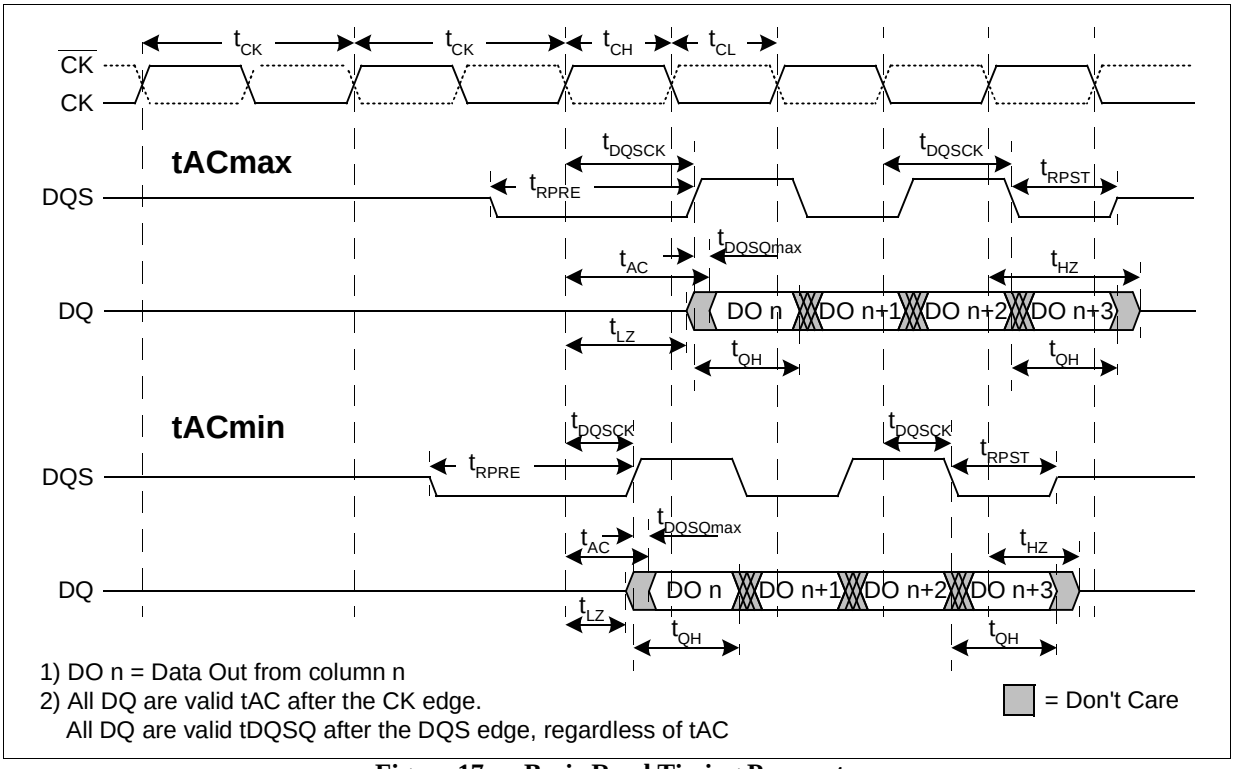


Figure 17 — Basic Read Timing Parameters

5 Operation (cont'd)
5.5 Read (cont'd)

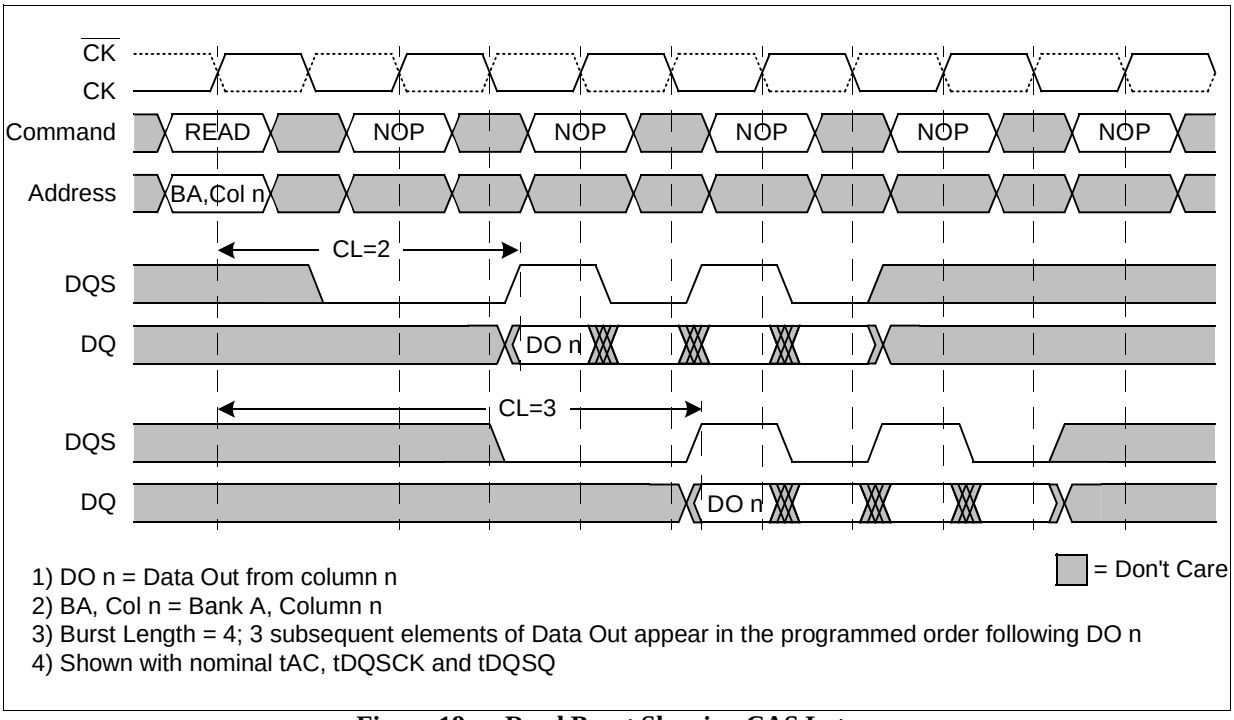


Figure 18 — Read Burst Showing CAS Latency

5.5.1 Read to Read

Data from a read burst may be concatenated or truncated by a subsequent READ command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data-out element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 19.

A READ command can be initiated on any clock cycle following a previous READ command. Non-consecutive Reads are shown in Figure 20.

Full-speed random read accesses within a page or pages can be performed as shown in Figure 21.

5.5.2 Read Burst Terminate

Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 22. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command where X equals the desired data-out element pairs.

5.5.3 Read to Write

Data from READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 23 for the case of nominal tDQSS .

5.5.4 Read to Precharge

A Read burst may be followed by or truncated with a PRECHARGE command to the same bank (provided Auto Precharge was not activated). The PRECHARGE command should be issued X cycles after the READ command, where X equal the number of desired data-out element pairs. This is shown in Figure 24. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met. Note that part of the row precharge time is hidden during the access of the last data-out elements.

In the case of a Read being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from Read burst with Auto Precharge enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address

5 Operation (cont'd)
5.5 Read (cont'd)

buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

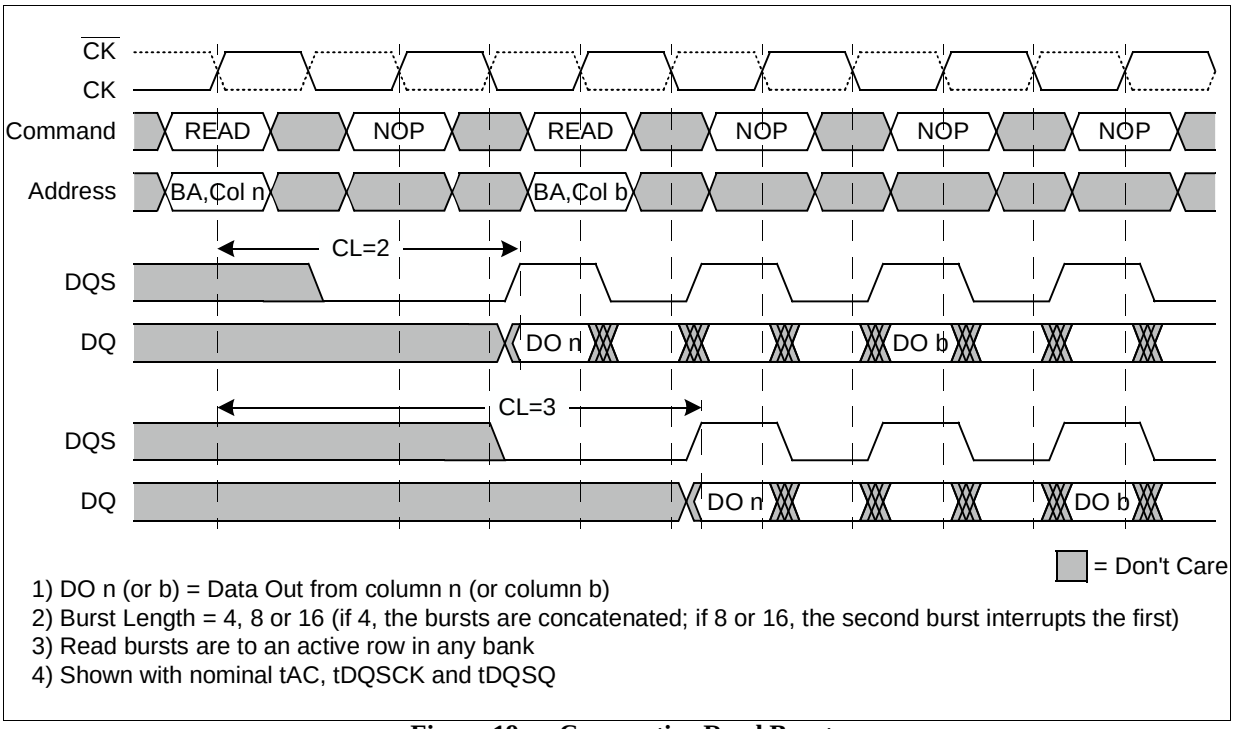


Figure 19 — Consecutive Read Bursts

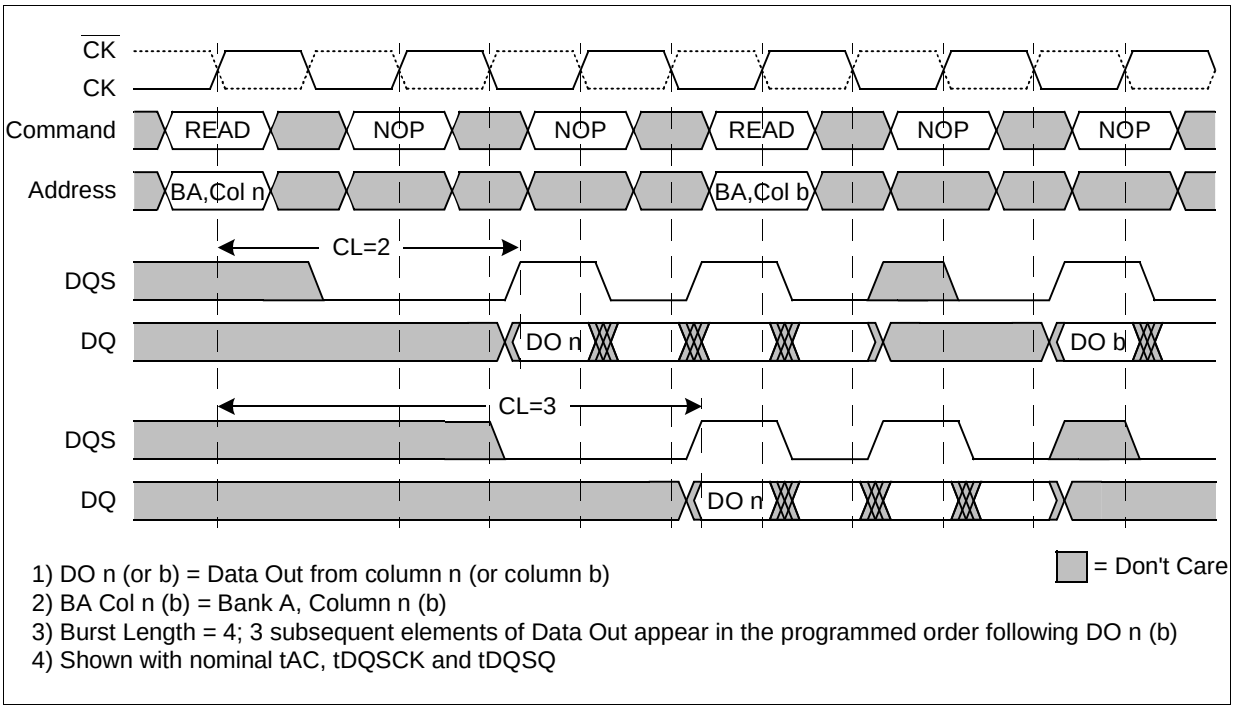


Figure 20 — Non-Consecutive Read Bursts

5 Operation (cont'd)
5.5 Read (cont'd)

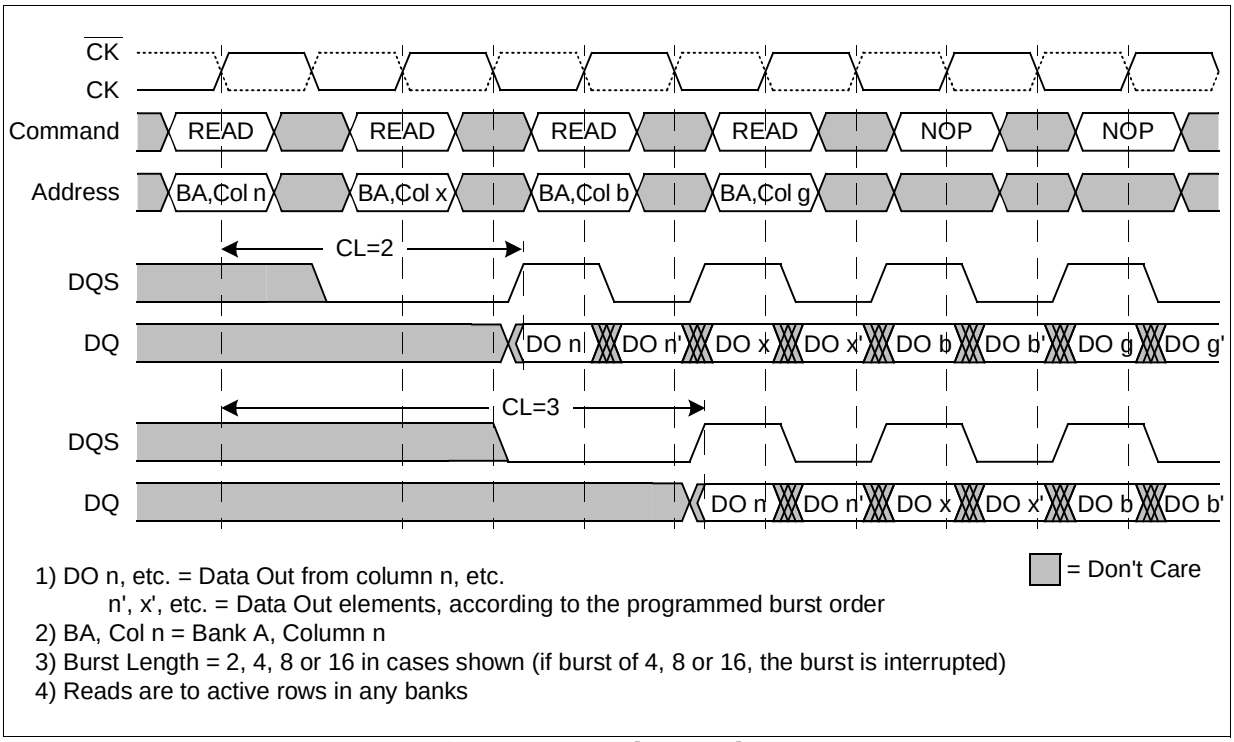


Figure 21 — Random Read Bursts

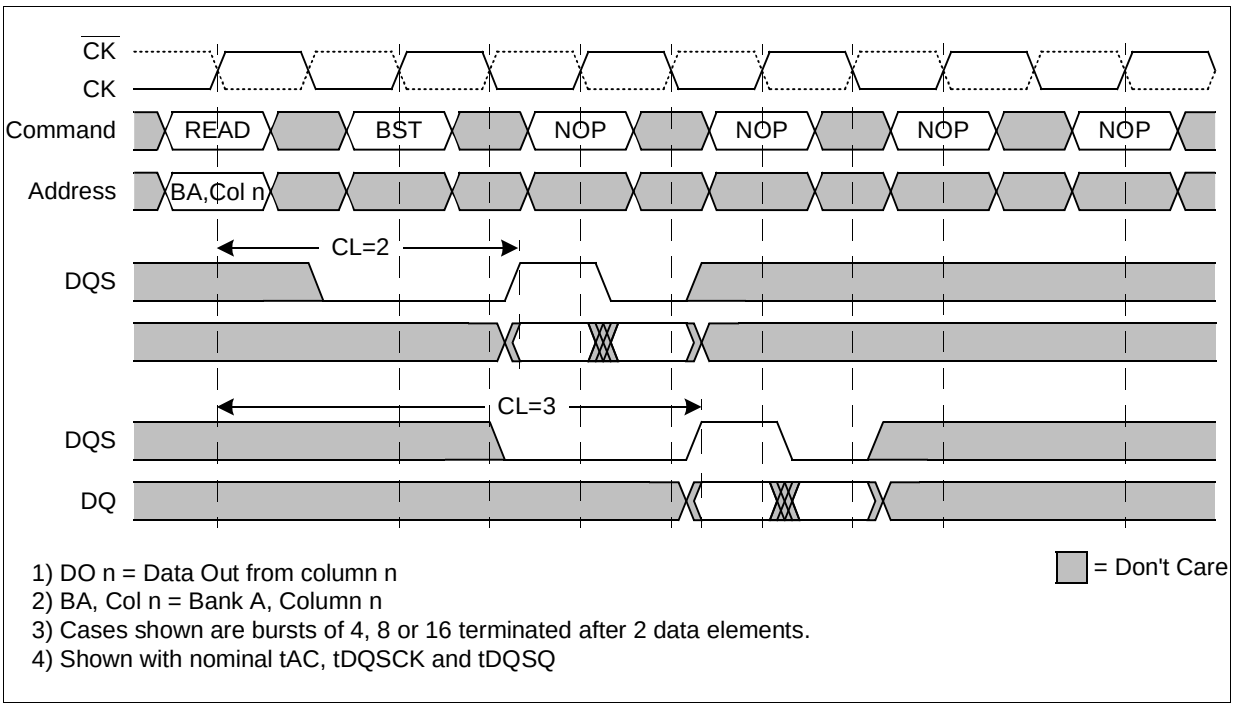


Figure 22 — Terminating a Read Burst

5 Operation (cont'd)
5.5 Read (cont'd)

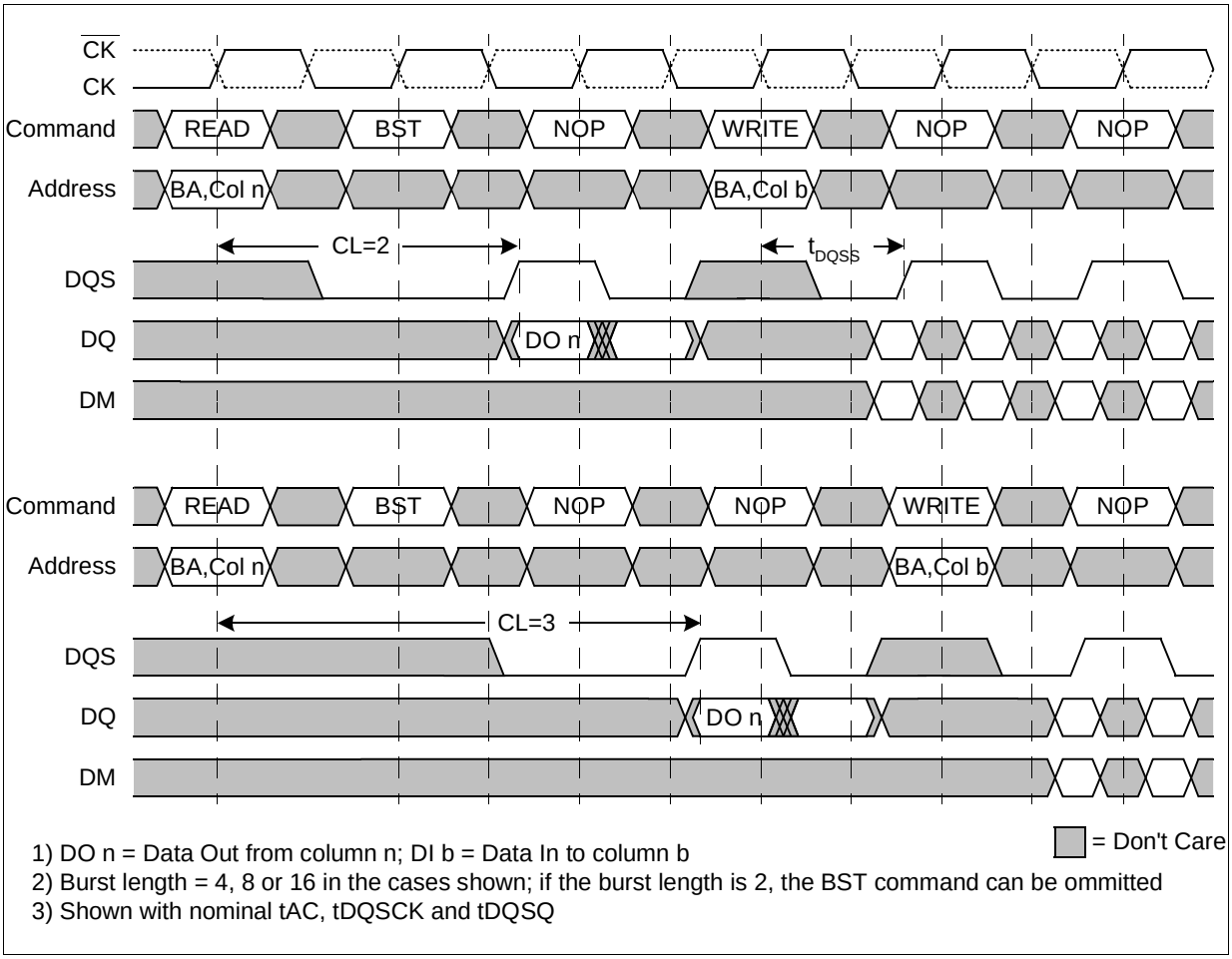


Figure 23 — Read To Write

5 Operation (cont'd)
5.5 Read (cont'd)

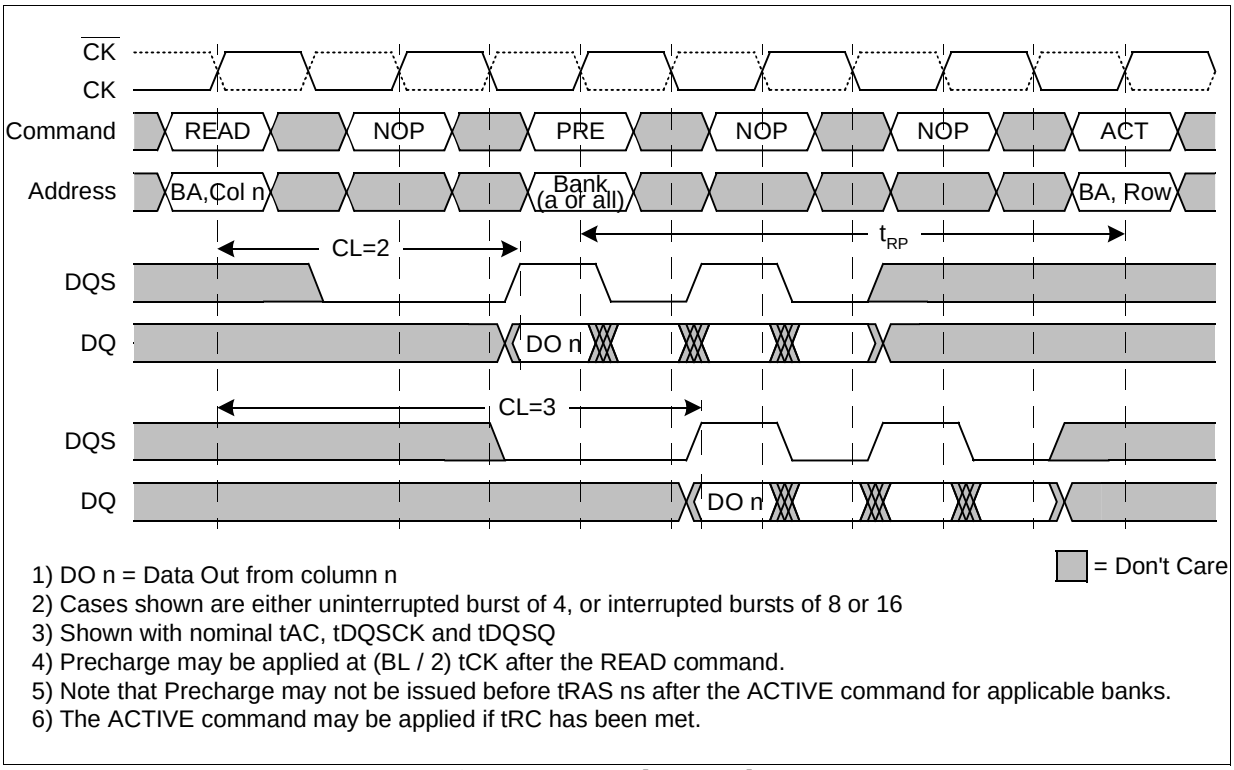


Figure 24 — Read To Precharge

5.5.5 Burst Terminate

The BURST TERMINATE command (see Figure 25) is used to truncate read bursts (with Auto Precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated. Note that the BURST TERMINATE command is not bank specific.

This command should not be used to terminate write bursts.

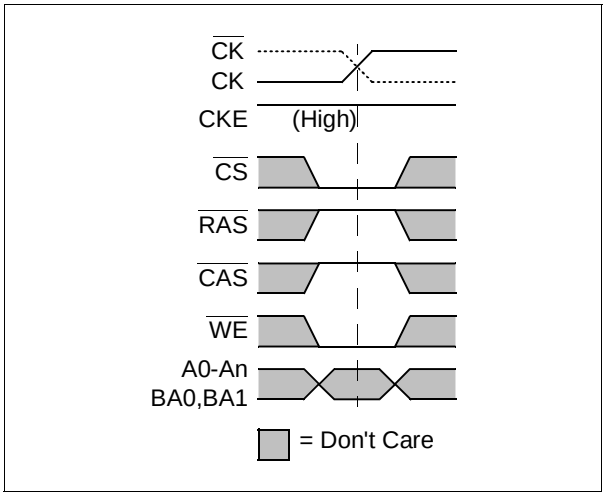


Figure 25 — Burst Terminate Command

5.6 Write

The WRITE command (see Figure 26) is used to initiate a burst write access to an active row, with a burst length as set in the Mode Register. BA0 and BA1 select the bank, and the address inputs select the starting column location. The value of A10 determines whether or not Auto Precharge is used. If Auto Precharge is

5 Operation (cont'd)
5.6 Write (cont'd)

selected, the row being accessed will be precharged at the end of the write burst; if Auto Precharge is not selected, the row will remain open for subsequent accesses.

Basic Write timing parameters for DQs are shown in Figure 27; they apply to all Write operations.

Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered Low, the corresponding data will be written to the memory; if the DM signal is registered High, the corresponding data inputs will be ignored, and a write will not be executed to that byte / column location.

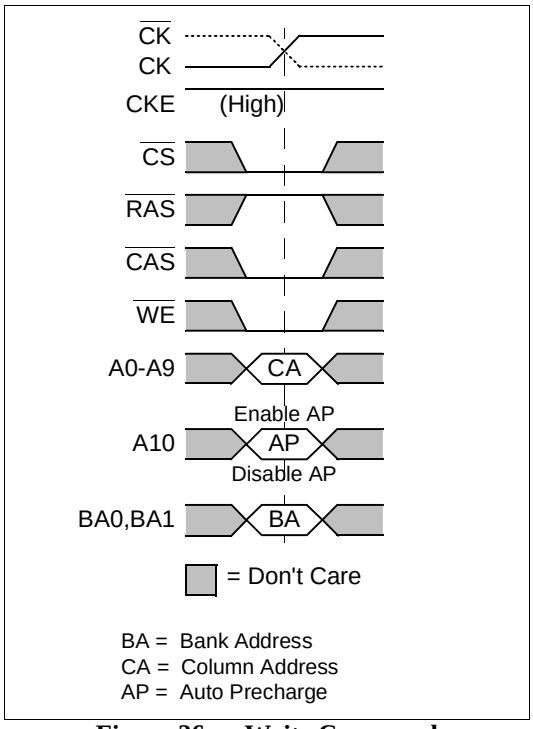


Figure 26 — Write Command

5 Operation (cont'd)
5.6 Write (cont'd)

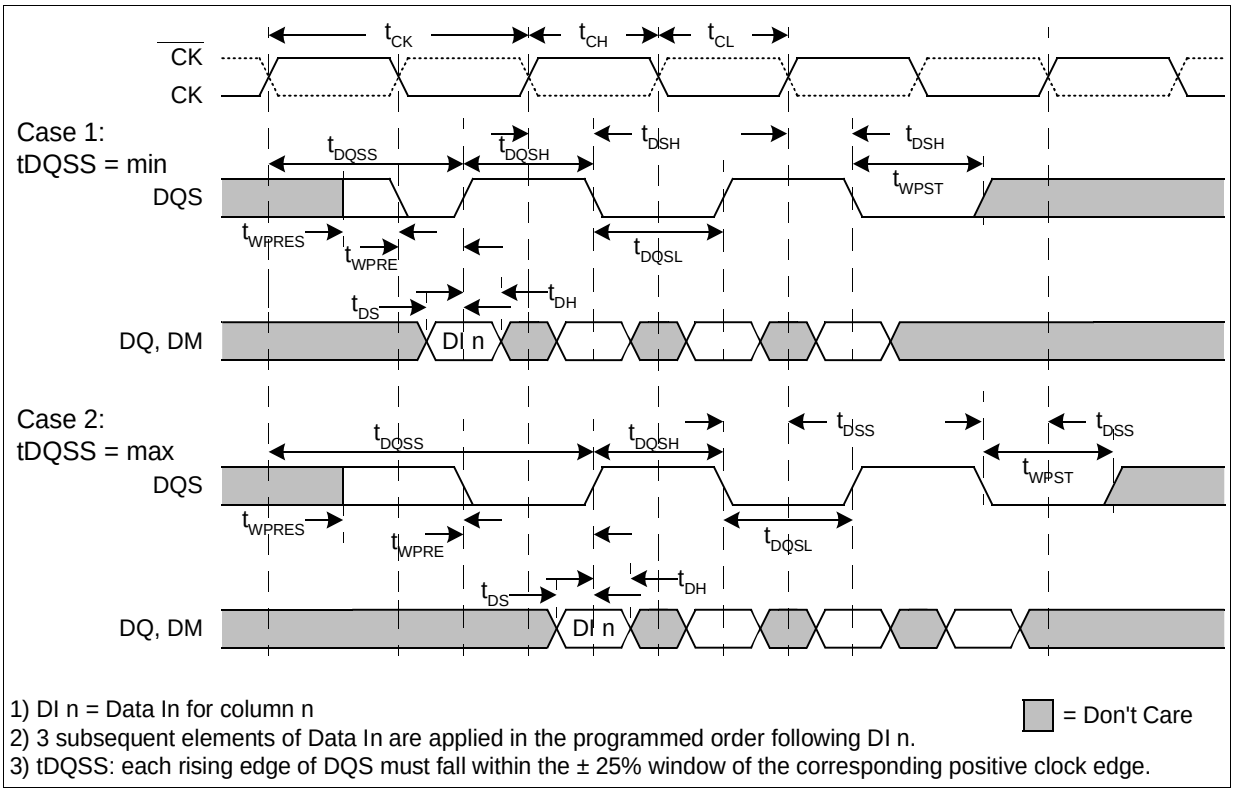


Figure 27 — Basic Write Timing Parameters

During Write bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and the subsequent data elements will be registered on successive edges of DQS. The Low state of DQS between the WRITE command and the first rising edge is called the write preamble, and the Low state on DQS following the last data-in element is called the write postamble.

The time between the WRITE command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range - from 75% to 125% of a clock cycle. Figure 28 shows the two extremes of t_{DQSS} for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain high-Z and any additional input data will be ignored.

5 Operation (cont'd)
5.6 Write (cont'd)

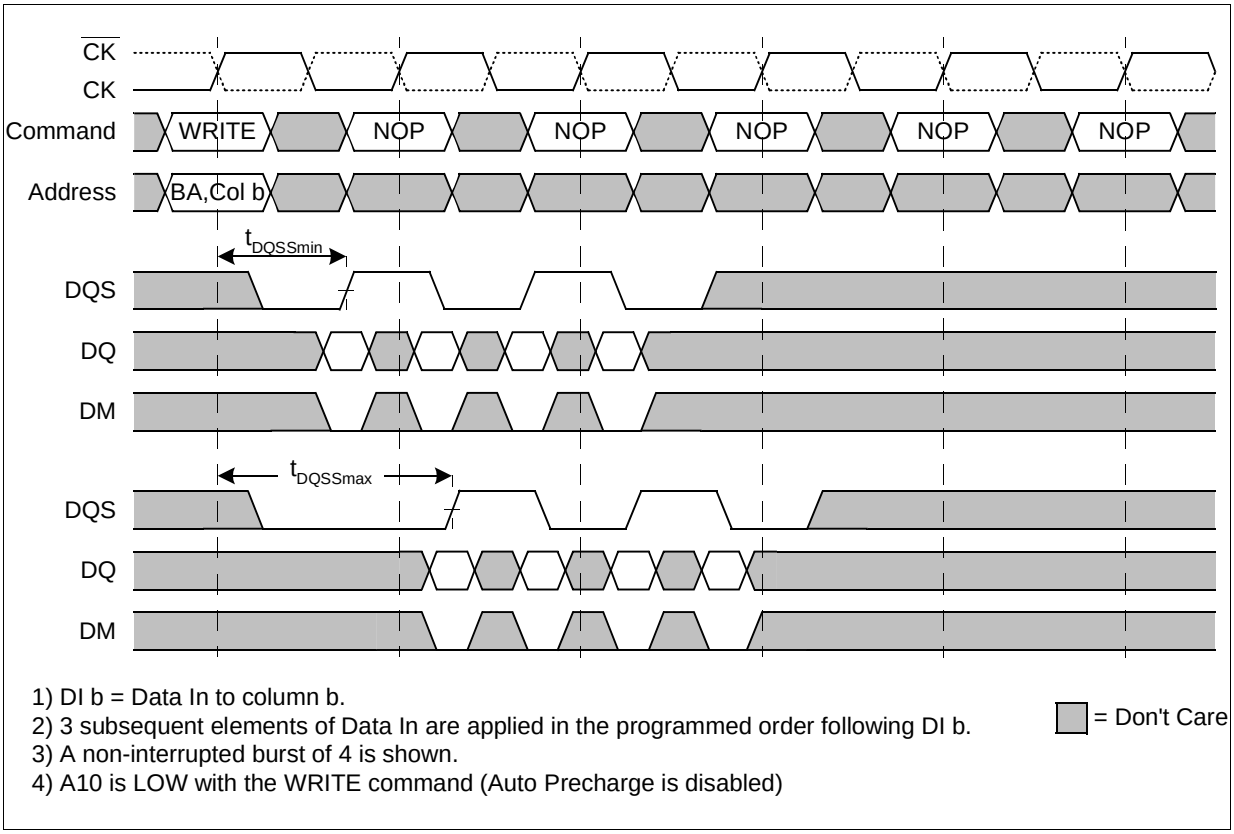


Figure 28 — Write Burst (min. and max. tDQSS)

5.6.1 Write to Write

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data, can be maintained. The new WRITE command can be issued on any positive edge of the clock following the previous WRITE command.

The first data-in element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data-in element pairs.

Figure 29 shows concatenated write burst of 4. An example of non-consecutive write bursts is shown in Figure 30.

Full-speed random write accesses within a page or pages can be performed as shown in Figure 31.

5.6.2 Write to Read

Data for any Write burst may be followed by a subsequent READ command. To follow a Write without truncating the write burst, t_{WTR} should be met as shown in Figure 32.

Data for any Write burst may be truncated by a subsequent READ command as shown in Figure 33. Note that the only data-in pairs that are registered prior to the t_{WTR} period are written to the internal array, and any subsequent data-in must be masked with DM.

5.6.3 Write to Precharge:

Data for any WRITE burst may be followed by a subsequent PRECHARGE command to the same bank (provided Auto Precharge was not activated). To follow a WRITE without truncating the WRITE burst, t_{WR} should be met as shown in Figure 34. Data for any WRITE burst may be truncated by a subsequent PRECHARGE command as shown in Figure 35. Note that only data-in pairs that are registered prior to the t_{WR} period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 35. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

5 Operation (cont'd)
5.6 Write (cont'd)

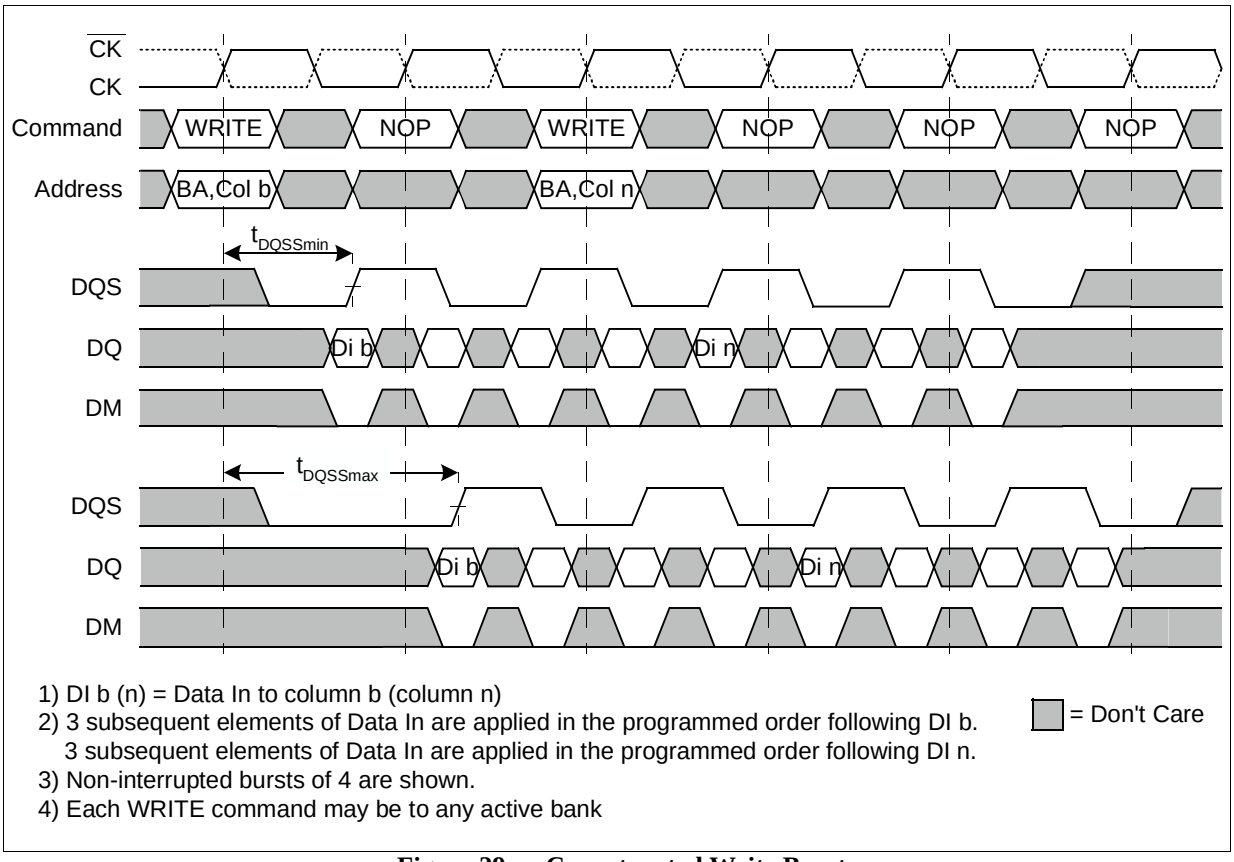


Figure 29 — Concatenated Write Bursts

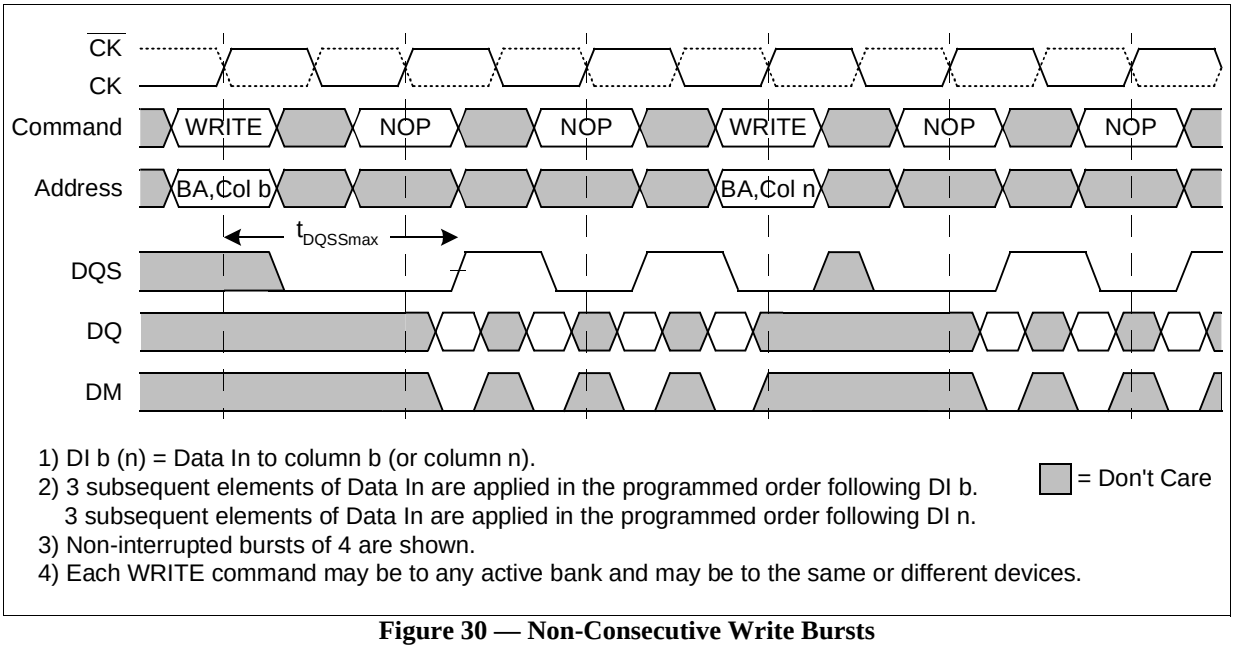
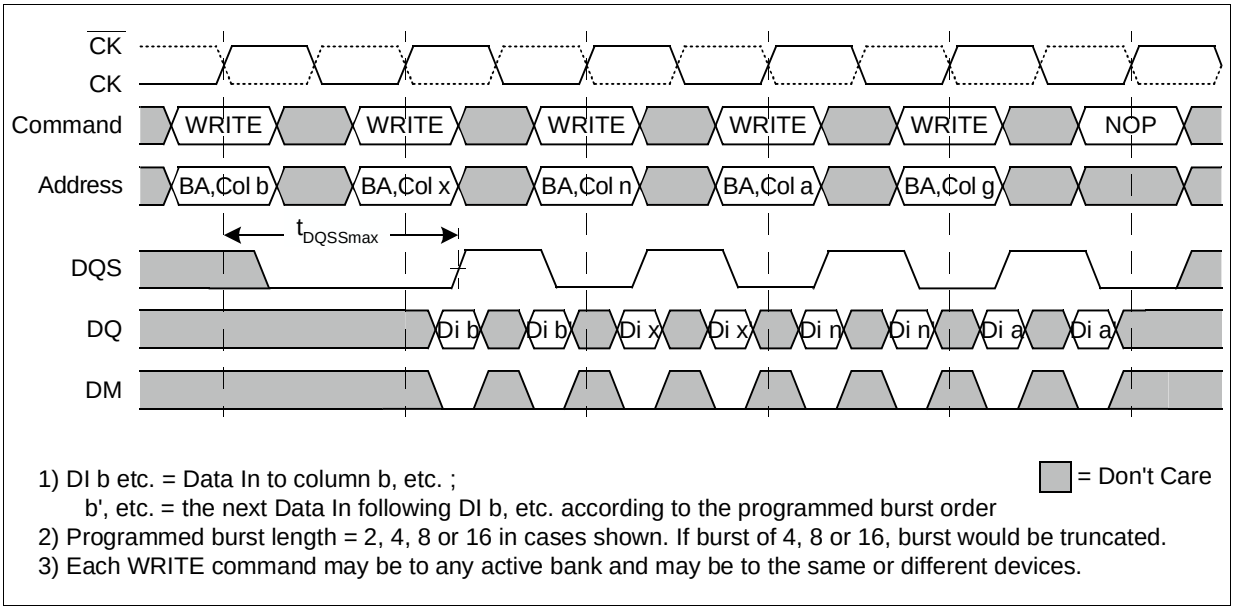


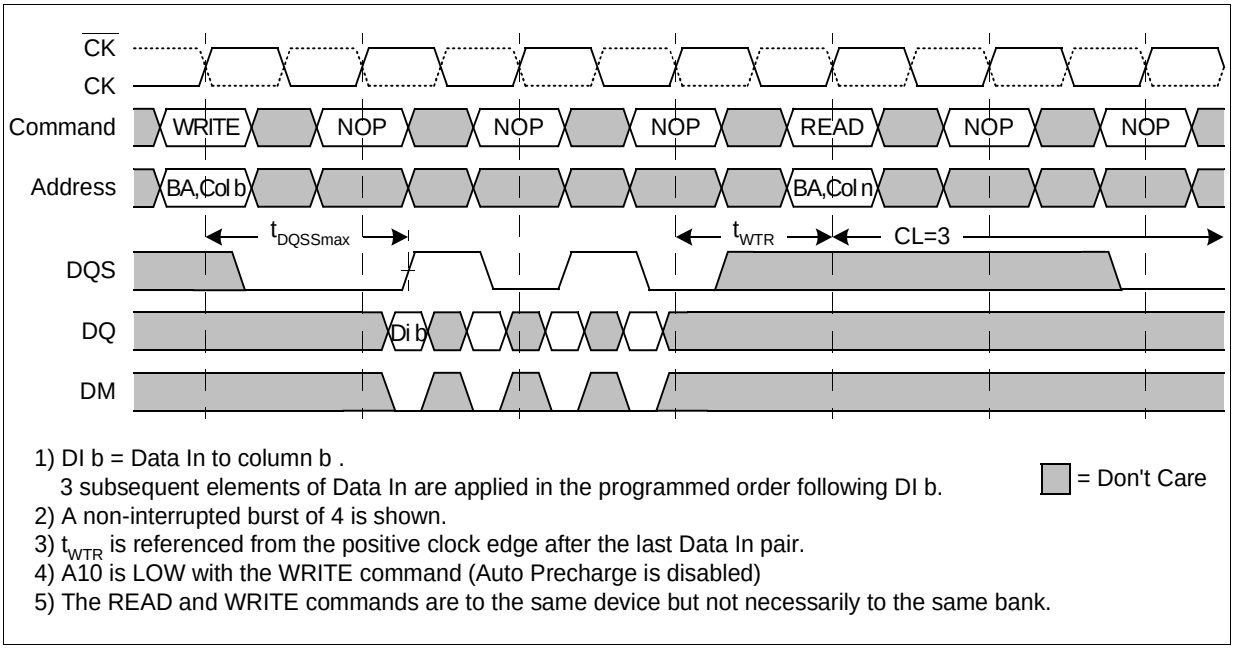
Figure 30 — Non-Consecutive Write Bursts

5 Operation (cont'd)
5.6 Write (cont'd)



1) DI b etc. = Data In to column b, etc. ;
b', etc. = the next Data In following DI b, etc. according to the programmed burst order
2) Programmed burst length = 2, 4, 8 or 16 in cases shown. If burst of 4, 8 or 16, burst would be truncated.
3) Each WRITE command may be to any active bank and may be to the same or different devices.

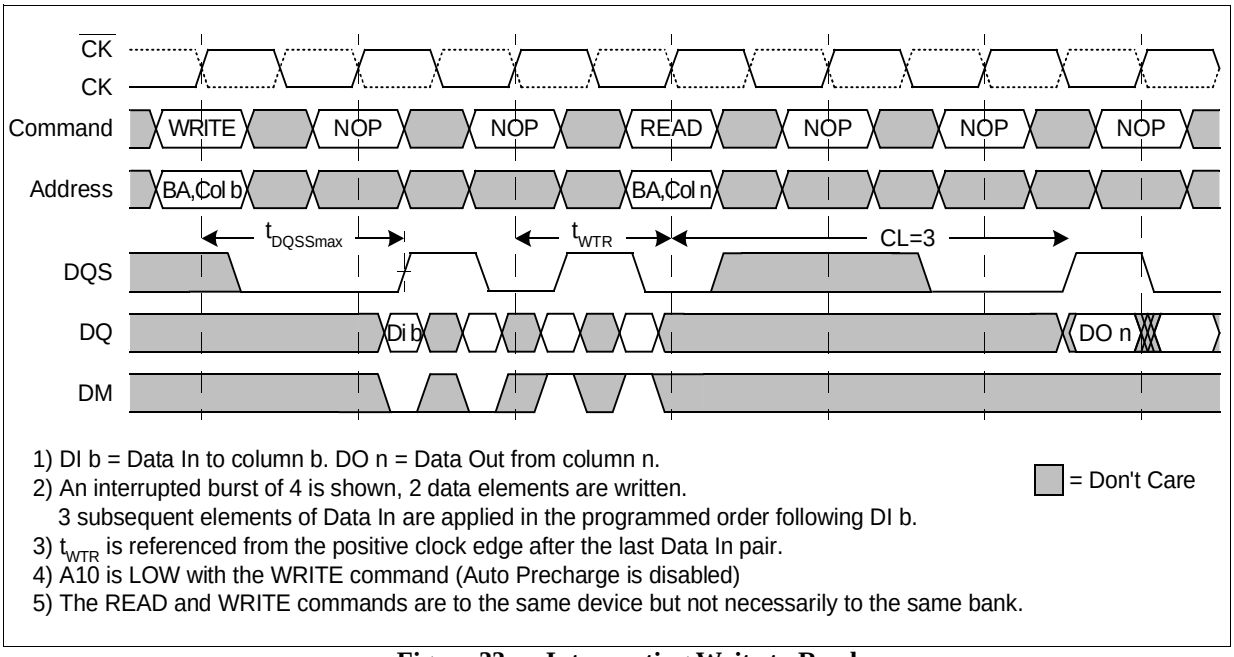
Figure 31 — Random Write Cycles



1) DI b = Data In to column b .
3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted burst of 4 is shown.
3) t_{WTR} is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

Figure 32 — Non-Interrupting Write to Read

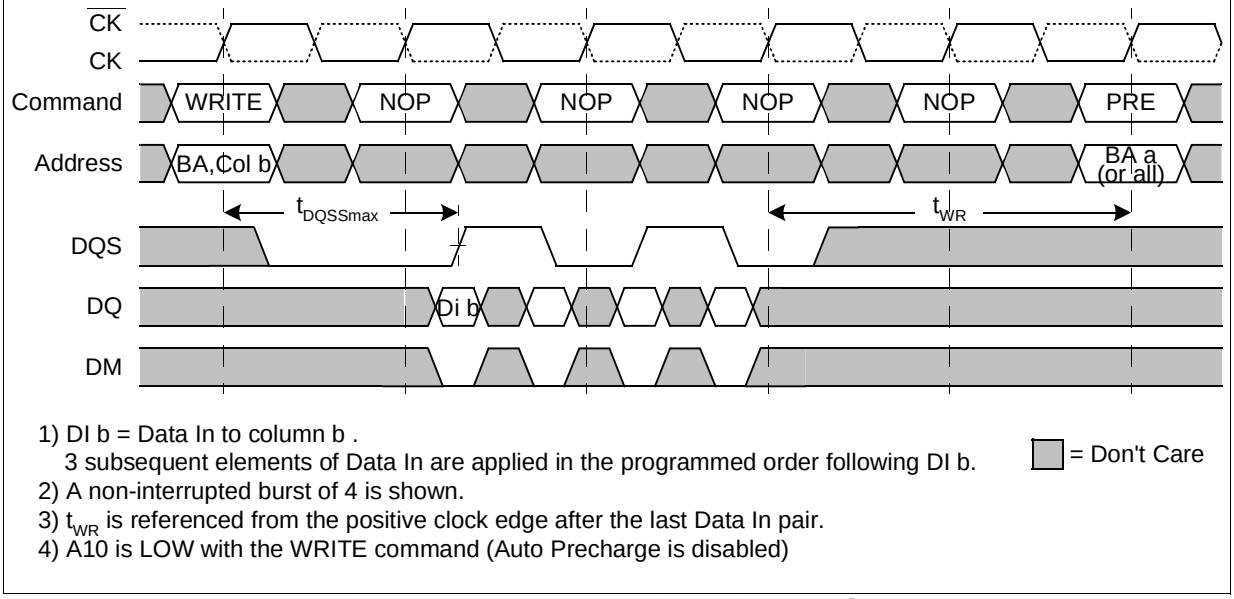
5 Operation (cont'd)
5.6 Write (cont'd)



1) DI b = Data In to column b. DO n = Data Out from column n.
2) An interrupted burst of 4 is shown, 2 data elements are written.
   3 subsequent elements of Data In are applied in the programmed order following DI b.
3) t_{WTR} is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

= Don't Care

Figure 33 — Interrupting Write to Read



1) DI b = Data In to column b .
   3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted burst of 4 is shown.
3) t_{WR} is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)

= Don't Care

Figure 34 — Non-Interrupting Write to Precharge

5 Operation (cont'd)
5.6 Write (cont'd)

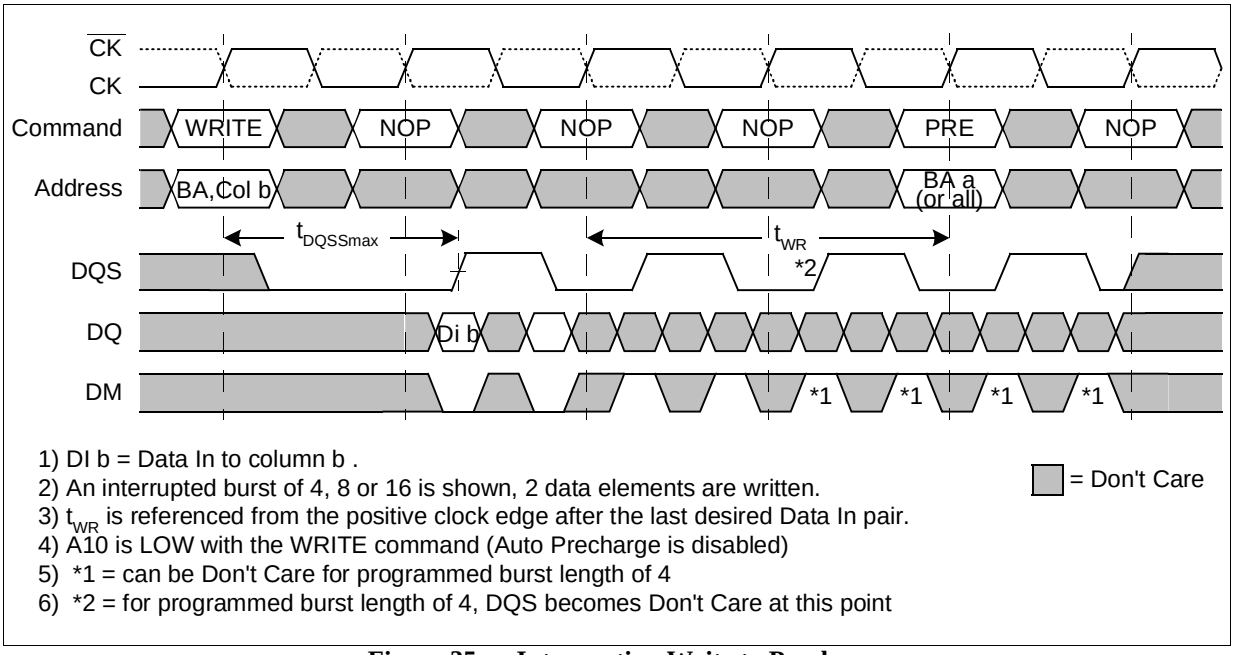


Figure 35 — Interrupting Write to Precharge

5.7 Precharge

The PRECHARGE command (see Figure 36) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued.

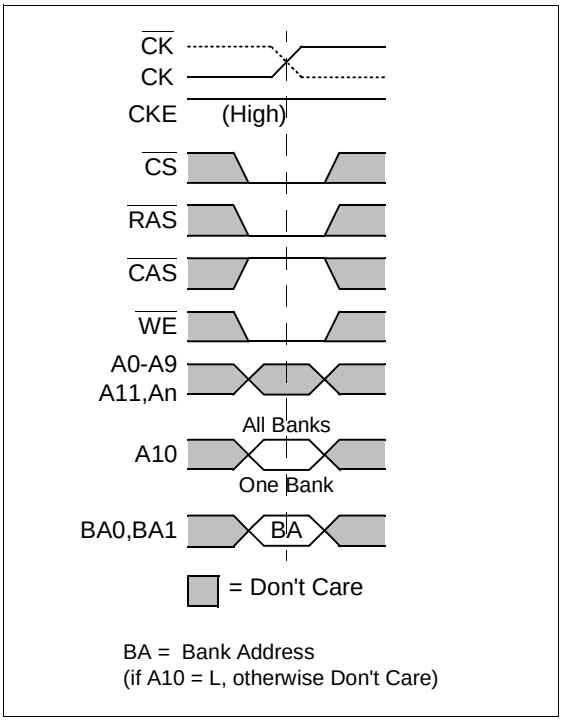


Figure 36 — Precharge command

Input A10 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care".

5 Operation (cont'd)
5.7 Precharge (cont'd)

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

5.8 Auto Precharge

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command. This is accomplished by using A10 (A10 = High), to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank / row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto Precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto Precharge ensures that a precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharging time (t_{RP}) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this specification.

5.9 Refresh Requirements

LPDDR SDRAM devices require a refresh of all rows in any rolling 64ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode. Dividing the number of device rows into the rolling 64ms interval defines the average refresh interval (t_{REFI}), which is a guideline to controllers for distributed refresh timing.

5.10 Auto Refresh

AUTO REFRESH command (see Figure 37) is used during normal operation of the LPDDR SDRAM. This command is non persistent, so it must be issued each time a refresh is required.

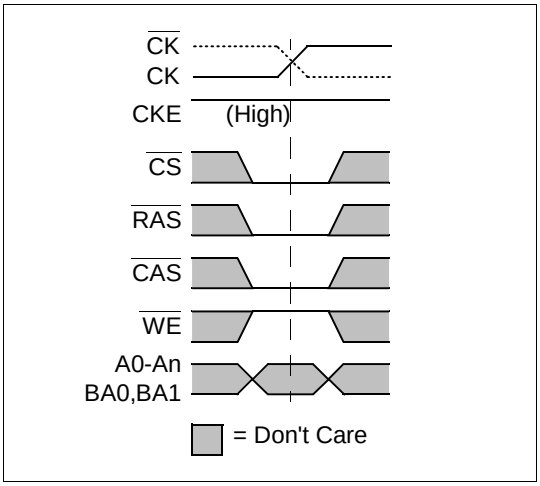


Figure 37 — Auto Refresh Command

The refresh addressing is generated by the internal refresh controller. The LPDDR SDRAM requires AUTO REFRESH commands at an average periodic interval of $t_{REFI.}$ The values of t_{REFI} for different densities and bus widths are listed in Table 2. Figure 39 shows an Auto Refresh cycle.

5.11 Self Refresh

The SELF REFRESH command (see Figure 38) can be used to retain data in the LPDDR SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the LPDDR SDRAM retains data without external clocking. The LPDDR SDRAM device has a built-in timer to accommodate Self Refresh operation. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is LOW. Input signals except CKE are "Don't Care" during Self Refresh. The user may halt the external clock one clock after the SELF REFRESH command is registered.

5 Operation (cont'd)
5.11 Self Refresh (cont'd)

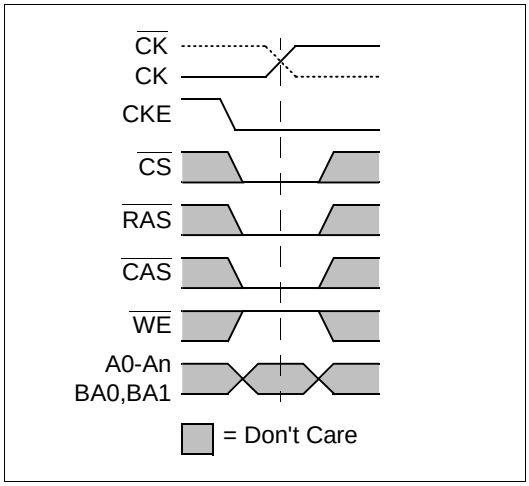


Figure 38 — Self Refresh command

Once the command is registered, CKE must be held low to keep the device in Self Refresh mode. The clock is internally disabled during Self Refresh operation to save power. The minimum time that the device must remain in Self Refresh mode is t_{RFC}.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back High. Once Self Refresh Exit is registered, a delay of at least t_{XS} must be satisfied before a valid command can be issued to the device to allow for completion of any internal refresh in progress.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh an extra AUTO REFRESH command is recommended.

Figure 40 shows Self Refresh entry and exit.

In the Self Refresh mode, two additional power-saving options exist: Temperature Compensated Self Refresh (TCSR) and Partial Array Self Refresh (PASR); they are described in the Extended Mode Register section (Figure 7).

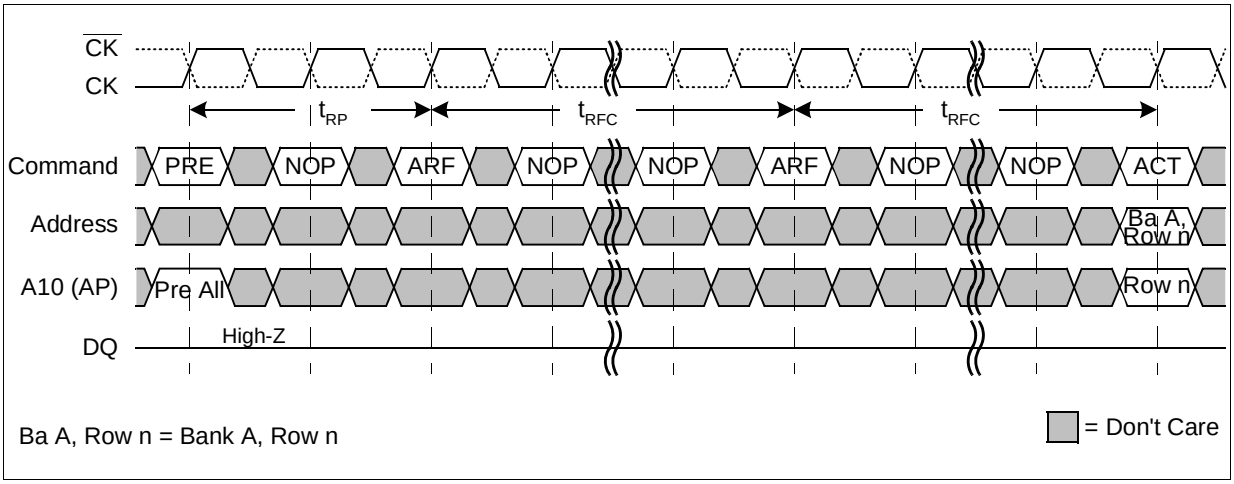


Figure 39 — Auto Refresh Cycles Back-to-Back

5 Operation (cont'd)
5.11 Self Refresh (cont'd)

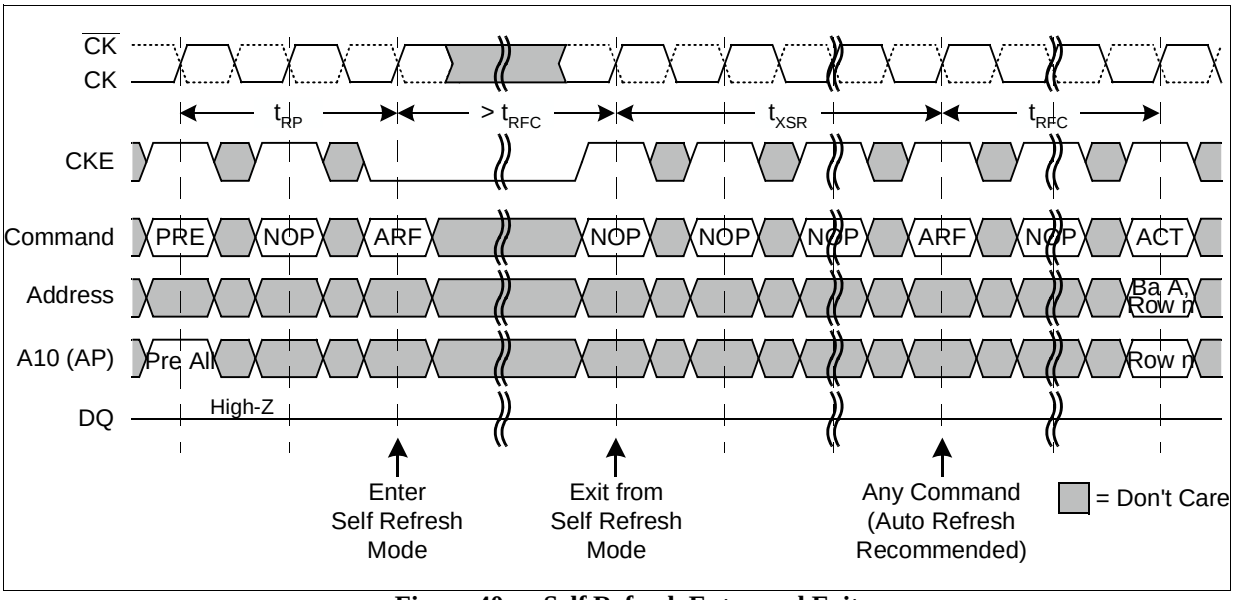


Figure 40 — Self Refresh Entry and Exit

5.12 Power-Down

Power-down is entered when CKE is registered Low (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. In power-down mode, CKE Low must be maintained, and all other input signals are "Don't Care". The minimum power-down duration is specified by t_{CKE}. However, power-down duration is limited by the refresh requirements of the device.

The power-down state is synchronously exited when CKE is registered High (along with a NOP or DESELECT command). A valid command may be applied t_{XP} after exit from power-down.

Figure 41 shows Power-down entry and exit.

For Clock Stop during Power-Down mode, please refer to the Clock Stop subsection in this specification.

5 Operation (cont'd)
5.12 Power-Down (cont'd)

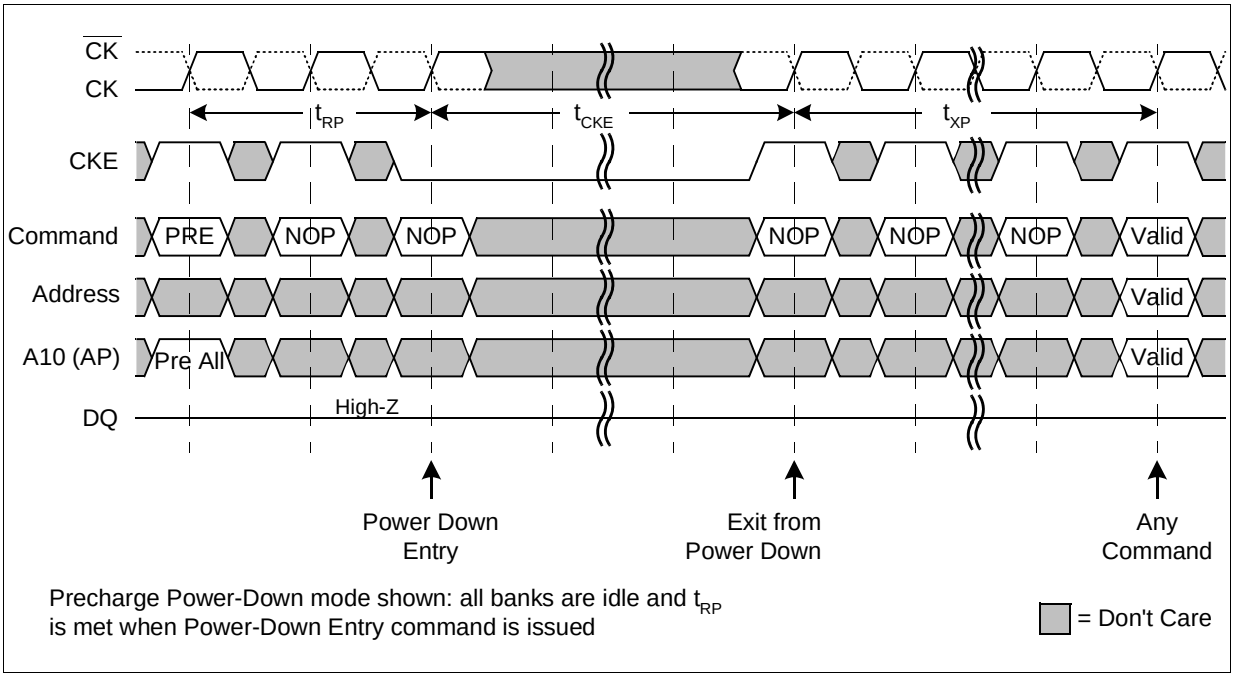


Figure 41 — Power-Down Entry and Exit

5.13 Deep Power-Down

The Deep Power-Down (DPD) mode enables very low standby currents. All internal voltage generators inside the LPDDR SDRAM are stopped and all memory data is lost in this mode. All the information in the Mode Register and the Extended Mode Register is lost.

Deep Power-Down is entered using the BURST TERMINATE command (see Figure 25) except that CKE is registered Low. All banks must be in idle state with no activity on the data bus prior to entering the DPD mode. While in this state, CKE must be held in a constant Low state.

To exit the DPD mode, CKE is taken high after the clock is stable and NOP commands must be maintained for at least 200 µs. After 200 µs a complete re-initialization is required following steps 4 through 11 as defined for the initialization sequence (see Figure 4).

There is an optional test pad, Test Power Down (TPD) for entering deep power down mode. Taking TPD HIGH asynchronously will place the die in deep power down mode. The assertion of TPD HIGH must meet all the initialization and sequencing of DPD mode.

Deep Power-Down entry and exit is shown in Figure 42.

5 Operation (cont'd)
5.13 Deep Power-Down (cont'd)

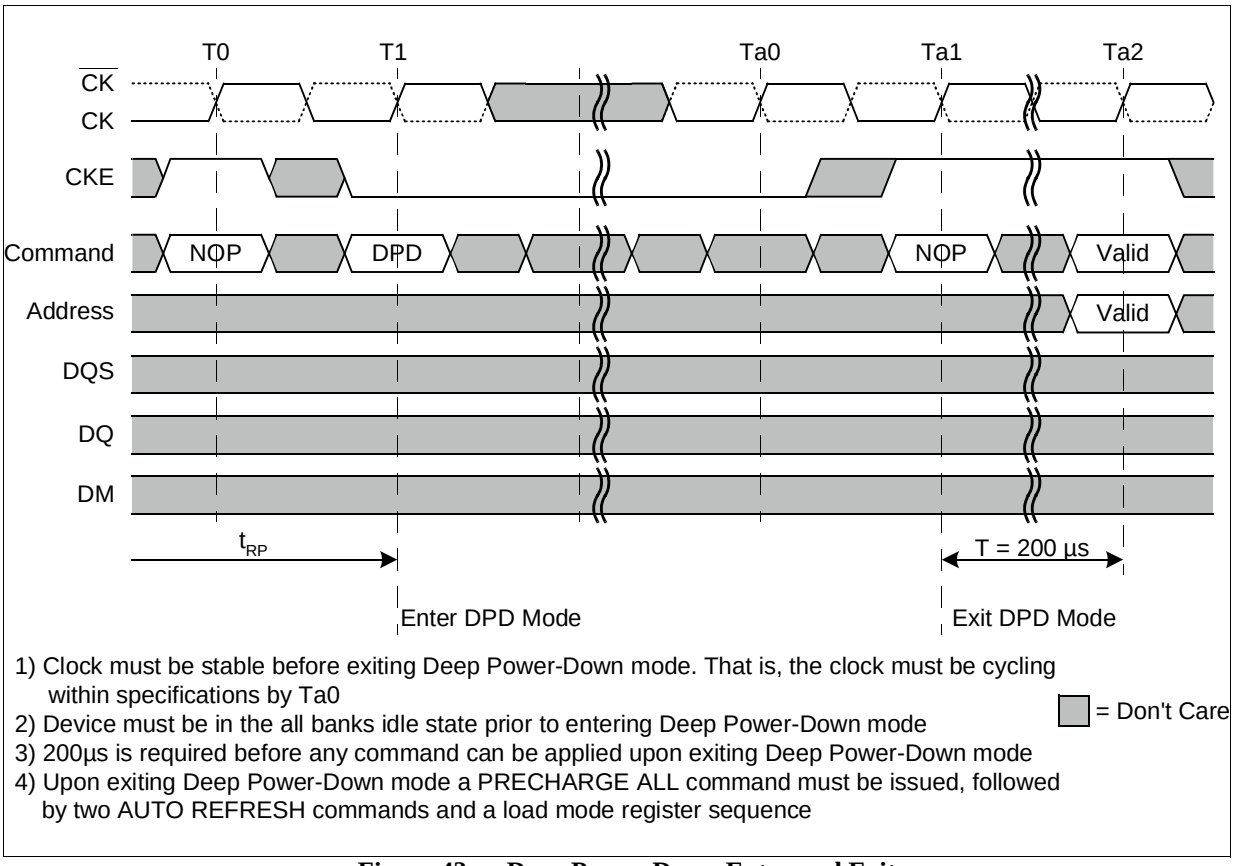


Figure 42 — Deep Power-Down Entry and Exit

5.14 Clock Stop

Stopping a clock during idle periods is an effective method of reducing power consumption.

The LPDDR SDRAM supports clock stop under the following conditions:

- the last command (ACTIVE, READ, WRITE, PRECHARGE, AUTO REFRESH or MODE REGISTER SET) has executed to completion, including any data-out during read bursts; the number of clock pulses per access command depends on the device's AC timing parameters and the clock frequency;
- the related timing conditions (t_{RCD}, t_{WR}, t_{RP}, t_{RFC}, t_{MRD}) has been met;
- CKE is held High

When all conditions have been met, the device is either in "idle state" or "row active state" and clock stop mode may be entered with CK held Low and $\overline{CK}$ held High.

Clock stop mode is exited by restarting the clock. At least one NOP command has to be issued before the next access command may be applied. Additional clock pulses might be required depending on the system characteristics.

Figure 43 shows clock stop mode entry and exit.

- Initially the device is in clock stop mode
- The clock is restarted with the rising edge of T0 and a NOP on the command inputs
- With T1 a valid access command is latched; this command is followed by NOP commands in order to allow for clock stop as soon as this access command is completed
- Tn is the last clock pulse required by the access command latched with T1
- The clock can be stopped after Tn

5 Operation (cont'd)
5.14 Clock Stop (cont'd)

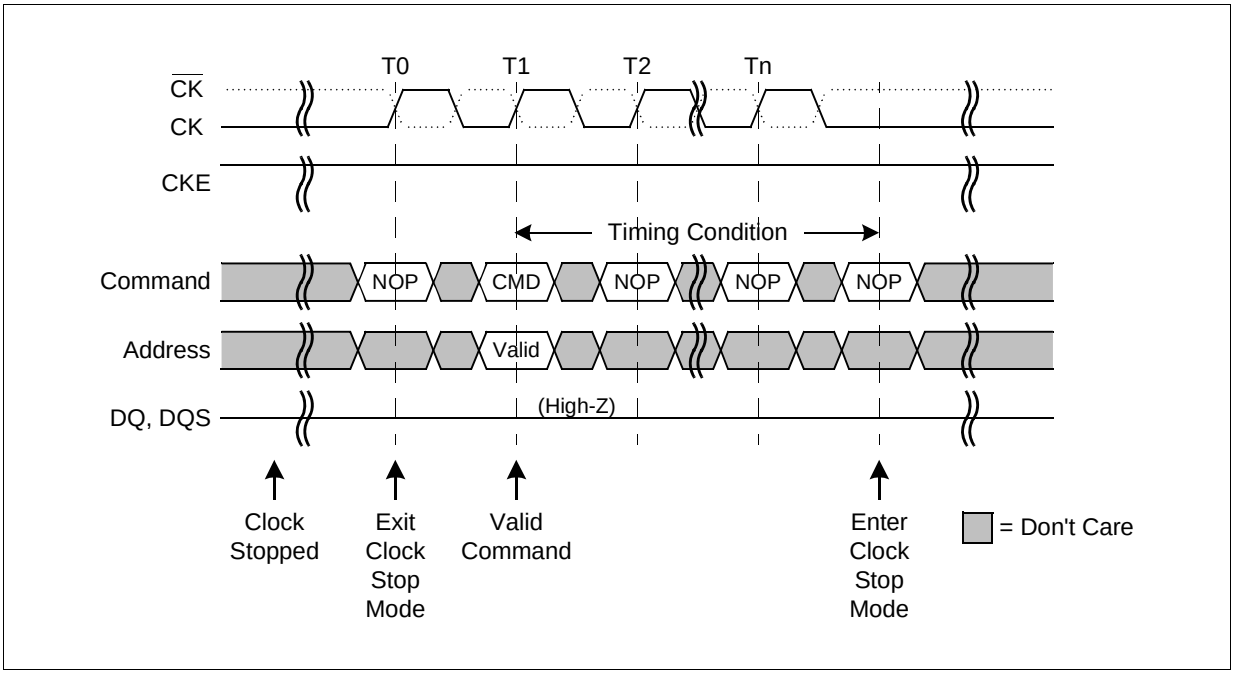


Figure 43 — Clock Stop Mode Entry and Exit

6 Absolute Maximum Ratings

(not specified herein)

7 AC & DC Operating Conditions

Table 10 — Operating Conditions

PARAMETER	SYMBOL	VALUES		UNIT
		MIN	MAX	
Operating Case Temperature	T_C	-25	+85	^oC

Table 11 — Input/Output Capacitance
[Notes 1-3]

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Input capacitance, CK, $\overline{CK}$	CCK	1.5	3.0	pF	
Input capacitance delta, CK, $\overline{CK}$	CDCK		0.25	pF	
Input capacitance, all other input-only pins	CI	1.5	3.0	pF	
Input capacitance delta, all other input-only pins	CDI		0.5	pF	
Input/output capacitance, DQ, DM, DQS	CIO	3.0	5.0	pF	4
Input/output capacitance delta, DQ, DM, DQS	CDIO		0.5	pF	4

NOTES:

1. These values are guaranteed by design and are tested on a sample base only.
2. These capacitance values are for single monolithic devices only. Multiple die packages will have parallel capacitive loads.
3. Input capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. VDD, VDDQ are applied and all other pins (except the pin under test) floating. DQs should be in high impedance state. This may be achieved by pulling CKE to low level.
4. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS and DM in the system.

7 AC & DC Operating Conditions (cont'd)

Table 12 — Electrical Characteristics and AC/DC Operating Conditions
[Notes 1-3]

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNIT	NOTES
Supply Voltage	VDD	1.7	1.9	V	-
I/O Supply Voltage	VDDQ	1.7	1.9	V	-
Address and Command Inputs (A0 - An, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)					
Input High Voltage	VIH	0.8 * VDDQ	VDDQ +0.3	V	-
Input Low Voltage	VIL	-0.3	0.2 * VDDQ	V	-
Clock Inputs (CK, $\overline{CK}$)					
DC Input Voltage	VIN	-0.3	VDDQ +0.3	V	-
DC Input Differential Voltage	VID(DC)	0.4 * VDDQ	VDDQ +0.6	V	2
AC Input Differential Voltage	VID(AC)	0.6 * VDDQ	VDDQ +0.6	V	2
AC Differential Crosspoint Voltage	VIX	0.4 * VDDQ	0.6 * VDDQ	V	3
Data Inputs (DQ, DM, DQS)					
DC Input High Voltage	VIHD(DC)	0.7 * VDDQ	VDDQ +0.3	V	-
DC Input Low Voltage	VILD(DC)	-0.3	0.3 * VDDQ	V	-
AC Input High Voltage	VIHD(AC)	0.8 * VDDQ	VDDQ +0.3	V	-
AC Input Low Voltage	VILD(AC)	-0.3	0.2 * VDDQ	V	-
Data Outputs (DQ, DQS)					
DC Output High Voltage (IOH = -0.1mA)	VOH	0.9 * VDDQ	-	V	-
DC Output Low Voltage (IOL = 0.1mA)	VOL	-	0.1 * VDDQ	V	-

NOTES:

1. All voltages referenced to VSS and VSSQ must be same potential.
2. VID(DC) and VID(AC) are the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
3. The value of VIX is expected to be 0.5 * VDDQ and must track variations in the DC level of the same.

7 AC & DC Operating Conditions (cont'd)

Table 13 — IDD Specification Parameters and Test Conditions
[Recommended Operating Conditions; Notes 1-3]

PARAMETER/CONDITION	SYMBOL
Operating one bank active-precharge current: $t_{RC} = t_{RCmin}$; $t_{CK} = t_{CKmin}$; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE	I_{DD0}
Precharge power-down standby current: all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2P}
Precharge power-down standby current with clock stop: all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2PS}
Precharge non power-down standby current: all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2N}
Precharge non power-down standby current with clock stop: all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2NS}
Active power-down standby current: one bank active, CKE is LOW; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3P}
Active power-down standby current with clock stop: one bank active, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3PS}
Active non power-down standby current: one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3N}
Active non power-down standby current with clock stop: one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3NS}
Operating burst read current: one bank active; BL = 4; CL = 3; $t_{CK} = t_{CKmin}$; continuous read bursts; I_{OUT} = 0 mA address inputs are SWITCHING; 50% data change each burst transfer	I_{DD4R}
Operating burst write current: one bank active; BL = 4; $t_{CK} = t_{CKmin}$; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer	I_{DD4W}
Auto-Refresh current: $t_{RC} = t_{RFCmin}$; $t_{CK} = t_{CKmin}$; burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD5}
Self refresh current CKE is LOW, CK = LOW, $\overline{CK}$ = HIGH; Extended Mode Register set to all 0's; address and control inputs are STABLE; data bus inputs are STABLE	I_{DD6}
Deep Power-Down current Address and control inputs are STABLE; data bus inputs are STABLE	I_{DD8}

7 AC & DC Operating Conditions (cont'd)

NOTES:

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is 1V/ns.
3. Definitions for IDD:
   LOW is defined as $V_{IN} \leq 0.1 * V_{DDQ}$;
   HIGH is defined as $V_{IN} \geq 0.9 * V_{DDQ}$;
   STABLE is defined as inputs stable at a HIGH or LOW level;
   SWITCHING is defined as:
   - Address and command: inputs changing between HIGH and LOW once per two clock cycles;
   - Data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.

7 AC & DC Operating Conditions (cont'd)

Table 14 — AC Timings
[Recommended Operating Conditions; Notes 1-9]

PARAMETER		SYMBOL	LPDDR266		LPDDR200		UNIT	NOTES
			MIN	MAX	MIN	MAX		
DQ output access time from CK/$\overline{CK}$		tAC	2.0	6.5	2.0	7.0	ns	
DQS output access time from CK/$\overline{CK}$		tDQSCK	2.0	6.5	2.0	7.0	ns	
Clock high-level width		tCH	0.45	0.55	0.45	0.55	tCK	
Clock low-level width		tCL	0.45	0.55	0.45	0.55	tCK	
Clock half period		tHP	min (tCL, tCH)		min (tCL, tCH)		ns	10, 11
Clock cycle time	CL = 3	tCK	7.5		10		ns	12
	CL = 2 (optional)		12		15		ns	
DQ and DM input setup time	fast slew rate	tDS	0.8		1.1		ns	13,14,15
	slow slew rate		0.9		1.2		ns	13,14,16
DQ and DM input hold time	fast slew rate	tDH	0.8		1.1		ns	13,14,15
	slow slew rate		0.9		1.2		ns	13,14,16
DQ and DM input pulse width		tDIPW	1.8		2.4		ns	17
Address and control input setup time	fast slew rate	tIS	1.3		1.5		ns	15,18
	slow slew rate		1.5		1.7		ns	16,18
Address and control input hold time	fast slew rate	tIH	1.3		1.5		ns	15,18
	slow slew rate		1.5		1.7		ns	16,18
Address and control input pulse width		tIPW	3.0		3.4		ns	17
$\overline{DQ}$ & DQS low-impedance time from CK/$\overline{CK}$		tLZ	1.0		1.0		ns	19
DQ & $\overline{DQS}$ high-impedance time from CK/$\overline{CK}$		tHZ		6.5		7.0	ns	19
DQS - DQ skew		tDQSQ		0.6		0.7	ns	20
DQ / DQS output hold time from DQS		tQH	tHP-tQHS		tHP-tQHS		ns	11
Data hold skew factor		tQHS		0.75		1.0	ns	11
Write command to 1st DQS latching transition		tDQSS	0.75	1.25	0.75	1.25	tCK	
DQS input high-level width		tDQSH	0.4		0.4		tCK	
DQS input low-level width		tDQSL	0.4		0.4		tCK	
DQS falling edge to CK setup time		tDSS	0.2		0.2		tCK	
DQS falling edge hold time from CK		tDSH	0.2		0.2		tCK	
MODE REGISTER SET command period		tMRD	2		2		tCK	
Write preamble setup time		tWPRES	0		0		ns	21
Write postamble		tWPST	0.4	0.6	0.4	0.6	tCK	22
Write preamble		tWPRE	0.25		0.25		tCK	
Read preamble	CL = 2 (optional)	tRPRE	0.5	1.1	0.5	1.1	tCK	23
	CL = 3		0.9	1.1	0.9	1.1	tCK	
Read postamble		tRPST	0.4	0.6	0.4	0.6	tCK	

7 AC & DC Operating Conditions (cont'd)

Table 14 — AC Timings
[Recommended Operating Conditions; Notes 1-9]

PARAMETER		SYMBOL	LPDDR266		LPDDR200		UNIT	NOTES
			MIN	MAX	MIN	MAX		
ACTIVE to PRECHARGE command period		tRAS	45	70,000	50	70,000	ns	
ACTIVE to ACTIVE command period		tRC	75		80		ns	
AUTO REFRESH to ACTIVE / AUTO REFRESH command period	128 Mb, 256 Mb	tRFC	80		80		ns	
	512 Mb		110		110		ns	
	1 Gb		140		140		ns	
ACTIVE to READ or WRITE delay		tRCD	22.5		30		ns	24
			30				ns	25
PRECHARGE command period		tRP	22.5		30		ns	24
			30				ns	25
ACTIVE bank A to ACTIVE bank B delay		tRRD	15		15		ns	
WRITE recovery time		tWR	15		15		ns	
Auto precharge write recovery + precharge time		tDAL	–		–		tCK	26
Internal write to Read command delay		tWTR	1		1		tCK	
Self refresh exit to next valid command delay		tXSR	200		200		ns	27
Exit power down to next valid command delay		tXP	25		25		ns	28
CKE min. pulse width (high and low pulse width)		tCKE	2		2		tCK	
Refresh Period		tREF		64		64	ms	
Average periodic refresh interval		tREFI					µs	29, 30
MRS for SRR to READ		tSRR	2		2		tCK	
READ of SRR to next valid command		tSRC	CL +1		CL +1		tCK	
Internal temperature sensor to valid temperature output enable		tTQ	2		2		ms	

Table 15 — AC Timings
[Recommended Operating Conditions; Notes 1-9]

PARAMETER	SYMBOL	LPDDR333		LPDDR370		LPDDR400		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
DQ output access time from CK/$\overline{CK}$	tAC	2.0	5.5	2.0	5.0	2.0	5.0	ns	
DQS output access time from CK/$\overline{CK}$	tDQSCK	2.0	5.5	2.0	5.0	2.0	5.0	ns	
Clock high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock half period	tHP	min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		ns	10, 11

7 AC & DC Operating Conditions (cont'd)

Table 15 — AC Timings
[Recommended Operating Conditions; Notes 1-9]

PARAMETER		SYMBOL	LPDDR333		LPDDR370		LPDDR400		UNIT	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
Clock cycle time	CL = 4 (optional)	tCK	-	100	5.4	100	5.0	100	ns	12
	CL = 3		6.0		5.4		5.0			
	CL = 2 (optional)		12		12		12			
DQ and DM input setup time	fast slew rate	tDS	0.6		0.54		0.48		ns	13,14,15
	slow slew rate		0.7		0.64		0.58		ns	13,14,16
DQ and DM input hold time	fast slew rate	tDH	0.6		0.54		0.48		ns	13,14,15
	slow slew rate		0.7		0.64		0.58		ns	13,14,16
DQ and DM input pulse width		tDIPW	2.1		1.9		1.8		ns	17
Address and control input setup time	fast slew rate	tIS	1.1		1.0		0.9		ns	15,18
	slow slew rate		1.3		1.2		1.1		ns	16,18
Address and control input hold time	fast slew rate	tIH	1.1		1.0		0.9		ns	15,18
	slow slew rate		1.3		1.2		1.1		ns	16,18
Address and control input pulse width		tIPW	2.7		2.5		2.3		ns	17
DQ & DQS low-impedance time from CK/CK		tLZ	1.0		1.0		1.0		ns	19
DQ & DQS high-impedance time from CK/CK		tHZ		5.5		5.0		5.0	ns	19
DQS - DQ skew		tDQSQ		0.5		0.45		0.4	ns	20
DQ / DQS output hold time from DQS		tQH	tHP-tQHS		tHP-tQHS		tHP-tQHS		ns	11
Data hold skew factor		tQHS		0.65		0.5		0.5	ns	11
Write command to 1st DQS latching transition		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS input high-level width		tDQSH	0.4		0.4		0.4		tCK	
DQS input low-level width		tDQSL	0.4		0.4		0.4		tCK	
DQS falling edge to CK setup time		tDSS	0.2		0.2		0.2		tCK	
DQS falling edge hold time from CK		tDSH	0.2		0.2		0.2		tCK	
MODE REGISTER SET command period		tMRD	2		2		2		tCK	
Write preamble setup time		tWPRES	0		0		0		ns	21
Write postamble		tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	22
Write preamble		tWPRE	0.25		0.25		0.25		tCK	

7 AC & DC Operating Conditions (cont'd)

Table 15 — AC Timings
[Recommended Operating Conditions; Notes 1-9]

PARAMETER		SYMBOL	LPDDR333		LPDDR370		LPDDR400		UNIT	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
Read preamble	CL = 2 (optional)	tRPRE	0.5	1.1	0.5	1.1	0.5	1.1	tCK	23
	CL = 3		0.9	1.1	0.9	1.1	0.9	1.1		
	CL = 4 (optional)		-	-	0.9	1.1	0.9	1.1		
Read postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
ACTIVE to PRECHARGE command period		tRAS	42	70,000	42	70,000	40	70,000	ns	
ACTIVE to ACTIVE command period		tRC	60		58.2		55		ns	
AUTO REFRESH to ACTIVE / AUTO REFRESH command period	64Mb 128 Mb, 256 Mb	tRFC	80		80		80		ns	
	512 Mb		110		110		110		ns	
	1 Gb & 2Gb		140		140		140		ns	
ACTIVE to READ or WRITE delay		tRCD	18		16.2		15		ns	24
			30		21.6		20		ns	25
PRECHARGE command period		tRP	18		16.2		15		ns	24
			30		21.6		20		ns	25
ACTIVE bank A to ACTIVE bank B delay		tRRD	12		10.8		10		ns	
WRITE recovery time		tWR	15		15		15		ns	
Auto precharge write recovery + precharge time		tDAL	–		–		–		tCK	26
Internal write to Read command delay		tWTR	2		2		2		tCK	
Self refresh exit to next valid command delay		tXSR	200		200		200		ns	27
Exit power down to next valid command delay		tXP	25		25		25		ns	28
CKE min. pulse width (high and low pulse width)		tCKE	2		2		2		tCK	
Refresh Period		tREF		64		64		64	ms	
Average periodic refresh interval		tREFI							µs	29, 30
MRS for SRR to READ		tSRR	2		2		2		tCK	
READ of SRR to next valid command		tSRC	CL +1		CL +1		CL +1		tCK	
Internal temperature sensor to valid temperature output enable		tTQ	2		2		2		ms	

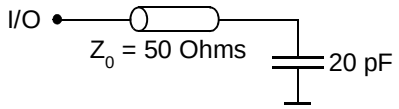
NOTES:

1. All voltages referenced to *VSS*.
2. All parameters assume proper device initialization.
3. Tests for AC timing may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage and temperature range specified.
4. The circuit shown below represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a

7 AC & DC Operating Conditions (cont'd)

production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half strength driver with a nominal 10 pF load parameters tAC and tQH are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design / characterization. Use of IBIS or other simulation tools for system design validation is suggested.

Timing Reference Load



5. The CK/$\overline{CK}$ input reference voltage level (for timing referenced to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference voltage level for signals other than CK/$\overline{CK}$ is *VDDQ*/2.
6. The timing reference voltage level is *VDDQ*/2.
7. AC and DC input and output voltage levels are defined in the section for Electrical Characteristics and AC/DC operating conditions.
8. A CK/$\overline{CK}$ differential slew rate of 2.0 V/ns is assumed for all parameters.
9. CAS latency definition: with CL = 3 the first data element is valid at (2 * tCK + tAC) after the clock at which the READ command was registered (see figure); with CL = 2 the first data element is valid at (tCK + tAC) after the clock at which the READ command was registered; with CL = 4 the first data element is valid at (3 * tCK + tAC) after the clock at which the READ command was registered.

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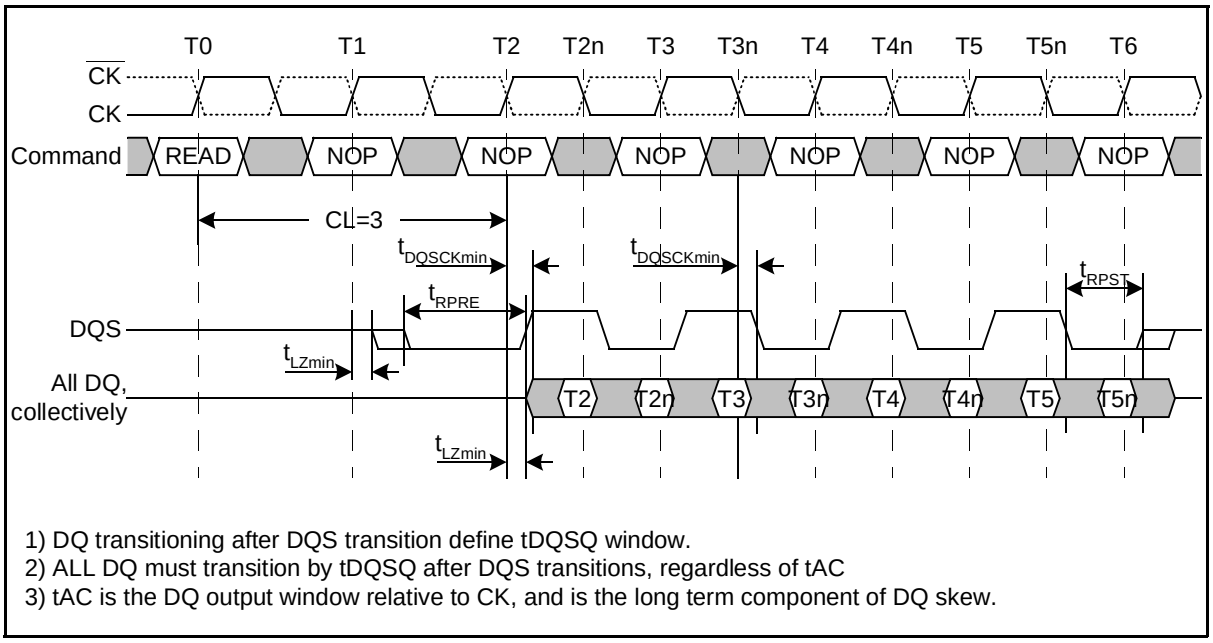

10. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH)
11. tQH = tHP - tQHS, where tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCL, tCH). tQHS accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
12. The only time that the clock frequency is allowed to change is during clock stop, power-down or self-refresh modes.
13. The transition time for DQ, DM and DQS inputs is measured between VIL(DC) to VIH(AC) for rising input signals, and VIH(DC) to VIL(AC) for falling input signals.
14. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
15. Input slew rate ≥ 1.0 V/ns.
16. Input slew rate ≥ 0.5 V/ns and < 1.0 V/ns.
17. These parameters guarantee device timing but they are not necessarily tested on each device.
18. The transition time for address and command inputs is measured between V_{IH} and V_{IL}.

7 AC & DC Operating Conditions (cont'd)

19. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving ($_{HZ}$), or begins driving ($_{LZ}$).
20. t_{DQSQ} consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
21. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before the corresponding CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
22. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
23. A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).
24. Speed bin (CL - tRCD - tRP) = 3 - 3 - 3
25. Speed bin (CL - tRCD - tRP) = 3 - 4 - 4 (all speed bins except LPDDR200)
26. tDAL = (tWR/tCK) + (tRP/tCK): for each of the terms, if not already an integer, round to the next higher integer.
27. There must be at least two clock pulses during the tXSR period.
28. There must be at least one clock pulse during the tXP period.
29. t_{REFI} values are dependant on density and bus width. Please refer to Table 2 on page 3.
30. A maximum of 8 Refresh commands can be posted to any given LPDDR, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is $8*t_{REFI}$.

7 AC & DC Operating Conditions (cont'd)

Table 16 — OUTPUT SLEW RATE CHARACTERISTICS

PARAMETER	MIN	MAX	UNIT	NOTES
Pull-up and Pull-Down Slew Rate for Full Strength Driver	0.7	2.5	V/ns	1,2
Pull-up and Pull-Down Slew Rate for Three-Quarters Strength Driver	0.5	1.75	V/ns	1,2
Pull-up and Pull-Down Slew Rate for Half Strength Driver	0.3	1.0	V/ns	1,2
Output Slew rate Matching ratio (Pull-up to Pull-down)	0.7	1.4	—	3

1. Measured with a test load of 20 pF connected to V_{SSQ}.
2. Output slew rate for rising edge is measured between VILD(DC) to VIHD(AC) and for falling edge between VIHD(DC) to VILD(AC).
3. The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

Table 17 — AC Overshoot/Undershoot Specification

PARAMETER	SPECIFICATION
Maximum peak amplitude allowed for overshoot	0.5 V
Maximum peak amplitude allowed for undershoot	0.5 V
The area between overshoot signal and VDD must be less than or equal to	3 V-ns
The area between undershoot signal and GND must be less than or equal to	3 V-ns

NOTES:

1. This specification is intended for devices with no clamp protection and is guaranteed by design.

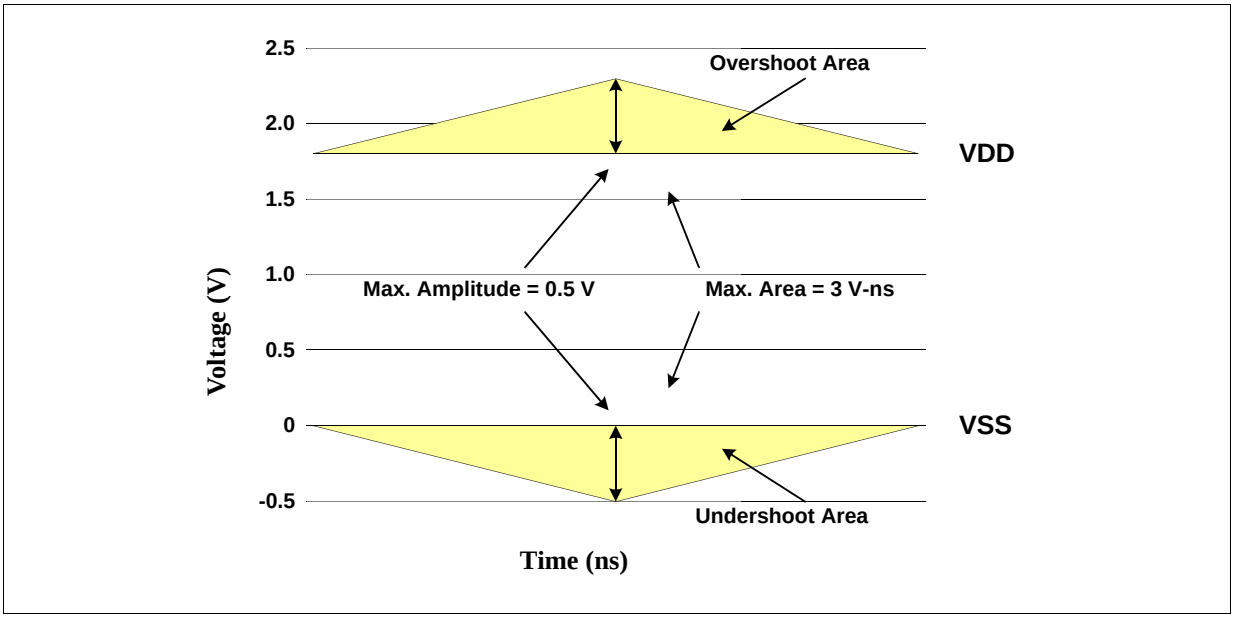

Figure 44 — AC Overshoot and Undershoot Definition

7 AC & DC Operating Conditions (cont'd)

7.1 Driver Characteristics

LPDDR SDRAM output driver characteristics are defined for full and half and three-quarters drive strength operation as selected in the Extended Mode Register. Table 18 and Table 19 show the data in a tabular format suitable for input into simulation tools. Figure 45 and Figure 47 and Figure 46 show the driver strength characteristics graphically.

Table 18 — I-V CURVES FOR FULL DRIVE STRENGTH AND HALF DRIVE STRENGTH
[Notes 1-4]

VOLTAGE [V]	FULL DRIVE STRENGTH				HALF DRIVE STRENGTH			
	PULL-DOWN CURRENT [mA]		PULL-UP CURRENT [mA]		PULL-DOWN CURRENT [mA]		PULL-UP CURRENT [mA]	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.10	2.80	18.53	-2.80	-18.53	1.27	8.42	-1.27	-8.42
0.20	5.60	26.80	-5.60	-26.80	2.55	12.30	-2.55	-12.30
0.30	8.40	32.80	-8.40	-32.80	3.82	14.95	-3.82	-14.95
0.40	11.20	37.05	-11.20	-37.05	5.09	16.84	-5.09	-16.84
0.50	14.00	40.00	-14.00	-40.00	6.36	18.20	-6.36	-18.20
0.60	16.80	42.50	-16.80	-42.50	7.64	19.30	-7.64	-19.30
0.70	19.60	44.57	-19.60	-44.57	8.91	20.30	-8.91	-20.30
0.80	22.40	46.50	-22.40	-46.50	10.16	21.20	-10.16	-21.20
0.85	23.80	47.48	-23.80	-47.48	10.80	21.60	-10.80	-21.60
0.90	23.80	48.50	-23.80	-48.50	10.80	22.00	-10.80	-22.00
0.95	23.80	49.40	-23.80	-49.40	10.80	22.45	-10.80	-22.45
1.00	23.80	50.05	-23.80	-50.05	10.80	22.73	-10.80	-22.73
1.10	23.80	51.35	-23.80	-51.35	10.80	23.21	-10.80	-23.21
1.20	23.80	52.65	-23.80	-52.65	10.80	23.67	-10.80	-23.67
1.30	23.80	53.95	-23.80	-53.95	10.80	24.14	-10.80	-24.14
1.40	23.80	55.25	-23.80	-55.25	10.80	24.61	-10.80	-24.61
1.50	23.80	56.55	-23.80	-56.55	10.80	25.08	-10.80	-25.08
1.60	23.80	57.85	-23.80	-57.85	10.80	25.54	-10.80	-25.54
1.70	23.80	59.15	-23.80	-59.15	10.80	26.01	-10.80	-26.01
1.80	—	60.45	—	-60.45	—	26.48	—	-26.48
1.90	—	61.75	—	-61.75	—	26.95	—	-26.95

NOTES:

1. Based on nominal impedance of 25 Ohms (Full Drive) and 55 Ohms (Half Drive) at $V_{DDQ}/2$
2. The full variation in driver current from minimum to maximum due to process, temperature and voltage will lie within the outer bounding lines of the I-V curve.
3. The I-V current for the optional quarter drive strength is approximately 50% of the half drive strength.
4. The IV current for the optional octant drive strength is approximately 25% of the half drive strength current.

7 AC & DC Operating Conditions (cont'd)
7.1 Driver Characteristics (cont'd)

Table 19 — I-V Curves for Three-Quarters Drive Strength [Notes 1-3]

VOLTAGE [V]	THREE-QUARTERS DRIVE STRENGTH			
	PULL-DOWN CURRENT [mA]		PULL-UP CURRENT [mA]	
	MIN	MAX	MIN	MAX
0.00	0.00	0.00	0.00	0.00
0.10	1.96	12.97	-1.96	-12.97
0.20	3.92	18.76	-3.92	-18.76
0.30	5.88	22.96	-5.88	-22.96
0.40	7.84	25.94	-7.84	-25.94
0.50	9.80	28.00	-9.80	-28.00
0.60	11.76	29.75	-11.76	-29.75
0.70	13.72	31.20	-13.72	-31.20
0.80	15.68	32.55	-15.68	-32.55
0.85	16.66	33.24	-16.66	-33.24
0.90	16.66	33.95	-16.66	-33.95
0.95	16.66	34.58	-16.66	-34.58
1.00	16.66	35.04	-16.66	-35.04
1.10	16.66	35.95	-16.66	-35.95
1.20	16.66	36.86	-16.66	-36.86
1.30	16.66	37.77	-16.66	-37.77
1.40	16.66	38.68	-16.66	-38.68
1.50	16.66	39.59	-16.66	-39.59
1.60	16.66	40.50	-16.66	-40.50
1.70	16.66	41.41	-16.66	-41.41
1.80	—	42.32	—	-42.32
1.90	—	43.23	—	-43.23

NOTES:

1. The IV current for the Three-Quarters Strength Driver is approximately 70% of the full drive strength current shown in Table 18. The Three-Quarters Strength Driver impedance is approximately 36 Ohms at VDDQ/2.
2. The full variation in driver current from minimum to maximum due to process, temperature and voltage will lie within the outer bounding lines of the I-V curve.
3. Implementation and availability of Three-Quarters Strength Driver is optional for speed bins LPDDR333 and below.

7 AC & DC Operating Conditions (cont'd)
7.1 Driver Characteristics (cont'd)

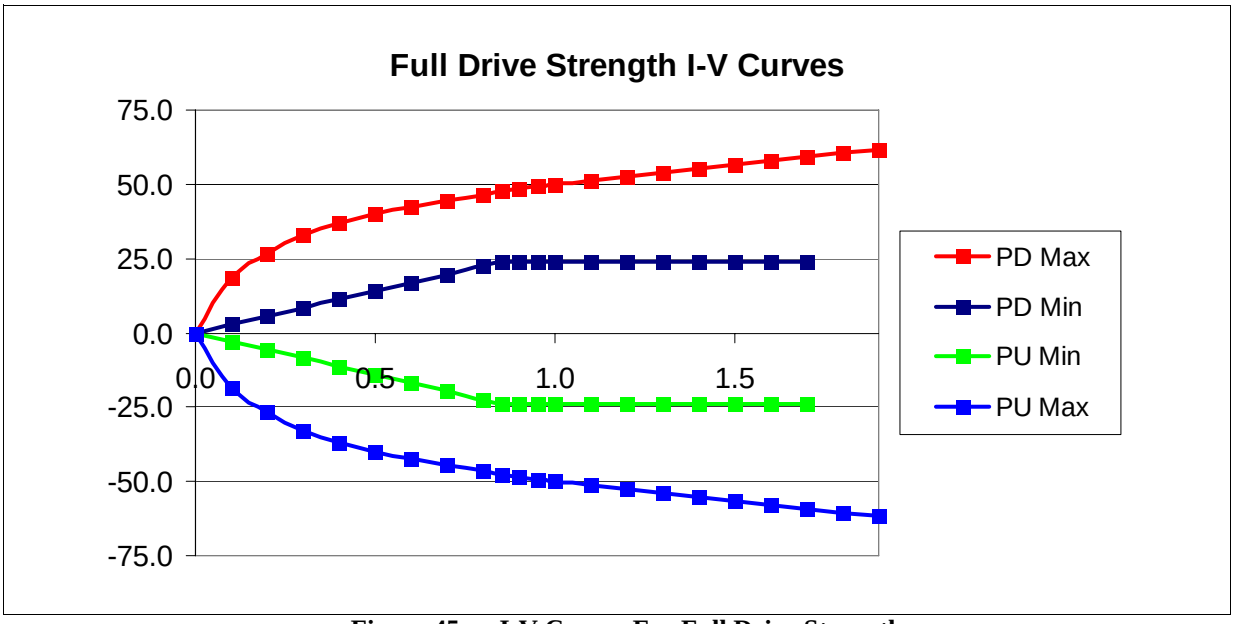

Figure 45 — I-V Curves For Full Drive Strength

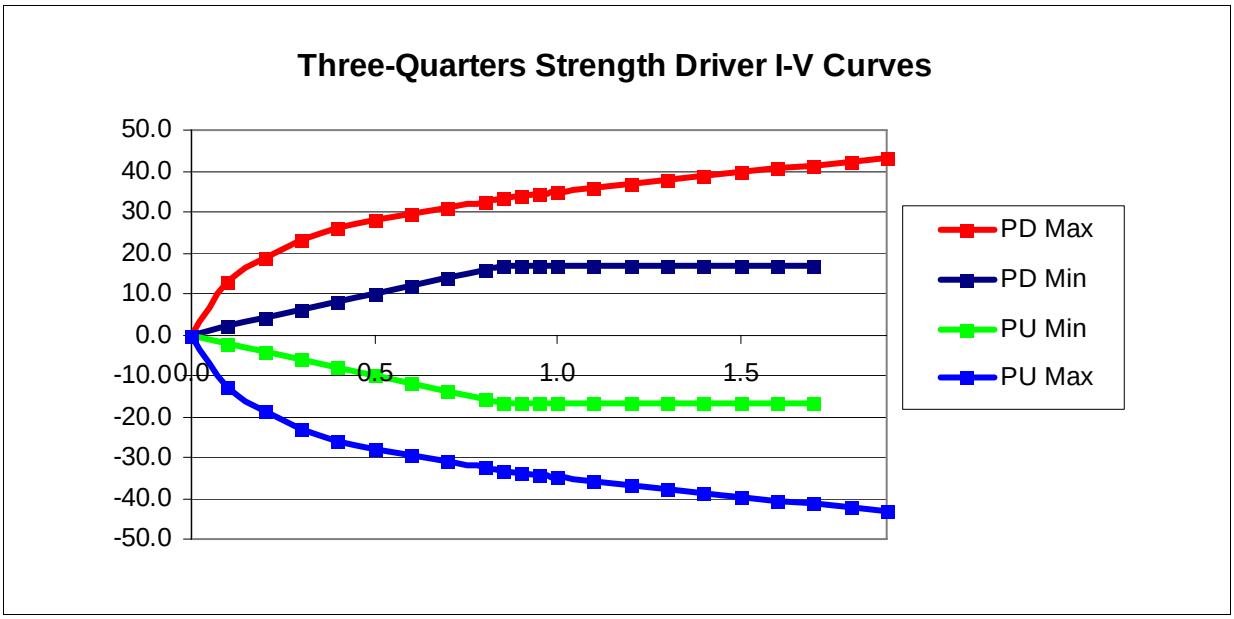

Figure 46 — I-V Curves For Three-Quarters Drive Strength

7 AC & DC Operating Conditions (cont'd)
7.1 Driver Characteristics (cont'd)

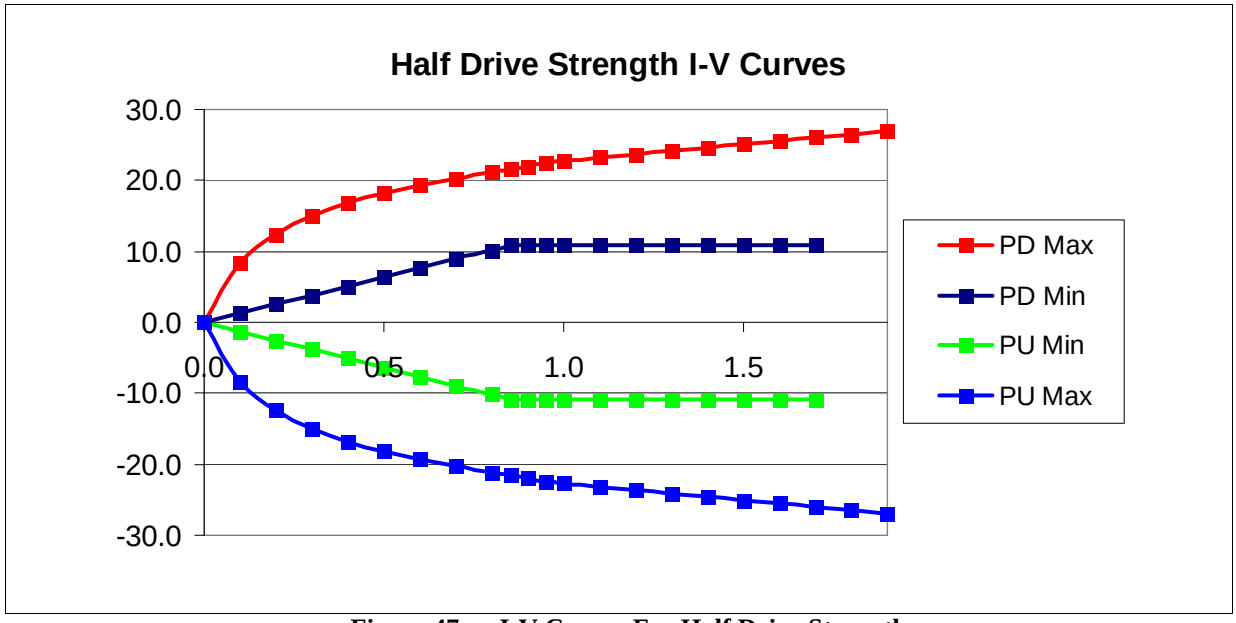

Figure 47 — I-V Curves For Half Drive Strength

NOTE 1 Implementation and availability of Three-Quarters Strength Driver is optional for speed bins LPDDR333 and below.

Annex A (informative) Differences between Document Revisions

A.3 Differences between JESD209A and JESD209

This table summarizes the changes made to this standard, JESD209-A, compared to its predecessor, JESD209 (August 2007).

Page	Description of Change
All	The JEDEC Standard number was updated from JESD209 to JESD209A
3	LPDDR SDRAM Addressing Table Added 64 Mb and 2 Gb densities Added 128 Mb x16 option
54	LPDDR400 SDRAM AC Parameters Added 370 MHz and 400 MHz AC Tables
5	LPDDR SDRAM 60-, 90-Ball BGA Ballouts with A13 ball
4 and 5	LPDDR SDRAM 60-, 90-Ball BGA Ballouts with additional CS#, CKE
16, 59, 60, 61, and 62.	LPDDR SDRAM Output Driver Characteristics Added three-quarters drive strength option
6, 12, 19	LPDDR400 SDRAM TQ Pad Proposal Added TQ pin description. Added TQ signal initialization sequence information Added TQ signal definition
18	LPDDR2 Extended Mode Register Added 64 Mb and 2 Gb densities Removed Note for 128 Mb density Removed LPDDR2 option from Device Type Register

A.2 Differences between JESD209 and JESD79-4A

This table summarizes the changes made to this standard, JESD209, compared to its predecessor, JESD79-4A (November 2006). .

Page	Description of Change
All	The JEDEC Standard number was corrected from JESD79-4A to JESD209

Annex A (informative) Differences between Document Revisions (cont'd)

A.1 Differences between JESD79-4A and JESD79-4

This table briefly describes most of the changes made to this standard, JESD79-4A, compared to its predecessor, JESD79-4 (May 2006). It should be used with both Versions at hand. Some editorial changes are not included.

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Page	Description of Change
7	Per JCB-06-005 Updtaed Figure 3 — Simplified State Diagram
15	Per JCB-06-005 Added Section 3.2.6 — Status Register Read (Optional)
16	Per JCB-06-006 Added Figure 8 — SRR Register (A[n:0]=0)
17	Per JCB-06-005 Added Figure 9 — Status Register Read Timing Diagram Subsequent figures renumbered.
52	Per JCB-06-005 Updtaed Table 14 — AC Timings Added tSRR and tSRC for LPDDR266 and LPDDR200
	Added Annex A


JEDEC