SiFive TileLink To APB Bridge (TL2APB) v1p0

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Proprietary Notice

Release Information

Version	Date	Changes
v1p0	Thursday 4th May, 2017	TL2APB Manual. • Describes the functionality of the SiFive TileLink To APB Bridge

Contents

Chapter 1

Introduction

SiFive's TileLink To APB Bridge (TL2APB) can be used to connect SiFive Coreplex IP to AMBA APB Protocol Specification v2.0 based systems. SiFive Coreplex IP natively uses TileLink for all system communication external to the Coreplex. The TL2APB bridge translates TileLink transactions to AMBA APB Protocol Specification v2.0.

Compliance

- The SiFive TL2APB is fully compliant with AMBA APB Protocol Specification v2.0 and this document should be read in conjunction with the AMBA APB Protocol Specification v2.0 Protocol Specification.
- The SiFive TL2APB is fully compatible with SiFive Coreplex IP. Some properties of the TL2APB are specific to a given Coreplex implementation. This document should be read in conjunction with the Coreplex IP manual.

Chapter 2

TL2APB Interfaces

Block Diagram

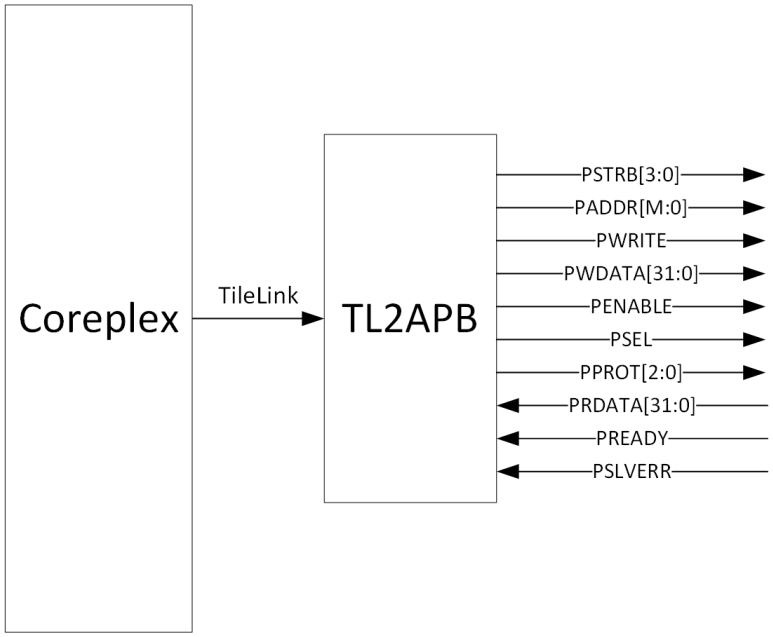

Figure 2.1: TL2APB Block Diagram.

TL2APBInterface

Name	Direction	Width	Description
PENABLE	Out	1	Indicates the second and subsequent cycles of an APB transfer.
PWRITE	Out	1	Indicates an APB write access when High, and an APB read access when Low.

PADDR	Out	[M:0]	The APB address bus where M is the minimum width necessary for the address range in a given Coreplex implementation.
PPROT	Out	[2:0]	Protection control signals.
PWDATA	Out	[31:0]	Write data bus.
PSTRB	Out	[3:0]	Byte strobe signal indicates which byte lanes to update during a write transfer.
PREADY	In	1	A slave uses this signal to extend an APB transfer.
PSLVERR	In	1	Used to indicate a transfer failure.
PRDATA	In	[31:0]	Read data bus.

Table 2.1: APB4 Interface

Integration

To simplify implementations, all SiFive bridges are pre-integrated with Coreplex IP. As such, the only exposed interface on the TL2APB is the APB4 interface. The APB4 interface is synchronous to the TileLink interface to which it is connected. Please consult the Coreplex manual for clocking information.

Chapter 3

Functional Description

This chapter will describe the functional behavior of the TL2APB in more detail.

Atomic Memory Operations (AMO)

- TileLink AMOs are translated to Read-Modify-Write operations and therefore no longer atomic.
- Because AMOs issued through the TL2APB can not guarantee automaticity, they should not be issued through the TL2APB in a multi-master system.

PADDR

- For a given Coreplex implementation, the width of PADDR is the minimum width necessary for the the address range of the TileLink bus it is connected to.

PSEL

- The TL2APB uses a single PSEL to indicate that the port is active.
- External logic is required to route PSEL to the appropriate slave.

PPROT

- PPROT is tied to 0x01: Privileged, non-secure data access.

PSLVERR

- When PSLVERR indicates a transfer failure, the signal is translated into the TileLink response **d_error**.