REVISION HISTORY

Revision	Description	Date	Drawn
Ver 1.0	draft	2017-03-08	linyu

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Design Name: XR871_EVB_MAIN_BRD

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A4	REVISION HISTORY	1.0

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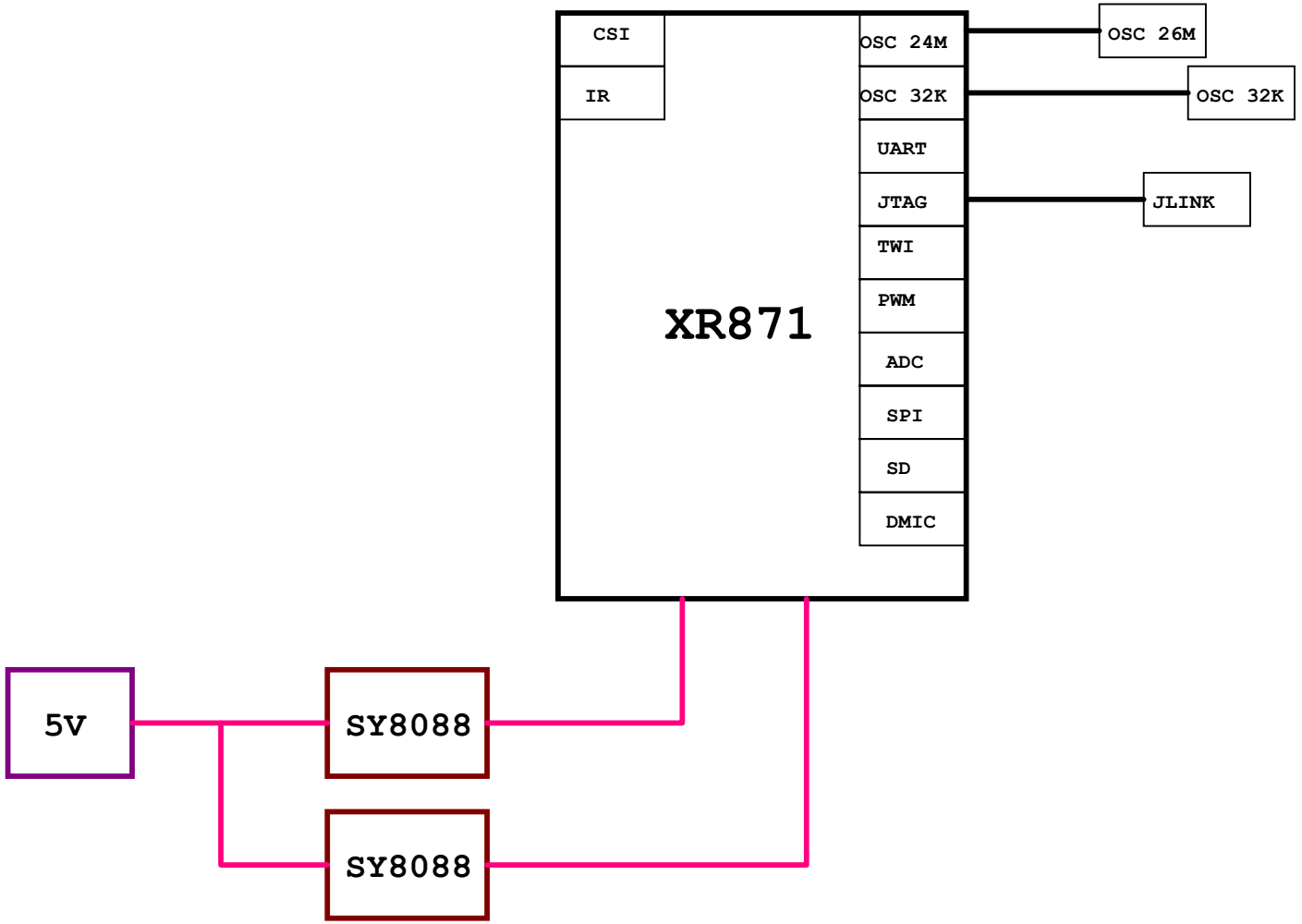
BLOCK DIAGRAM



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GPIO ASSIGNMENT

MAIN_BRD

PIN	NAME	CFG
PB0	UART0_TX	1
PB1	UART0_RX	2/4
PB2	SWD_TMS/SPI0_WP/BOOT0	2/5/0
PB3	SWD_TCK/SPI0_HD/BOOT1	2/5/1
PB4	SPI0_MOSI	2/5
PB5	SPI0_MISO	2/5
PB6	SPI0_CS	2/5
PB7	SPI0_CLK	2/5

ARDUNIO

PIN	NAME	CFG
PA0	RESET	2/4
PA1	SPI1_MISO	2/4
PA2	SPI1_CLK	2/4
PA3	ICP1	
PA4	TWI0_SCL	4
PA5	TWI0_SDA	4
PA6	I/O	
PA7	I/O	
PA8	ADC5/TWI1_SCL	3
PA9	ADC4/TWI1_SDA	3
PA10	ADC3	3
PA11	ADC2	2
PA12	ADC1	2
PA13	ADC0	2
PA14	PWM	3
PA15	PWM	3
PA16	I/O	1
PA17	UART1_TX	1
PA18	UART1_RX	1
PA19	SPI1_MOSI/PWM	5
PA20		
PA21		
PA22	SPI1_CS/PWM	5

DEV_SENSOR_BRD

PIN	NAME	CFG
PA0	SD-CMD/SPI1_MOSI	2/3
PA1	SD-DATA0/SPI1_MISO	2/3
PA2	SD-CLK/SPI1_CLK	2/3
PA3	SD-DET/SPI1_CS	2/6
PA4	TWI0_SCL	4
PA5	TWI0_SDA	4
PA6	LED	
PA7	LED	
PA8	PWM0	3
PA9	PWM1	3
PA10	PWM3	3
PA11	Akey	2
PA12	PA12	2
PA13	PA13	2
PA14	M-CTRL	3
PA15	DHT	6
PA16	RESET	1
PA17	IR-RX	1
PA18	IR-TX	1
PA19	SPI1_MOSI/KEY	5
PA20	SPI1_MISO/KEY	5
PA21	SPI1_CLK	5
PA22	SPI1_CS0	5

DEV_AUDIO_BRD

PIN	NAME	CFG
PA0	SD-CMD/SPI1_MOSI	2/3
PA1	SD-DATA0/SPI1_MISO	2/3
PA2	SD-CLK/SPI1_CLK	2/3
PA3	SD-DET/SPI1_CS0	2/6
PA4	TWI0_SCL	4
PA5	TWI0_SDA	4
PA6	DKEY1	0
PA7	DKEY2	0
PA8	RESET	1
PA9	AKEY	2
PA10	DMIC_CLK	4
PA11	DMIC_DATA	4
PA12	I2S_MCLK	4
PA13	I2S_BCLK	4
PA14	I2S_DI	4
PA15	I2S_DO	4
PA16	I2S_LRCLK	4
PA17	IR-RX	2
PA18	IR-TX	2
PA19	SPI1_MOSI	5
PA20	SPI1_MISO	5
PA21	SPI1_CLK	5
PA22	SPI1_CS0	5

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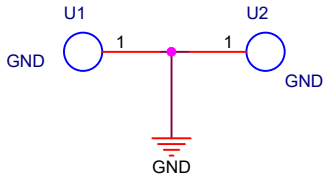
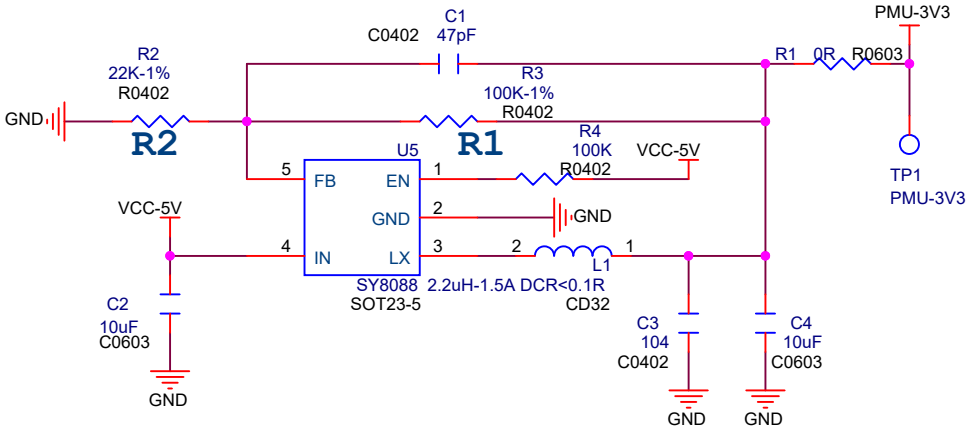
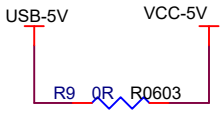
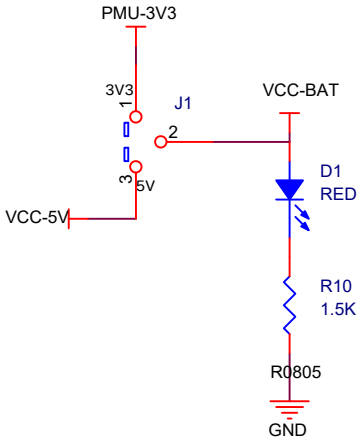
POWER

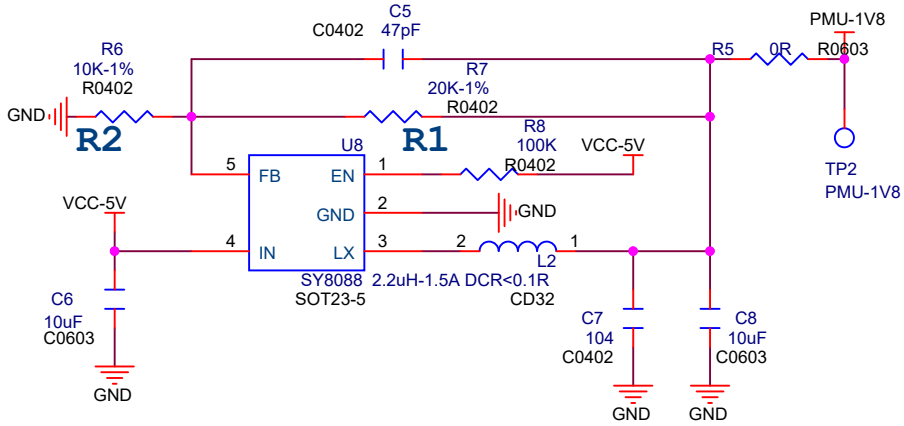




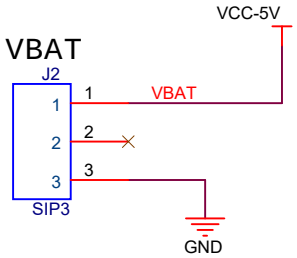
Vout = 0.6*(1+R1/R2)≈ 3.3V

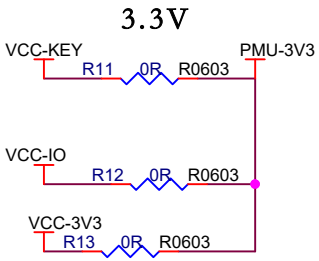






Vout = 0.6*(1+R1/R2)=1.8V





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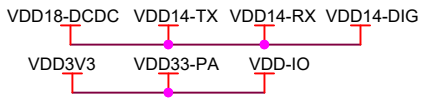
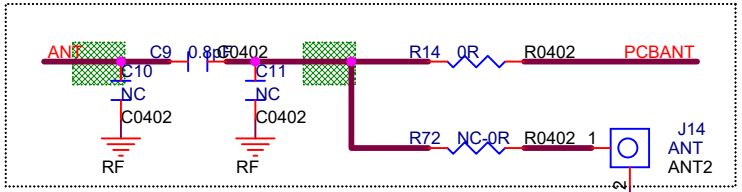
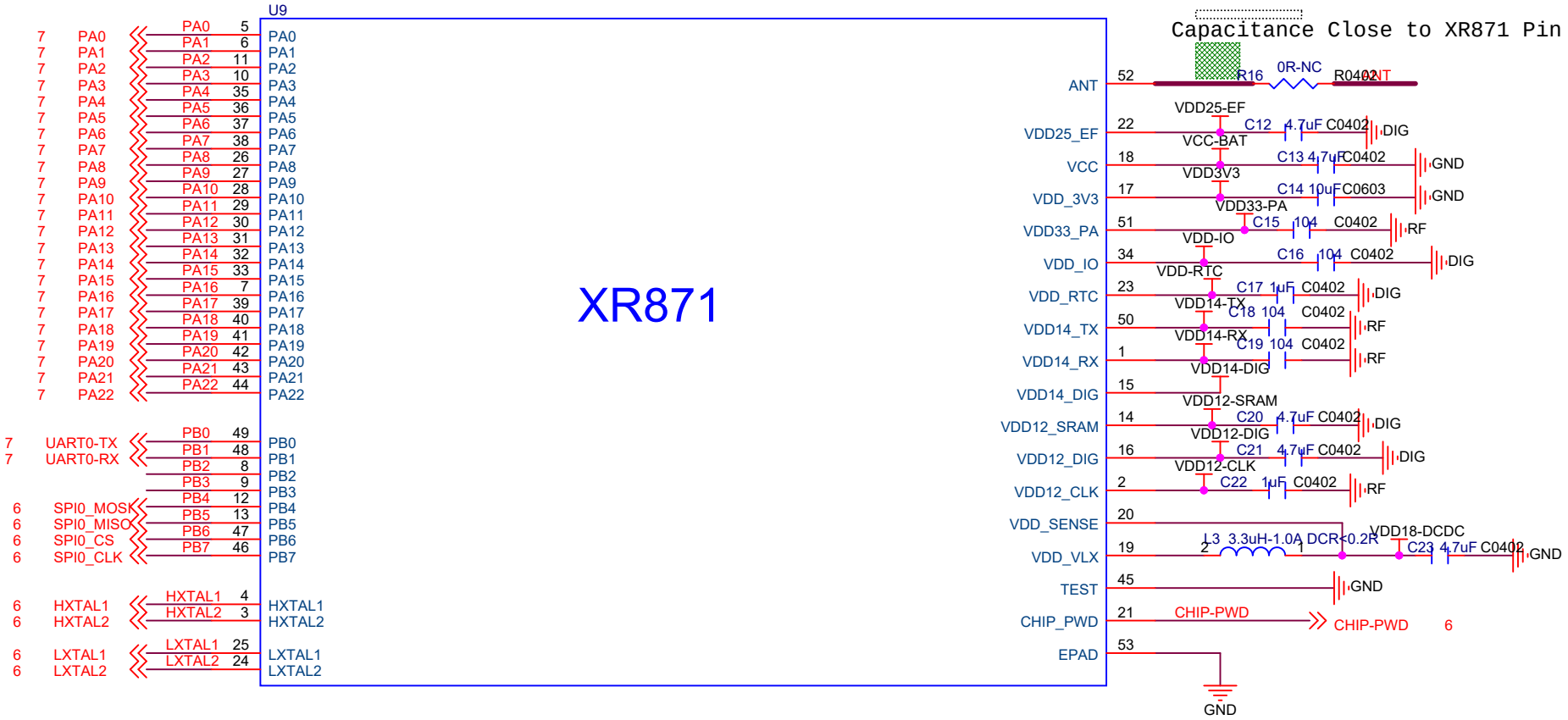
MCU & RF

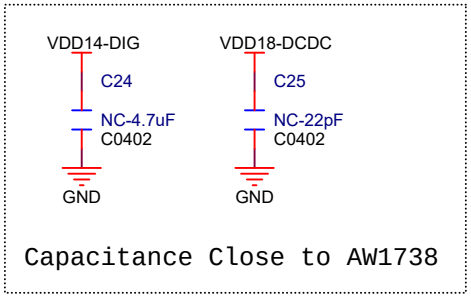
该50ohm阻抗线需参考，即 参 考 L3层 。



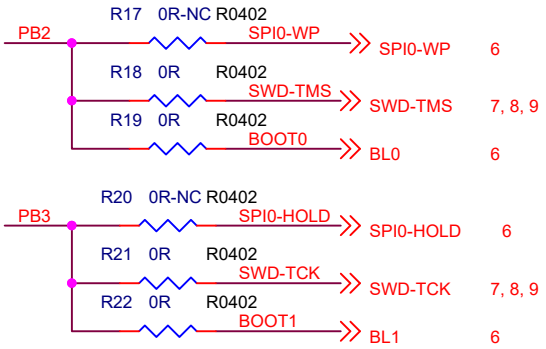


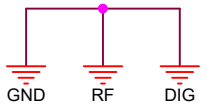


Capacitance Close to XR871 Pin



Capacitance Close to AW1738





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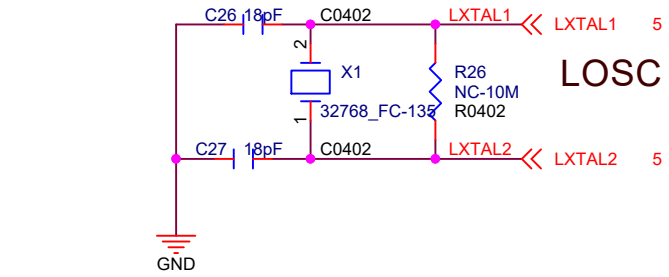
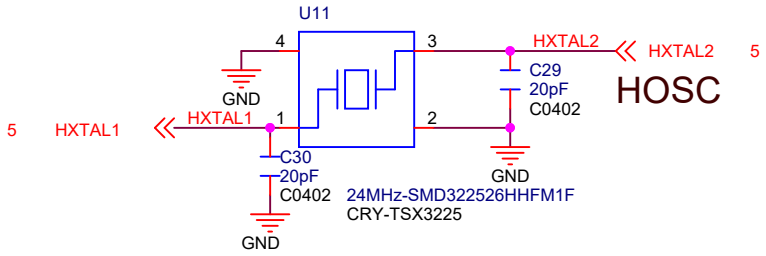
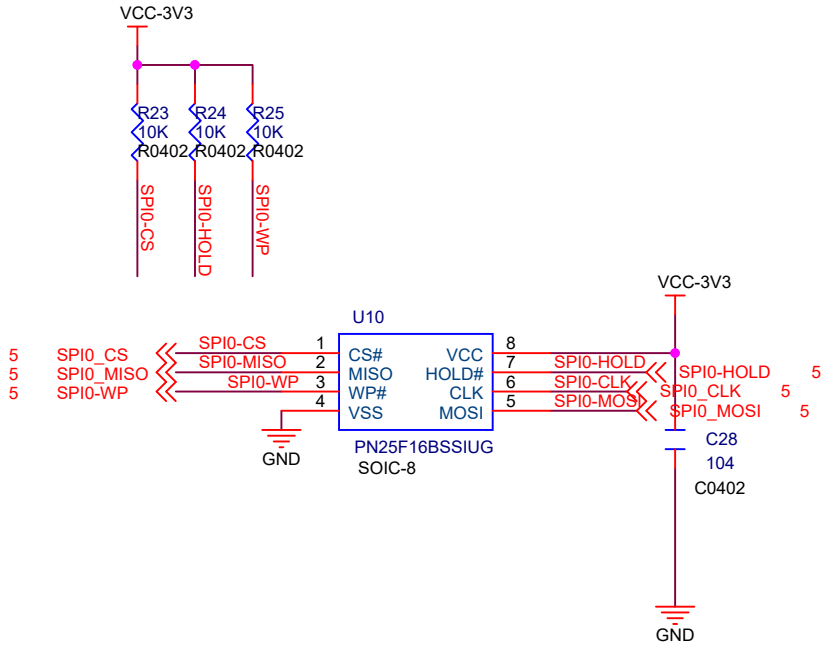
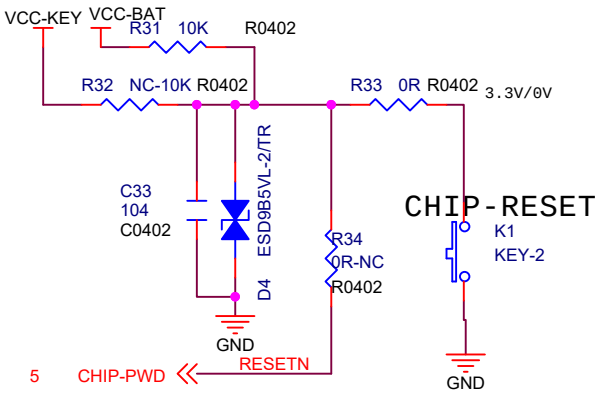
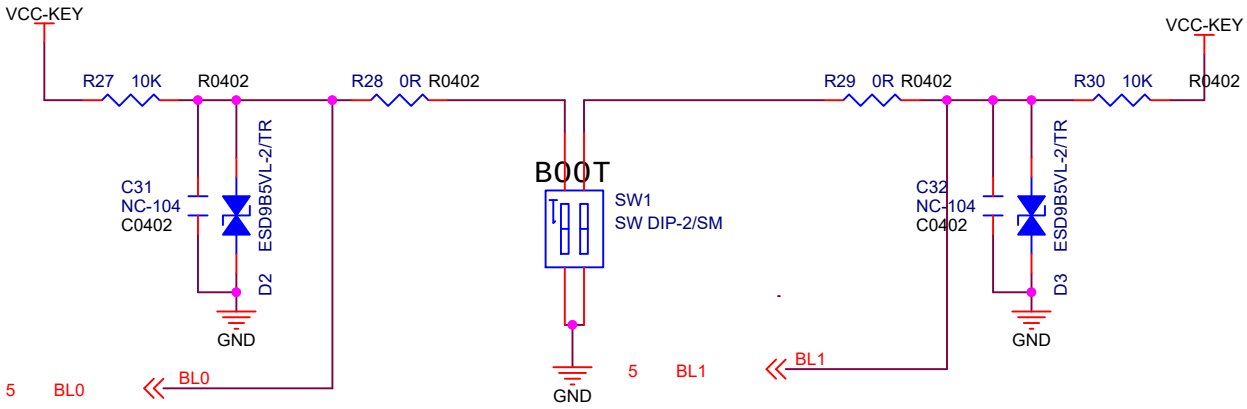
CLK & FLASH & RESET











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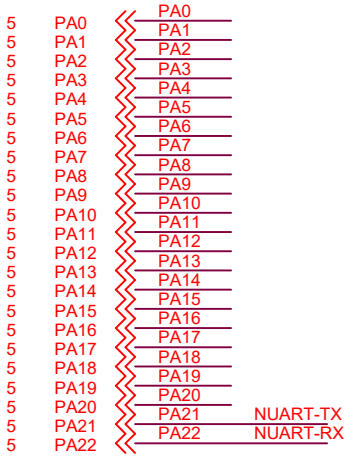
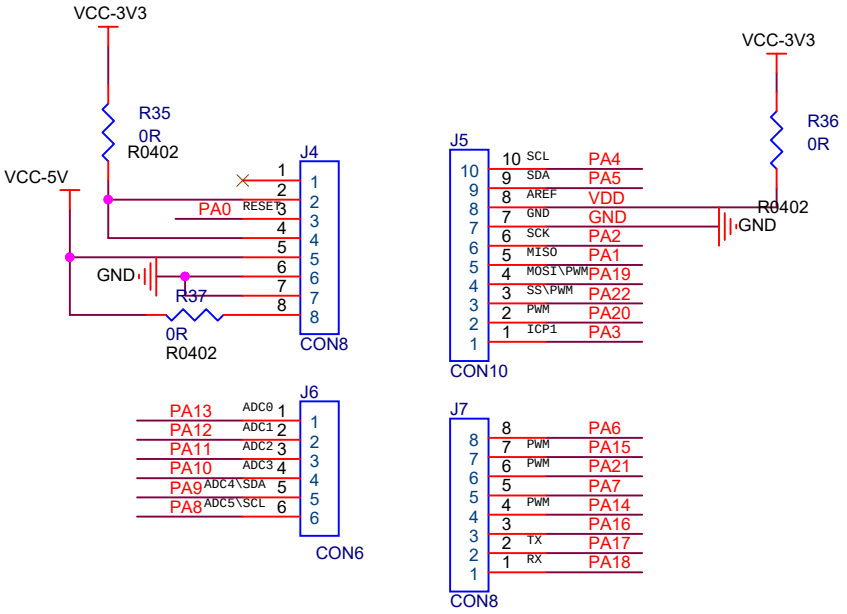
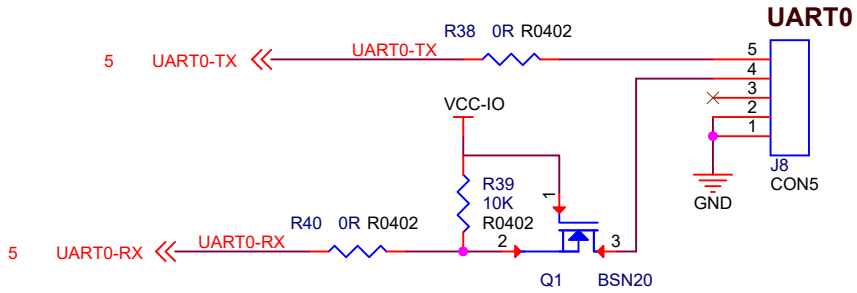
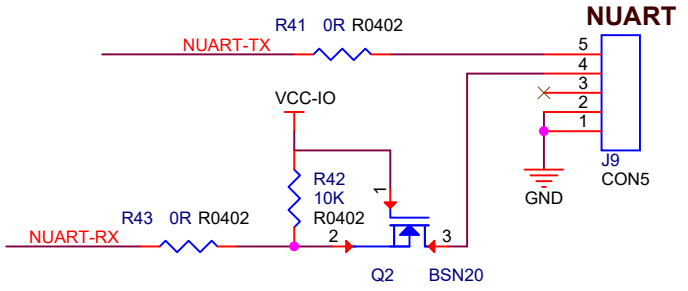
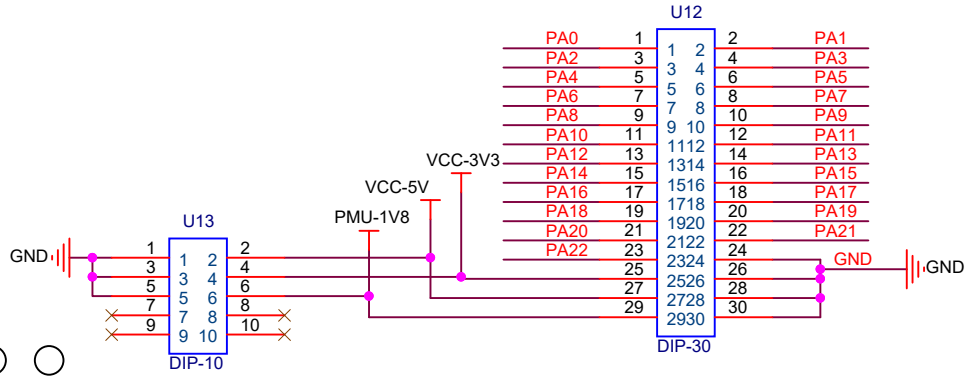
INTERFACE











板子固定支架孔，分布于大板四个角
孔直径 3 mm

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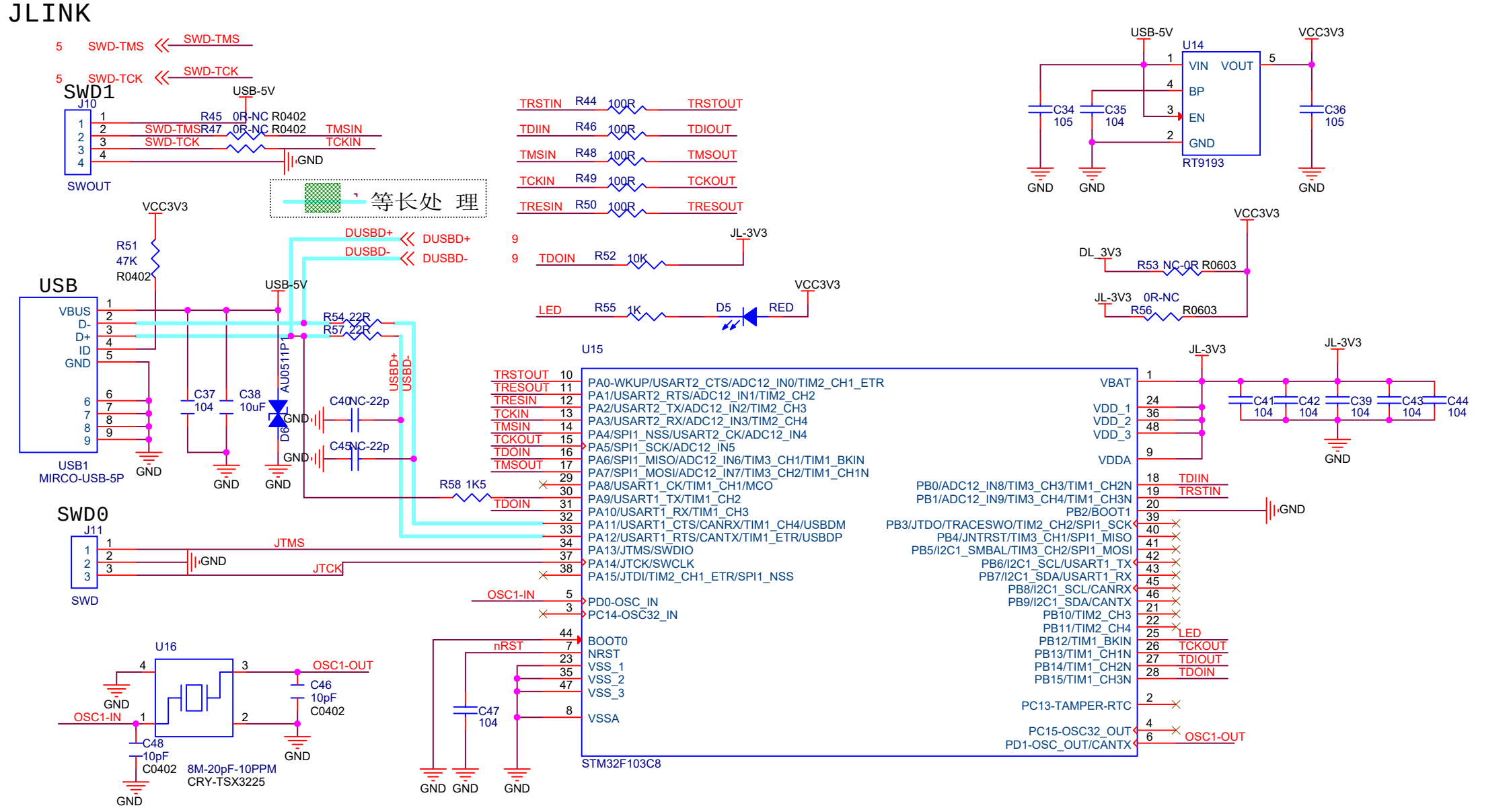
JLINK



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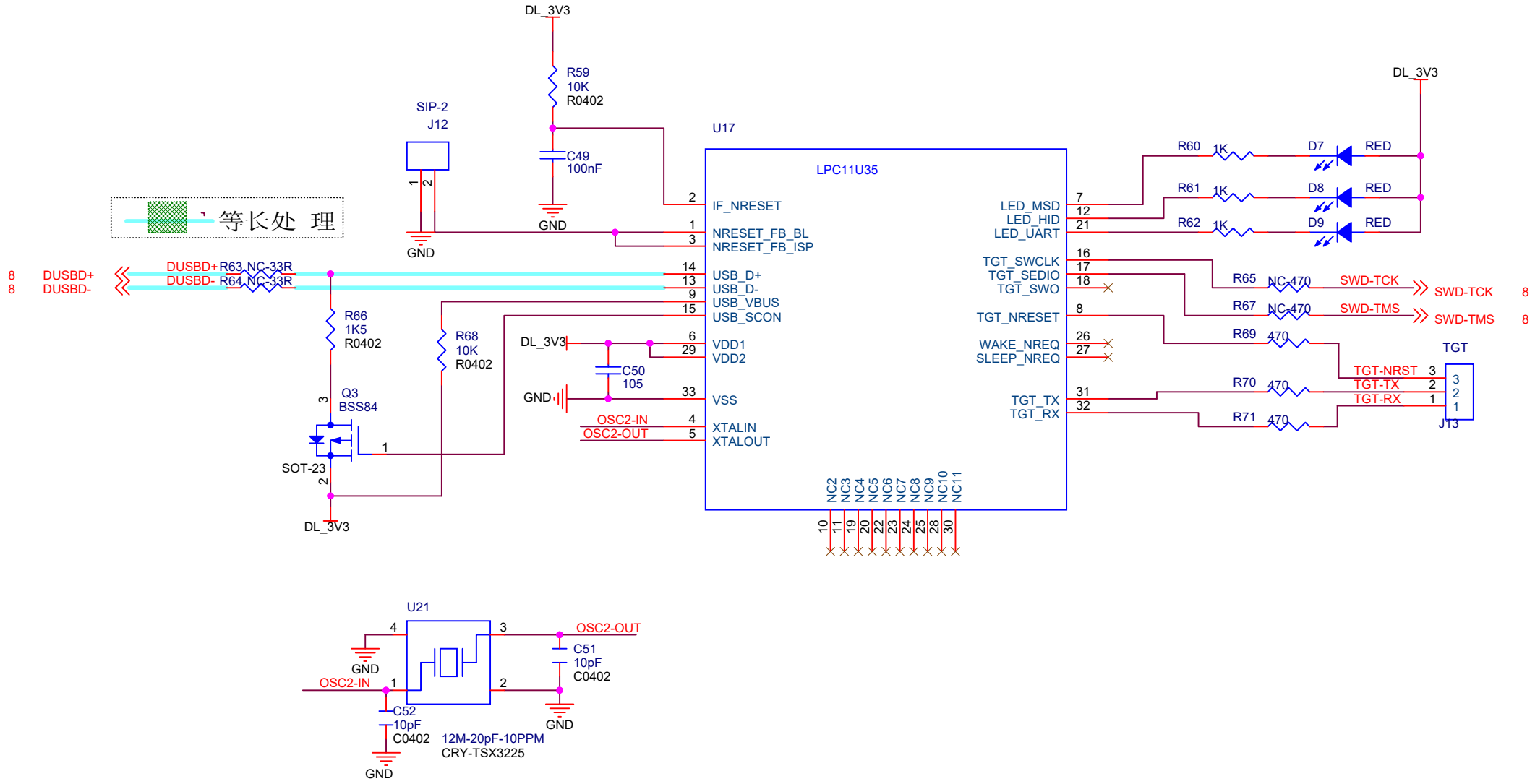
DAPLINK



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