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# A Brief Introduction to Lattice-Based Cryptography in Hardware

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# Content

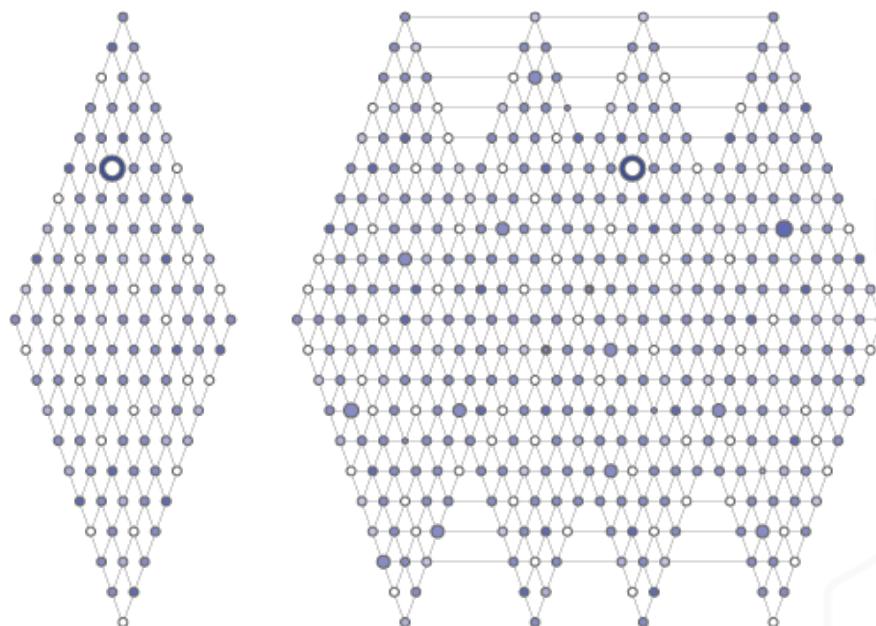


- Why is lattice-based cryptography hard?
  - Operations / components / sizes required.
- What's changed within candidates?
  - M-LWE and LWR.
- Designs pre-/post-standardisation announcement.
  - Specifically, some lattice-based signature and KEM hardware designs.
- Other / miscellaneous.

**Please interrupt me with questions, comments, or (more likely) errors.**

# Why Lattices?

- Mathematics easier to understand (vs e.g. ECC).
- Operations require simple multiplication, addition, modular reduction.
- Simple parameter selection / scalable to fit security needs.
- Average-case to worst-case hardness.
- Offers KEM, signatures, FHE, IBE, etc.
- Highest candidate numbers submitted to NIST.
- No major security issues in 30+ years.
- Already used by Google, strongSwan VPN, etc.
- Efficient KeyGen, Encrypt/Sign, Decrypt/Verify.
- Relatively small keys, ciphertexts, and signatures.



# Learning With Errors



- There is a secret vector  $s \leftarrow \mathbb{Z}_q^n$ .
- An oracle (who knows  $s$ ) generates a uniform matrix  $A$  and noise vector  $e$  distributed normally with standard deviation  $\alpha q$ .
- The oracle outputs:  $A$  and  $b = A \times s + e \bmod q$ .
- The distribution of  $A$  is uniformly random,  $b$  is pseudo-random.
- Can you find  $s$ , given access to  $(A, b)$ ?
- Can you distinguish  $(A, b)$  from a uniformly random  $(A, b')$ ?

# Ideal and Module Lattices



- Standard lattices deal with matrices / vectors.
- Adding additional structure, one can deal with *ideal* or *module* lattices.
- Thus, (cyclic) matrices can be replaced with polynomials.
- Efficiencies are then gained using polynomial multiplication (e.g. NTT) over the ring

$$R_q = \mathbb{Z}_q[x]/(x^n + 1) \text{ for } q = 1 \bmod 2n.$$

- Multiplication complexity reduces from  $O(n^2)$  to  $O(n \log(n))$ .

# Classification of Lattices (Simplified)

- Lattice-based cryptographic schemes generally fall under three classes:

$$\text{LWE} \leftrightarrow \text{Module-LWE} \leftrightarrow \text{Ring-LWE}$$

- Added structures hinder security:

$$\text{LWE} \geq^{\text{sec.}} \text{Module-LWE} \geq^{\text{sec.}} \text{Ring-LWE}$$

- However, it can also enhance performance:

$$\text{LWE} \leq^{\text{per.}} \text{Module-LWE} \leq^{\text{per.}} \text{Ring-LWE}$$

# Modules: Multiplication

- NTTs typically aren't generic; require ad-hoc designs.
- Research done investigating high-performance vs. low-cost designs.
- Some candidates specify NTTs explicitly, i.e. NewHope.
- NTTs get modular reduction for free, but restrict parameters (e.g. requiring a prime modulus).
- Matrix / schoolbook / Karatsuba multiplication more generic.
- General multiplication has more liberal parameter selection, but requires modular reduction.
- Sparse multiplication is used often in signature schemes and LWR, using binary or ternary values, which can simply use shift-and-adds.

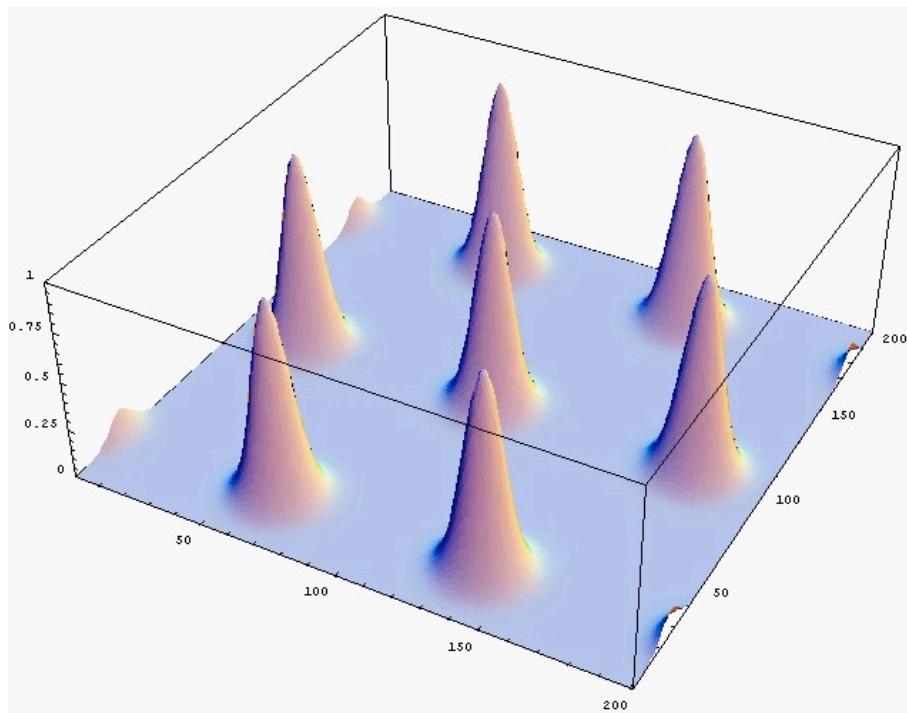
# Modules: Multiplication

- Typically require <<32-bit integer multiplication (no floating points) most actually <16 bits.
- Thus, DSPs are ideal for MAC (or just multiply) operations.
- BRAMs typically used for key / input / output storage.
- Inputs drawn from memory, PRNG, and/or error sampler.
- Most candidates provide constant-time multiplication.

# Modules: Error Samplers

- Error adds noise to computations on secret data; computationally hard.

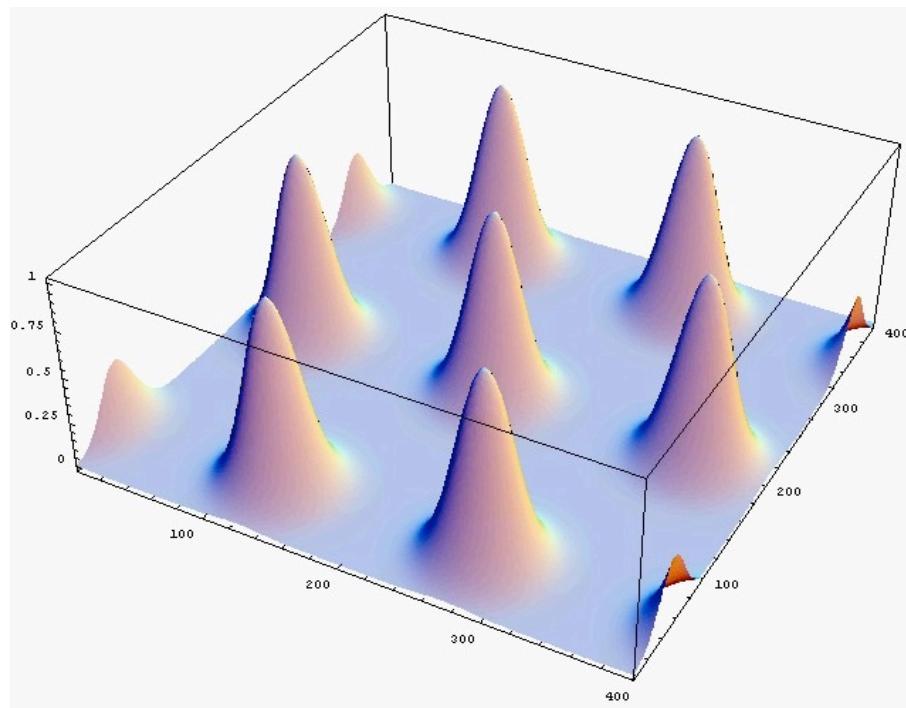
For  $B = A * S + E$



# Modules: Error Samplers

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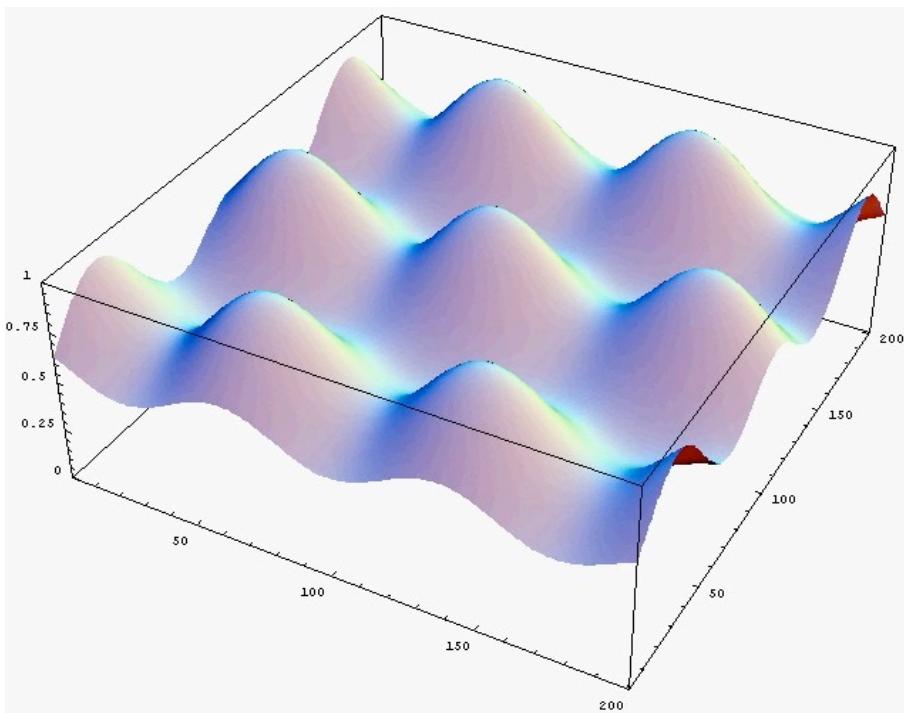
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# Modules: Error Samplers

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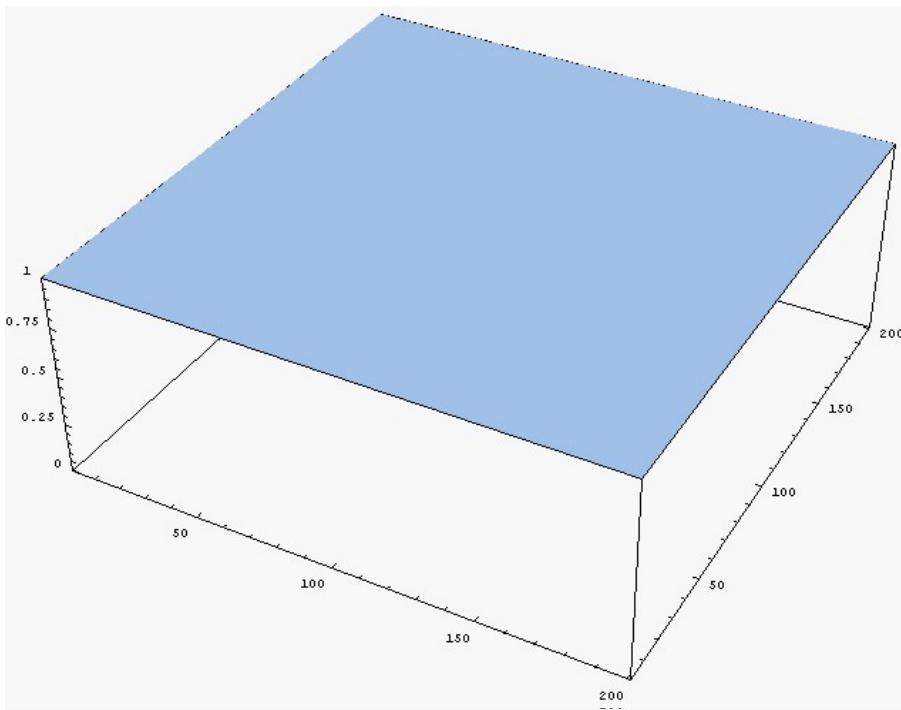
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# Modules: Error Samplers

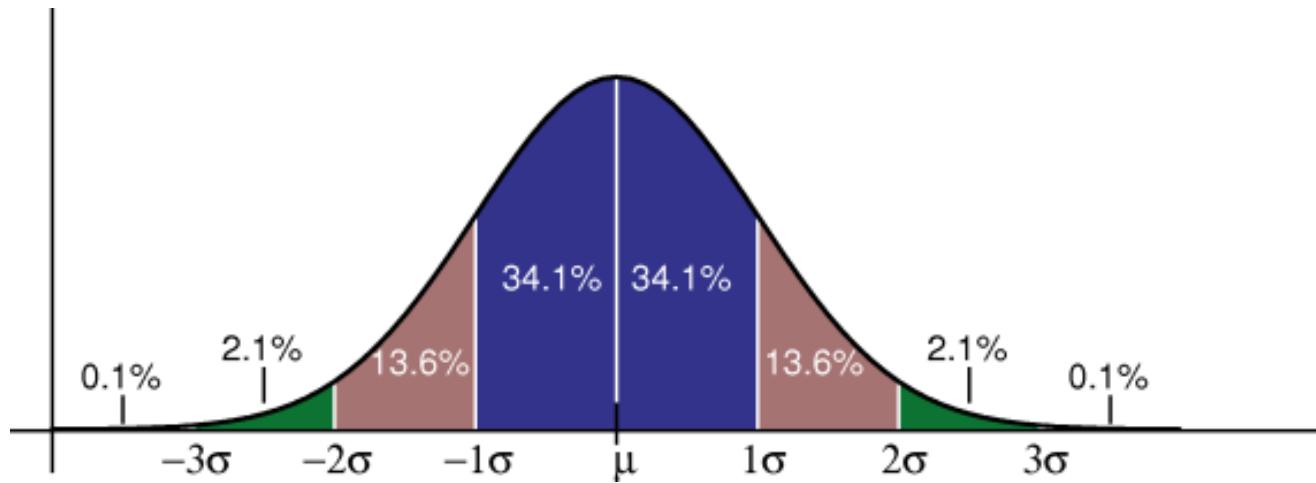
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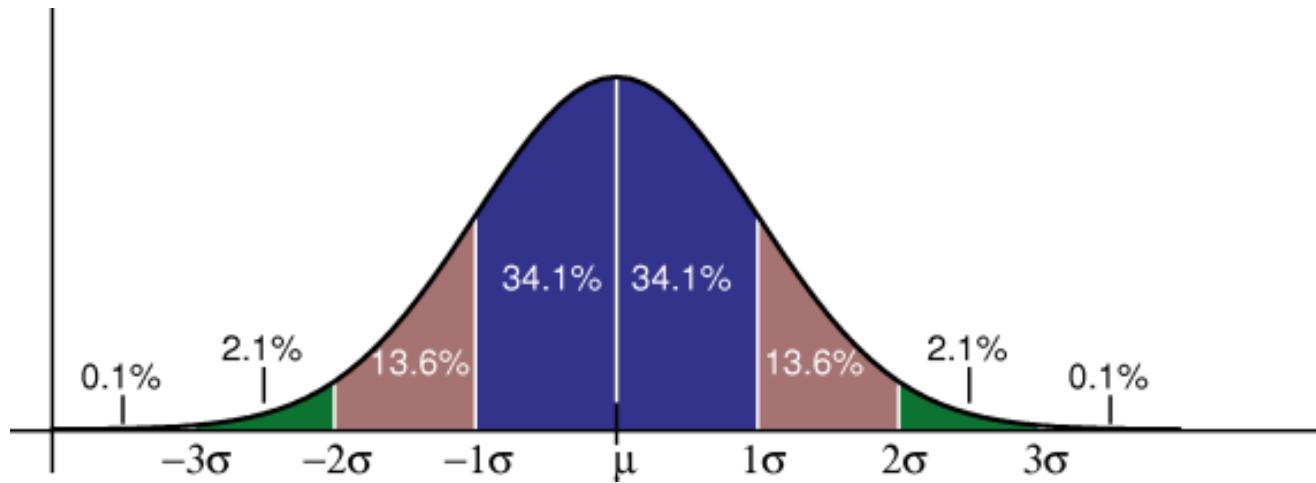
# Modules: Error Samplers

- Error adds noise to computations on secret data; computationally hard.
- Error sampled from Gaussian-like or Binomial distribution.
- Look-up table methods: CDT sampler.
- Arithmetic-based methods: discrete Ziggurat sampler.
- Hybrid table / arithmetic methods: Bernoulli and Knuth-Yao samplers.
- Standard deviations depend on cryptographic schemes and parameters:



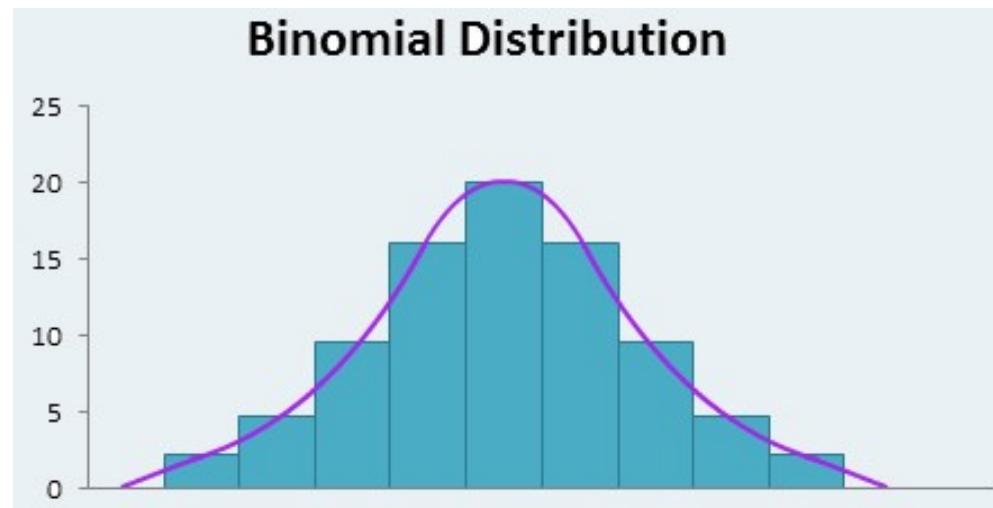
# Modules: Error Samplers

- Error samplers linked to computational hardness, thus a side-channel target.
- Important to ensure independent-time design (e.g. constant time).
- Some recent research considers masked and fault attack protection for these modules.
- One can use Gaussian convolutions to make larger parameters efficient, e.g. for signature schemes.



# Modules: Error Sampling

- Alternatively, some schemes (NewHope, Kyber) use Binomial sampling.
- One simply subtracts the Hamming weight of two uniform bit vectors.
- LWR schemes instead use ‘rounding’ instead of error addition.
- Dilithium (and maybe others?) uses uniform random noise.



# Module Lattices

- (Ring-)LWE deals with vectors/polynomials in  $R_q^1$ , for example  $\mathbf{A} * \mathbf{S} + \mathbf{E}$ .
- Module-LWE deals with polynomials in  $R_q^k$ , for example  $k = 3$  in Kyber.
- Higher security parameters increase  $k$ , instead of  $n$ .
- Thus, virtually no re-implementation for changing security levels.
- “One way to informally view the MLWE problem is to take the RLWE problem and replace the single ring elements ( $\mathbf{A}$  and  $\mathbf{s}$ ) with module elements over the same ring. Using this intuition, RLWE can be seen as MLWE with module rank  $k = 1$ .”

$$\left[ \begin{array}{c|c} A_1(x) \in R_q & A_2(x) \in R_q \\ \hline A_3(x) \in R_q & A_4(x) \in R_q \end{array} \right] \times \left[ \begin{array}{c} S_1(x) \in R_q \\ \hline S_2(x) \in R_q \end{array} \right] + \left[ \begin{array}{c} E_1(x) \in R_q \\ \hline E_2(x) \in R_q \end{array} \right]$$

# Learning With Rounding

- SABER uses module-LWR problem.
- Polynomials are always of  $n = 256$  coefficients.
- Flexibility: matrix dimensions ( $k$ ) is parameterizable.
- 2-by-2 for 115-bit post-quantum security



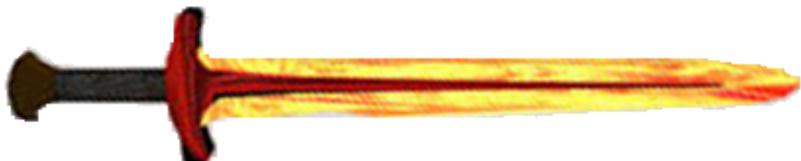
Light SABER

- 3-by-3 for 180-bit post-quantum security



SABER

- 4-by-4 for 245-bit post-quantum security



Fire SABER

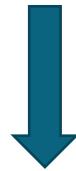
# Differences in LWE and LWR

- SABER uses module-LWR problem.

$$\left\lfloor \frac{p}{q} \quad \text{Uniform in } [0, q-1] \right\rfloor \quad \text{where } p < q$$

- Rounds a product  $p = a * s$  to the nearest integer.

Prime  $q$  introduces rounding bias



- Cannot use prime  $q$  ☹
- Hence, no NTT-based fast polynomial multiplication

→ Thus, one needs to use generic polynomial multiplication algorithm.

# Generic Polynomial Multiplication

- SABER uses hybrid of Toom-Cook, Karatsuba, and schoolbook multiplication.
- Generic techniques (Toom-3, Toom-4, Karatsuba) can be applied to SABER, NTRU-HRSS, and NTRUEncrypt.
- NTRU Prime also uses non-NTT multiplication.
- Round5 only requires LHW shift-and-add multiplication.
- Generic hardware techniques have been researched for Ring-TESLA.



# Lattice-based Signatures in Hardware

A hardware design of Ring-TESLA

# Generic Polynomial Multiplication

- qTESLA is (somewhat) based upon the signature scheme; Ring-TESLA.

## KeyGen( $a_1, a_2$ ):

Discrete Gaussian polynomials:  $s, e_1, e_2 \leftarrow D_\sigma^n$ ,  $t_1 \equiv a_1 s + e_1 \pmod{q}$ ,  $t_2 \equiv a_2 + e_2 \pmod{q}$

Secret-Key:  $(s, e_1, e_2)$  // Public-Key:  $(t_1, t_2)$ .

## Sign( $\mu; a_1, a_2, s, e_1, e_2$ ):

Uniform polynomial:  $y \leftarrow \mathbb{Z}_q[x]/(x^n + 1)$

- $v_1 \equiv a_1 y \pmod{q}$ ,  $v_2 \equiv a_2 y \pmod{q}$

Compute the hash function:

- $c = H(v_1 || v_2, \mu)$

Compute signature/rejections:

- $z \equiv y + sc \pmod{q} \leftarrow$ signature
- $w_1 \equiv v_1 + e_1 c \pmod{q}$
- $w_2 \equiv v_2 + e_2 c \pmod{q}$

## Verify( $\mu; z, c; a_1, a_2, t_1, t_2$ ):

Compute hash inputs:

- $w'_1 \equiv a_1 z + t_1 c \pmod{q}$
- $w'_2 \equiv a_2 z + t_2 c \pmod{q}$

Compute the hash function:

- $c'' = H(w'_1 || w'_2, \mu)$

Accept/reject signature:

- If  $c' = c''$

128-bit security parameters:

$$\begin{aligned} n &= 512, \\ q &= 51750913, \\ \sigma &= 52. \end{aligned}$$

Signature is 11.9 kb,  
public-key is 26 kb,  
and secret-key is 13.7 kb.

<sup>1)</sup> Sedat Akleylek, Nina Bindel, Johannes A. Buchmann, Juliane Krämer, and Giorgia Azzurra Marson. An efficient lattice-based signature scheme with provably secure instantiation. In AFRICACRYPT, pages 44–60, 2016.  
<sup>2)</sup> Howe, J., Rafferty, C., Khalid, A. and O'Neill, M., 2017. Compact and provably secure lattice-based signatures in hardware. In 2017 IEEE International Symposium on Circuits and Systems (ISCAS) (pp. 1-4). IEEE.

# Ring-TESLA in Hardware

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## Algorithm 1 Ring-TESLA Sign

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**procedure** SIGN( $\mu, \mathbf{a}_1, \mathbf{a}_2, \mathbf{s}, \mathbf{e}_1, \mathbf{e}_2$ )

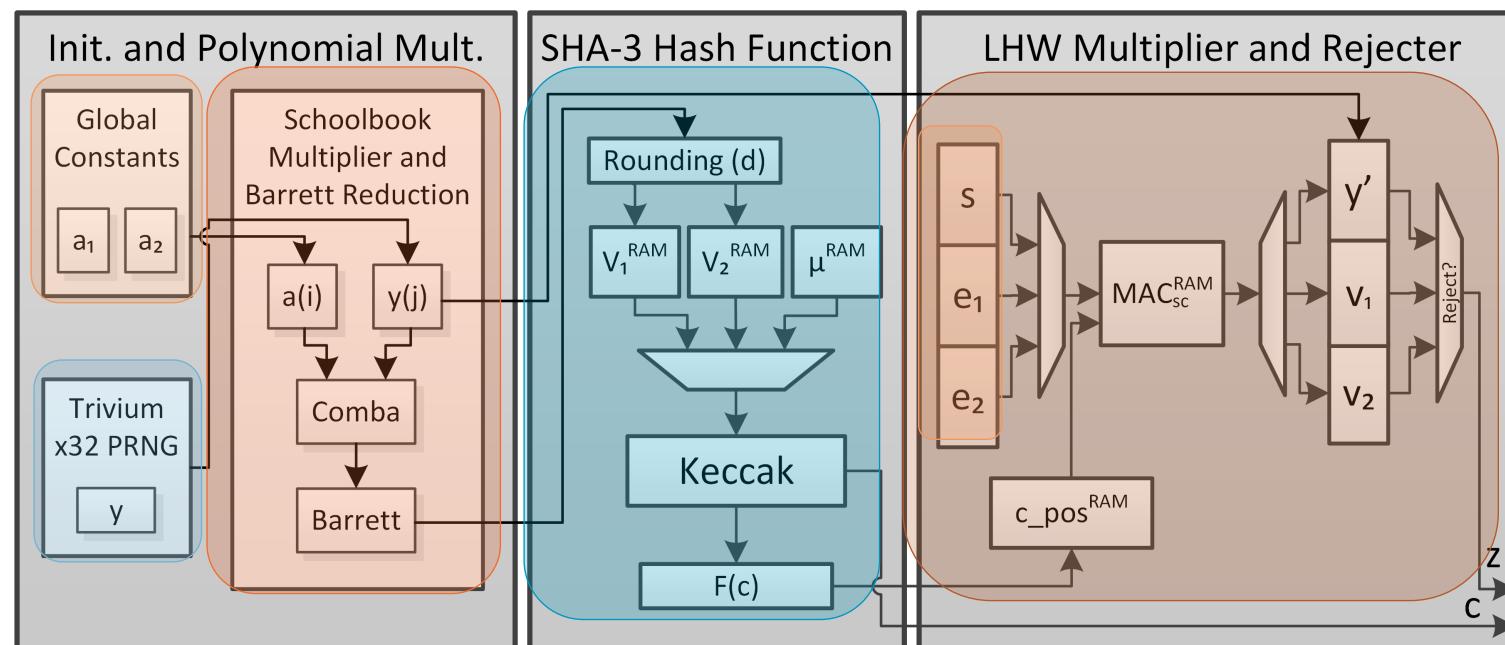
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 $y \leftarrow \mathcal{R}_{q, [B]}$ 
 $v_1 \equiv \mathbf{a}_1 y \pmod{q}$ 
 $v_2 \equiv \mathbf{a}_2 y \pmod{q}$ 
 $c = H([v_1]_{d,q}, [v_2]_{d,q}, \mu)$ 
 $\mathbf{c} = F(c)$ 

 $z \leftarrow y + \mathbf{s}\mathbf{c}$ 
 $w_1 \equiv v_1 - \mathbf{e}_1\mathbf{c} \pmod{q}$ 
 $w_2 \equiv v_2 - \mathbf{e}_2\mathbf{c} \pmod{q}$ 
if  $[w_1]_{2^d}, [w_2]_{2^d} \notin \mathcal{R}_{2^d-L}$ 
    or  $z \notin \mathcal{R}_{B-U}$  then
        Restart
    end if
    return  $(z, c)$ 
end procedure

```

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# Finite-State Machine of Ring-TESLA

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## Algorithm 1 Ring-TESLA Sign

---

```

procedure SIGN( $\mu, \mathbf{a}_1, \mathbf{a}_2, \mathbf{s}, \mathbf{e}$ )
     $\mathbf{y} \xleftarrow{\$} \mathcal{R}_{q, [B]}$ 
     $\mathbf{v}_1 \equiv \mathbf{a}_1 \mathbf{y} \pmod{q}$ 
     $\mathbf{v}_2 \equiv \mathbf{a}_2 \mathbf{y} \pmod{q}$ 
     $c = H([\mathbf{v}_1]_{d,q}, [\mathbf{v}_2]_{d,q}, \mu)$ 
     $\mathbf{c} = F(c)$ 
     $\mathbf{z} \leftarrow \mathbf{y} + \mathbf{s}\mathbf{c}$ 
     $\mathbf{w}_1 \equiv \mathbf{v}_1 - \mathbf{e}_1\mathbf{c} \pmod{q}$ 
     $\mathbf{w}_2 \equiv \mathbf{v}_2 - \mathbf{e}_2\mathbf{c} \pmod{q}$ 

```



# Finite-State Machine of Ring-TESLA



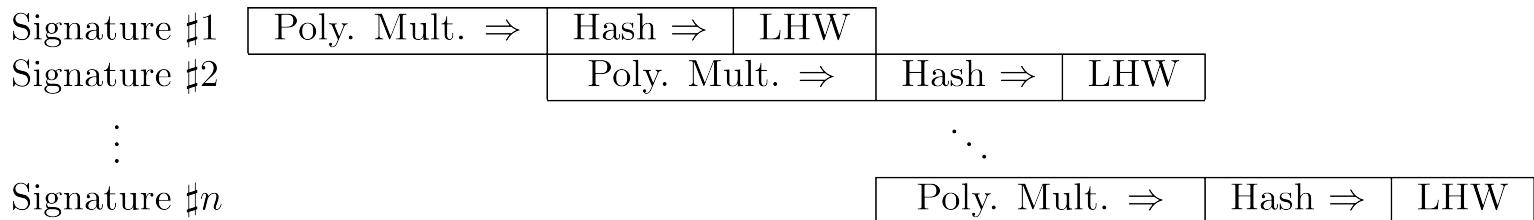
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## Algorithm 1 Ring-TESLA Sign

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 $c = H([\mathbf{v}_1]_{d,q}, [\mathbf{v}_2]_{d,q}, \mu)$ 
 $\mathbf{c} = F(c)$ 
 $\mathbf{z} \leftarrow \mathbf{y} + \mathbf{s}\mathbf{c}$ 
 $\mathbf{w}_1 \equiv \mathbf{v}_1 - \mathbf{e}_1 \mathbf{c} \pmod{q}$ 
 $\mathbf{w}_2 \equiv \mathbf{v}_2 - \mathbf{e}_2 \mathbf{c} \pmod{q}$ 
```

- Pipeline created for pre-hash computations.
- After pre-hash polynomial multiplication;
  - $\mathbf{y}$  is copied to another register for  $\mathbf{z}$ .
  - $\mathbf{y}$  is generated for next signature in parallel.
- Hash, LHW calculations of  $\mathbf{z}$ ,  $\mathbf{w}_1$ , and  $\mathbf{w}_2$ , and rejections then outside the critical path.
- Sign/Verify critical path thus pre-hash phase.



# Ring-TESLA Hardware Results

- Ring-TESLA, ideal lattice-based signatures on a Spartan 6 – LX25.
- Smaller than other lattice-based signature designs, suffers in throughput.
- Significantly smaller and faster in comparison to RSA and ECDSA.
- Further work generated hardware friendly parameters.

	Operation, Configuration	Security	Device	LUT/FF/Slice	BRAM/DSP	MHz	Cycles	Ops/sec
↓ 8	Ring-TESLA (Sign, SB-I)	128-bits	S6 LX25	4447/3345/1257	3/6	190	1835540	104
	Ring-TESLA (Sign, SB-II)	128-bits	S6 LX25	4828/3790/1513	4/8	196	917771	214
	Ring-TESLA (Sign, SB-IV)	128-bits	S6 LX25	5071/3851/1503	4/12	187	458891	408
	Ring-TESLA-(Sign, SB-VIII)	128-bits	S6 LX25	6848/5457/2254	4/20	180	229446	785
↓ 8	Ring-TESLA (Verify, SB-I)	128-bits	S6 LX25	3714/3023/1172	3/6	188	1835540	102
	Ring-TESLA (Verify, SB-II)	128-bits	S6 LX25	3917/3253/1238	3/8	194	917771	212
	Ring-TESLA (Verify, SB-IV)	128-bits	S6 LX25	4793/3939/1551	3/12	186	458891	406
	Ring-TESLA (Verify, SB-VIII)	128-bits	S6 LX25	6473/5582/2103	3/20	178	229446	776
GLP (Sign, Schoolbook x3)		80-bits	S6 LX16	7465/8993/2273	30/28	162	-	931
GLP (Verify, Schoolbook x3)		80-bits	S6 LX16	6225/6663/2263	15/8	158	-	998
BLISS (Sign, NTT)		128-bits	S6 LX25	7193/6420/2291	6/5	139	15864	8761
BLISS (Verify NTT)		128-bits	S6 LX25	5065/4312/1687	4/3	166	16346	17101
RSA (Sign)		103-bits	V5 LX30	3237 slices	7/17	200	-	89
ECDSA (Sign)		128-bits	V5 LX110	32299 LUT/FF pairs	10/37	139	-	-
ECDSA (Verify)		128-bits	V5 LX110	32299 LUT/FF pairs	10/37	110	-	-

# Frodo: Take off the Ring!

Practical post-quantum key exchange and key encapsulation from LWE.



# Frodo: Why Should We Take off the Ring?



The design philosophy of FrodoKEM combines:

- Conservative yet practical post-quantum constructions.
- Security derived from cautious parameterizations of the well-studied learning with errors problem.
- Thus, close connections to conjectured-hard problems on generic, “algebraically unstructured” lattices.
- Parameter selection is far less constrained than vs ideal lattice schemes.
- FrodoKEM multiplication can also be generic.

# Frodo: Why Should We Take off the Ring?



These qualities are appealing for practitioners;

- Probably the most secure lattice-based candidate.
  - Many IoT use cases require long-term, efficient cryptography.
- Frodo is ideal for long-term security and constrained platforms.
  - Suitable for use cases such as satellite communications and V2X.
- Frodo is extremely versatile and theoretically sound.
- However, it has less implementations than ideal lattice schemes.
  - And how do we manage the larger keys and no NTT...

# Frodo: Why Should We Take off the Ring?



- Simple design:
  - Free modular arithmetic ( $q = 2^{16}$ ).
  - Simple Gaussian sampling.
  - Parallelisable matrix-vector operations.
  - Key encapsulation without reconciliation.
  - Simple code, no complex use of NTT.
- CCA-secure with negligible error rate.
- Flexible, fine-grained choice of parameters.
- Dynamically generated  $A$  to defend against all-for-the-price-of-one attacks (AES and cSHAKE variants).

# Frodo: Why Should We Take off the Ring?



- Round 2 changes add high-security parameters and use of SHAKE.
- Main operations are of the form from before:

$$\mathbf{B} = \mathbf{S}' * \mathbf{A} + \mathbf{E} \bmod q$$

- $\mathbf{S}'$  is a matrix with dimensions 8-by-640 (or 8-by-976).
- $\mathbf{A}$  is a matrix with dimensions 640-by-640 (or 976-by-976).
- Thus, we design a LWE vector-matrix multiplication core, and repeat.
- DSPs are ideal; Artix-7 FPGAs have 48-bit MAC operations.
- $q$  is always a power-of-two, thus modular reduction is free!
- Uniform and “Gaussian” error generation.
- Random oracles via cSHAKE for CCA security.

# FrodoKEM in Hardware



“A massive design challenge was to balance **memory utilisation**, whilst not deteriorating the **performance** too much to not overexert the limited computing capabilities of the embedded devices.”



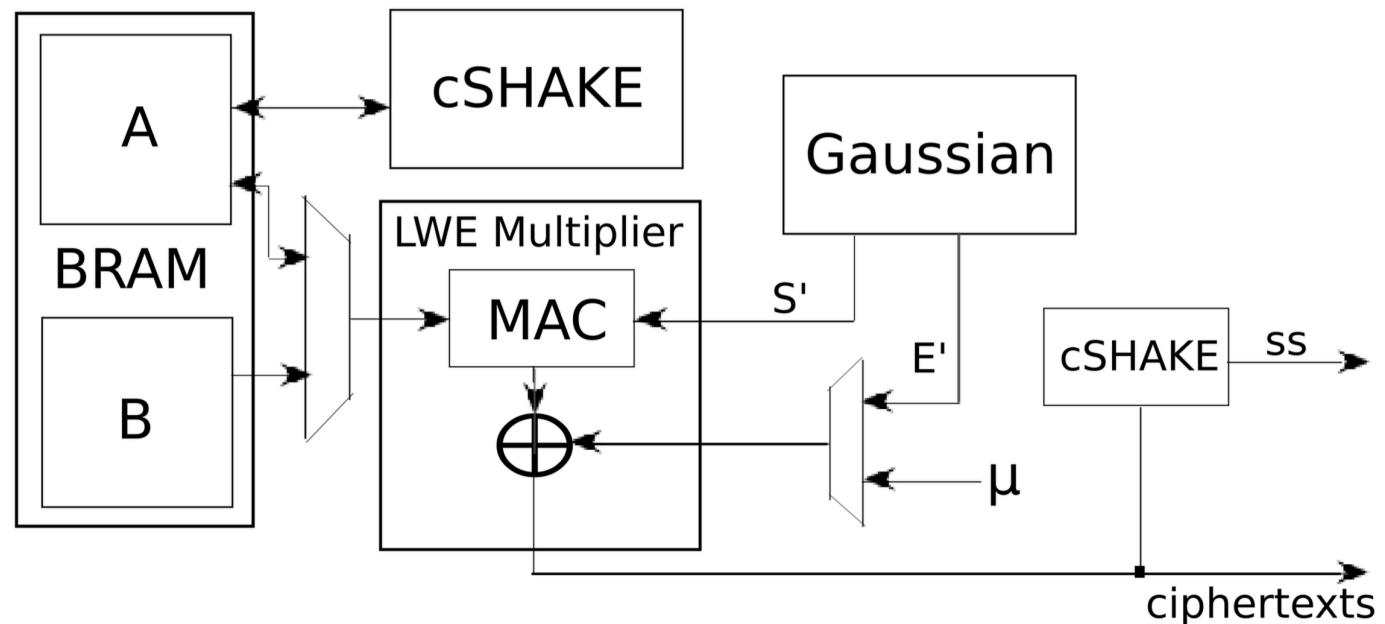
# FrodoKEM in Hardware



- Proposes a generic LWE multiplication core which computes vector-matrix multiplication and error addition.
- Generates future random values in parallel, minimising delays between vector-matrix multiplications.
- Hybrid pre-calculated / on-the-fly memory management is used, which continuously updates previous values.
- Ensures constant runtime by parallelising other modules with multiplication.
- FrodoKEM-640 has a total execution time of 60 ms, running at 167MHz.

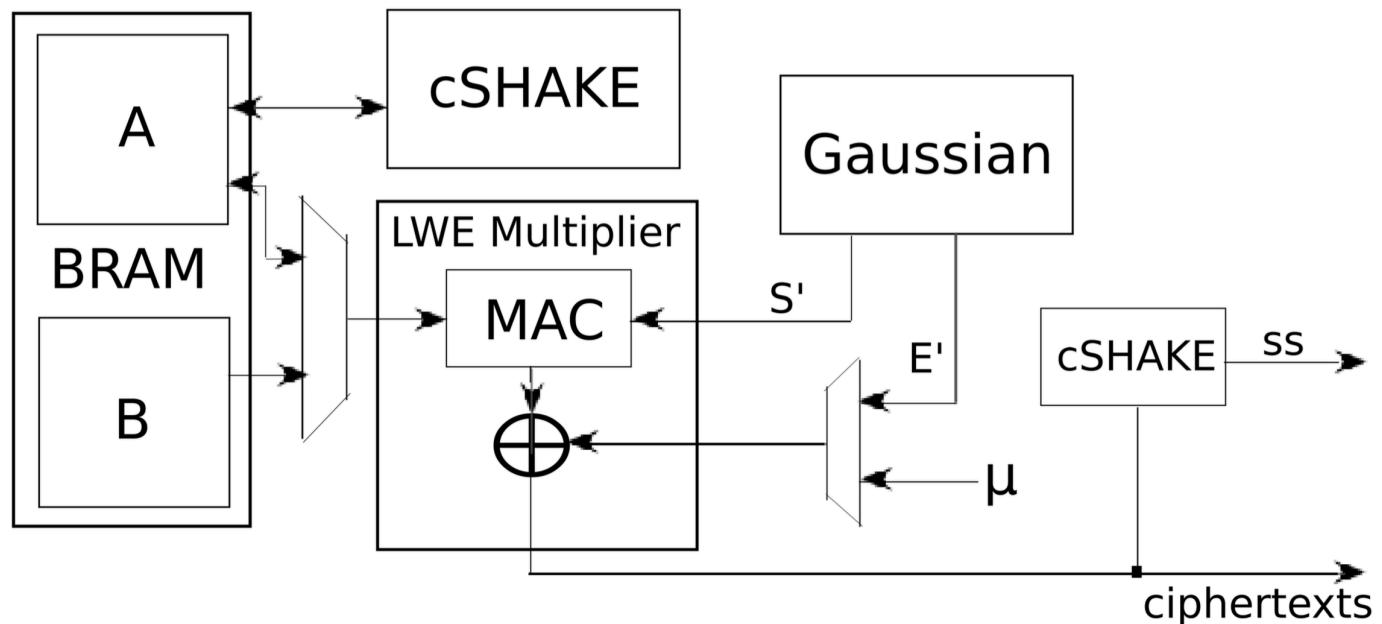
# FrodoKEM in Hardware

- Similarities in KeyGen, Encaps, and Decaps mean much of this is reused.
- Most of the generation of  $A$  is done on-the-fly to save BRAM.
- LWE multiplier is reused in all modules and all LWE calculations.



# FrodoKEM in Hardware

- For  $S'*A$  we generate the first row of  $S'$  and enough randomness in  $A$ .
- Whilst they multiply, we use ping-pong buffering to generate future values.
- This removes latency and ensures a practical constant-time design.



# FrodoKEM in Hardware



- Competes with NewHope area consumption, but much slower performance.
- Due to memory optimisations, we have huge savings in BRAM compared to LWE Encryption [HMO+16].
- Results also provided for FrodoKEM's modules; that is cSHAKE and Error sampling.

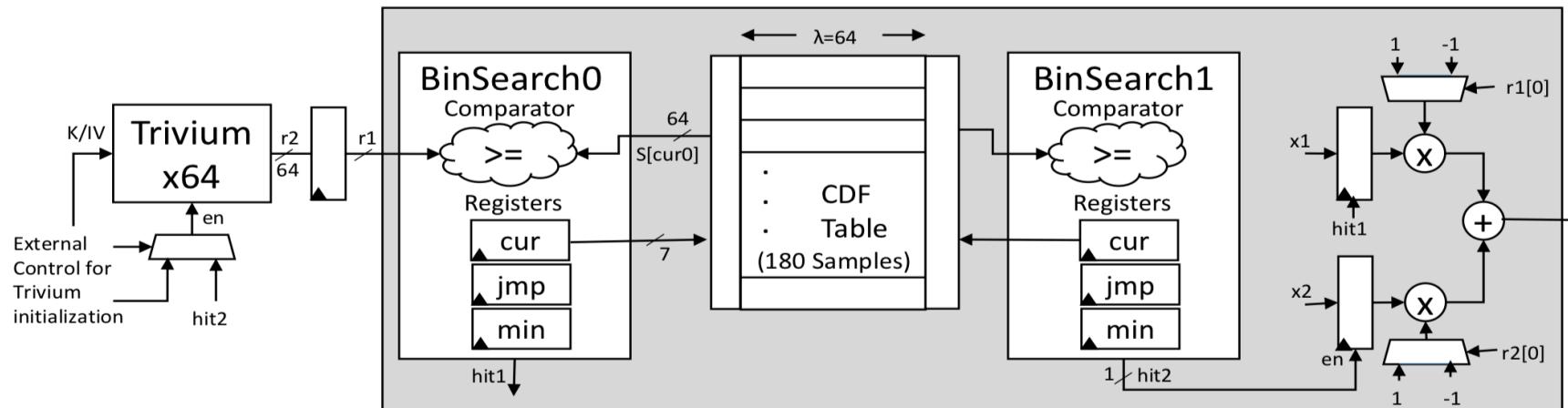
Cryptographic Operation	LUT/FF	Slice	DSP	BRAM	MHz	Ops/sec
FrodoKEM-640 Keypair <sup>2</sup>	3771/1800	1035	1	6	167	51
FrodoKEM-640 Encaps	6745/3528	1855	1	11	167	51
FrodoKEM-640 Decaps	7220/3549	1992	1	16	162	49
FrodoKEM-976 Keypair <sup>2</sup>	7139/1800	1939	1	8	167	22
FrodoKEM-976 Encaps	7209/3537	1985	1	16	167	22
FrodoKEM-976 Decaps	7773/3559	2158	1	24	162	21
cSHAKE*	2744/1685	766	0	0	172	1.2m
Error+AES Sampler*	1901/1140	756	0	0	184	184m
NewHopeUSENIX Server [OG17]	5142/4452	1708	2	4	125	731
NewHopeUSENIX Client [OG17]	4498/4635	1483	2	4	117	653
LWE Encryption [HMO <sup>+16</sup> ]	6078/4676	1811	1	73	125	1272

# Other / Miscellaneous

(Don't worry, its nearly over!)

# Other: Gaussian Sampling Designs

- In a comprehensive study we found CDT sampling the most efficient in hardware, running in constant-time is key for these modules.
- Survey available on error samplers for Round 1 candidates.
- Gaussian convolution tricks can be used to make these efficient for large parameters, which provide some ‘masking’ for free.
- Simple tricks can make these modules protected against fault attacks.



# Other: PQCzoo.com



- PQCzoo.com is a website collecting results for optimised software and hardware designs as well as side-channel analysis papers.
- One can add their own results with a simple GitHub commit.
- Please add your own results!

The screenshot shows the 'Hardware Designs' section of the PQCzoo website. The page title is 'Hardware Designs' and the subtitle is 'Hardware designs of NIST PQC candidates'. A brief description follows: 'Here is a searchable and sortable list of optimised hardware designs of candidates to the NIST post-quantum standardisation project. To add your own results, please follow the instructions on the [About section](#)'. Below this is a search bar and a table with 8 columns: Authors, PQC Type, Crypto Type, Crypto Target, Device, Date, Reference, and Conference. The table contains one row of data:

Authors	PQC Type	Crypto Type	Crypto Target	Device	Date	Reference	Conference
James Howe, Tobias Oder, Markus Krausz, Tim Güneysu	Lattice-Based	KEM	Frodo	Artix-7 FPGA	17 July 2018	eprint/2018/686	CHES 2018

# Conclusion



- Most Round 2 schemes have yet to be implemented in hardware.
- But, many require aspects that have already been researched.
  - I've put together a list of references which should be helpful.
- Important that future designs specify design philosophy.
  - e.g. high throughput or low area.
- Also, these designs should be evaluated on the same FPGA.
  - e.g. the Xilinx Artix-7 FPGA.
- This ensures comparisons between hardware designs are fair and straightforward.

**PQShield is hiring software/hardware post-quantum specialists.**

# Useful References: PhD Theses

- Howe, J., 2017. Practical Lattice-Based Cryptography in Hardware. <https://jameshowe.eu/files/thesis.pdf>
- Pöppelmann, T., 2017. Efficient implementation of ideal lattice-based cryptography. it-Information Technology, 59(6), pp.305-309. <https://hss-opus.ub.ruhr-uni-bochum.de/opus4/frontdoor/index/index/docId/4917>
- Roy, S. S., 2017. Public Key Cryptography on Hardware Platforms: Design and Analysis of Elliptic Curve and Lattice-based Cryptoprocessors. <https://www.esat.kuleuven.be/cosic/publications/thesis-288.pdf>

# Useful References: Multiplication

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- Post-Quantum Cryptography - Ruhr-Universität Bochum. <https://www.seceng.ruhr-uni-bochum.de/research/projects/pqc/>
- PQM4: Post-quantum crypto library for the ARM Cortex-M4. <https://github.com/mupq/pqm4>
- KECCAK in hardware. <https://keccak.team/hardware.html>
- PQCzoo. <https://pqczoo.com>