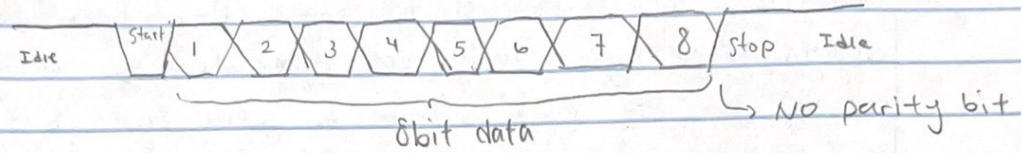
James Huang

ECE121 Midterm Honor Code: James Huang

1. UART was created to solve problems with seperate CPU system communicating with each other. It also is used for serral communication.



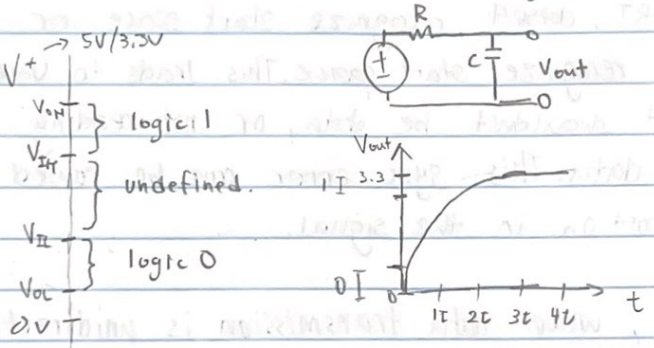
2. When UART doesn't recognize start space or when UART wrongly recognize start space. This leads to UART reading data that shouldn't be data, or not reading data when there is data. This sync error can be caused by noise and distortion in the signal.

3. Simplex, when data transmission is unidirectional
Half duplex, data transmission is bidirectional, but can't occur at the same time.
Full duplex, data transmission is bidirectional, and it can occur at the same time.

4. Data bus, it transmit data in and out of the CPU to its peripherals. This allows the CPU to read/write data from memory to other devices connected to it (Birectional)
Address bus, this transmit the specific memory address where data should be read/write to. The CPU assigns the address to memory. Without this, CPU have no way to directly access the memory, and cannot perform memory management. It is unidirectional, carries the binary address for memory.

Control bus, this transmit all the command signals to other peripherals, such as interrupts and clock signals. It controls the bus activities from the CPU, and it is needed to control flow of data and its operations.

5. Solid logic level refers to logic 0 or 1. In terms of voltages, these logic levels are represented by a range of voltages. Tri-state level is not a solid logic 0 or 1, it can be any voltages depending on the circuit, refered as "high-impedance" or Z, It is basically disconnected, not high or low.



6. UART is asynchrous, doesn't use the clk, instead it uses baudrate. This is set by the transmit and receive devices to ensure synchronization. It uses start and stop bit to recognize data. For SPI, a clock line is used to synchronize data between master and slave. The master generates to clock, and controls when data transmits. It can also have multiple slaves to one master.

7. Bus contention is when multiple devices tries to add/control the same bus at the same time. This can lead to incorrect data and possible damages to the hardware. A tri-state buffer is used to solve this problem. It acts like a switch for devices, it can tap in or tap out of the bus. This makes sure only one device is using the bus at a time.

6. $V_{out} = V_{DD}(1 - e^{\frac{-t}{R_{pu}C_L}})$ $R_{pu} = 4.7K\Omega$ $V_{DD} = 3.3V$ $V_{IH} = 2.7$ $V_{IL} = 0.5$

$C_L = 15pF$

$t_{rise} = t_{2.7V} - t_{0.5V}$

$2.7V = 3.3V(1 - e^{\frac{-t}{4700\Omega(1.5\times10^{-11})F}})$

$t_{2.7} = 1.20\times10^{-7}s$

$t_{rise} = 1.20\times10^{-7}s - 1.16\times10^{-8}s$

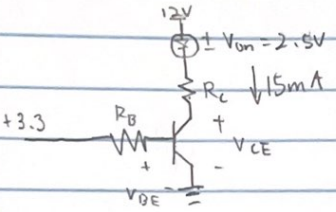
$0.5V = 3.3V(1 - e^{\frac{-t}{4700\Omega(1.5\times10^{-11})F}})$

$t_{rise} = 1.084\times10^{-7}s$

$= 108\ nS$

$t_{0.5} = 1.16\times10^{-8}s$

9.



$V_{BEON} = 0.7V$ $V_{CESAT} = 0.3V$ overdrive = 10

$B = 30$

$0.015A = \frac{12V - 2.5V - 0.3V}{R_C}$

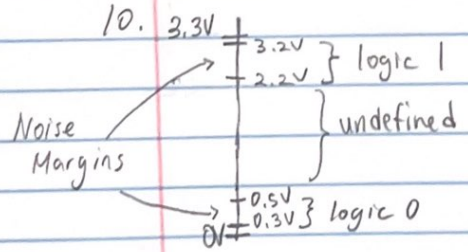
$R_C = 613.33\Omega$

$R_B = \frac{3.3V - 0.7V}{0.005A} = 520\Omega$

$I_{B(EOS)} = \frac{0.015A}{30} = 0.0005A$

$I_B = 10(0.005A) = 0.005A$

10.



$N_{MH} = 3.2V - 2.2V = 1V$

$N_{ML} = 0.5V - 0.3V = 0.2V$

Noise margins are important because it gives a range of voltage to define logic 0 or 1. It doesn't need a specific voltage, which would be hard to do. This compensates for noise in signals, slight distortion can still be defined correctly.