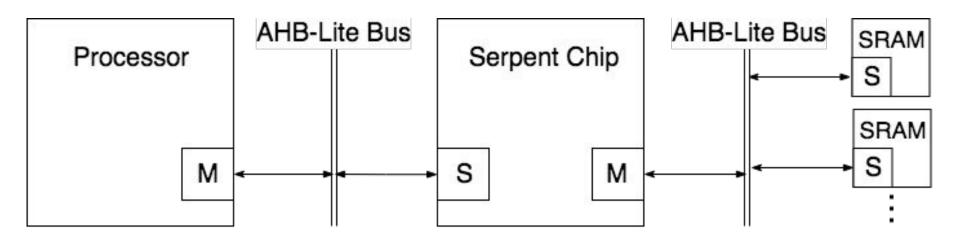
Automatic Encryption: Serpent (AES)

James Weber Spencer Deak John Kansky

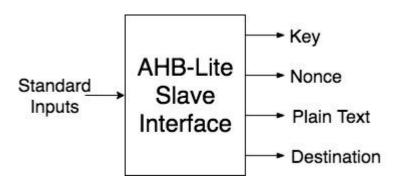
Overview



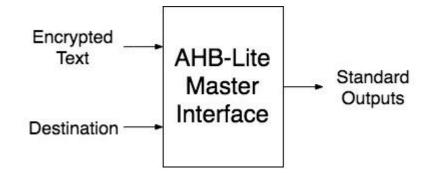
- AHB-Lite I/O for fast, pipelined data transfer.
- Serpent encryption, designed for secure, efficient hardware implementations

System Design: AHB Lite

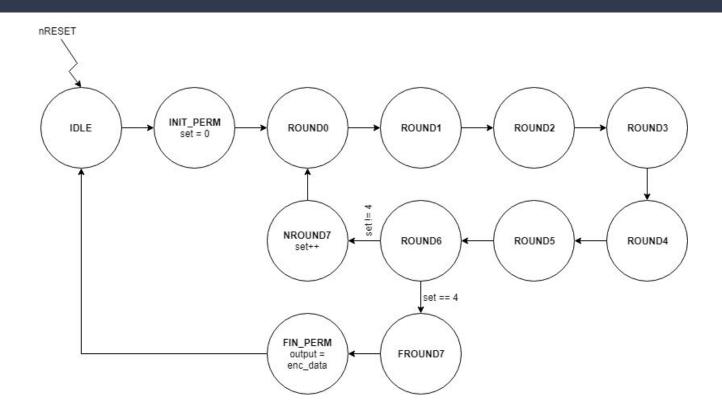
Slave



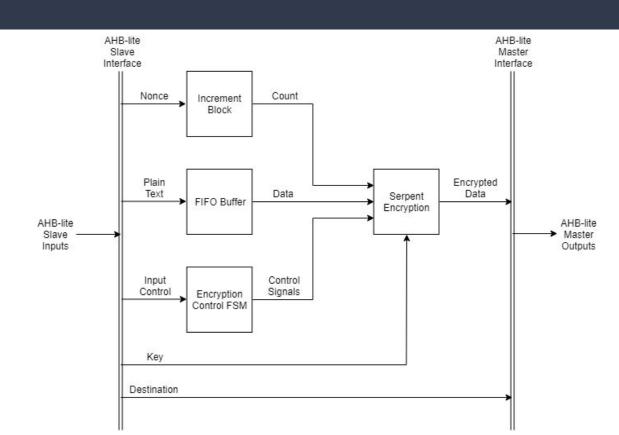
Master



System Design: Encryption



System Design: Integration

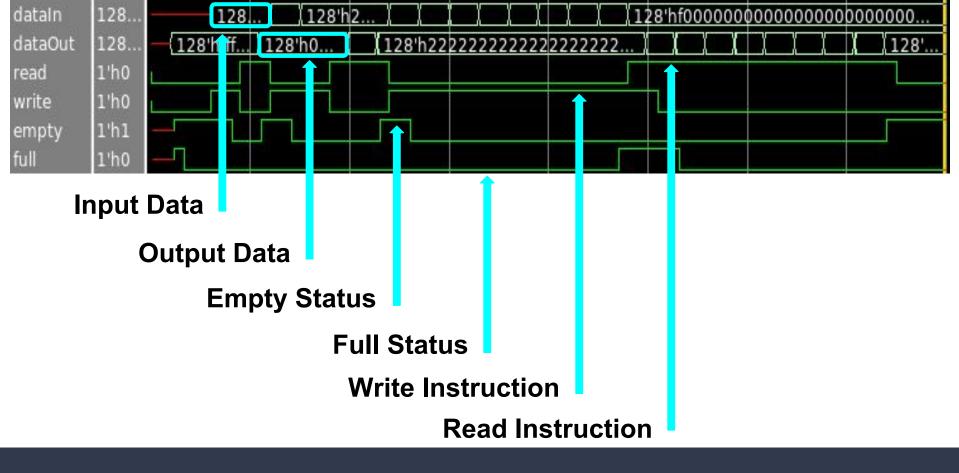


Success Criteria and Results

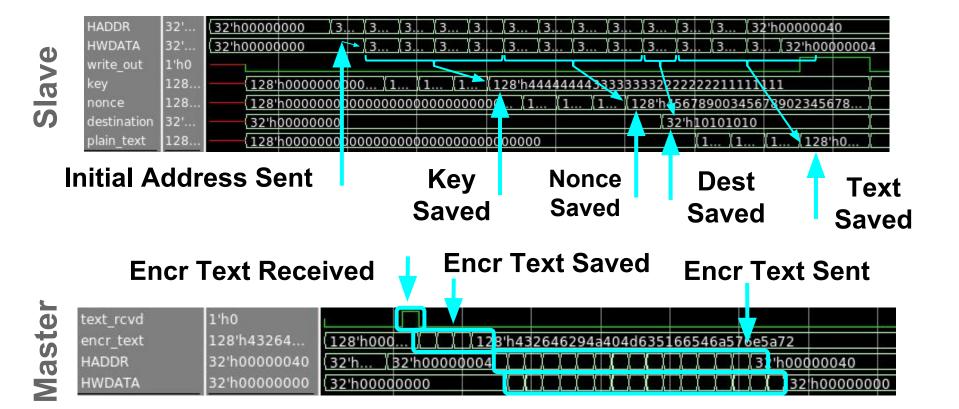
Test Benches	All top level modules have test benches that adequately demonstrate the functionality of the module in both source and mapped situations.
Proper Synthesis	All modules compile and synthesize without error, do not generate latches, and do not raise any warnings.
Source and Mapped	All modules operate as intended in source, and generate proper netlists in mapped versions that do not yield timing errors.
IC Layout	A complete IC layout has been generated that contains valid geometry and connectivity.

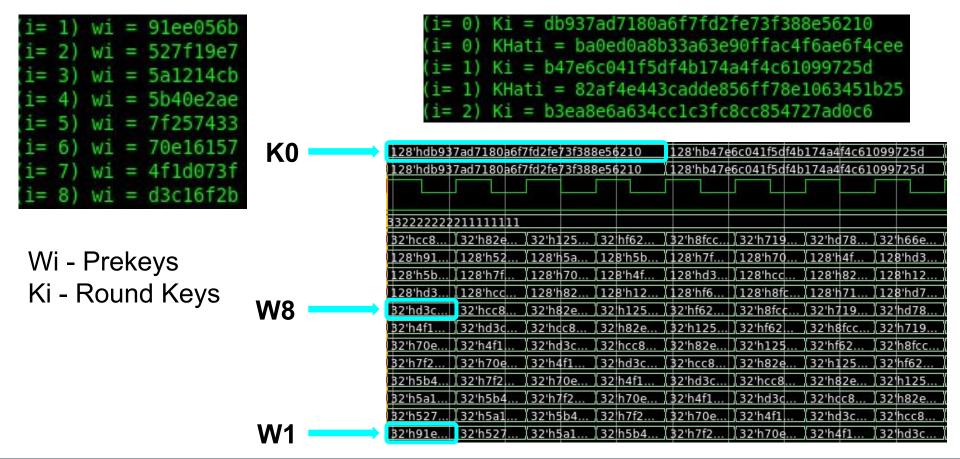
Success Criteria and Results

Successful Encryption	Encrypts and decrypts data, but does not adhere to Serpent-1 standard.
AHB-Lite Master	Correctly transfers data from the encryption module to the SRAM as specified by standard protocol.
AHB-Lite Slave	Adequately passes data from the processor to the FIFO buffer while following AHB-List standards.
FIFO Buffer Operation	Enqueues and dequeues data in one clock cycle for fast data storage and retrieval by the chip.
Round Key Generation	Successfully generates 33 unique round keys for one encryption in compliance with Serpent.

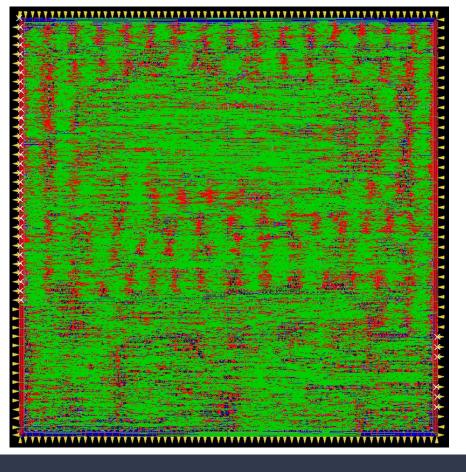


Specific Criteria: FIFO Buffer





Specific Criteria: Encryption Round Keys



Design Area: 4,610 μm x 4,610 μm

21,252,100 μm²

Layout Critical Path: 9.58 ns CLK -> CLK

Synthesis Critical Path: 4.66 ns CLK -> HWRITE

Estimated Critical Path: 2.40 ns R_STA -> R_STA

Conclusion

- Serpent is worthwhile and secure cipher, but documentation is somewhat scarce.
- Break AHB interfaces into smaller modules to avoid monolithic debugging.
- More efficient S-box implementation can reduce the chip area by a significant factor.