

# Jameson Thies

San Diego, CA  
jamesonthies@gmail.com

## EDUCATION

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### **Bachelor of Science in Computer Engineering**

August 2014 - May 2018

San Diego State University

Overall GPA: 3.62

Major GPA: 3.81

## EXPERIENCE

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### **San Diego State University Research Foundation**

*Research Assistant*

June 2017 - Present

- As a Research Assistant in SDSU's VLSI Design and Test Laboratory, I am researching efficient FPGA and ASIC data processing for applications including Brain Computer Interfaces through funding from the Center for Sensorimotor Neural Engineering and the SDSU Summer Undergraduate Research Program

### **Cognuse Inc.**

*Software Engineering Intern*

May 2016 – September 2016

- Developed React/Redux application interfaces that adapt to a range of API responses creating modular, adaptable applications which allow for accurate patient diagnoses, and responsive user interactions

## SKILLS & INTEREST

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**Skills:** C, C++, Python, MATLAB, Verilog, VHDL, JavaScript, C#, R

**Interest:** Parallel Computing, Data Science, VLSI Design, Embedded Systems Programming

## PROJECTS

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### **ASIC Compression for Brain Computer Interfaces**

- Investigating the feasibility of low power integrated circuit implementations of undercomplete autoencoders for compression of neural spikes
- Funded by the Center for Sensorimotor Neural Engineering

### **Reconfigurable FPGA Based Discrete Cosine Transform Architectures**

- Created a fully reconfigurable RTL design for the high throughput computation of Fast DCT algorithms of various lengths
- Used MATLAB for fixed-point simulations and Verilog for hardware description
- Presented at 2018 SDSU Research Symposium

### **FPGA MIDI Synthesizer**

- Worked as Project Manager with four other electrical and computer engineers in the design and implementation of a MIDI Synthesizer based on a Spartan 6 FPGA with a mobile Bluetooth interface
- Presented at Fall 2017 Senior Design Day