Jameson Thies

jamesonthies@gmail.com Davis, CA

EDUCATION

Master of Science in Electrical and Computer Engineering

September 2018 - Present

University of California, Davis

Bachelor of Science in Computer Engineering

San Diego State University

Cum Laude

August 2014 - May 2018

EXPERIENCE

San Diego State University Research Foundation

June 2017 – October 2018

Undergraduate Research Assistant

Researched into efficient digital circuit processing for brain-computer interfaces through funding
from the Center for Sensorimotor Neural Engineering and the SDSU Summer Undergraduate
Research Program. Primary focuses include autoencoder based neural spike compression, and neural
network based spike classification. (Verilog, MATLAB, Machine Learning)

Cognuse Inc.

May 2016 – September 2016

Software Engineering Intern

 Developed React/Redux JavaScript applications that adapt to a range of REST API responses creating modular, adaptable applications which allow for accessible data presentation and responsive user interactions. (JavaScript, React, HTML/CSS, RESTful APIs)

SKILLS

- C, C++, Python, MATLAB, Verilog, Assembly, JavaScript, R, C#
- Embedded Systems Programming (C, Assembly), Digital Circuit Design and Testing (Verilog), Analog
 Circuit Design (SPICE), CI/CD (Git)

PROJECTS

Double Heart Rate Monitor

- Graduate level Embedded Computing System term project
- Built photodetector-based heartrate monitor with analog signal processing (Filters, Amplifiers) and microcontroller interface capable of separating two pulses in the voltage signal (C Programming)

Reconfigurable FPGA Based Discrete Cosine Transform Architectures

- Created a reconfigurable digital circuit design for the high throughput computation of Fast DCT algorithms using fixed-point simulations (MATLAB) and RTL hardware description (Verilog)
- Poster presentation at 2018 SDSU Research Symposium

FPGA MIDI Synthesizer

- Worked as Project Lead with team of electrical and computer engineering students in the design and implementation of a MIDI Synthesizer based on a Spartan 6 FPGA with a mobile Bluetooth interface. (Verilog, FPGA, PCB Design)
- Presented at San Diego State University Senior Design Day Fall 2017