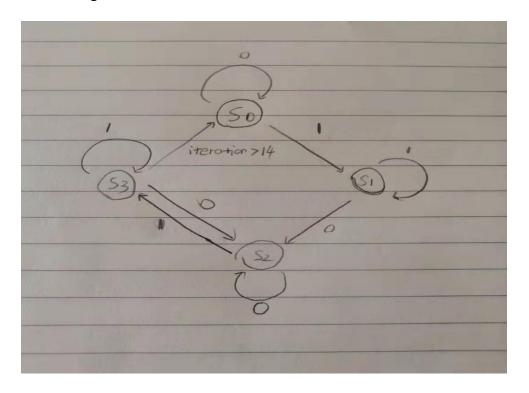
## LAB 7 notebook

## Jiajun, Guan

## a). Comments on the storing and moving text design:

For the 16 bit CORDIC computer, the design is used to calculate the cosine and sine value of a given value. It will take as input a 16-bit signed binary fixed point number, corresponding to an angle in the range 0 to  $\pi/2$ . There are two methods available. The first method is calculated in parallel. It require at least 16 full adders at the same time, as well as a large shift register which do not map well into an FPGA. We used the bit-serial design with 3 sets of shift registers, serial adder-subtractor and two input multiplexers. X and y are coupled wire 13 input multiplexers to the serial adder-subtractor in the other register datapath. Z is input to the third serial adder-subtractor along with the corresponding value in TAN\_ROM. In my program, the module cordic will be used to calculate the cosine and sine value given x0,y0,z0 in serial. Each time the cordic module will return a new value of x, and y, when the button is pressed, the new\_x and new\_y will be sent as the new input.

The top file will be in charge of the display and control. In my file, there are totally four states. The state diagram is shown as followed:



For the state S0, it is the initial state and do nothing. When pushed button is pressed, it entered state S1. For the S1, it will pass the initial value to the cordic module, in which x = 26dd, y = 0, z is read from the 16 switches. After passing the value, the state machine enter S2 until the user release the button. In S2, cordic module will execute the calculation and return a new value of the x, y,z. It will be passed to the module again when enter S3 by pressing the button. When release the button, the state will enter S2 again, and the iteration number increase by 1. If there is more than 14 iteration, the state will finally enter S0 and start from beginning.

B) RTL file and testbench file

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C) Constrain file		
D) 1.Utilization report		
2.Power report		
3.Timing report		

2. Testbench file

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F) Waveform analysis