James Root
Project 3 Report
ECE 6100
12 April 2023

Report Purpose

This Project was created to design a Tomasulo simulator, which utilizes the functionality of a Out of Order FOCO using PREGS/RAT. From this simulator system, our goal is to find the most optimal configuration (i.e., reduces size of simulator) that stays within the margin of defined sizes for the overall simulators and optimizes the instructions per cycle rate (i.e., stays within 90% of the highest possible IPC rate) of simulation between all trace files.

Simulation Parameters

The simulator parameters are as follows and are given the following restrictions:

- **A:** Number of ALU units (A = {1, 2, 3})
- **M:** Number of MUL units (M = {1, 2})
- **L:** Number of LSU units (L = {1, 2, 3})
- **S:** Number of reservation stations per FU (S = {2, 4, 8})
- **P:** Number of P-regs (32 + P total regs) (P = {64, 96, 128})
- **F:** Fetch width of the simulator (F = {2, 4, 8})

For more information on these parameters, please consult the project3_v1_2.pdf document included in submission.

Experiment Overview

In order to find an optimal configuration that minimizes unit usage and maximizes IPC, every possible configuration of A, M, L, S, P, and F are iterated over for each of the 4 trace files given. Using different traces allows for a greater diversity of simulator to be seen and better represents how a simulator would operate in a system with multiple programs running. We use the following trace files to simulate:

1. bfs_2_15_full.trace
2. cachesim_gcc_full.trace
3. perceptron_gcc_full.trace
4. tiledmm_full.trace

The configurations defined in **Simulation Parameters** are simulated over a bash script and merged into a csv file, which with the help of Microsoft Excel creates the following visualizations and conclusions.

A	M	L	S	P	F	Sum	bfs_ rank	perc_ rank	cache _rank	tiled_ rank	avg_ipc	rank	avg_top_90
3	2	3	8	128	8	152	4	2	2	2	1.66066394	1	TRUE
3	2	3	8	96	8	120	3	1	1	1	1.66066394	2	TRUE
3	1	3	8	128	8	151	2	3	3	3	1.66059261	3	TRUE
3	1	3	8	96	8	119	1	4	4	4	1.66059092	4	TRUE
3	2	3	4	128	8	148	6	8	8	8	1.66015436	5	TRUE

3	2	3	4	96	8	116	5	7	7	7	1.66015436	6	TRUE
3	1	3	4	128	8	147	8	11	11	11	1.6599849	7	TRUE
3	1	3	4	96	8	115	7	10	10	10	1.6599849	8	TRUE
3	2	3	8	64	8	88	11	6	6	6	1.65941337	9	TRUE

Chart 1: Top 9 performing configurations for harmonic mean IPC over the 4 provided traces.

In *Chart 1*, we see that the highest performing configurations are generally of the larger size. The overall performing config is the largest possible config, with the sum of item numbers being 152. Next, we will look for configs that minimize this sizing and are in the bottom range of the top 90%.

A	M	L	S	P	F	Sum	bfs_rank	perc_rank	cache_rank	tiled_rank	avg_ipc	rank	Avg_top_90
3	1	2	2	64	4	76	72	72	195	141	1.59861302	72	TRUE
2	1	3	2	64	4	76	108	108	105	84	1.55979818	108	TRUE
2	2	2	2	64	4	76	130	172	202	121	1.52953929	138	TRUE
3	2	3	2	64	2	76	159	195	45	159	1.51990714	159	TRUE
2	1	3	4	64	2	76	174	228	90	174	1.5151006	174	TRUE
2	1	2	2	64	4	75	136	178	229	142	1.52315255	144	TRUE
3	1	3	2	64	2	75	162	198	54	162	1.51938899	162	TRUE
2	2	3	2	64	2	75	177	231	99	177	1.51319409	177	TRUE
2	1	3	2	64	2	74	178	232	106	178	1.50985946	180	TRUE

Chart 2: bottom 9 sized configurations performing in the top 90% of configs.

In Chart 2, we find the smallest configurations (denoted by the sum category, finding a combination of the A, M, L, S, P, and F parameters) which satisfy having an avg_ipc within the top IPC seen in Chart 1. It is worth noting that the top config, (3, 1, 2, 2, 64, 4) has the highest avg_ipc for any simulator that has a sum of 76 (there are no other sum=76 in the dataset). This configuration is the only config featured that has each trace IPC within 90% of the highest IPC for each trace. **All other configs are not within 90% for bfs and perceptron.**

Using the sum of parameter values was determined to be the most straightforward method to determine size of a simulator. It is worth noting the distinct differences in the values and how they may impact a physical system.

- **A, M, and L** all impact the number of function. units in the execute stage. This may lead to higher power consumption as the number of units increase due to density of units.
    - **These items and S** Determine the size of the scheduling queue, which may impact power density as it allows for more units to hold data in the schedule phase.
- **P** impacts the power dissipation of the dispatch and state update phases.
- **F** impacts the fetch phase mostly, allowing for more instructions to be fetched in one cycle. This may also impact power dissipation.

In general, these units do not line up 1:1 with each other in terms of power dissipation. an ALU unit could provide more power consumption than a MUL does. Without knowing these exact values of the system, it was determined using a simple sum to be the best decision for minimal size.

From this consideration on sum of parameters and the information seen in *chart 2*, The most optimal configuration is determined to be **A=3, M=1, L=2, S=2, F=4, P=64** (the top entry of the chart). This configuration has only 2 units more than the smallest passing configuration and passes the 90% test for each configuration – allowing for better performance on a system that may see a more evenly distributed workload. There is a boost in average IPC of ~0.1 from this system to the smallest system, a noticeable increase for the addition of only 2 units.