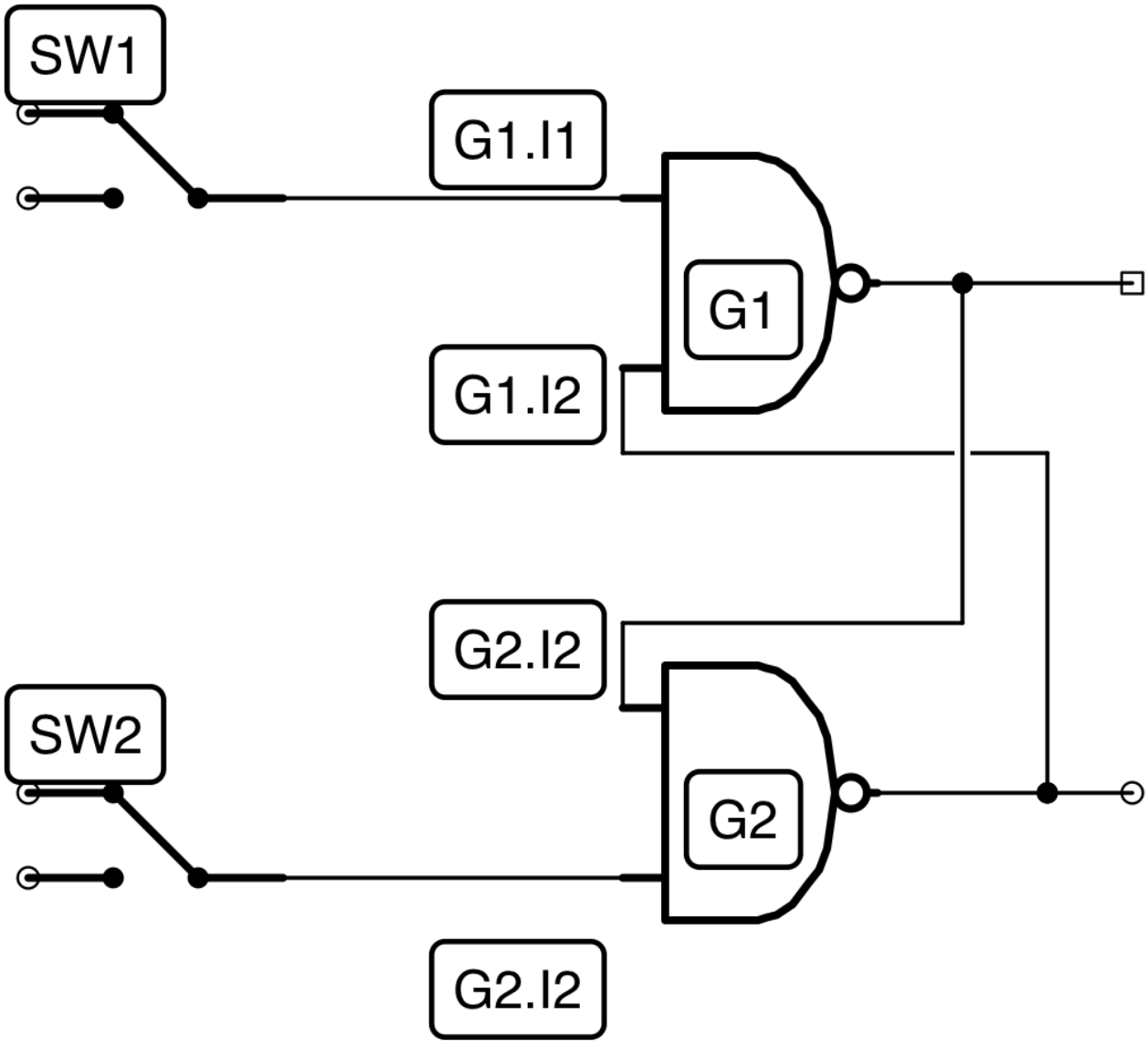
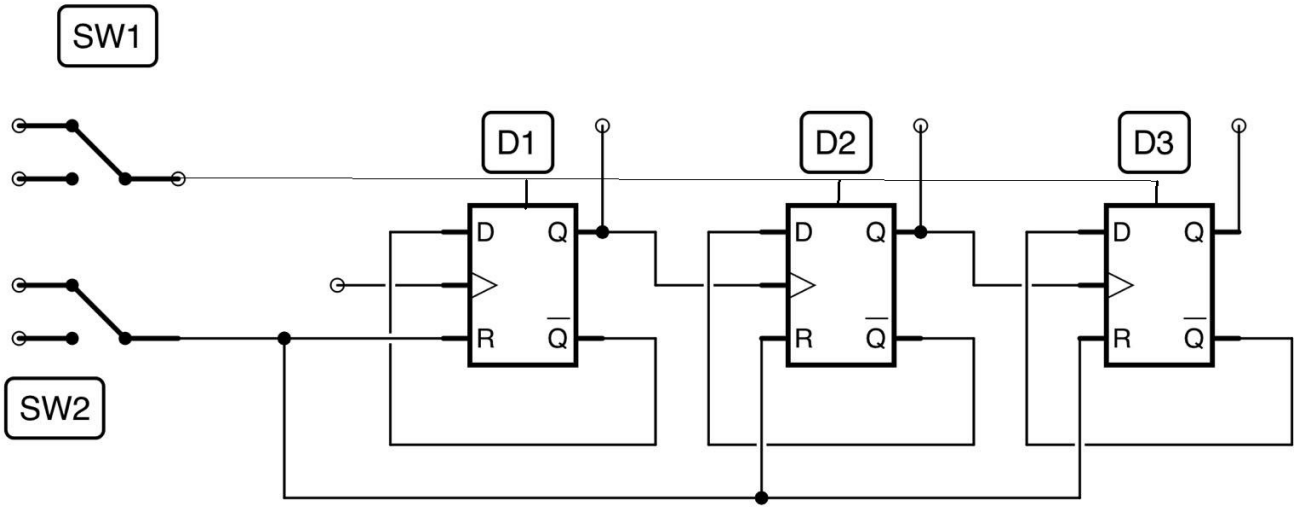
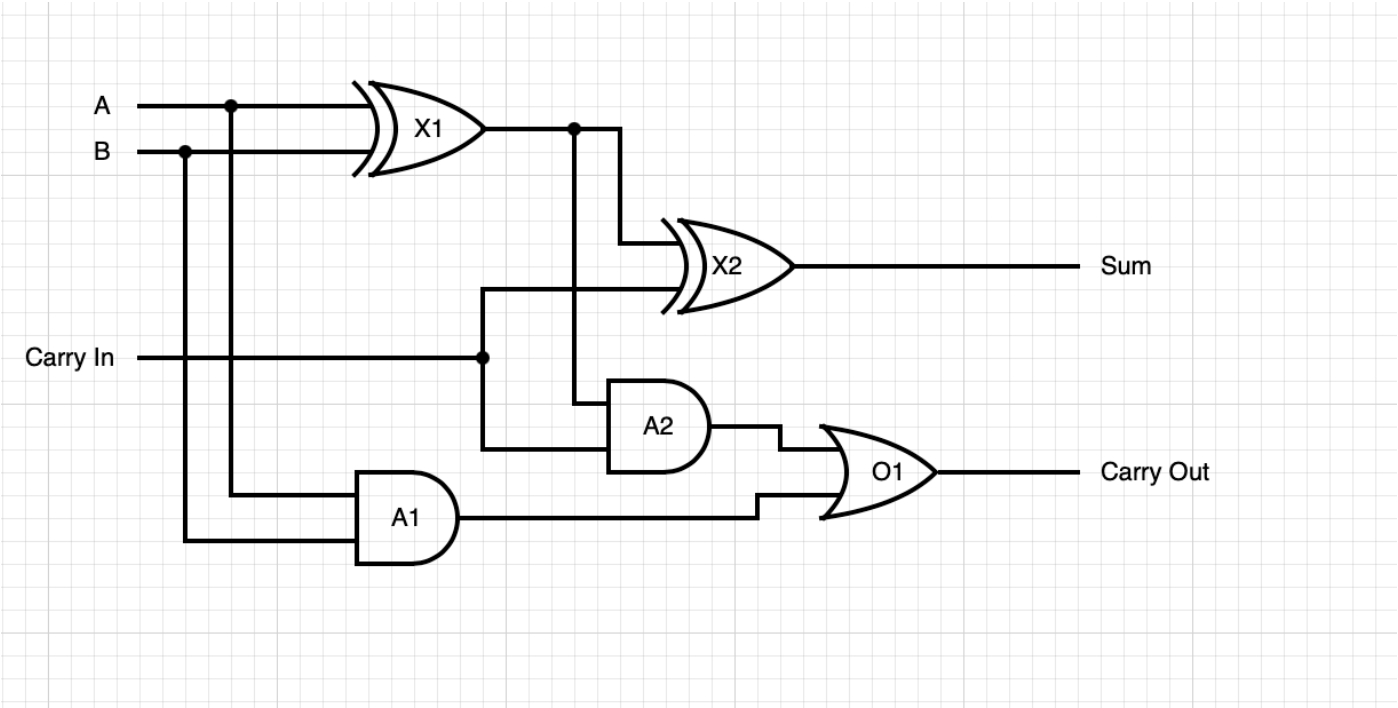
```
define G1 G2 as NAND 2 inputs;
define SW1 SW2 as SWITCH 0 state;
connect SW1 to G1.I1;
connect SW2 to G2.I2;
connect G1 to G2.I1;
connect G2 to G1.I2;
monitor G1 G2;
END
```


SW1
G1.I1
G1
G1.I2
G2.I2
SW2
G2
G2.I2

```
define CL1 as CLOCK period 2;
define SW1 as SWITCH 0 state;
define SW2 as SWITCH 0 state;
define D1 D2 D3 as DTYPE;
connect SW1 to D1.SET;
connect SW2 to D1.CLEAR;
connect SW1 to D2.SET;
connect SW2 to D2.CLEAR;
connect SW1 to D3.SET;
connect SW2 to D3.CLEAR;
connect CL1 to D1.CLK;
connect D1.Q to D2.CLK;
connect D2.Q to D3.CLK;
connect D1.QBAR to D1.DATA;
connect D2.QBAR to D2.DATA;
connect D3.QBAR to D3.DATA;
monitor D1.Q D2.Q D3.Q;
END
```


SW1
SW2
D1
D2
D3
D
Q
R
Q

```
define X1 X2 as XOR;
define A1 A2 as AND 2 inputs;
define O1 as OR 2 inputs;
define A B Ci as SWITCH 0 state;
connect A to X1.I1;
connect B to X1.I2;
connect Ci to X2.I1;
connect X1 to X2.I2;
connect A to A1.I1;
connect B to A1.I2;
connect Ci to A2.I1;
connect X1 to A2.I2;
connect A1 to O1.I1;
connect A2 to O1.I2;
monitor X2 O1;
END
```


A
B
X1
X2
Sum
Carry In
A2
O1
Carry Out
A1