Lab Report 4 by Jamie O'Brien, Sabrina Pereira, and Shyheim Russell

1 Introduction

In this lab, we familiarized ourselves with nMOS and pMOS transistors. We collected data using a source-measurement unit (SMU) which allows us to analyze charcteristics of channel current when we sweep gate voltage, source voltage, or drain voltage for both types of transistors.

2 Experiment 1: Gate Characteristics

In this experiment, we used an ALD1106 nMOS transistor array and an ALD1107 pMOS transistor array containing four individual transistors. To capture the gate characteristics of the nMOS transistor, we measured channel current as a function of gate voltage, V_G, with the source voltage, V_S, at ground and the drain voltage, V_D at 5V to guarantee that the transistor remains in saturation. For the pMOS gate characteristics, the set up was similar, except the source voltage was set to 5V and the drain voltage to ground.

We fit the EKV model to each of these current-voltage characteristics using the provided EKVFIT matlab function, extracting a values of I_s, κ, and V_{T0} to create our theoretical fits. The EKV model for current is $I_s * log^2(1 + e^{(\kappa(V_G - V_{T0}) - V_S)/2U_T})$ which we used to extract the listed parameters, as seen in the following table.

	nMOS	pMOS
I_s	$1.9013e^{-06}$	$4.2283e^{-06}$
κ	0.6974	-0.6833
V_{T0}	0.5472	4.2735

To assess our data, we plotted it alongside our theoretical fits, as seen in Figure 1. The EKV model fits our experimental data very well, with the exception of small divergence between the nMOS data and nMOS EKV when reaching high gate voltages.

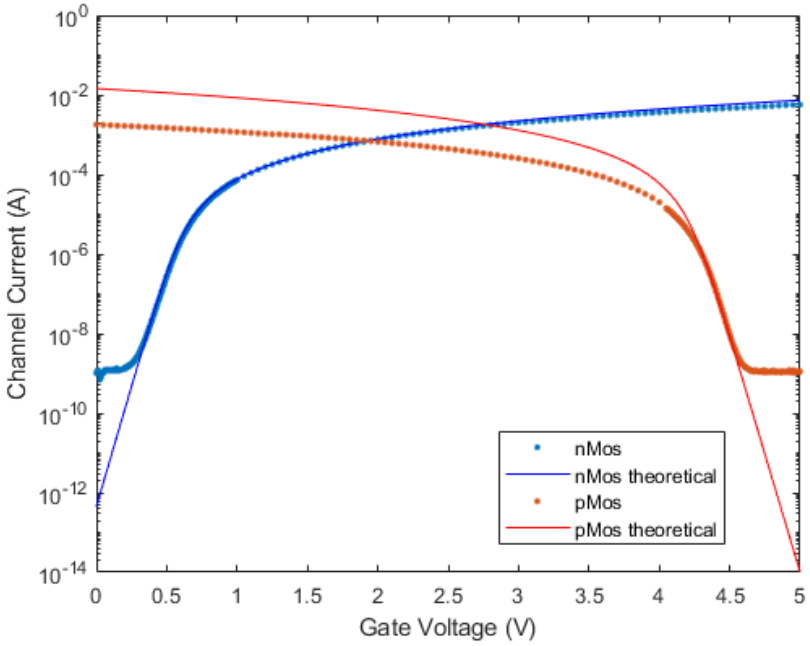

Figure 1: nMOS and pMOS Channel Current Vs. Gate voltage

We then extracted the incremental transconductance gain, g_m of each transistor using the `diff` operator in Matlab to find $g_m = \frac{\delta I_{sat}}{\delta V_G}$. We used the equation $g_s = \frac{\kappa I_{sat}}{U_T}$ for the theoretical line fit for the weak inversion section, and the equation $g_s = \frac{\kappa\sqrt{I_s I_{sat}}}{U_T}$.

As can be seen in Figure 2, our fits for the weak and strong inversion regions fit very closely for their respective regions, especially well for the nMOS data. The theoretical fits for the pMOS data are set a little higher than what we observed.

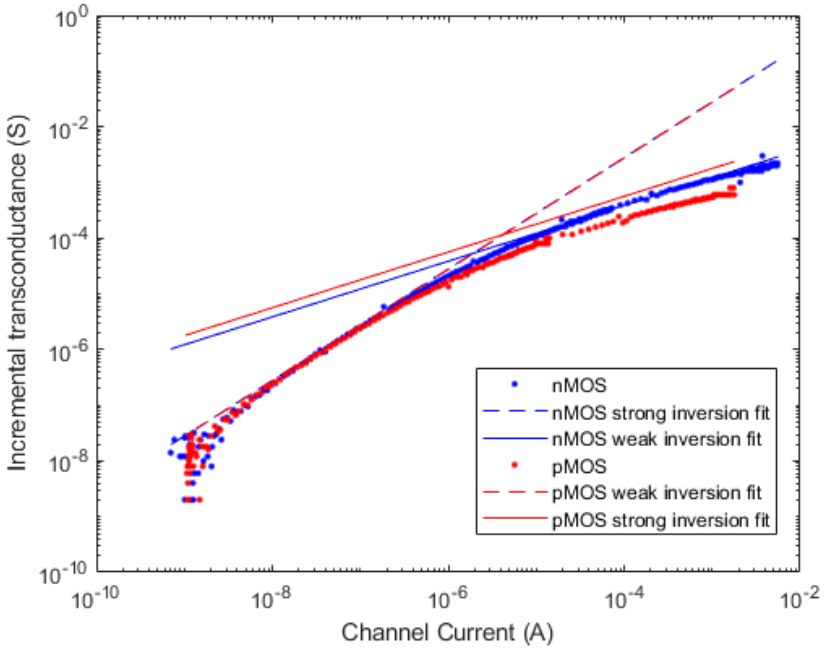

Figure 2: nMOS and pMOS Incremental Transconductance Gain Vs. Channel Current

3 Experiment 2: Source Characteristics

In this experiment, for the nMOS transistor, we measured channel current as a function of source voltage with the gate and drain voltages both set at 5V. For the pMOS transistor we set the gate and drain voltages at ground. The slopes of the line of the weak inversion regions we fit were $m = 21.50$ Mhos for the nMOS graph and $m = 25.48$ Mhos for the pMOS graph. Using the EKV model for weak inversion equation $I_s e^{(\kappa(V_{BG}-V_{T0})-V_{BS})/U_T}$, the theoretical slopes of the exponential in this region would be κ/U_T, or $m = 27.90$ Mhos for the nMOS graph and $m = -27.33$ Mhos for the pMOS graph. These characteristics look very similar to those obtained in Experiment 1, and the overall same shape and trend of the lines are observed in both.

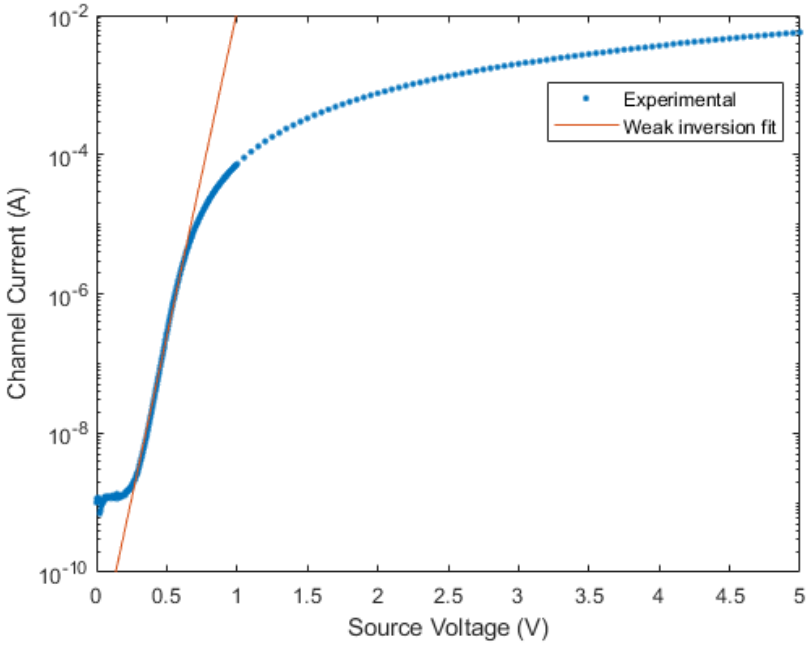

Figure 3: nMOS Channel Current Vs. Source voltage

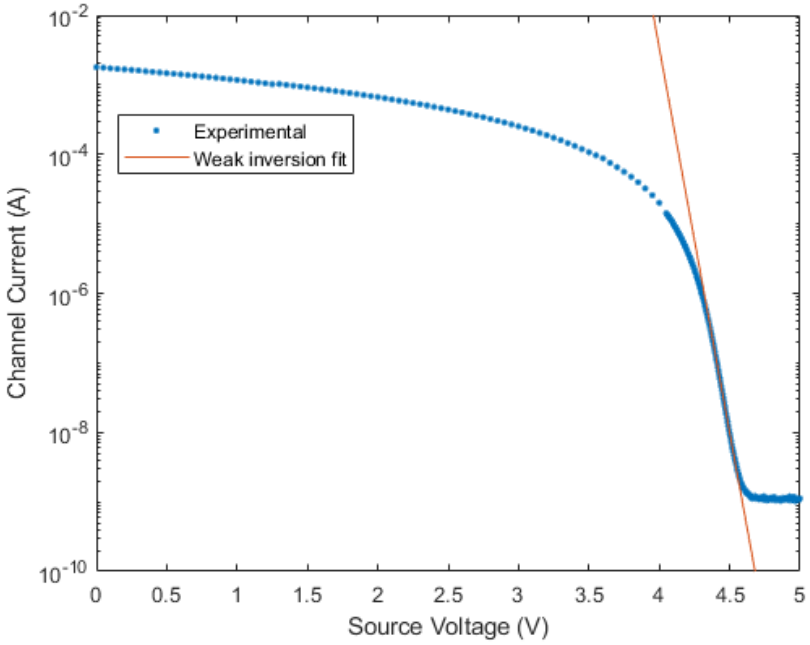

Figure 4: pMOS Channel Current Vs. Source voltage

We then extracted the source transconductance, g_s, from the the data we collected using $g_s = \frac{\delta - I_{sat}}{\delta V_s}$. We used the equation $g_s = \frac{I_{sat}}{U_T}$ for the theoretical line fit for the weak inversion section, and the equation $g_s = \frac{\sqrt{I_s I_{sat}}}{U_T}$.

Seen in Figure 5, our fits for the weak and strong inversion regions fit very closely

for their respective regions. Similarly to the fits for g_m, they are especially good for the nMOS data, while the theoretical fits for the pMOS data are set a little higher than what we observed.

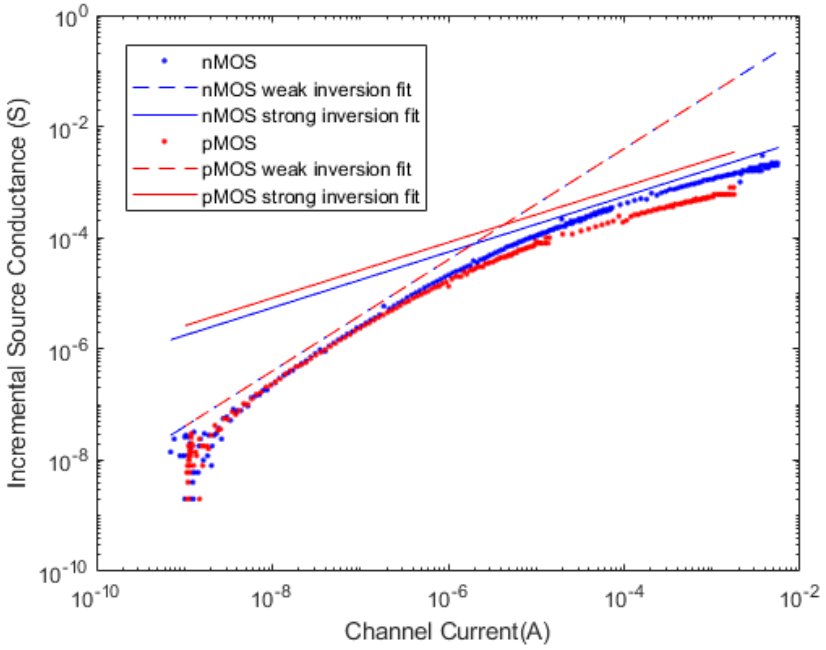

Figure 5: nMOS and pMOS Source Transconductance Vs. Channel Current

4 Experiment 3: Drain Characteristics

In this experiment, we measured channel current and swept drain voltage for three different gate voltage values which are shown in the following table.

Gate Voltage Values	
nMOS	pMOS
$500mV$	$0V$
$600mV$	$4400mV$
$5V$	$4550mV$

The results of these sweeps are shown in Figures 6 and 7. From these fits, we extracted the Early voltage, V_A, the saturation current, I_{sat}, and the intrinsic gain, $g_s r_o$, as can be seen in the following table.. If we were to fit lines to the drain characteristics, the y-intercept would be I_{sat} and the x-intercept would be V_A. To find the intrinsic gain, we found that if the same fit has a slope m, then $r_o = \frac{1}{m}$ and that $g_s = \frac{\sqrt{I_s I_{sat}}}{U_T}(1 - e^{-\sqrt{I_{sat}/I_s}})$. In Figure 8 we plotted Early voltage as a function of saturation current, and in Figure 9 we plotted intrinsic gain as a function of saturation current.

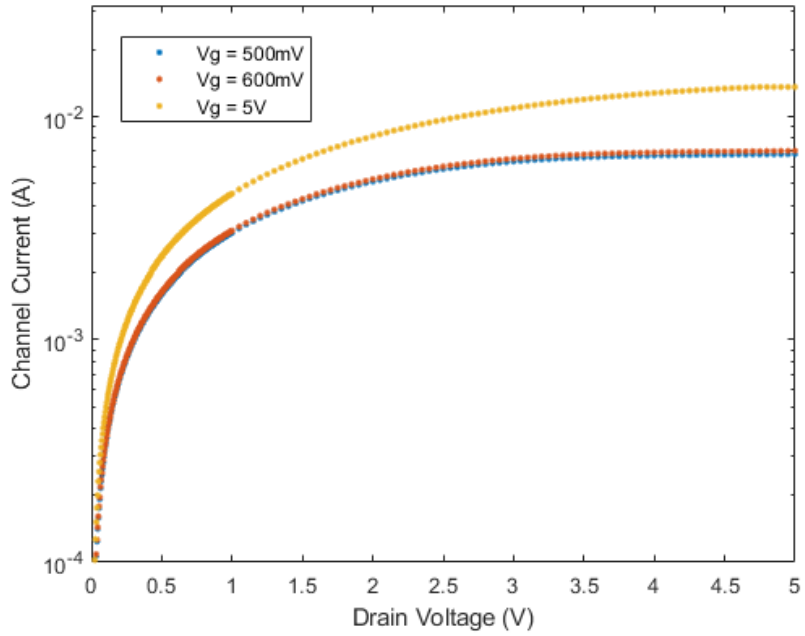

Figure 6: nMOS Channel Current Vs. Drain Voltage

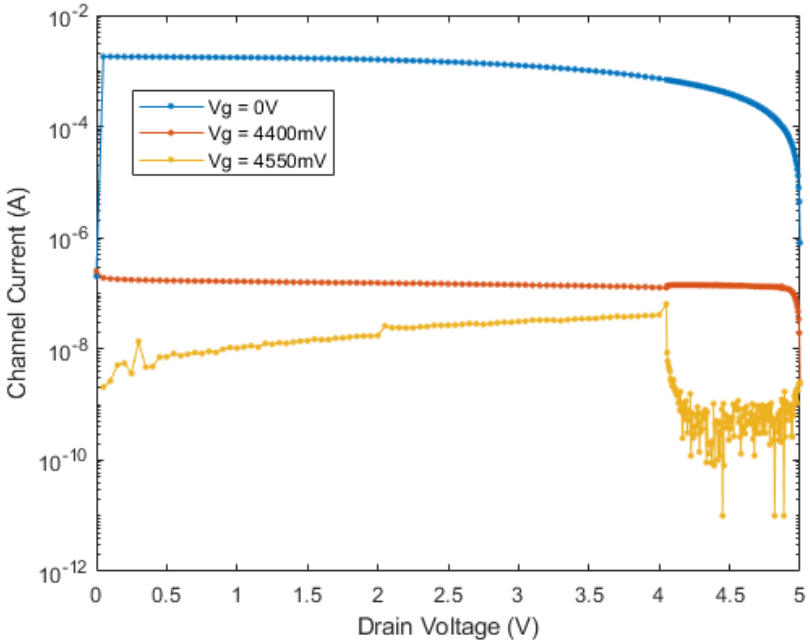

Figure 7: pMOS Channel Current Vs. Drain Voltage - the $V_g = 4550mV$ negative line was graphed in order to fit on the graph

The data gathered from the pMOS in weak inversion were negative currents, and were not nearly as clean or clear of data as in the strong and moderate inversion cases.

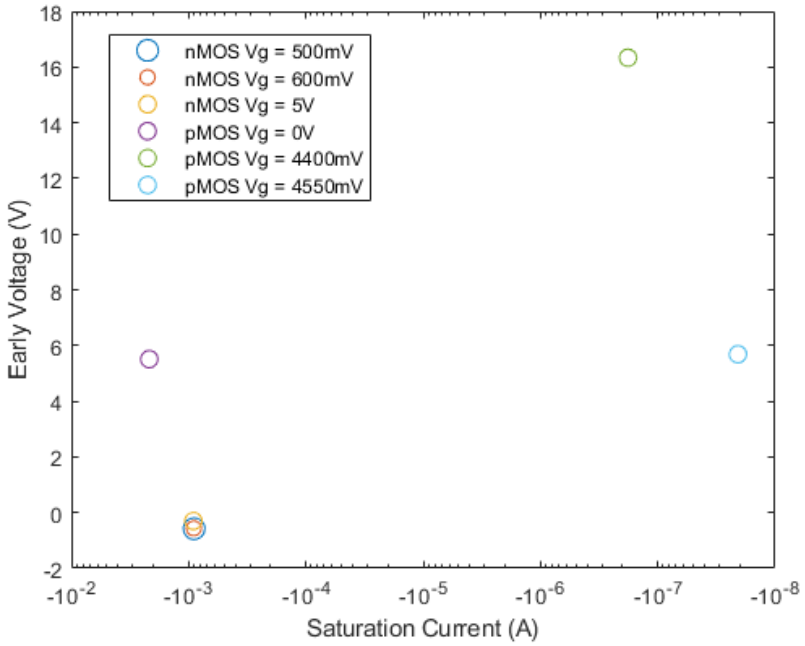

Figure 8: Early Voltage Vs. Saturation Current

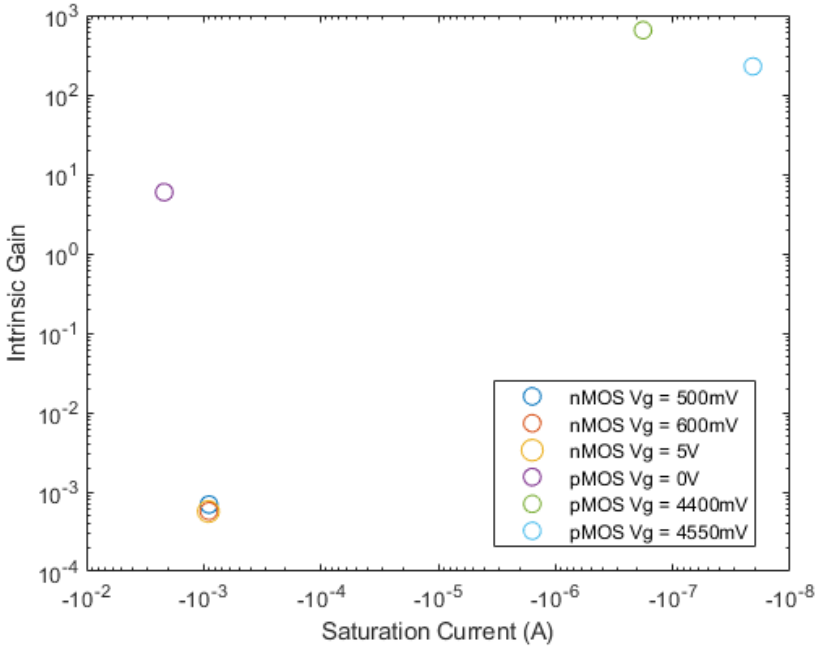

Figure 9: Intrinsic Gain Vs. Saturation Current