Lab Report 7 by Jamie O'Brien, Sabrina Pereira, and Shyheim Russell

1 Introduction

The purpose of this lab is to measure current-voltage characteristics of the differential pair across several values of common-mode input voltage. The characteristics are measured as a function of the bias current level. We also assessed the behavior of the common-source node voltage. We used an ALD1106 quad nMOS transistor array, and we used a source-measurement unit (SMU) to supply and measure current and voltage.

2 Experiment 1: Differential Pair Current Voltage Characteristics

In this Experiment, we began by constructing a differential-pair circuit using three nMOS transistors. To measure the circuit behavior at or slightly below bias, we set the bias voltage, V_b, to $0.65V$ such that the bias current, I_b, would be between $100nA$ and $1\mu A$. We then set the value for the voltage for the second transistor, $V2$, to $3V$ to begin with. We then took measurements of $I1$, $I2$, $I1 - I2$, $I1 + I2$, and V. We then took all the measurements again with two different values of $V2$, $2V$ and $4V$. The current measurements are shown in Figure 1, and the voltage measurements are shown in Figure 2.

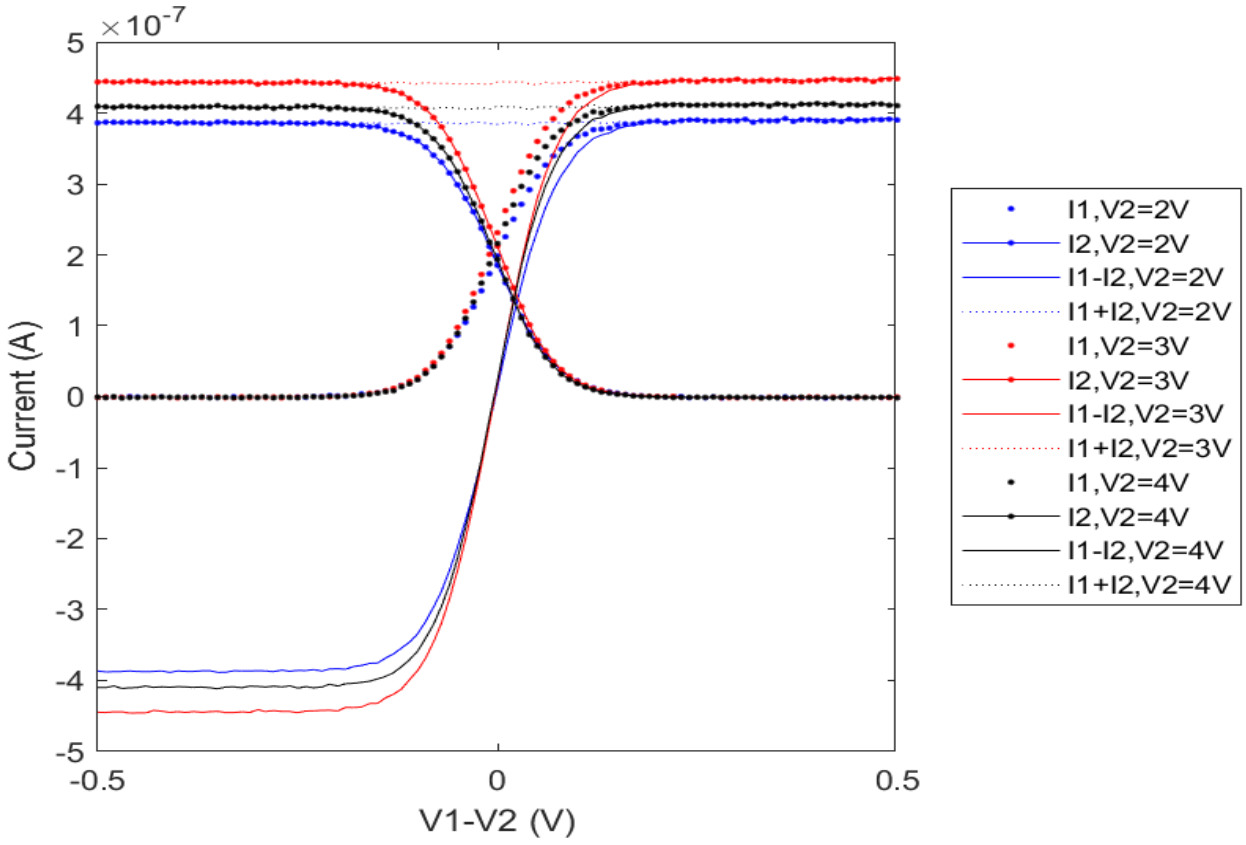

Figure 1: Current behavior of differential-pair measured at or slightly below bias.

As seen in Figure 1, the current-voltage characteristics do not change greatly as $V2$ changes. While there is some difference in exact values, the qualitative behavior remains the same. In Figure 2, the common-source node voltage, V, shows that as $V1 < V2$, V remains constant, and when $V1 > V2$, V increases steadily.

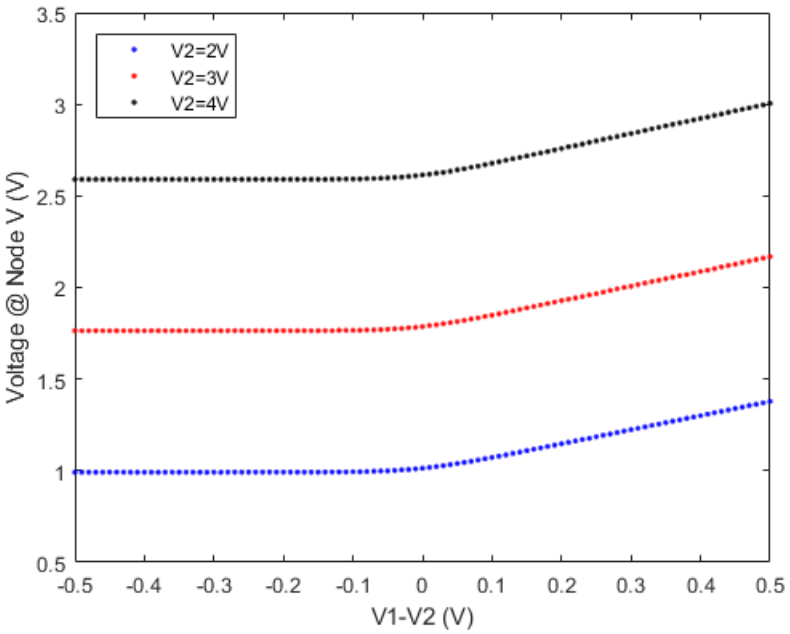

Figure 2: Voltage behavior of differential-pair measured at or slightly below bias.

We also included linear fits to $I1 - I2$ around $V1 - V2 = \ 0V$ in Figure 3. These lines fit the data well, and their slopes are actually the differential-node incremental transconductance gain, G_{dm}, which is given by

$$G_{dm} = \frac{\partial I_{dm}}{\partial V_{dm}}\Big|_{V_{dm}=0} = \frac{\partial(I_1-I_2)}{\partial(V_1-V_2)}\Big|_{V_1=V_2}$$

The values of G_{dm} for the various values of $V2$ do not differ gretaly, and are shown in the following table.

$V2$	G_{dm}
$2V$	$3.8293e^{-06}$
$3V$	$4.4728e^{-06}$
$4V$	$4.1856e^{-06}$

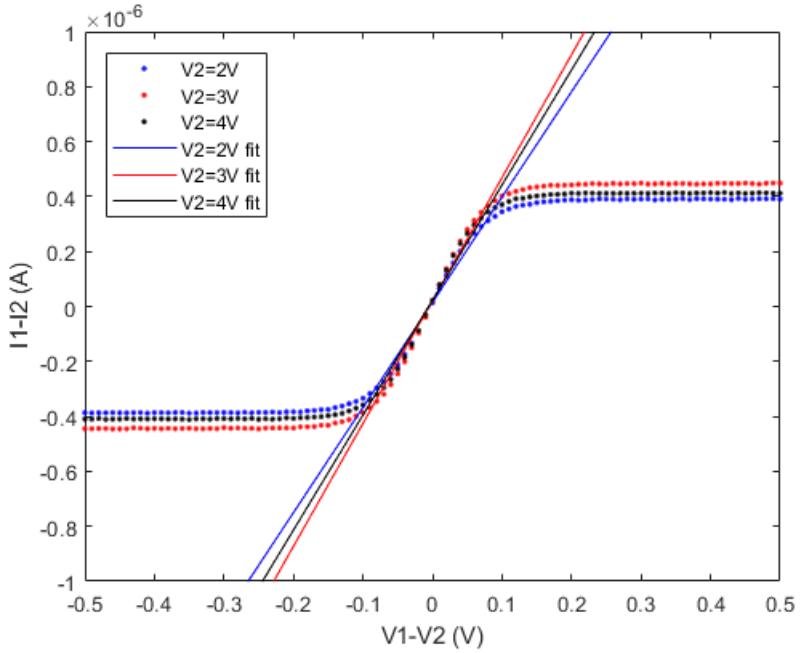

Figure 3: $I1 - I2$ and linear fits

Finally, using only a measurement of $V2 = 2V$, we repeated the same measurements again, but this time with $Vb = \ 1.5V$ to make $Ib = \ 100nA$ to measure the circuit behavior above bias. The current-voltage characteristics are shown in Figure 4, and the common-source node voltage measurements are shown in Figure 5.

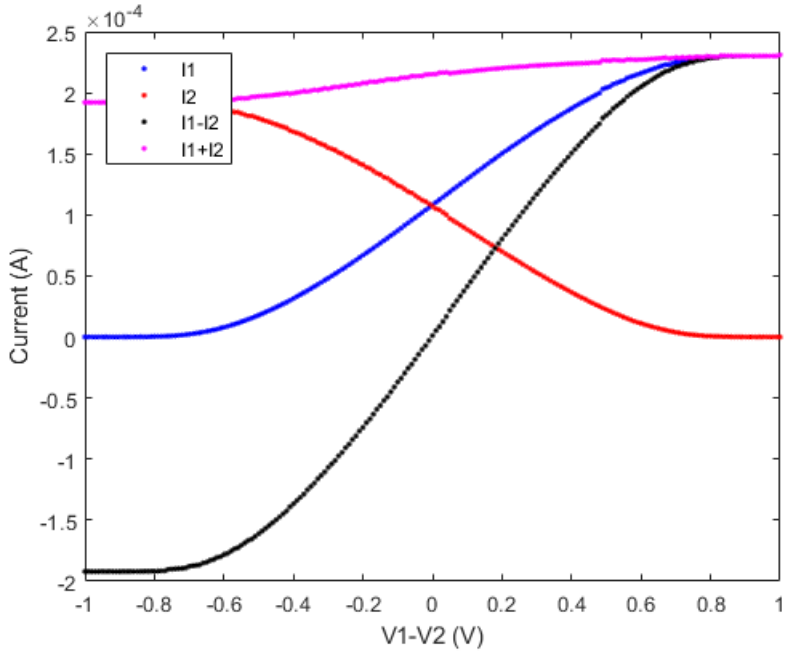

Figure 4: Above bias current behavior of differential-pair

As shown in Figure 4, the current values are larger than they were when the

circuit was operating below bias, though the qualitative behavior remains the same. Also, the values for $I1 + I2$ do not remains as steady as they did below bias, but instead increase a bit. This is probably due to the highest value of $I2$ being less than the highest value of $I1$. The affects both $I1 - I2$ and $I1 + I2$.

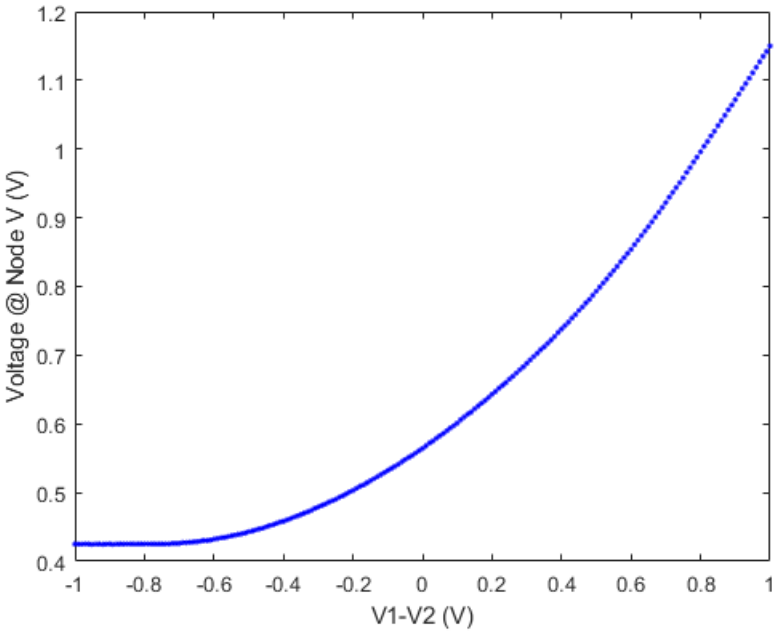

Figure 5: Above bias voltage behavior of differential-pair

As shown in Figure 5, the common-source node voltage V also behaves differently above bias than it did below bias. Above bias, it follow more of an exponential form, still increasing as $V1 - V2$ increases, but not linearly. This suggests that all around, the circuit may be less stable or precise above bias than it is below bias.

From our experimental results, we also see that as the bias current changes from weak or moderate inversion to strong inversion, the behavior of the circuit changes in that in strong inversion, there is softer non-linearity when looking at the $I1 - I2$ vs. $V1 - V2$ graphs. The qualitative behavior is very similar, but with a strong inversion bias current there is a wider linear range.