A MOSFET-Only Current-Output D/A Converter

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1 Introduction

In this project, we have simulated and analyzed a current-output digital-to-analog converter based on a MOS transistor only R-2R ladder network. To do this, we looked deeper into understanding how a typical R-2R ladder network works through reviewing academic sources along with Postlab 6. From here, we set out to construct and to analyze the behavior of the circuit in LTspice using the nMOS components provided to us.

2 Overview on nMOS Transistor R-2R ladder network

The nMOS R-2R ladder network we investigate in this paper is shown in Figure 1. Each "unit" in the ladder consists of one nMOS transistor in series with two nMOS transistors in parallel. The two parallel transistors, when in saturation, act as a single nMOS transistor with twice the strength ration of the individual transistors. So effecitvely, each unit is an nMOS transistor in series with a second nMOS transistor with twice the strength ratio of the first. Additionally, the two parallel transistors act essentially as a resistive current divider using non-linear resistors. The accuracy of the current division depends solely on the matching of the VI-curves of the two transistors, not the linearity of the two components [1].

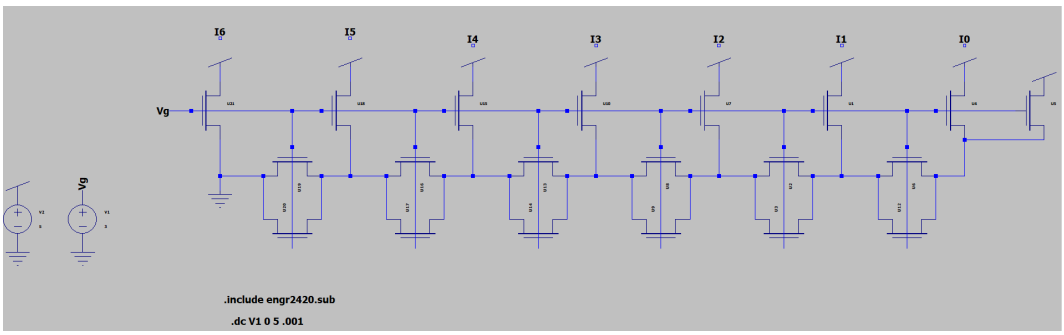

Figure 1: nMOS Transistor R-2R Ladder Circuit.

The branch of each unit with the two parallel transistors will split the current such that current flowing through the next channel equally, thus the current halves from each channel to the next. Following the indexing in Figure 1, where I_0 is the current channel closest to the ladder termination, the current in each branch can be modeled as

$$I_n = I_0 * 2^n \tag{1}$$

where I_n is the channel current through the nth single-transistor branch. When simulating the circuit from Figure 1 in LTSpice, we observed the data shown in Figure 2. As shown, Equation 1 holds true in strong inversion as well as in weak inversion, as the channel currents are half that of the previous, as long as the gate voltage allows the transistors to remain saturated.

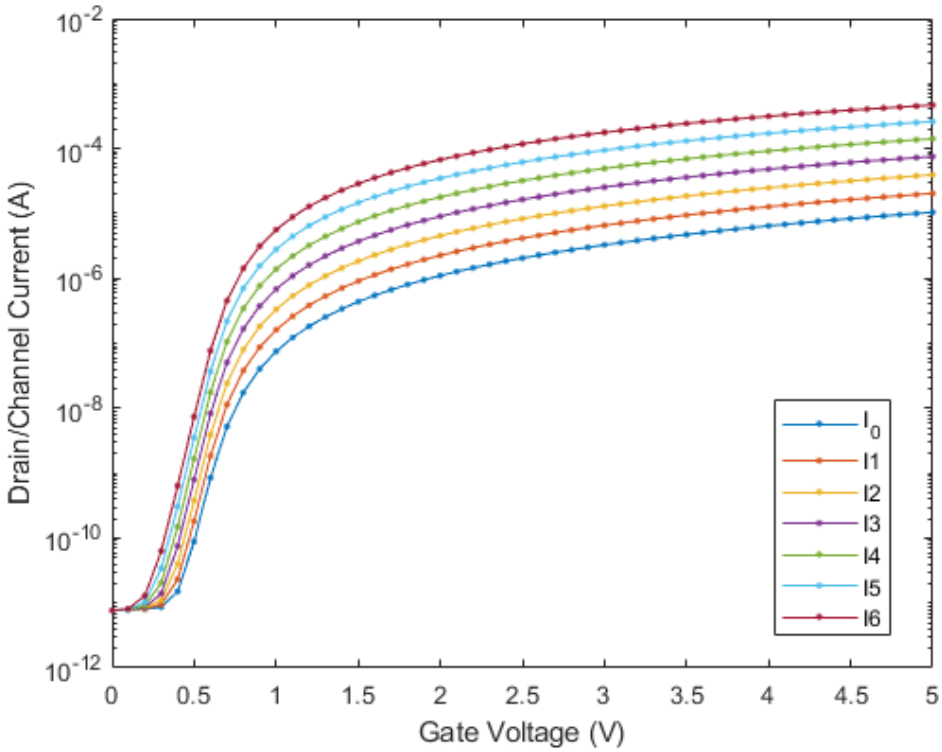

Figure 2: Channel currents I_n as a Function of Gate Voltage

To more directly compare the channel currents of each transistor, we selected a specific value for the gate voltage (V=3V) for which to plot these currents. As seen in Figure 3, the theoretical fit created based on Equation 1 closely maps the values collected from the simulation. While our simulation provided values that followed this slope almost perfectly for the transistors $n = 0$ to $n = 3$, the transistors afterwards do not follow the fit perfectly. It seems that the model works better for the transistors closer to the termination of the ladder than those furthest from it. We fit a line onto the data points themselves in order to find out about how much this circuit differs from the ideal power function of base 2. With the slope, we found that our data for this specific gate voltage overall fit a power function of a base of approximately 1.9. Given all this, we expect that these deviations from the ideal model will impact the ability of this circuit to be used as a digital to analog converter. Additionally, it has been found that some models of Spice approximate some of the calculations involved with this circuit, so this could have negatively affected the simulation accuracy if our model of LTSpice used those approximations [1].

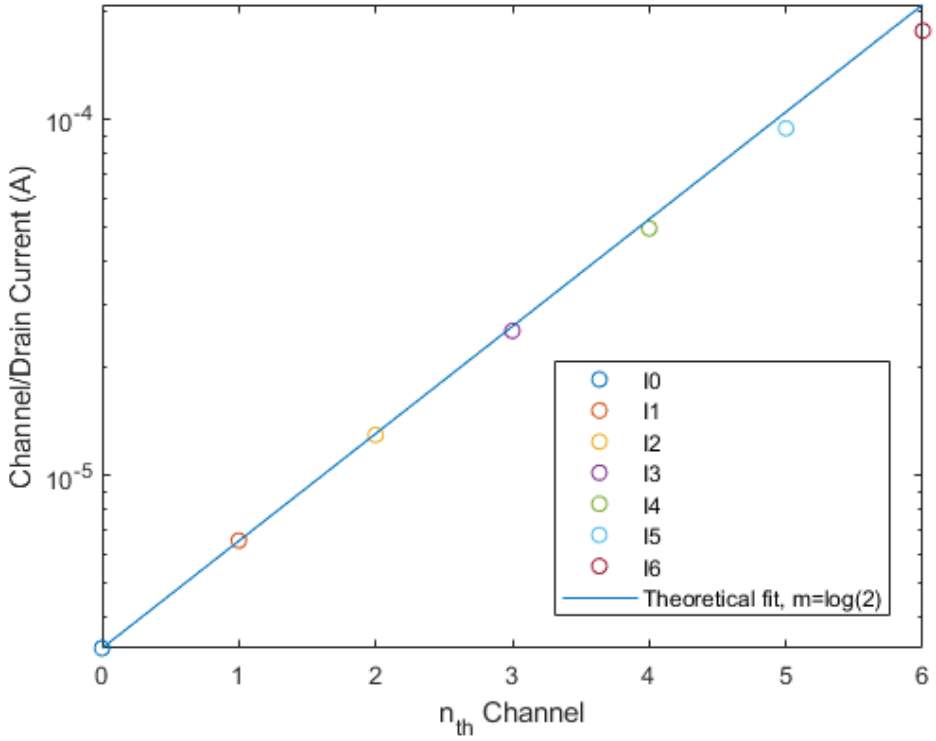

Figure 3: Channel currents I_n as a Function of Gate Voltage

3 Channel connections to Differential Pairs as Switches

To be able to use the R-2R ladder as a digital-to-analog converter, you must have a way to selectively add up the values of each of the branches. To do this, we implemented a system of differential pairs where the transistors of each branch served as the bias transistors. We then connected the differential pair transistors to one of two wires - one that would give us our desired I_{out}, and the other to be used as "dump" wire that's purpose is to continue supplying current to the branches we want to disregard in order to keep the R-2R ladder functioning properly. Figure 4 shows this circuit schematic.

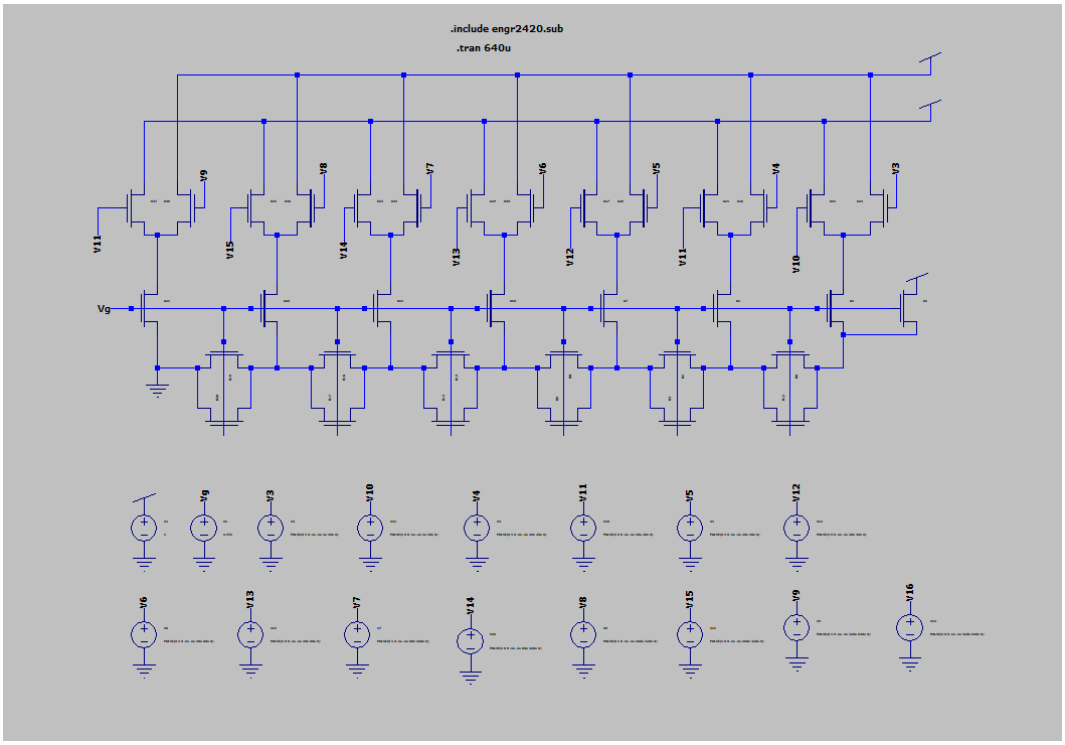

Figure 4: nMOS Transistor R-2R Ladder Circuit with Differential Pair Switches

To simulate all possible results for the digital to analog converter, we simulated every possible combination of current branches to represent all $2^7 = 128$ binary numbers possible with our setup. To do this, we controlled each gate voltage by pulsing from rail to rail with differing periods at each gate to generate a square wave that is a multiple of two from the next smallest (for example, the gate voltages for the transistor setting I_0 were set to have a square wave with a period of 10μs, while the gate voltages for the transistors setting I_1 had periods of 20μs). We ensured that each of the differential pair voltages had inverted square waves to ensure that the bias current would be drawn through the desired wire and not upset the R-2R ladder's current system. We chose a gate voltage for the transistors in the ladder that would make $I_0 = 1\mu$A in order to facilitate digital to analog conversion.

Figure 5 demonstrates the results from simulation with the square waves. We extracted the values at each step to then produce the graph seen in Figure 6 that also shows the theoretical values we would expect to see.

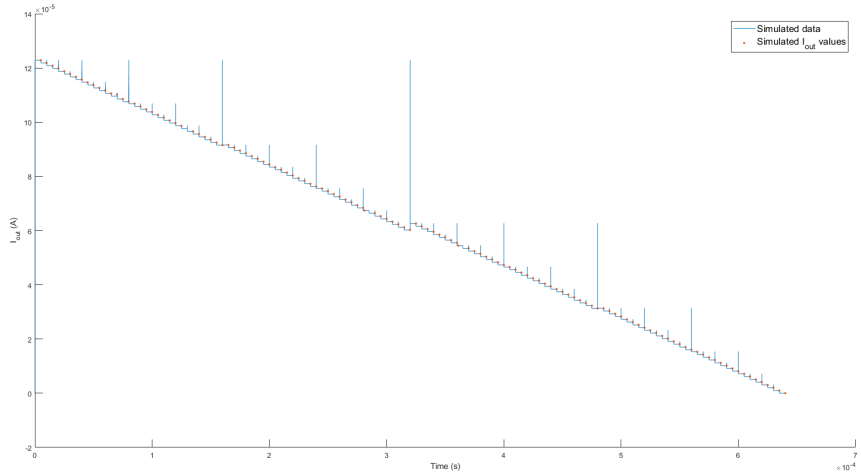

Figure 5: I_{out} Time Lapse with Square Wave Gate Voltages with Different Periods

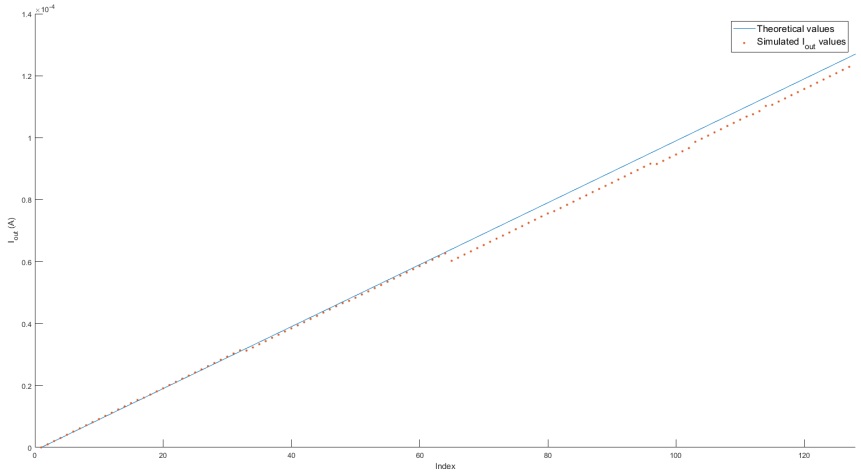

Figure 6: Simulation Results vs. Theoretical Fit for $I_{out} with Square Wave Gate Voltages with Different Periods$

As seen in Figure 5, our simulation overall yielded distinguishable results that were very close to the values we would expect to see for analog values below 64. However, for values 64 and above, the digital-to-analog converter ceases to be as reliable. This is likely due to what we observed in Figure 3 - the transistors furthest from the termination of the ladder deviate from the theoretical power function the most. We see this effect to a lesser extent happen at the value 32.

References

[1] Clemens M. Hammerschmied, "Design and Implementation of an Untrimmed MOSFET-Only 10-Bit A/D Converter with 79-dB THD", *IEEE Journal of Solid-State Circuits*

[2] Minch, Bradley A. Introduction to Microelectronic Circuits. Jan. - May 2019, Franklin W. Olin College of Engineering. Class lectures and office hours.