Lab Report 9 by Jamie O'Brien, Sabrina Pereira, and Shyheim Russell

1 Introduction

In this lab, we examine the voltage transfer characteristics of the current-mirror differential amplifier and its output-voltage range. We then compute the differential mode-voltage gain in two different ways. Finally, we investigate the time response of the amplifier configured as a unity-gain follower to both small-amplitude and large-amplitude steps. The circuits are constructed using ALD1106 quad nMOS and ALD1107 quad pMOS transistor arrays, and a source-measurement unit (SMU) was used to supply and measure voltage and current.

2 Experiment 1: Voltage Transfer Characteristics

In this experiment, we constructed a current-mirror differential amplifier with an nMOS differential pair, two simple pMOS current mirror, and a simple nMOS current mirror. We set three values of the inverting input, $V_2 = 2V, 3V, 4V$. For each value of V_2, we swept the noninverting input, V_1, from rail to rail and measure the output, V_{out}. As seen in Figure 1, $V_{out} = 0$ when $V_1 < V_2$, and $V_{out} = 5$V when $V_1 > V_2$. This is different from the amplifier we looked at in Lab 8 under the condition $V_1 < V_2$. In Lab 8, we saw V_{out} increase up to the point where $V_1 = V_2$, while in this lab, it appears that V_{out} remains at zero up until that point.

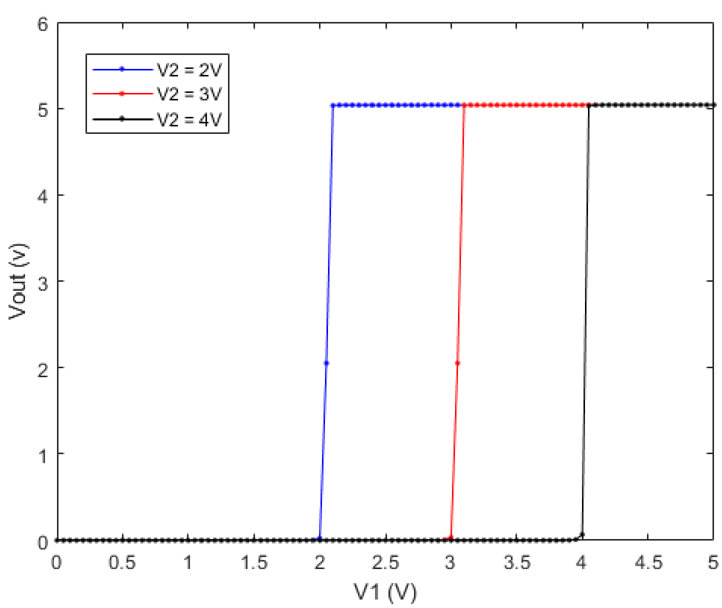

Figure 1: V_{out} vs. V_1 for three values of V_2 with V_b=.65V

3 Experiment 2: Transconductance, Output Resistance, and Gain

In this experiment, we started with the same circuit as Experiment 1 and set $V_2 = 3V$ and measured V_{out}, but instead of sweeping V_1 from rail to rail, we swept it around V_2 in fine increments. As seen in Figure 2, the linear fit matches the steep part of our voltage transfer characteristic. The slope of the linear fit is the differential-mode gain, A_{dm}, of the amplifier, where A_{dm}=234.2.

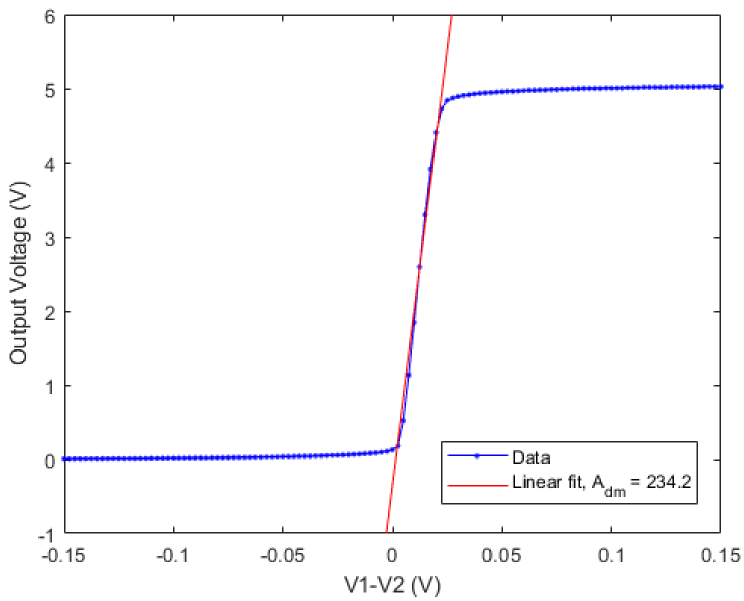

Figure 2: V_{out} vs. $V_1 - V_2$ for fixed $V_2 = 3$, V_b=.8V

Next, we set the differential-mode input voltage, V_{dm}, to zero, and swept V_{out} from one rail to the other while we measured the current out, I_{out}, of the amplifier. The linear fit displayed in Figure 4 matches the data where the amplifier's gain is large. The slope of this fit allows us to find the incremental output resistance, R_{out} = 4.06e+06 Ω.

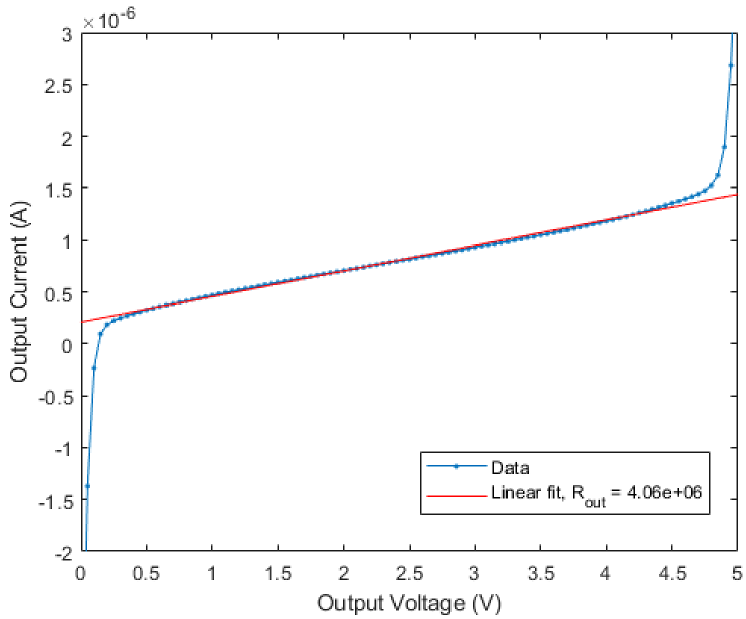

Figure 3: I_{out} vs. V_{out} when $V_{dm} = 0$, V_b=.8V

Finally, we fixed $V_{out} = 3V$, swept V_{dm} around zero, and measured I_{out}. The slope of the linear fit in Figure 4 gives us the incremental transconductance gain, G_m = 5.96e-05 Mhos.

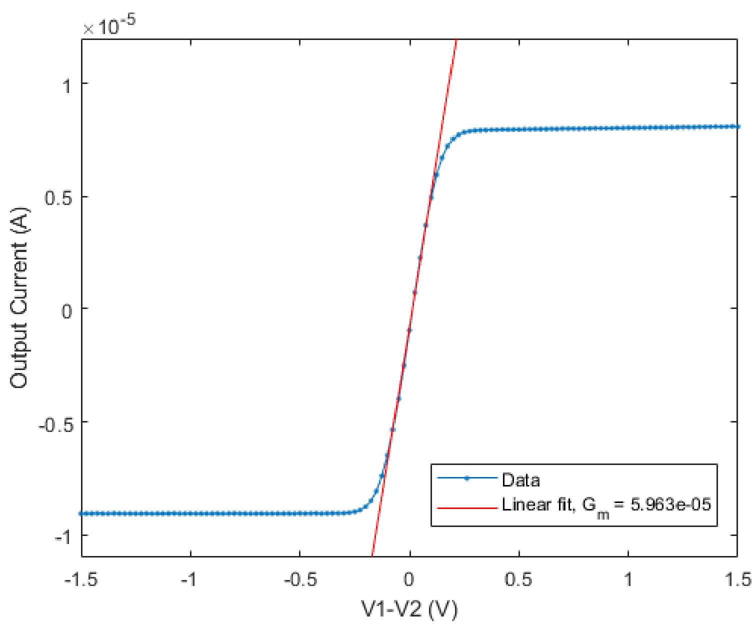

Figure 4: I_{out} vs. $V_1 - V_2$ when $V_{out} = 3$, V_b=.8V

From the equation, $A_{dm} = R_{out} * G_m = 242.3$. This is very close to the value $A_{dm} = 234.2$ that we got from the slope of the VTC. The differential-mode gain of this amplifier is also close to the one we investigated in Lab 8, where we found that $A_{dm} = 260.47$.

4 Experiment 3: Unity-Gain Follower

In this experiment, we configured the amplifier as a unity-gain follower by connecting V_{out} to V_2. We then added a $1nF$ pull-down capacitor between the output of the amplifier and ground. We applied a small-amplitude square wave of .1V to the input of the circuit and observed both the input and output waveforms as a function of time. The DC offset was set to 3V.

The response is symmetrical, as seen in Figure 5. The amplifier does not exhibit linear behavior.

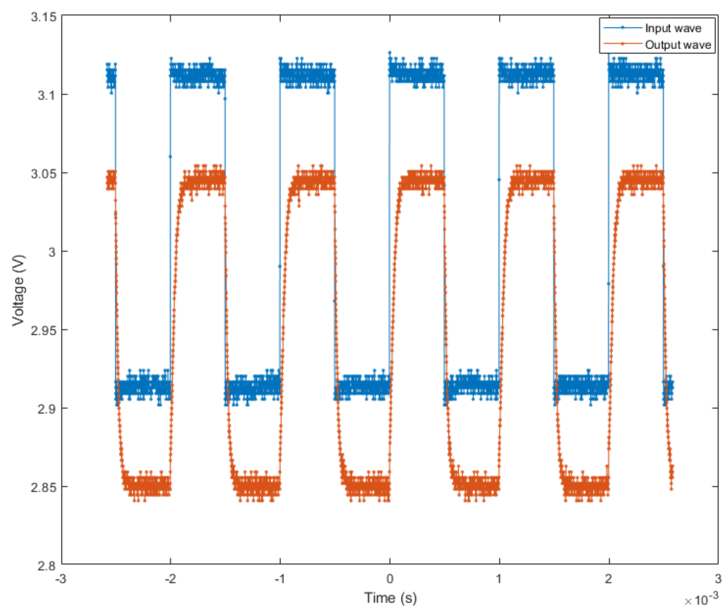

Figure 5: Input and Output Voltages with a small-amplitude square wave of .1V

We then increased the amplitude of our square wave so that it has an amplitude of 1.5V. The response was not symmetrical, as seen in Figure 6. The slew rate for the up-going part is 2.8388e+03 V/s, while for the down-going part it is -6.9521e+03 V/s.

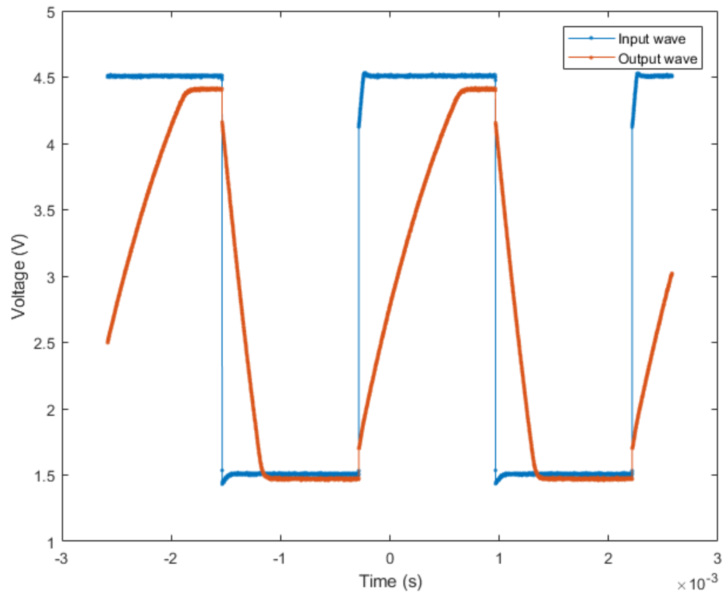

Figure 6: Input and Output Voltages with a large-amplitude square wave of 1.5V