Lab Report 6 by Jamie O'Brien, Sabrina Pereira, and Shyheim Russell

1 Introduction

In this lab, we continued exploring nMOS transistors. We collected data using a source-measurement unit (SMU) to analyze the currentâvoltage characteristics of the transistors and of pairs of matched transistors in series and in parallel in various operating regimes. We also used these to construct current dividers and examine their current transfer characteristics.

2 Experiment 1: Transistor Matching

In this experiment, we used an ALD1106 chip to compare the current-voltage characteristics of four matched nMOS transistors. To do this, we measured the channel current as we swept the gate voltage, V_G. We held the source voltage, V_S, at ground and the drain voltage, V_D, at 5V. The current-voltage characteristics for each transistor can be seen in Figure 1.

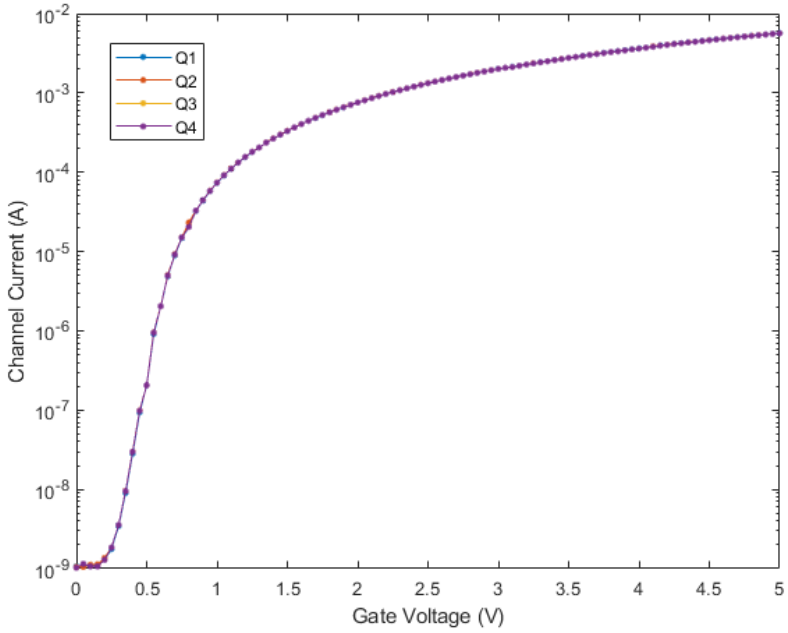

Figure 1: Current-Voltage characteristic of four matched transistors

To determine that the transistors are well matched we found the mean channel current from all four transistors, and then plotted each transistor's percent difference from the mean as a function of the mean channel current, as seen in Figure 2. From this we can see that the four transistors are very well matched. As the channel current decreases, the percent differences from the mean become larger for all four transistors. We can see that Q1 and Q4 have a positive percent difference from the mean, while Q2 and Q3 have negative percent differences from the mean. This indicates that Q1 and Q4 are match each other better than

they match the other two, and Q2 and Q3 match each other better than they match the other two.

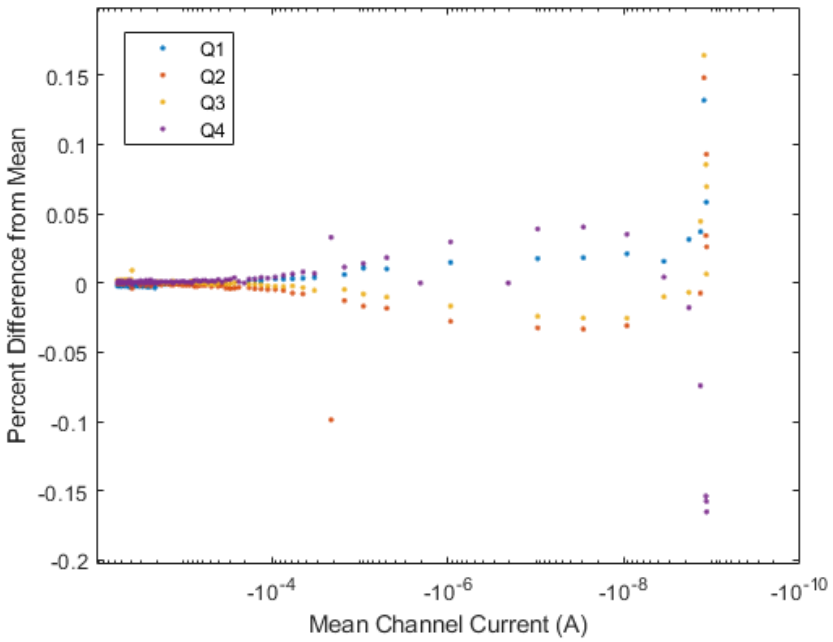

Figure 2: Percent difference from mean current for each of four matched transistors

3 Experiment 2: Source Characteristics

In this experiment, we wanted to compare the characteristics of a single transistor, two transistors in parallel, and two transistors in series. In theory, two transistors in parallel will have twice the channel current of a single transistor, and two transistors in series will have half the channel current of a single transistor. For each of the three setups, we held the V_S at ground and swept V_G twice, once with $V_D = 10mV$ and once with $V_D = 5V$. Figure 3 shows the six characteristic curves we found from these configurations. We see that all three curves with $V_D = 10mV$ show smaller channel currents than the curves with $V_D = 5V$. We also see that the parallel transistors produce higher current than the single transistor, and the series transistors produce lower current than the single transistor. This indicates that our results match the theoretical assumptions, but we wanted to check the ratios.

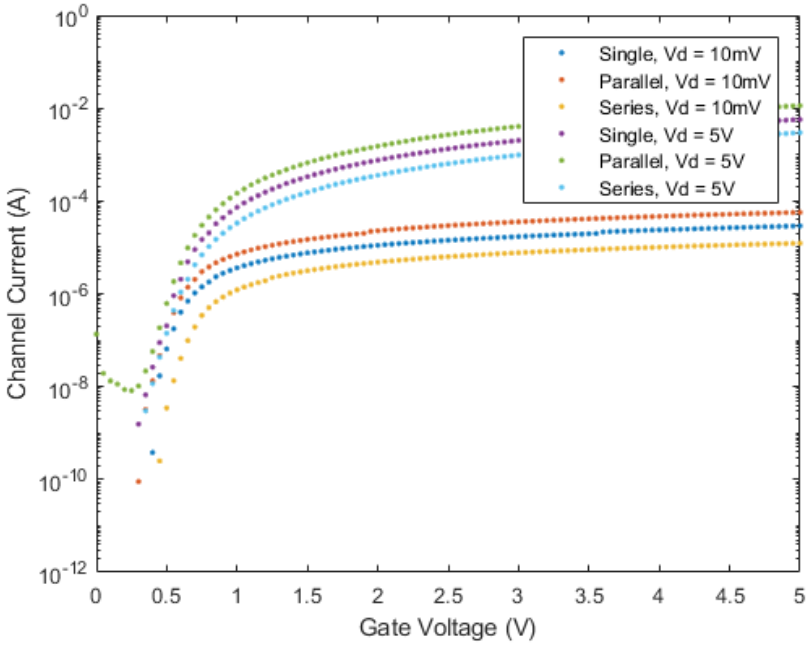

Figure 3: Current-voltage characteristics of a single nMOS transistor, two nMOS transistors in parallel, and two nMOS transistors in series with two drain voltages

For the parallel transistors, we calculated the ratio of the measurements from the parallel transistor to the measurements of the single transistor, which theoretically should be equal to two. As seen in Figure 3, the channel current through a pair of parallel transistors is consistently twice that of a single transistor. However, there is some discrepancy at very low values of V_G, which is why we zoomed in on the graph for Figure 5 to more clearly display that the ratio is equal to two.

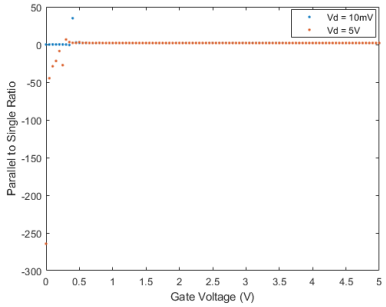

Figure 4: Parallel transistors to single transistor ratio zoomed out (including extreme values at low currents)

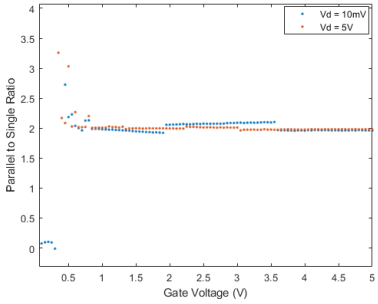

Figure 5: Parallel transistors to single transistor ratio zoomed in (excluding extreme values at low currents

For the series transistors, we calculated the ratio of the measurements of the single transistor to the measurements of the series transistors, which theoretically should be equal to two. As seen in Figure 3, the channel current through a pair of transistors in series is consistently half that of a single transistor, again with some discrepancy at low values of V_G, which is why we zoomed in on Figure 7 to more clearly display that the ratio is equal to two.

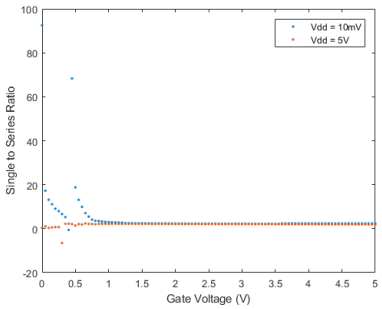

Figure 6: Single transistor to series transistors ratio zoomed out (including extreme values at low currents)

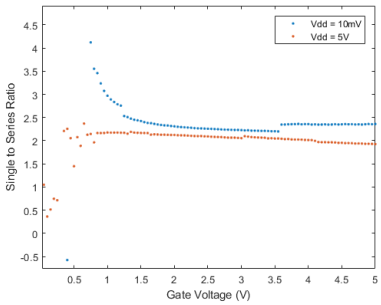

Figure 7: Single transistor to series transistors ratio zoomed in (excluding extreme values at low currents

4 Experiment 3: Drain Characteristics

In this experiment, we constructed a two-way current divider in which we supplied a current sink, $V_G = V_{dd}$, and $V_D = 5V$. We chose this value for V_D to ensure that the transistors are saturated. We measured output current as a function of input current, as can be seen in Figure 8. The extracted divider ratio of .5029 is very close to the theoretical divider ratio .5.

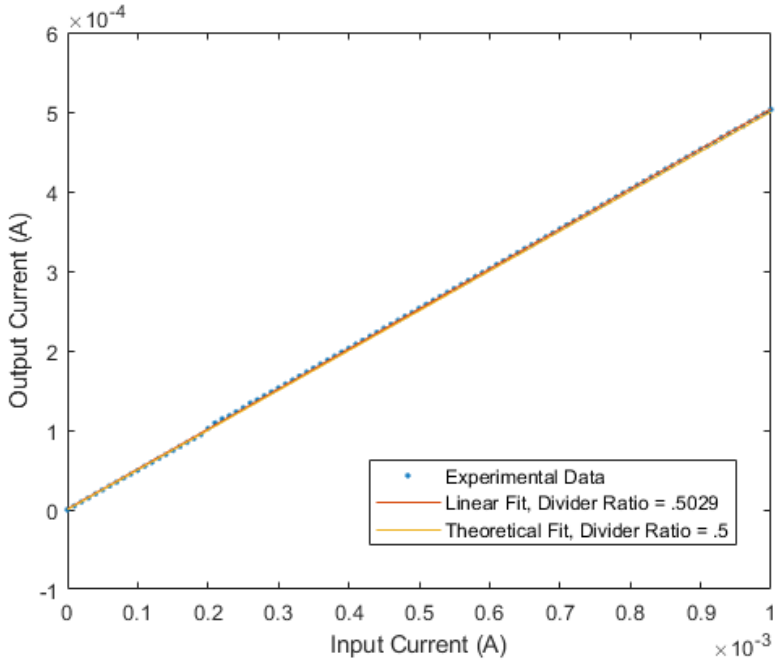

Figure 8: Output Current versus Input Current for Current Divider 6.2a

We built a second two-way current divider using a current soure instead of a current sink. We again measured output current as a function of input current, as can be seen in Figure 9. The extracted divider ratio of .4546 is not as close to the theoretical divider ratio .5 as the one we had found previously, but it is still very close.

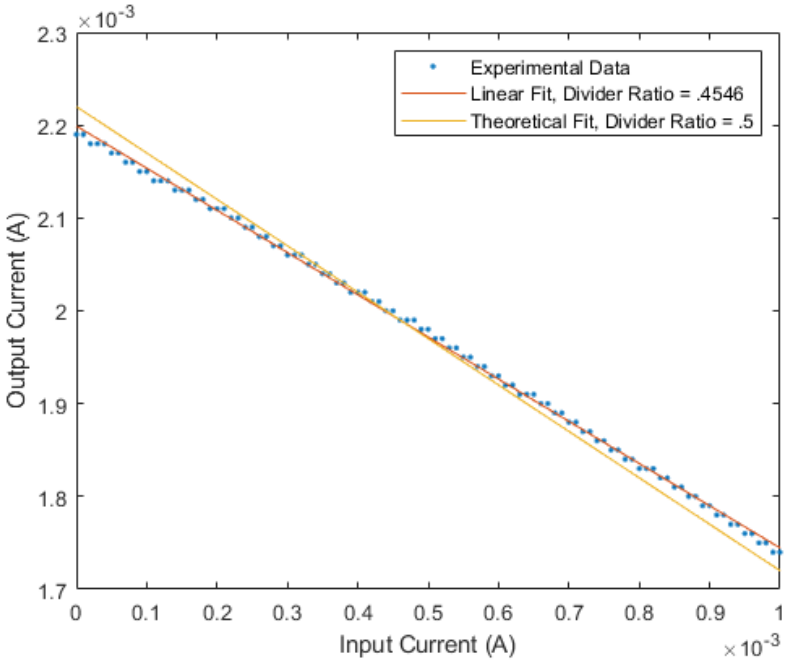

Figure 9: Output Current versus Input Current for Current Divider 6.2b