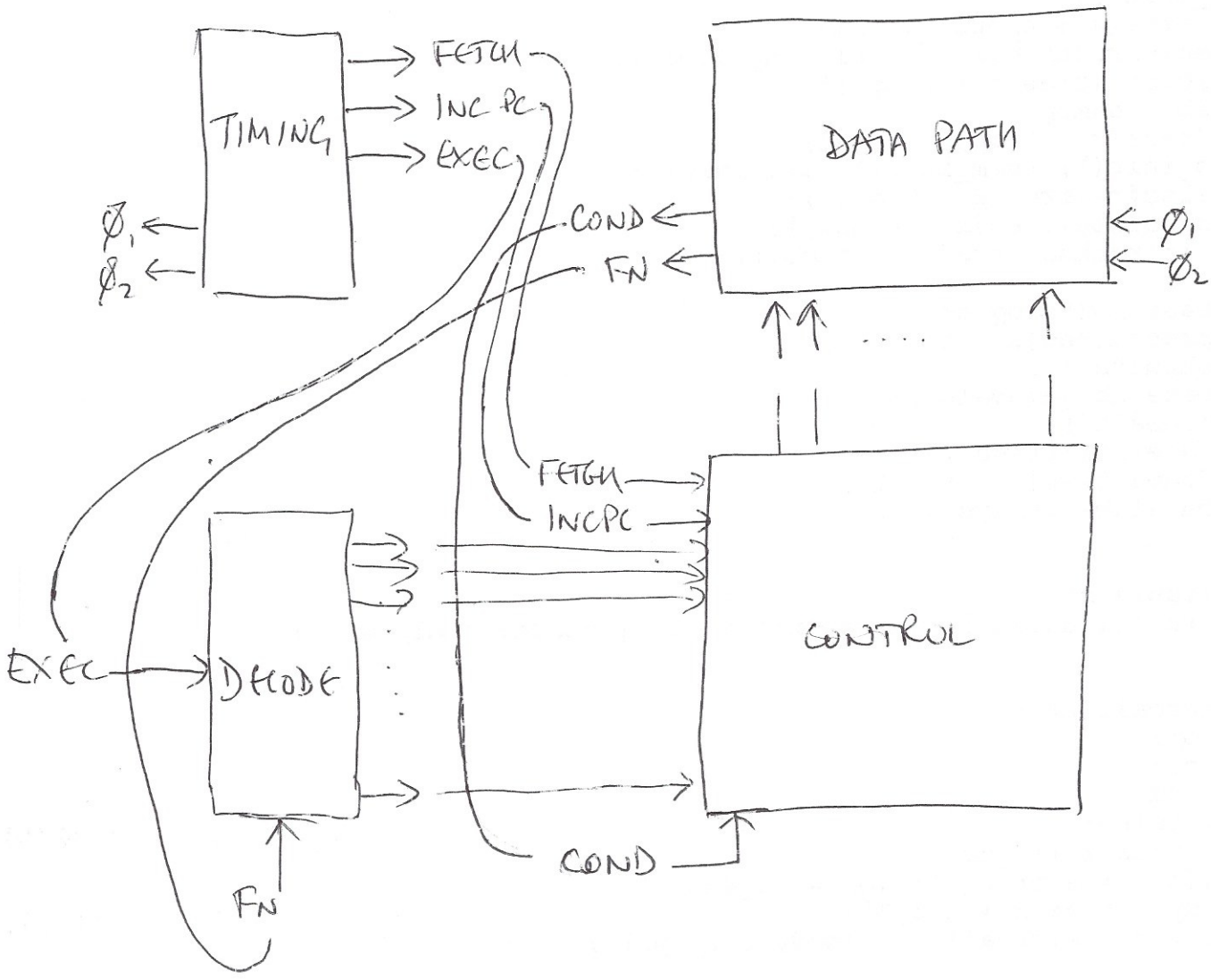
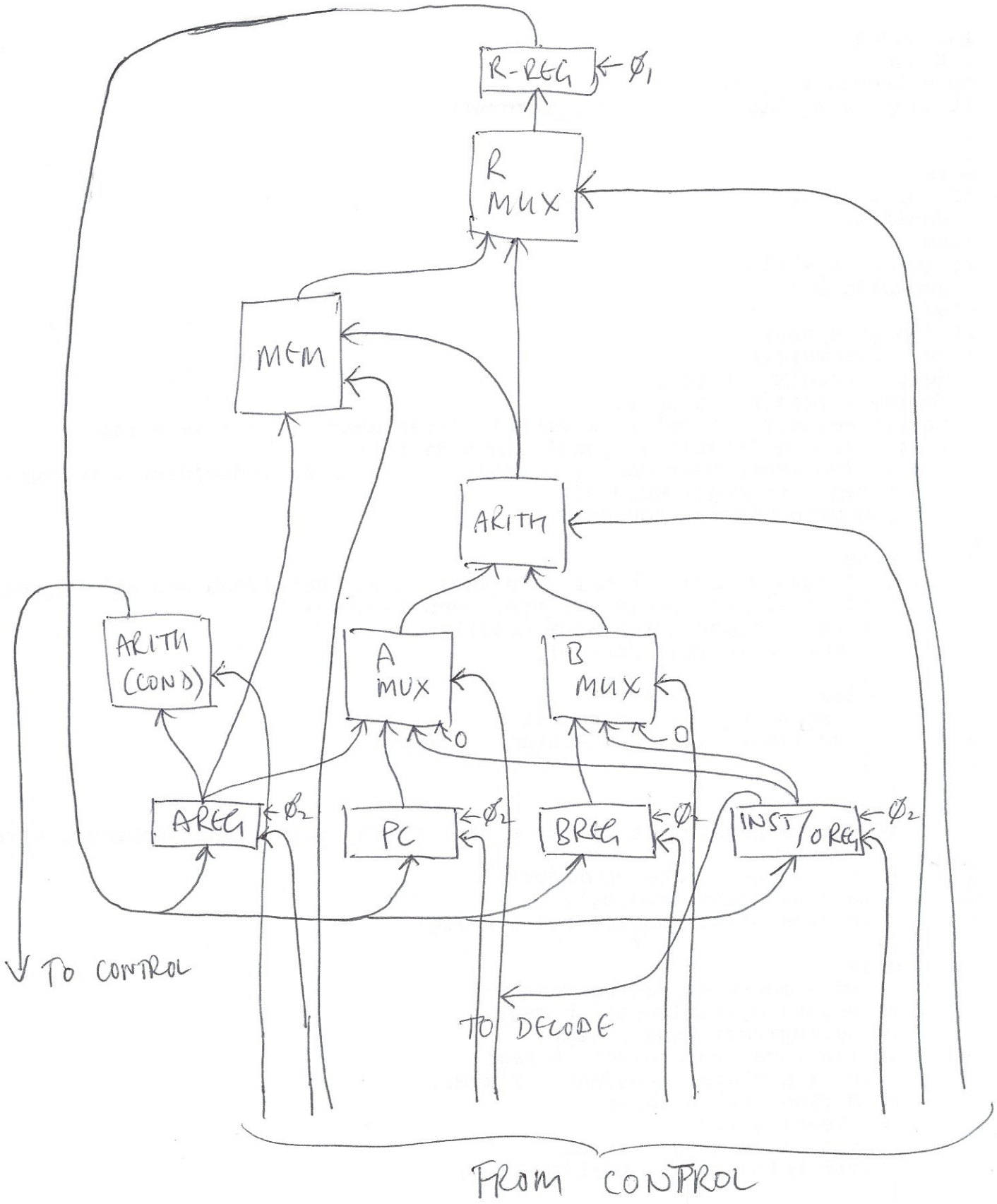


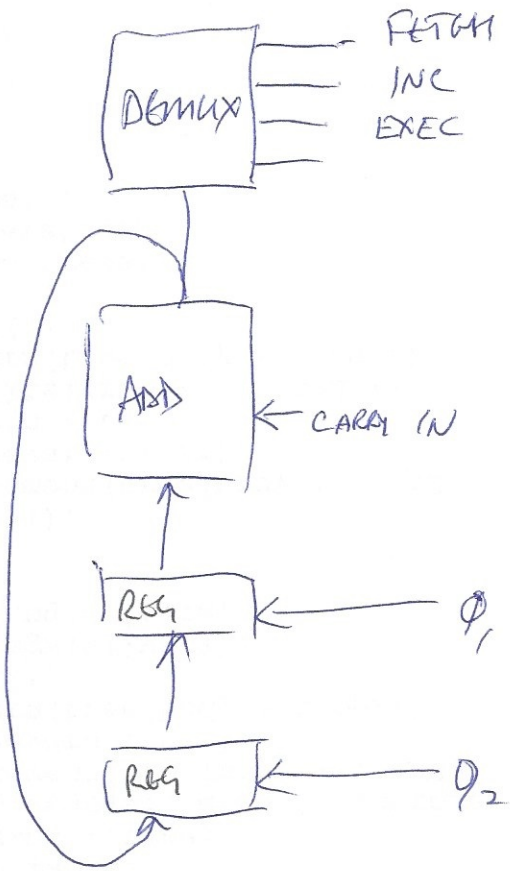
STRUCTURE

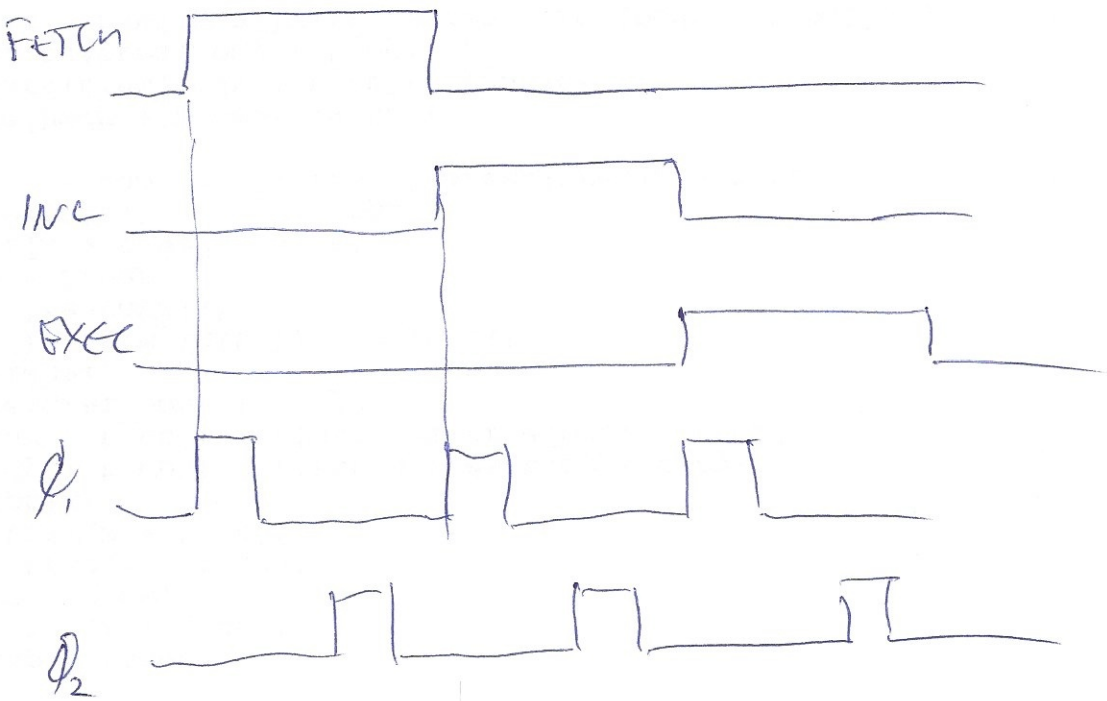
(8-BIT COMPUTER)


R-REG
ϕ_1
R MUX
MEM
ARITH
ARITH (COND)
A MUX
B MUX
0
0
AREG
PC
BREG
INST REG
ϕ_2
ϕ_2
ϕ_2
ϕ_2
TO CONTROL
TO DECODE
FROM CONTROL

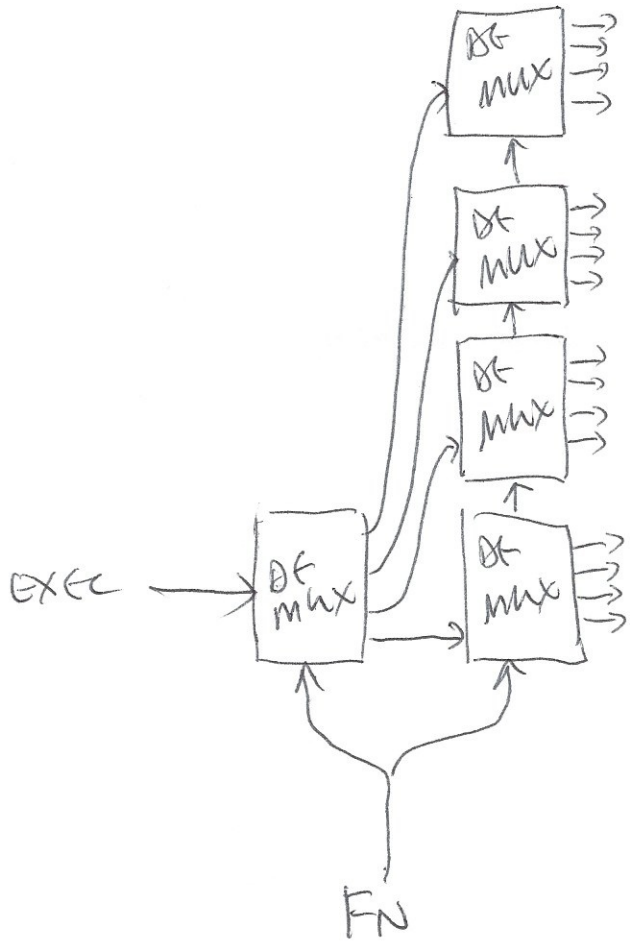
DATAPATH

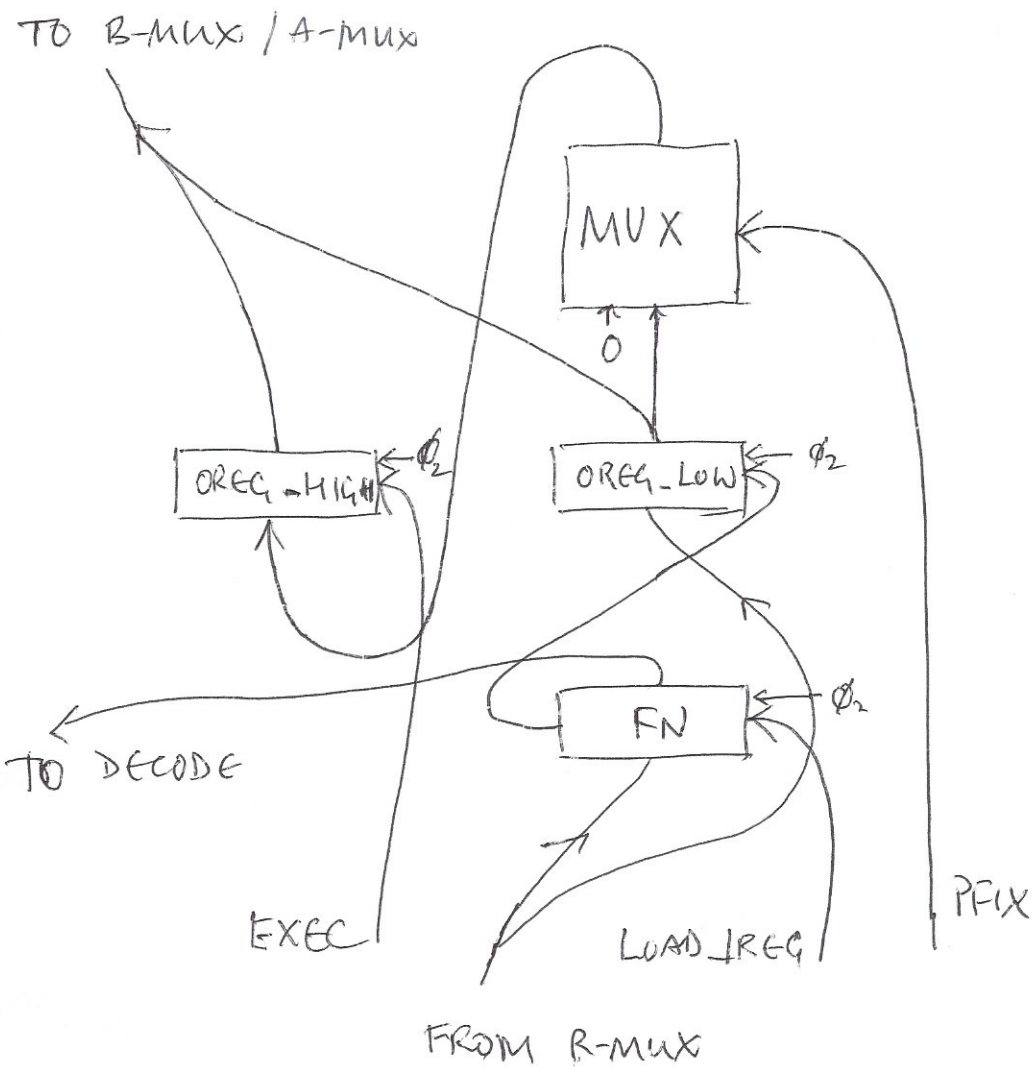
TIMING


DEMUX
FETCH
INC
EXEC
ADD
CARRY IN
REG
ϕ_1
REG
ϕ_2

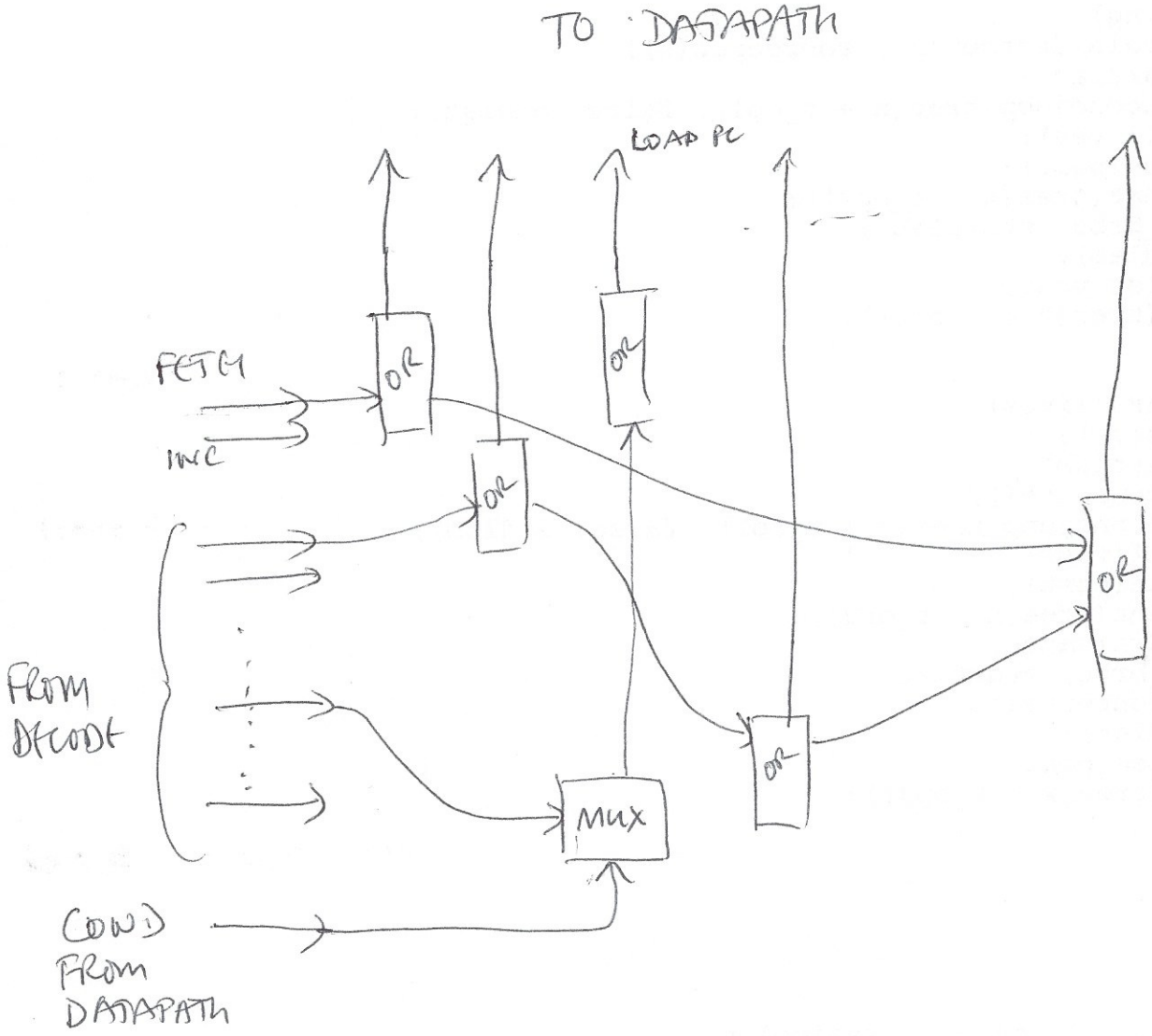

FETCH
INC
EXEC
ϕ_1
ϕ_2

DECODE





INSTRUCTION & OPERAND REGISTER



CONTROL - EXAMPLE