Binary to Gray
– Reference Solution

Instructor:-

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Pre-Lab Tasks:

1. What do you mean by binary codes for the decimal digits? Give some examples and codes (tables) for the decimal digits.

In computing and electronics, binary coded decimal (BCD) is a class of binary encoding of decimal numbers, where each decimal digit is represented by a fixed number of bits.

Decimal	BCD
0	0 0
1	0 1
2	1 0
3	1 1

2. What is a self-complementing code? Name any two of them; show their complementing nature with examples and describe advantages.

Self complementing code is one in which the 9's complement is obtained by taking the 1's complement.

(i) Excess-3 e.g. 1 in decimal <=> 0100 in Excess-3

(ii) 84-2-1 e.g. 1 in decimal <=> 0001 in 84-2-1

Advantage is that the hardware is easier to design.

3. In the lab you would be implementing a gray to binary and binary to gray code converter. Make a truth table for both the codes by filling in the following tables and Simplify the expressions for W,X,Y,Z in terms of A,B,C,D and vice versa. Also give some applications in which gray code could be used.

Dec	Binary				Gray			
	A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1

HINT:

Our inputs and outputs are of 4-bit each. You will have to make 4 K-Maps (Consider W as independent function of A,B,C,D, Make K-Map and simplify it). Arrive at the simplest expression for each output.

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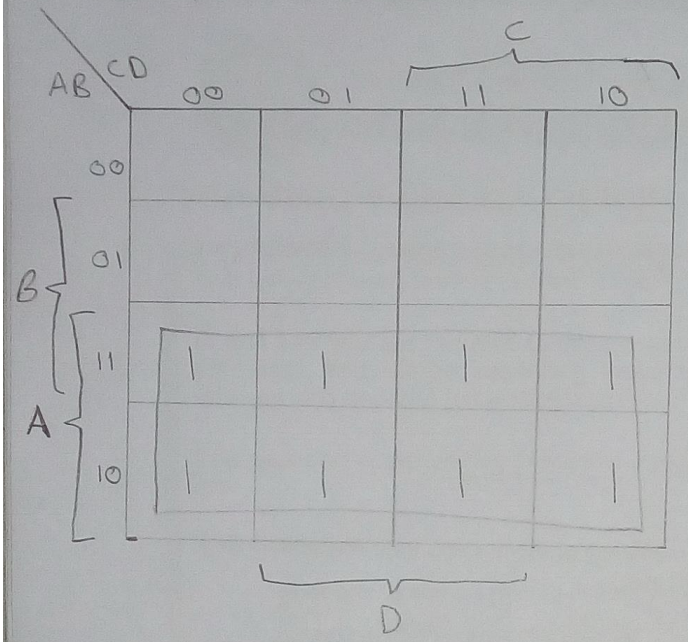
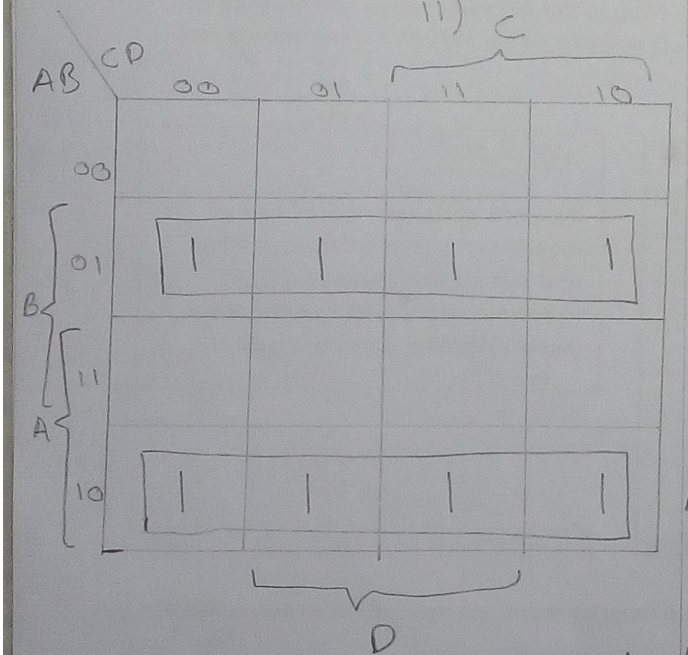
① $W(A,B,C,D) = \sum(8,9,10,11,12,13,14,15)$



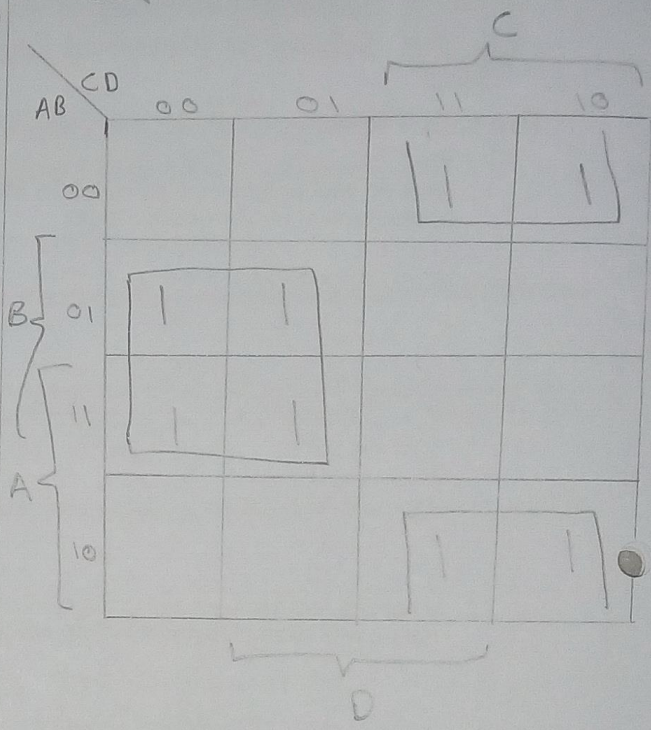
$W(A,B,C,D) \Rightarrow A$

② $X(A,B,C,D) = \sum(4,5,6,7,8,9,10,11)$



$X(A,B,C,D) \Rightarrow A'B + AB'$

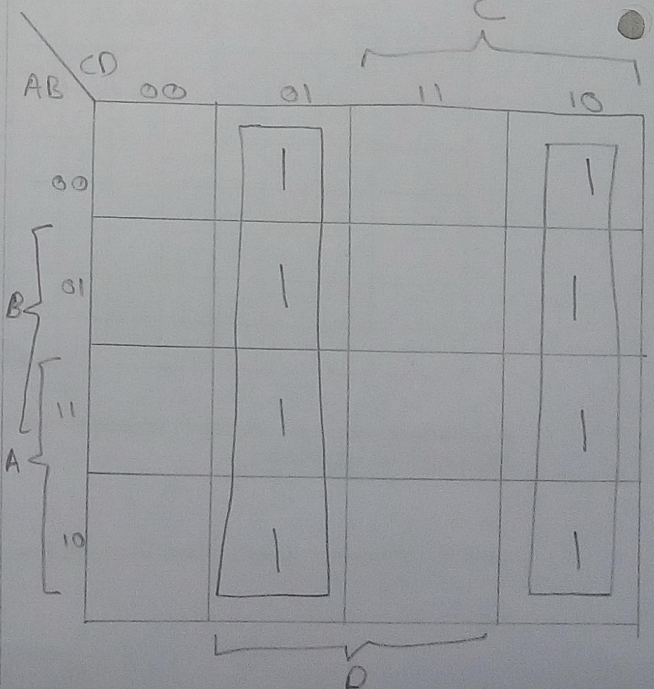
③ $Y(A,B,C,D) = \sum(2,3,4,5,10,11,12,13)$



$Y(A,B,C,D) = BC' + B'C$

④ $Z(A,B,C,D) = \sum(1,2,5,6,9,10,13,14)$

$= C'D + CD'$



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7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

W= A

X= A'B + AB'

Y= BC' + B'C

Z= C'D + CD'

Dec	Gray				Binary			
	W	X	Y	Z	A	B	C	D
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	1	0	0	1	0
3	0	0	1	0	0	0	1	1
4	0	1	1	0	0	1	0	0
5	0	1	1	1	0	1	0	1
6	0	1	0	1	0	1	1	0
7	0	1	0	0	0	1	1	1
8	1	1	0	0	1	0	0	0
9	1	1	0	1	1	0	0	1
10	1	1	1	1	1	0	1	0
11	1	1	1	0	1	0	1	1
12	1	0	1	0	1	1	0	0
13	1	0	1	1	1	1	0	1
14	1	0	0	1	1	1	1	0
15	1	0	0	0	1	1	1	1

HINT:

Our inputs and outputs are of 4-bit each. You will have to make 4 K-Maps (Consider A as independent function of W,X,Y,Z.

Make K-Map and simplify it). Arrive at the simplest expression for each output.

A= W

B= W'X + WX'

C= WX'Y' + WXY + W'XY' + W'X'Y

D= W'X'Y'Z + W'X'YZ' + W'XY'Z' + W'XYZ + WXY'Z + WXYZ' + WX'Y'Z' + WX'YZ

Reducing

C = Y'(WX' + W'X) + Y(WX + W'X')

= Y'(W ⊕ X) + Y(W ⊕ X)'

= (W ⊕ X) ⊕ Y

EE221 Digital Logic Design Page 4

D = Y'Z(W'X' + WX) + YZ'(W'X' + WX) + Y'Z'(W'X + WX') + YZ(W'X + WX')

= Y'Z(W ⊕ X)' + YZ'(W ⊕ X)' + Y'Z'(W ⊕ X) + YZ(W ⊕ X)

= (W ⊕ X)'(Y'Z + YZ') + (W ⊕ X)(Y'Z' + YZ)

= (W ⊕ X)'(Y ⊕ Z) + (W ⊕ X)(Y ⊕ Z)'

= (W ⊕ X) ⊕ (Y ⊕ Z)

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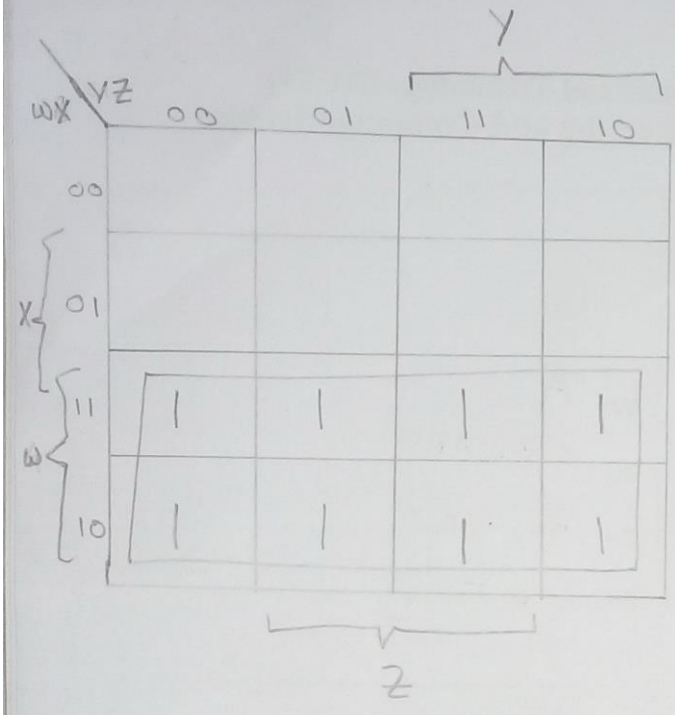
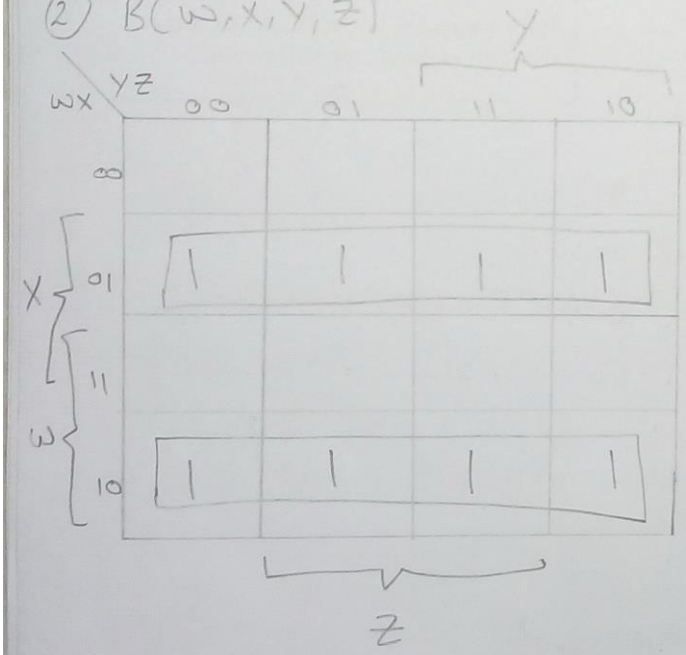
① $A(w,x,y,z)$



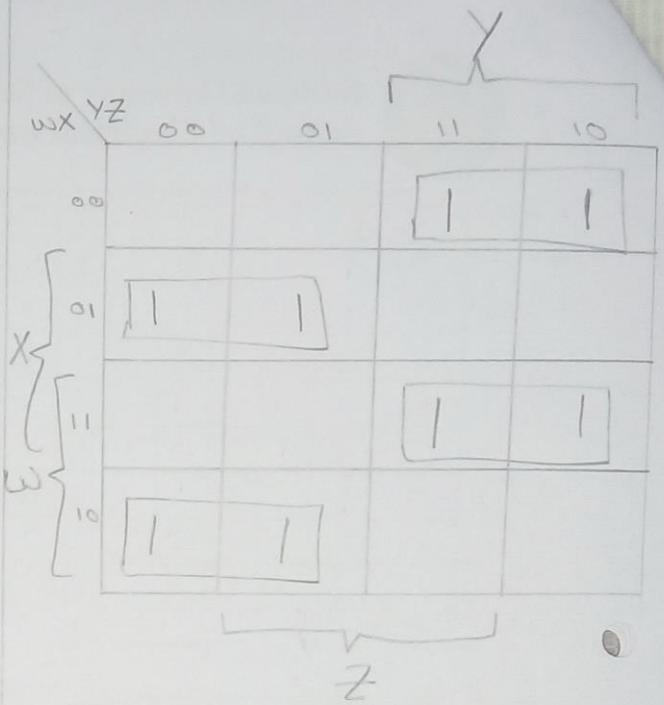
$A(w,x,y,z) \Rightarrow w$

② $B(w,x,y,z)$



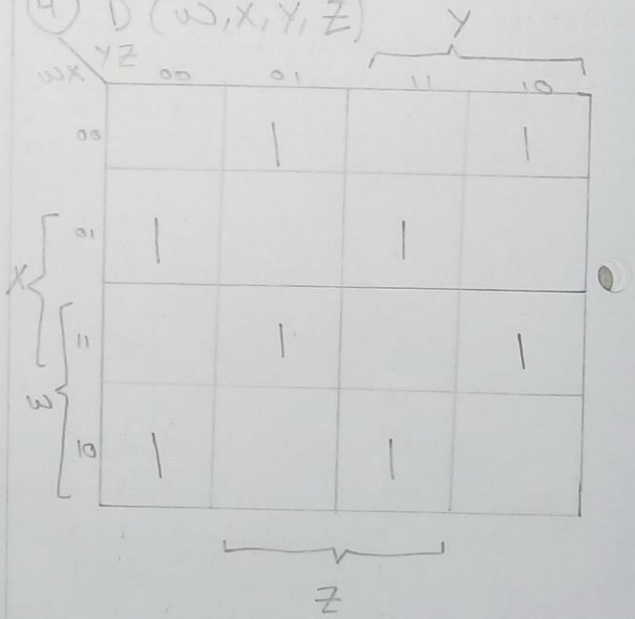
$B(w,x,y,z) \Rightarrow w'x + wx'$

③ $C(w,x,y,z)$



$C(w,x,y,z) \Rightarrow wx'y' + wxy + w'xy' + w'x'y$

④ $D(w,x,y,z)$



$D(w,x,y,z) \Rightarrow w'x'y'z + w'x'yz' + w'xy'z' + w'xyz + wxy'z + wxyz' + wx'y'z' + wx'yz$

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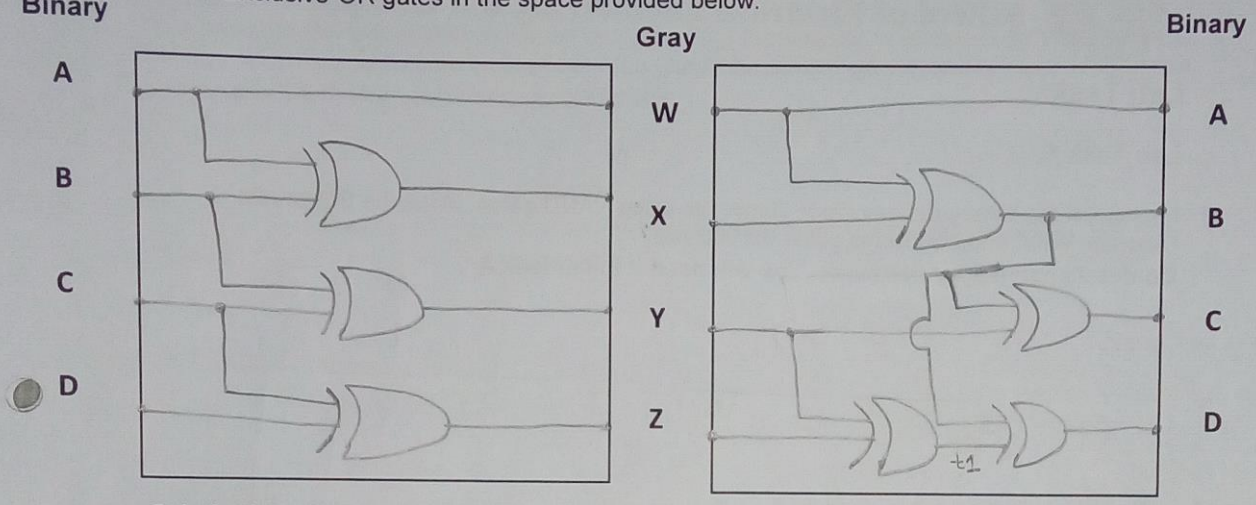
4. Draw the logic diagram for the Binary-to-Gray and Gray-to-Binary code converters using Exclusive-OR gates in the space provided below.



Only the following gates are available to you for lab tasks.

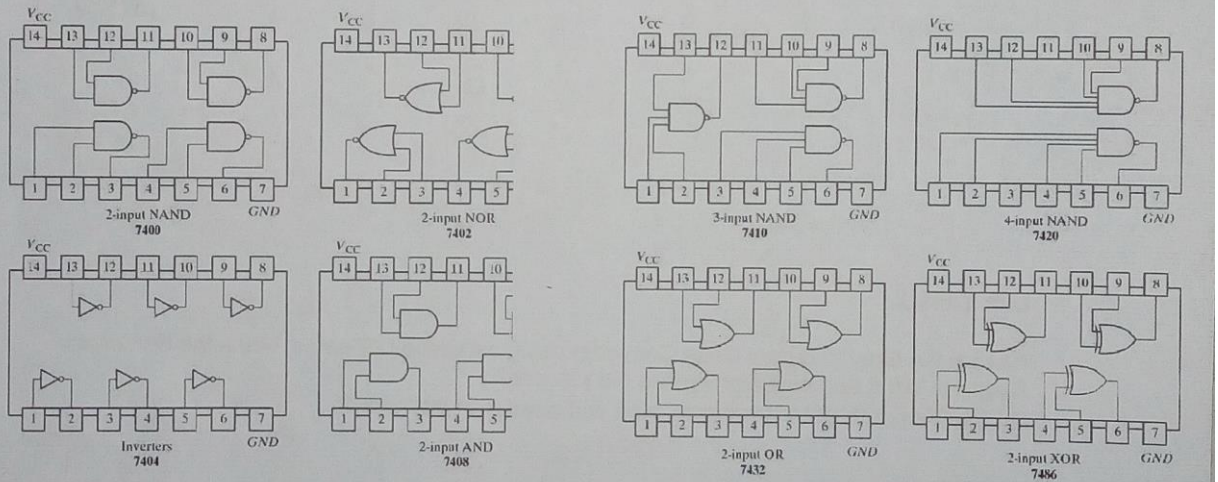
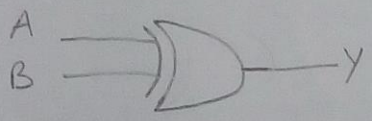


Fig. 11-1(cond) Digital Gates in IC Packages with Identification Numbers and Pin Assignments

XOR

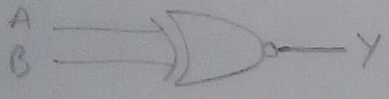


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$Y = A \oplus B$

$= AB' + A'B$

XNOR



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

$Y = \overline{A \oplus B}$

$= AB + A'B'$

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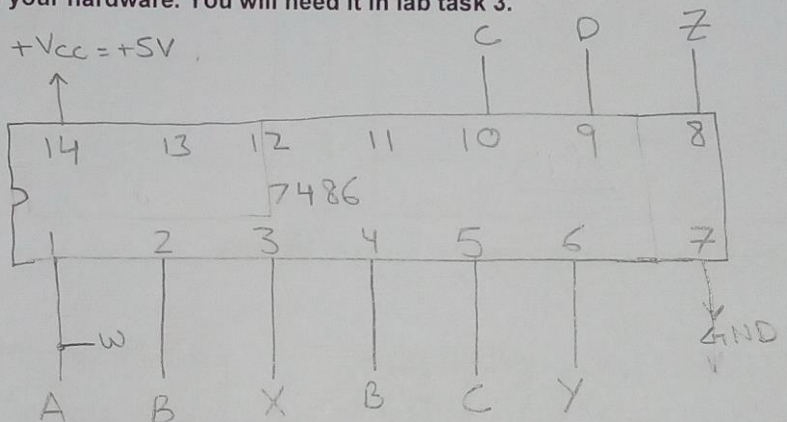
Lab Tasks:

Lab Task 1:

Implement the Binary to Gray Code Converter using XOR gates. Make the Schematic Diagram. What and how many gates did you use?

Do not dispatch your hardware. You will need it in lab task 3.

A → SW3
B → SW2
C → SW1
D → SW0
W → LED 3
X → LED 2
Y → LED 1
Z → LED 0



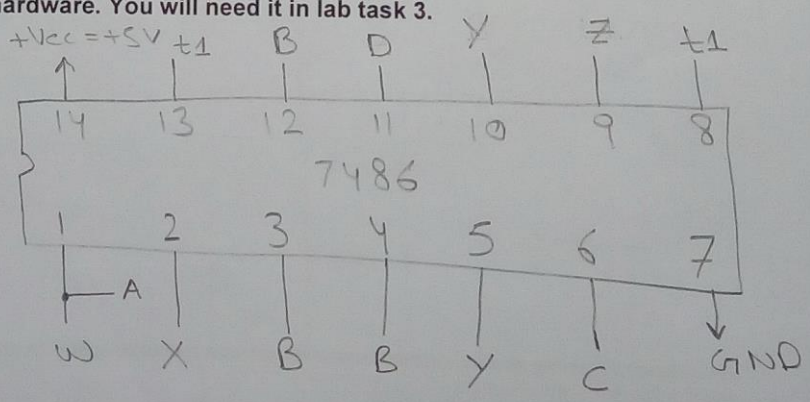
XOR gates used. Total number of gates = 3

Lab Task 2:

Realize the Gray to Binary Code Converter using exclusive-OR gates. Make the Schematic Diagram. What and how many gates did you use?

Do not dispatch your hardware. You will need it in lab task 3.

W → SW7
X → SW6
Y → SW5
Z → SW4
A → LED 7
B → LED 6
C → LED 5
D → LED 4



t1 = Y ⊕ Z

XOR gates used. Total number of gates = 4

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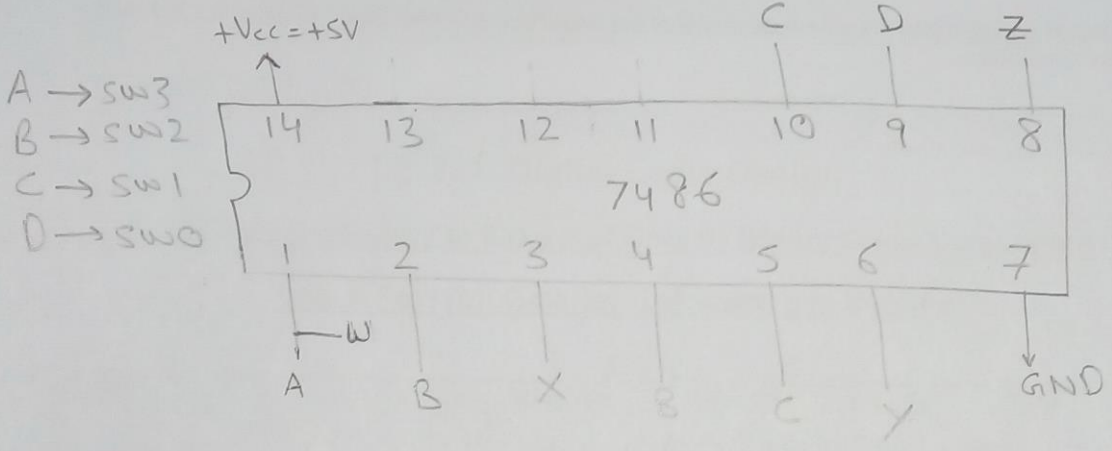
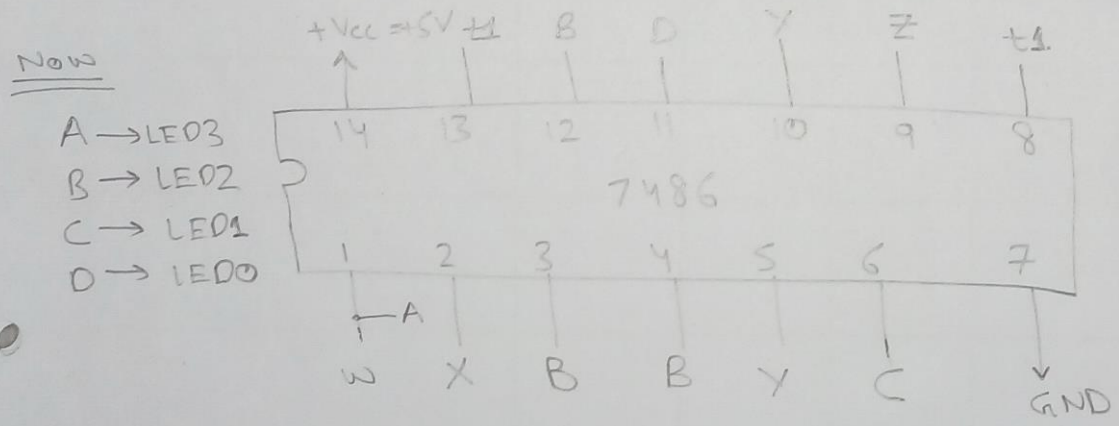
Lab Task 3:

Now cascade the two circuits in series by connecting the outputs of binary-to-gray converter to the inputs of the gray-to-binary converter. You should be able to get the binary input at output as well. Use LEDs to show input-output relationship.





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Lab Task 4:

Design and simulate the gate-level model of the circuit you patched. Give the code in the space provided below.

Write code over here.

Snapshots

— Verilog code snaps
— Simulation result waveform snaps

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