National University of Sciences and Technology (NUST)
School of Electrical Engineering and Computer Science

Department of Electrical Engineering

Faculty Member:_____ **Dated:** _____

Course/Section:_____ **Semester:**_____

EE-221: Digital Logic Design

Lab 5: Part (a): Binary to Gray and Gray to Binary Code Conversion

Lab 5: Part (b): Gate-level Modelling in Verilog

Name	Reg. No.	Report Marks / 10	Viva Marks / 5	Total Marks / 15

Lab 5: Binary-to-Gray and Gray-to-Binary Code Conversion

This Lab has been divided into two parts:

In first part you are required to design and implement a binary to gray and gray to binary code converter. You will be cascading these two converters thus implementing a binary to gray encoder and decoder (gray to binary).

The next part is the Verilog Modelling and Simulation of the Circuit you implemented in you first lab.

Objectives:

- ✓ Understand steps involved in design of combinational circuits
- ✓ Understand binary codes for decimals and their hardware realization
- ✓ Write code for combinational circuits using Verilog Gate Level Modelling
- ✓ Design a circuit in Verilog by calling different modules

Pre-Lab Tasks:

1. What do you mean by binary codes for the decimal digits? Give some examples and codes (tables) for the decimal digits.

2. What is a self-complementing code? Name any two of them; show their complementing nature with examples and describe advantages.

3. In the lab you would be implementing a gray to binary and binary to gray code converter. Make a truth table for both the codes by filling in the following tables and Simplify the expressions for W,X,Y,Z in terms of A,B,C,D and vice versa. Also give some applications in which gray code could be used.

Dec	Binary				Gray			
	A	B	C	D	W	X	Y	Z

HINT:

Our inputs and outputs are of 4-bit each. You will have to make 4 K-Maps (Consider W as independent function of A,B,C,D, Make K-Map and simplify it). Arrive at the simplest expression for each output.

W=

X=

Y=

Z=

Dec	Gray				Binary			
	W	X	Y	Z	A	B	C	D

A=

B=

C=

D=

HINT:

Our inputs and outputs are of 4-bit each. You will have to make 4 K-Maps (Consider A as independent function of W,X,Y,Z.

Make K-Map and simplify it). Arrive at the simplest expression for each output.

4. Draw the logic diagram for the Binary-to-Gray and Gray-to-Binary code converters using Exclusive-OR gates in the space provided below.

Binary

A

B

C

D

Gray

W

X

Y

Z

Binary

A

B

C

D

Only the following gates are available to you for lab tasks.

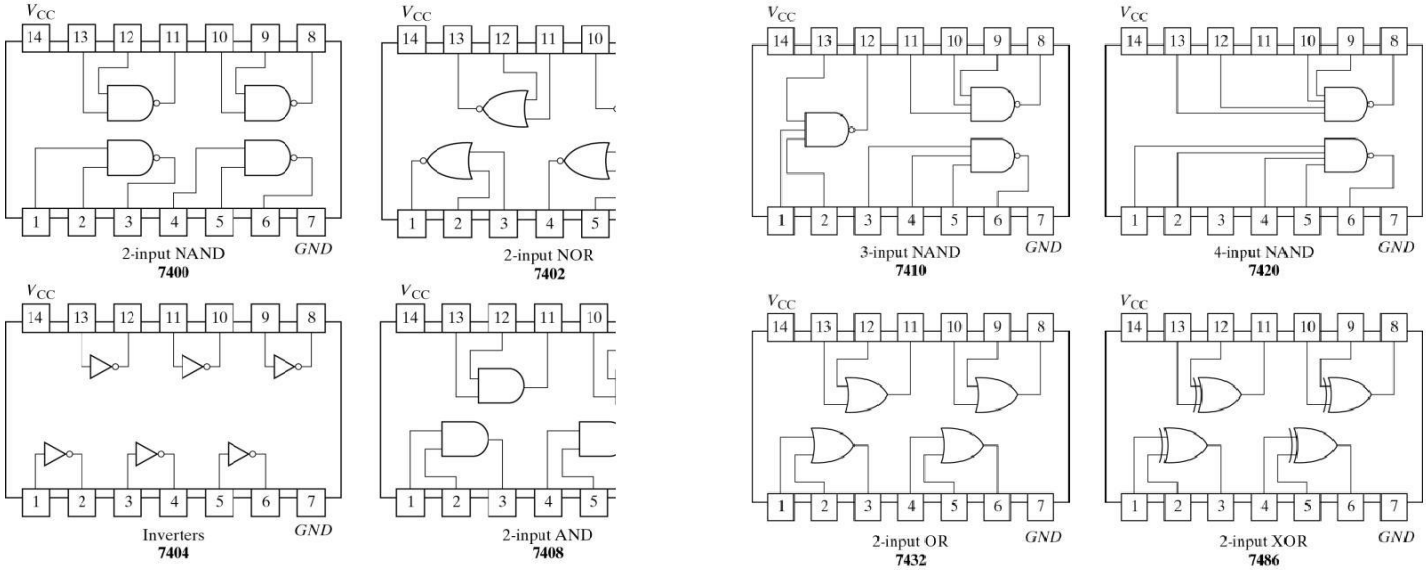

Fig. 11-1(cond) Digital Gates in IC Packages with Identification Numbers and Pin Assignments

Lab Tasks:

Lab Task 1:

Implement the Binary to Gray Code Converter using exclusive-OR gates. Make the Schematic Diagram. What and how many gates did you use?

Do not dispatch your hardware. You will need it in lab task 3.

Lab Task 2:

Realize the Gray to Binary Code Converter using exclusive-OR gates. Make the Schematic Diagram. What and how many gates did you use?

Do not dispatch your hardware. You will need it in lab task 3.

Lab Task 3:

Now cascade the two circuits in series by connecting the outputs of binary-to-gray converter to the inputs of the gray-to-binary converter. You should be able to get the binary input at output as well. Use LEDs to show input-output relationship.

Lab Task 4:

Design and simulate the gate-level model of both the circuits you patched. Give the code in the space provided below.