

Introduction To Verilog

Instructor:-

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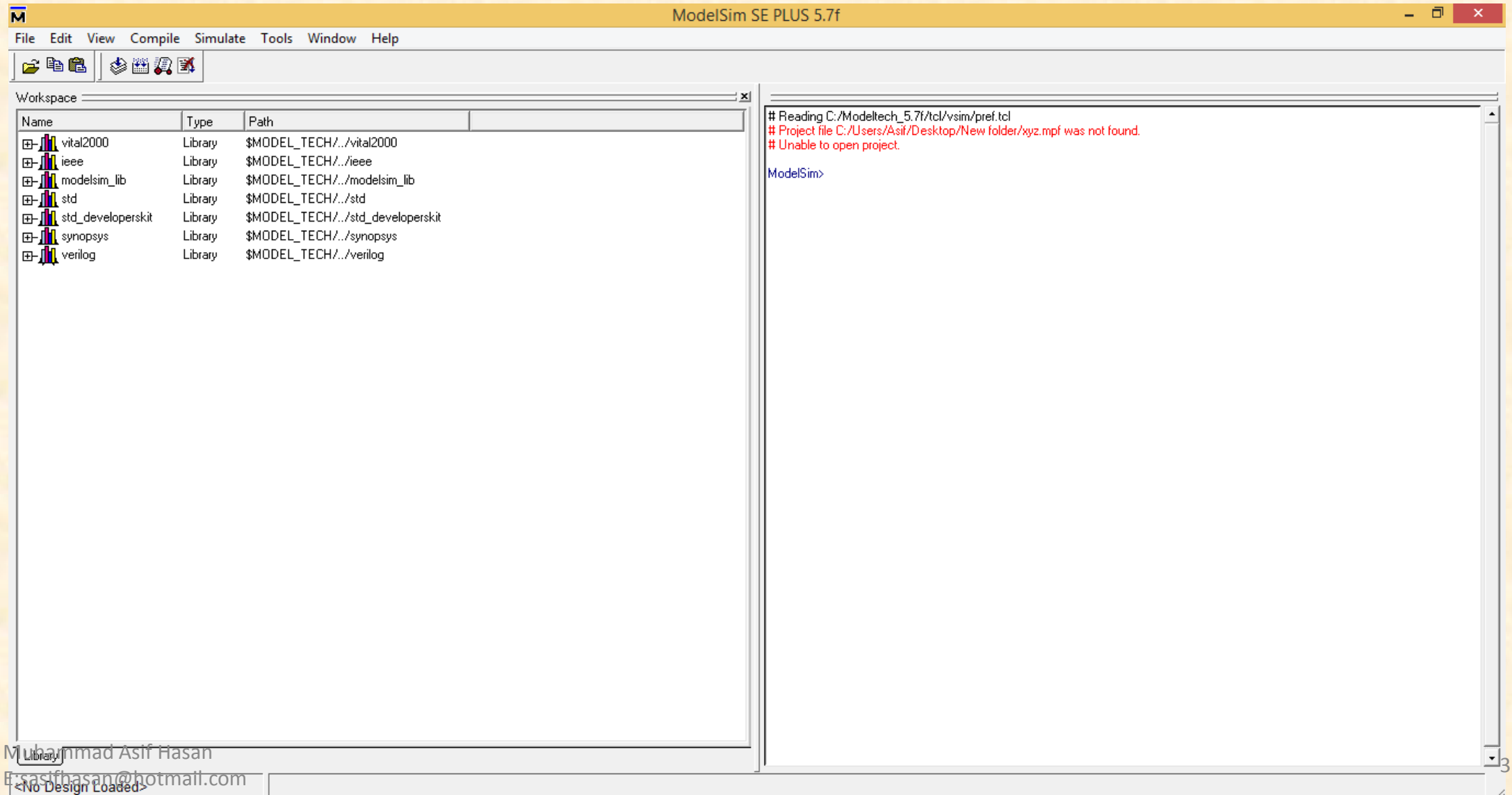
School of Electrical Engineering and Computer Sciences (SEECs)

H-12 Campus, National University of Sciences and Technology (NUST)

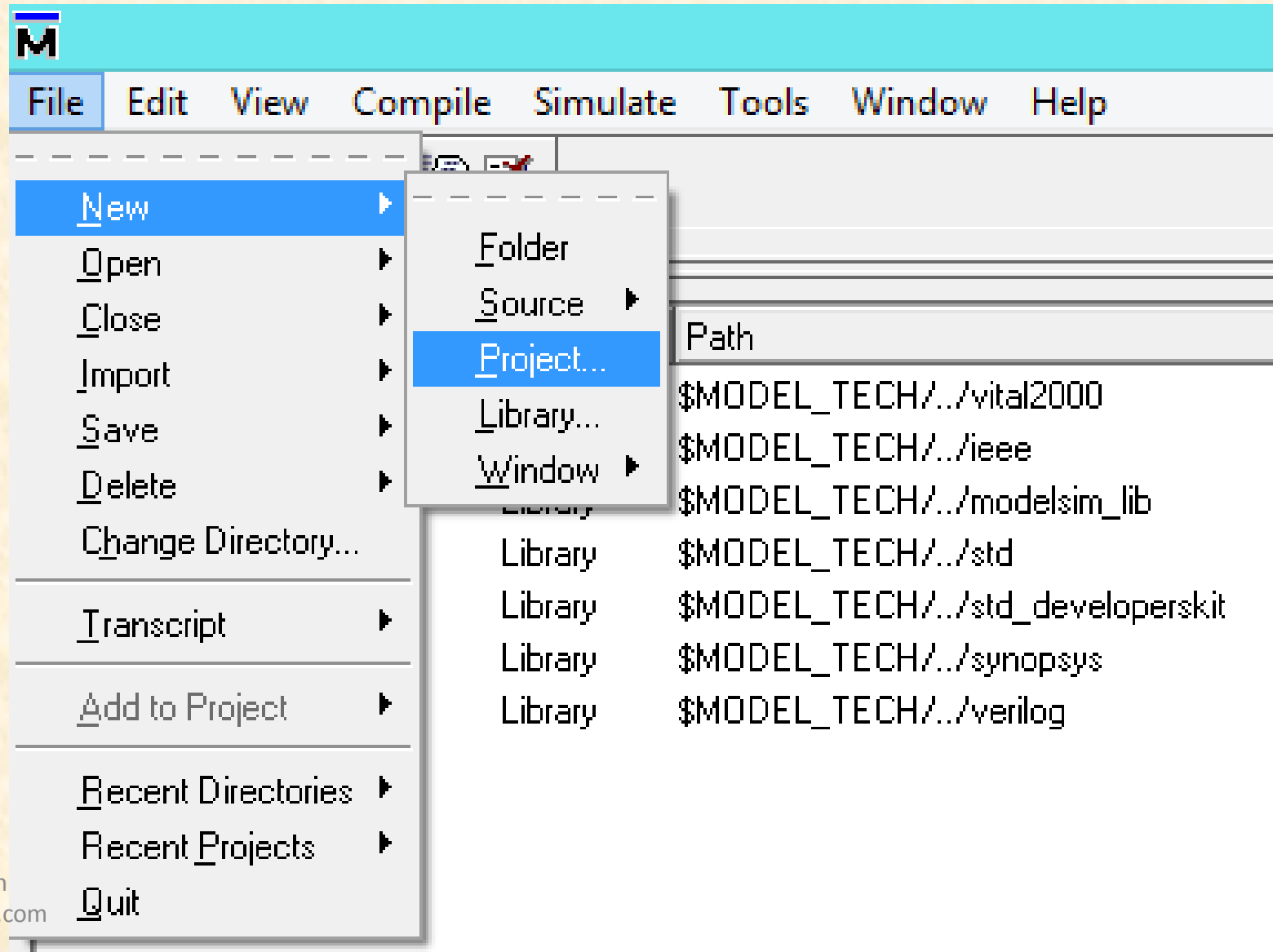
Create a New Folder on Desktop and open ModelSim



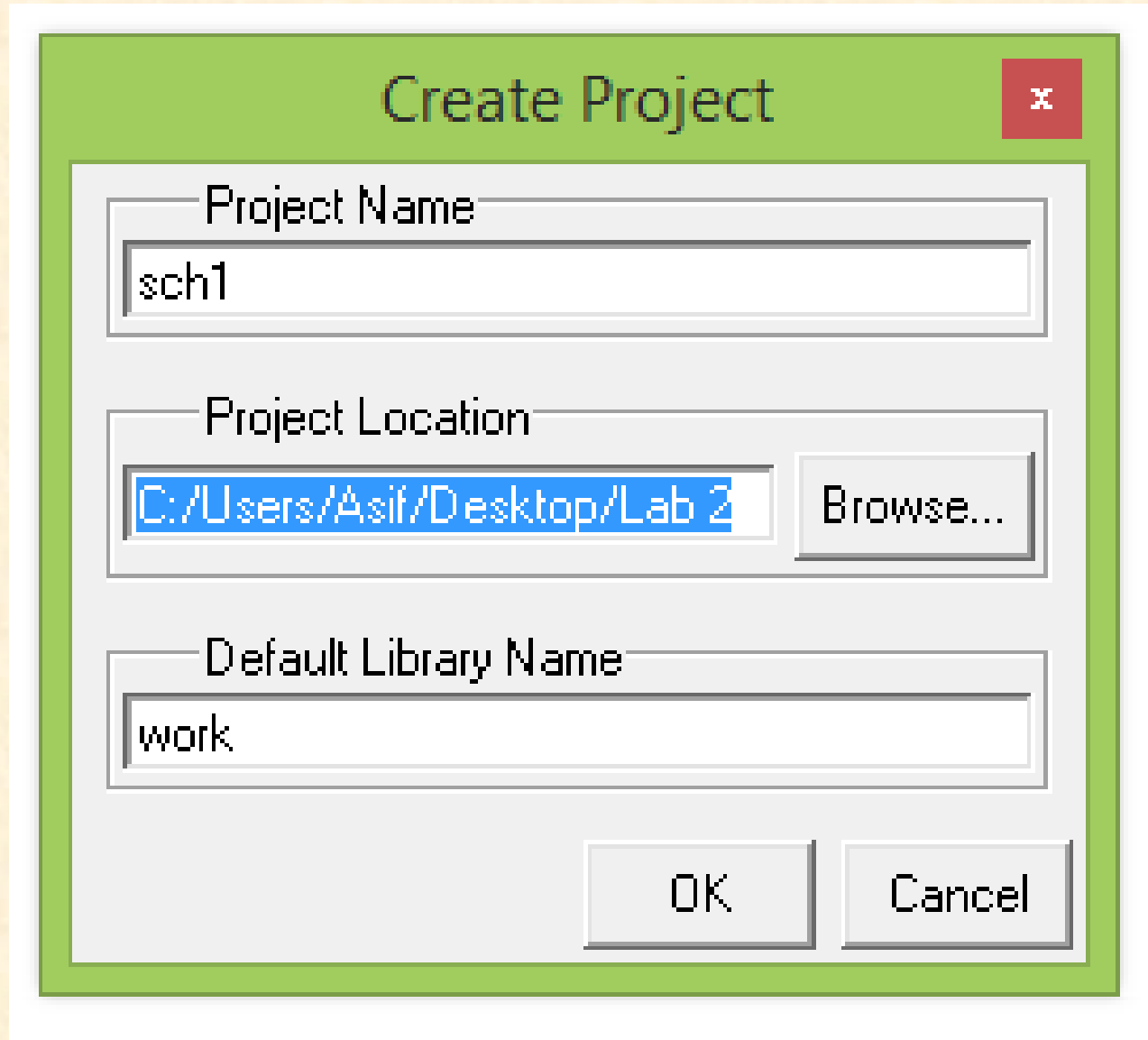
Below window will appear



Create New Project



Give name and location to the new folder created

A screenshot of a 'Create Project' dialog box. The dialog has a green title bar with the text 'Create Project' and a red close button with a white 'x'. Inside the dialog, there are three text input fields. The first is labeled 'Project Name' and contains the text 'sch1'. The second is labeled 'Project Location' and contains the text 'C:/Users/Asif/Desktop/Lab 2', with a 'Browse...' button to its right. The third is labeled 'Default Library Name' and contains the text 'work'. At the bottom of the dialog are two buttons: 'OK' and 'Cancel'.

Create Project

Project Name

sch1

Project Location

C:/Users/Asif/Desktop/Lab 2

Browse...

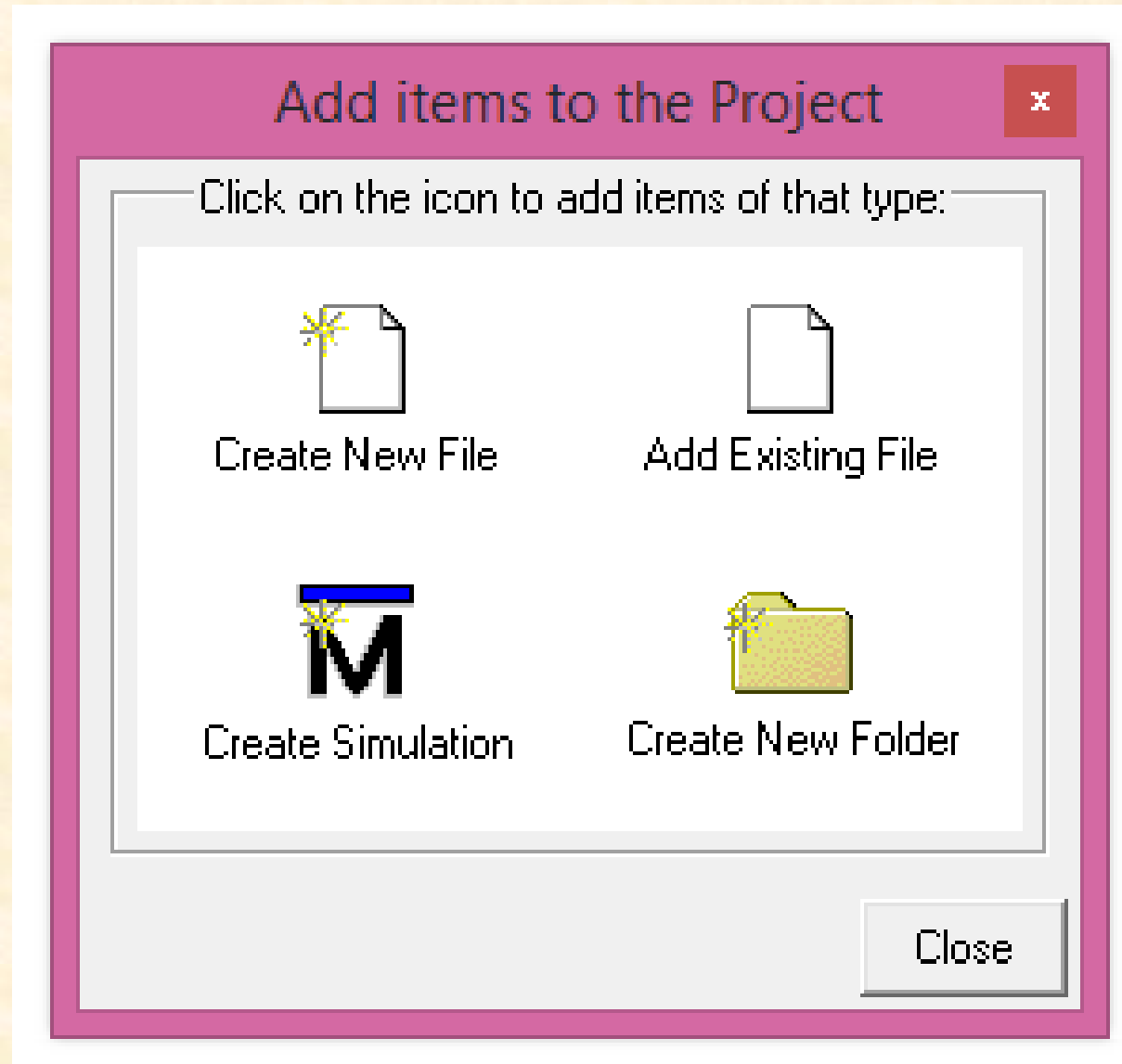
Default Library Name

work

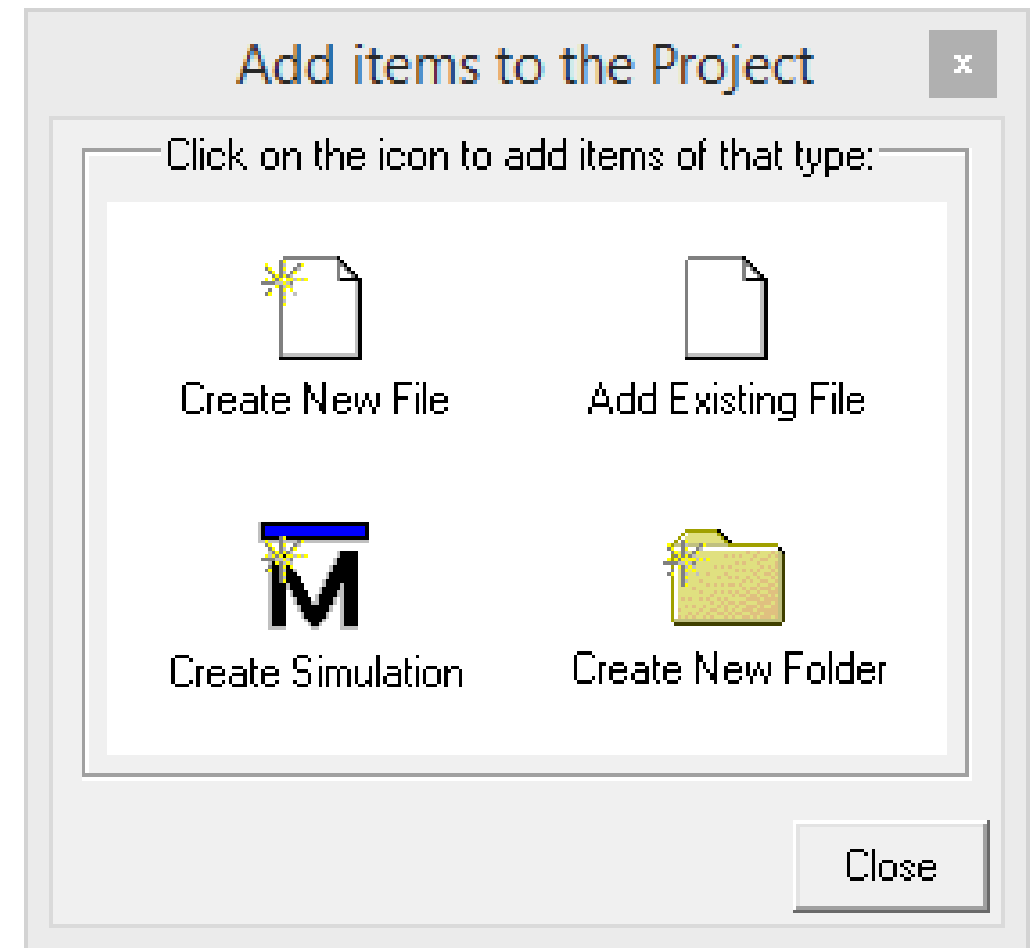
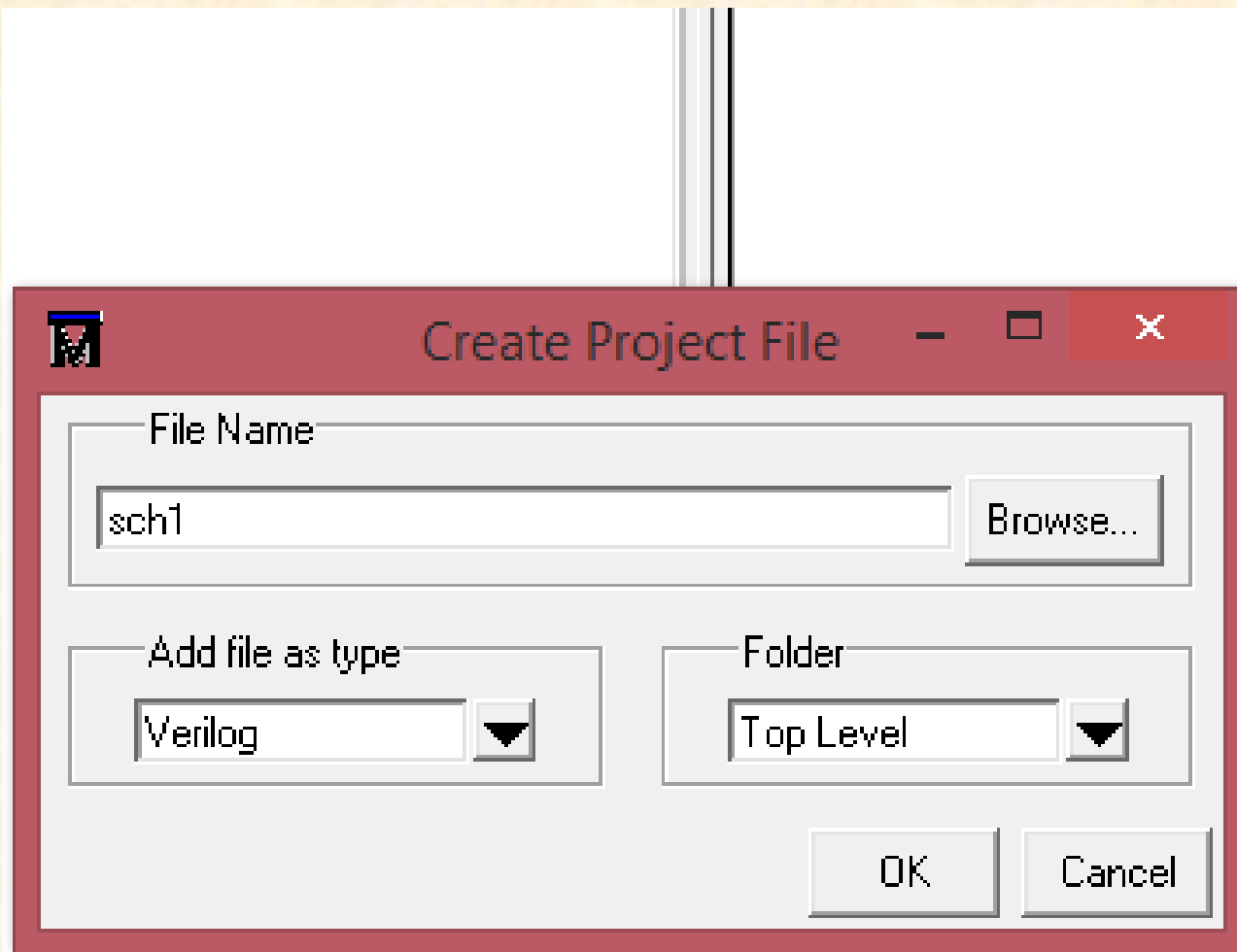
OK

Cancel

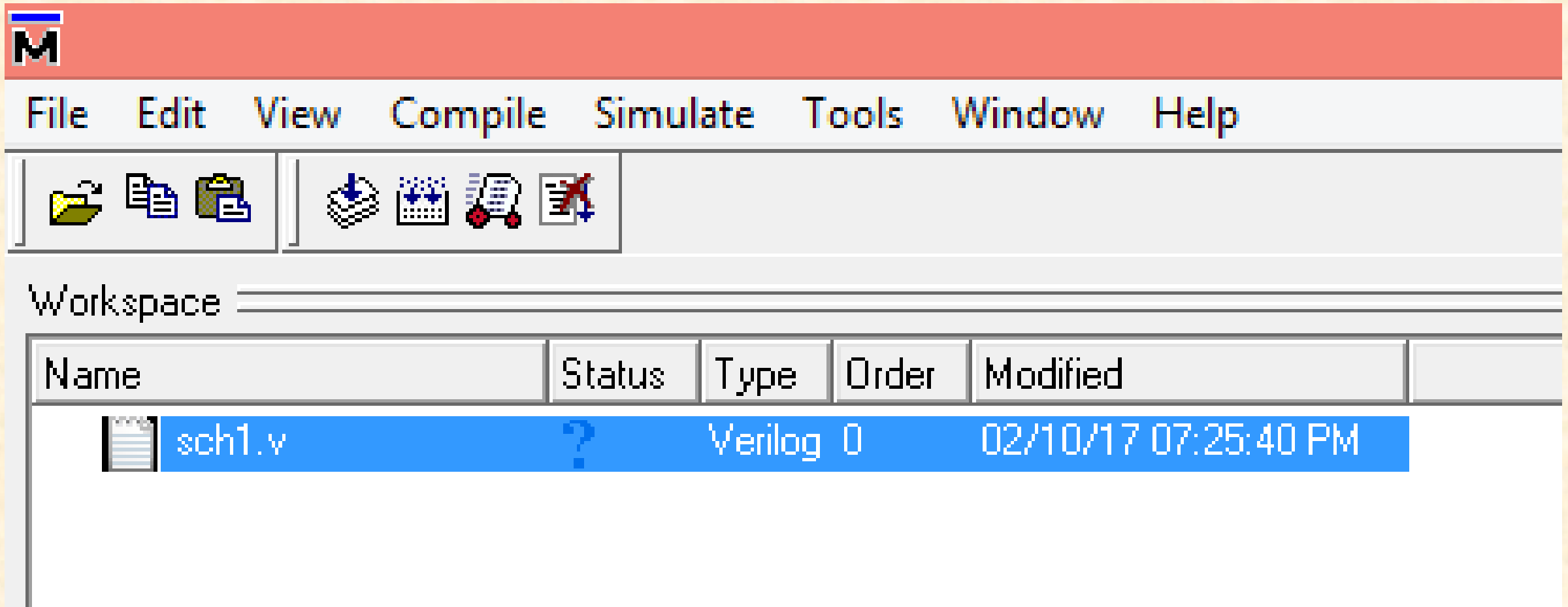
Click New File



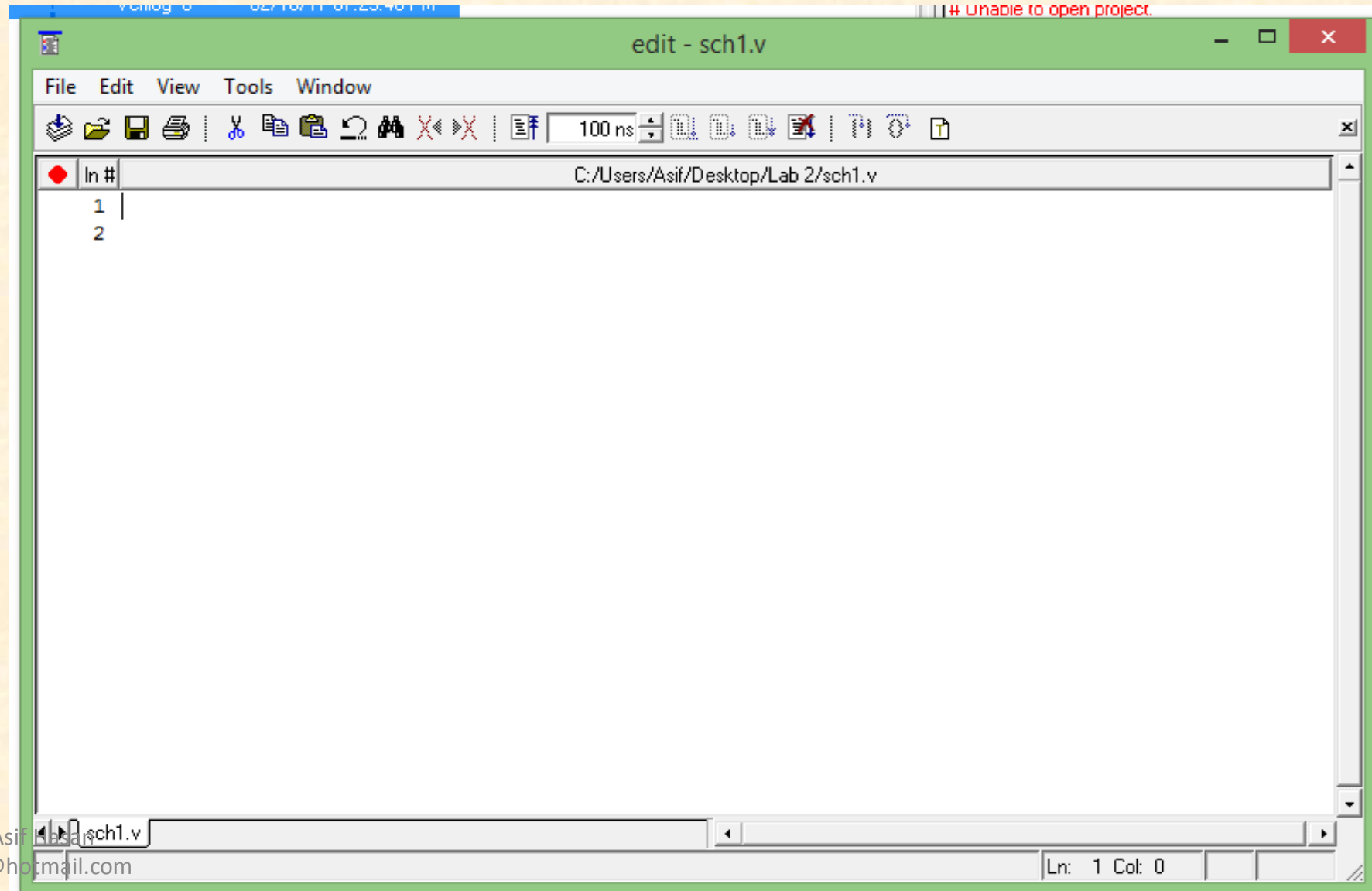
Give name and chose as below



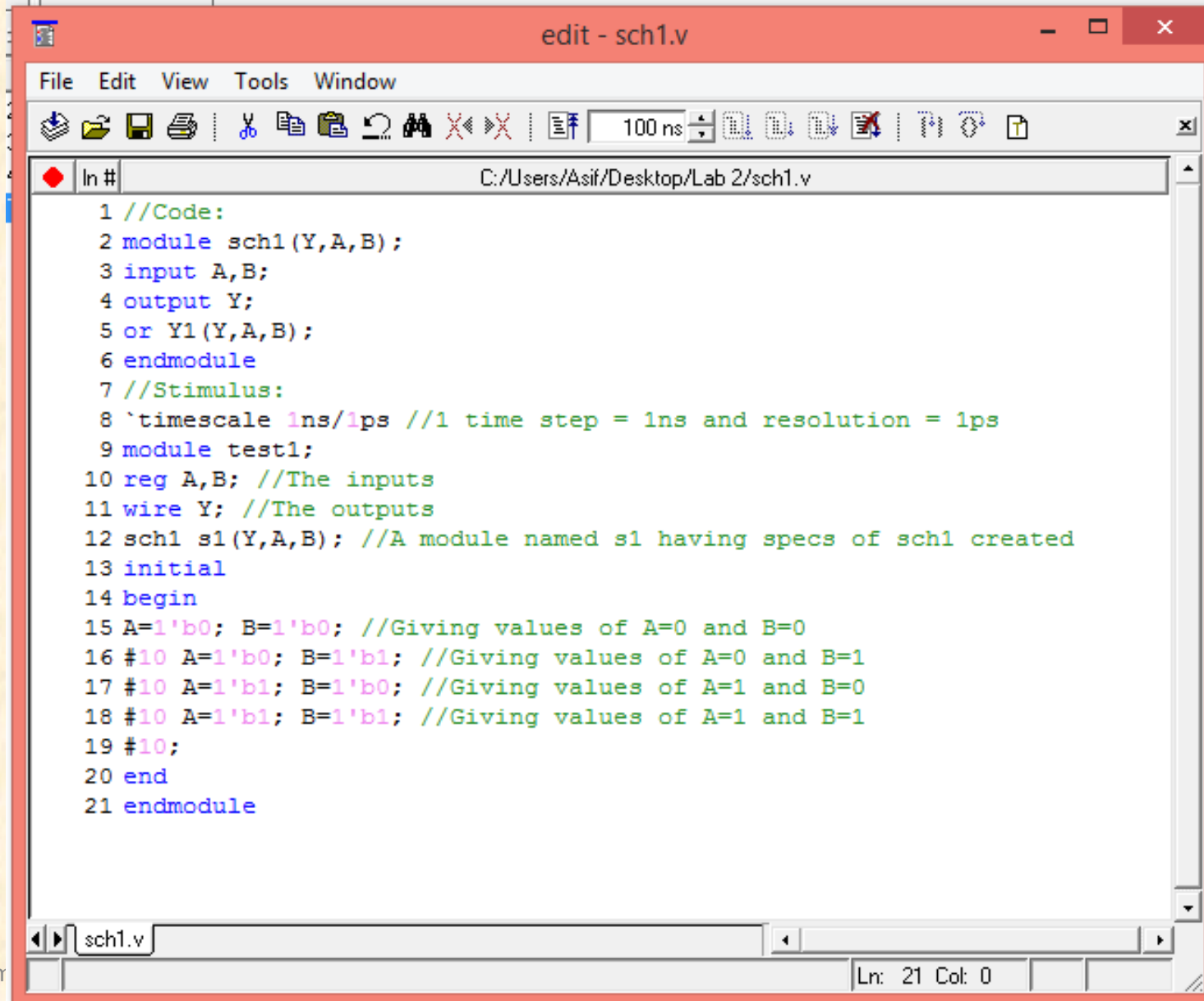
Double click on file



Below window will appear

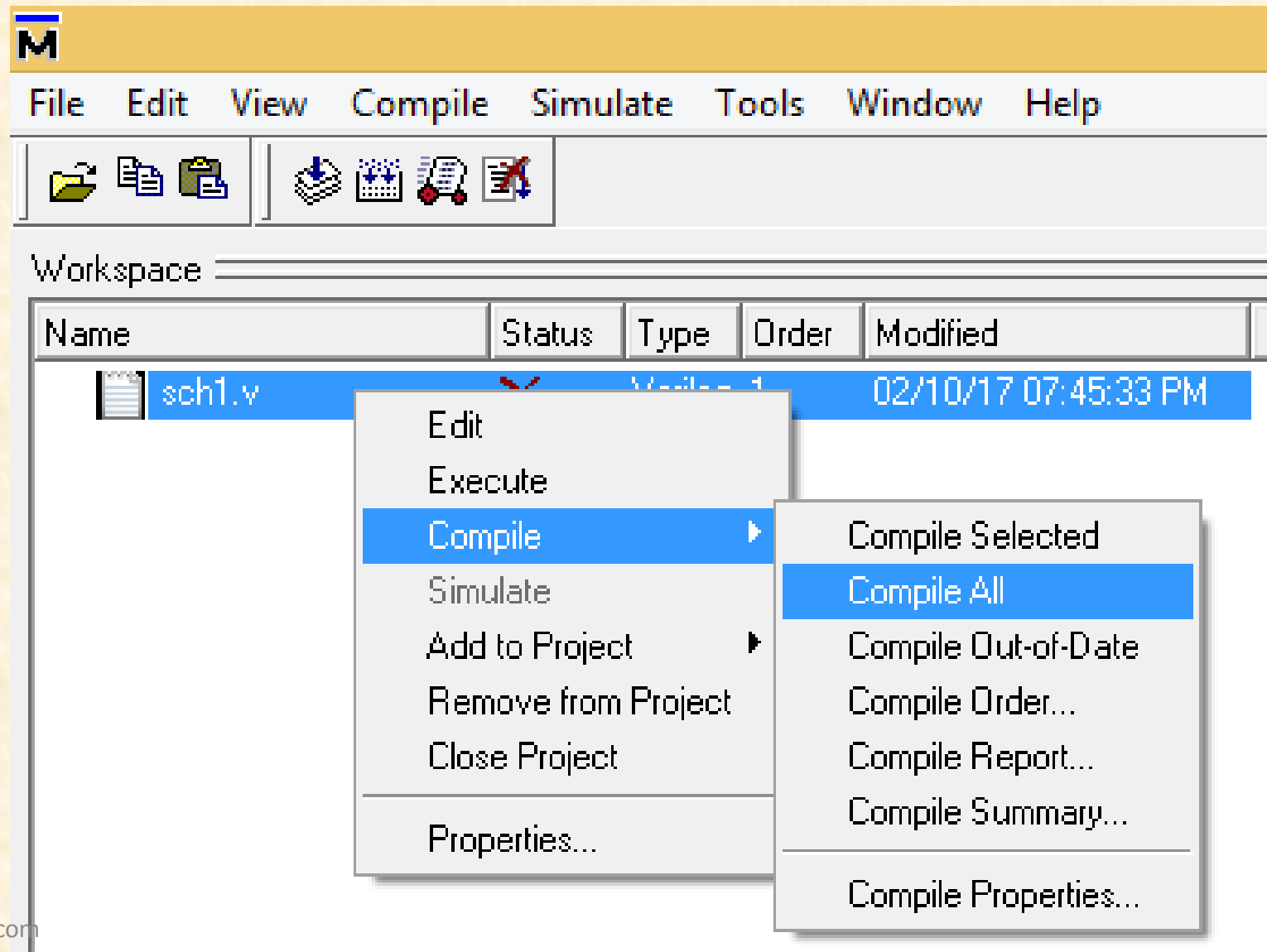


Type code as below

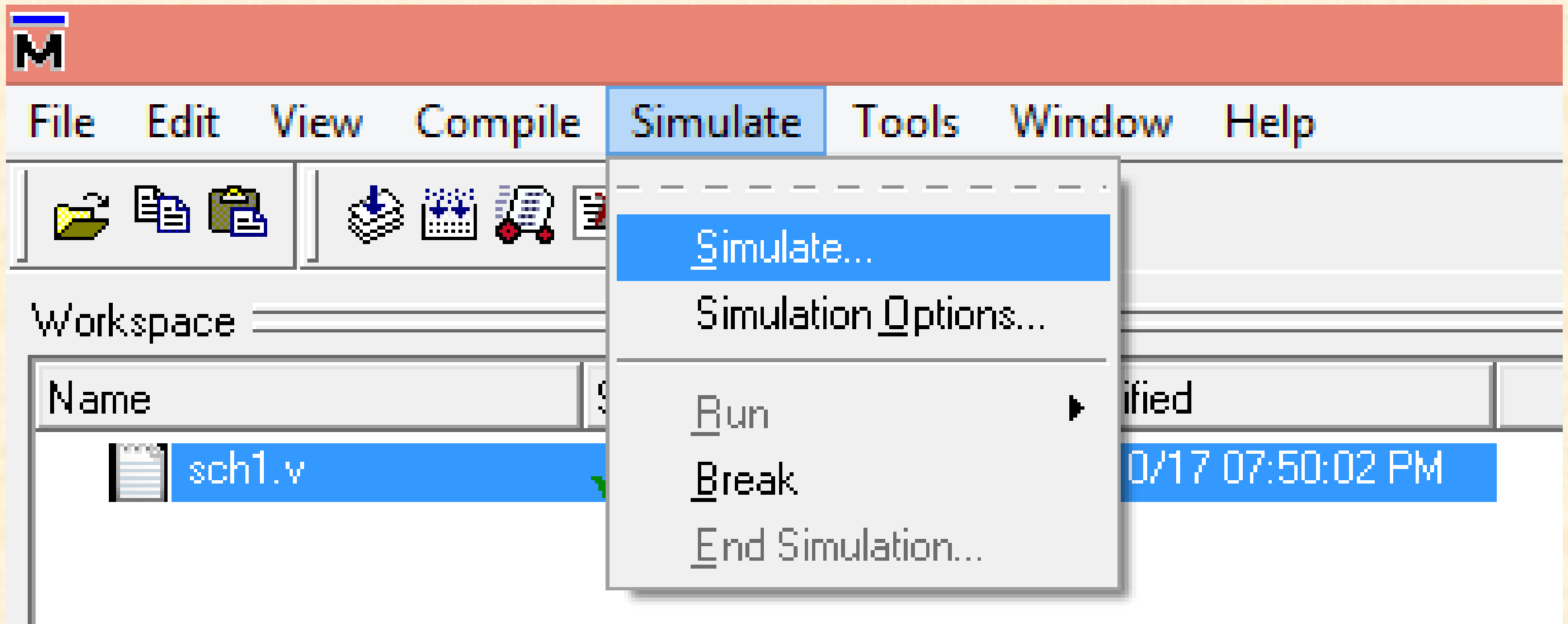


```
1 //Code:
2 module sch1(Y,A,B);
3 input A,B;
4 output Y;
5 or Y1(Y,A,B);
6 endmodule
7 //Stimulus:
8 `timescale 1ns/1ps //1 time step = 1ns and resolution = 1ps
9 module test1;
10 reg A,B; //The inputs
11 wire Y; //The outputs
12 sch1 s1(Y,A,B); //A module named s1 having specs of sch1 created
13 initial
14 begin
15 A=1'b0; B=1'b0; //Giving values of A=0 and B=0
16 #10 A=1'b0; B=1'b1; //Giving values of A=0 and B=1
17 #10 A=1'b1; B=1'b0; //Giving values of A=1 and B=0
18 #10 A=1'b1; B=1'b1; //Giving values of A=1 and B=1
19 #10;
20 end
21 endmodule
```

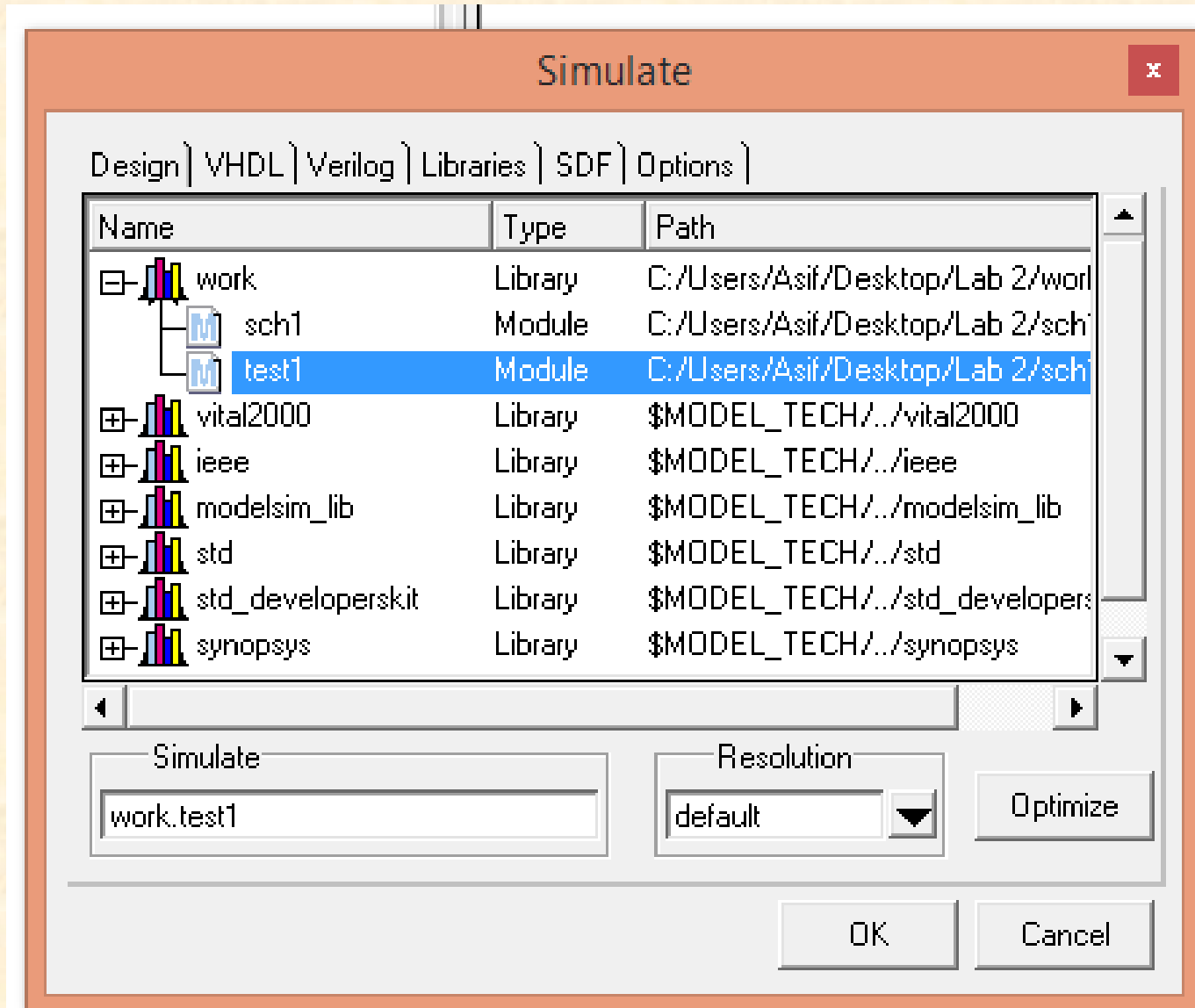
Compile code



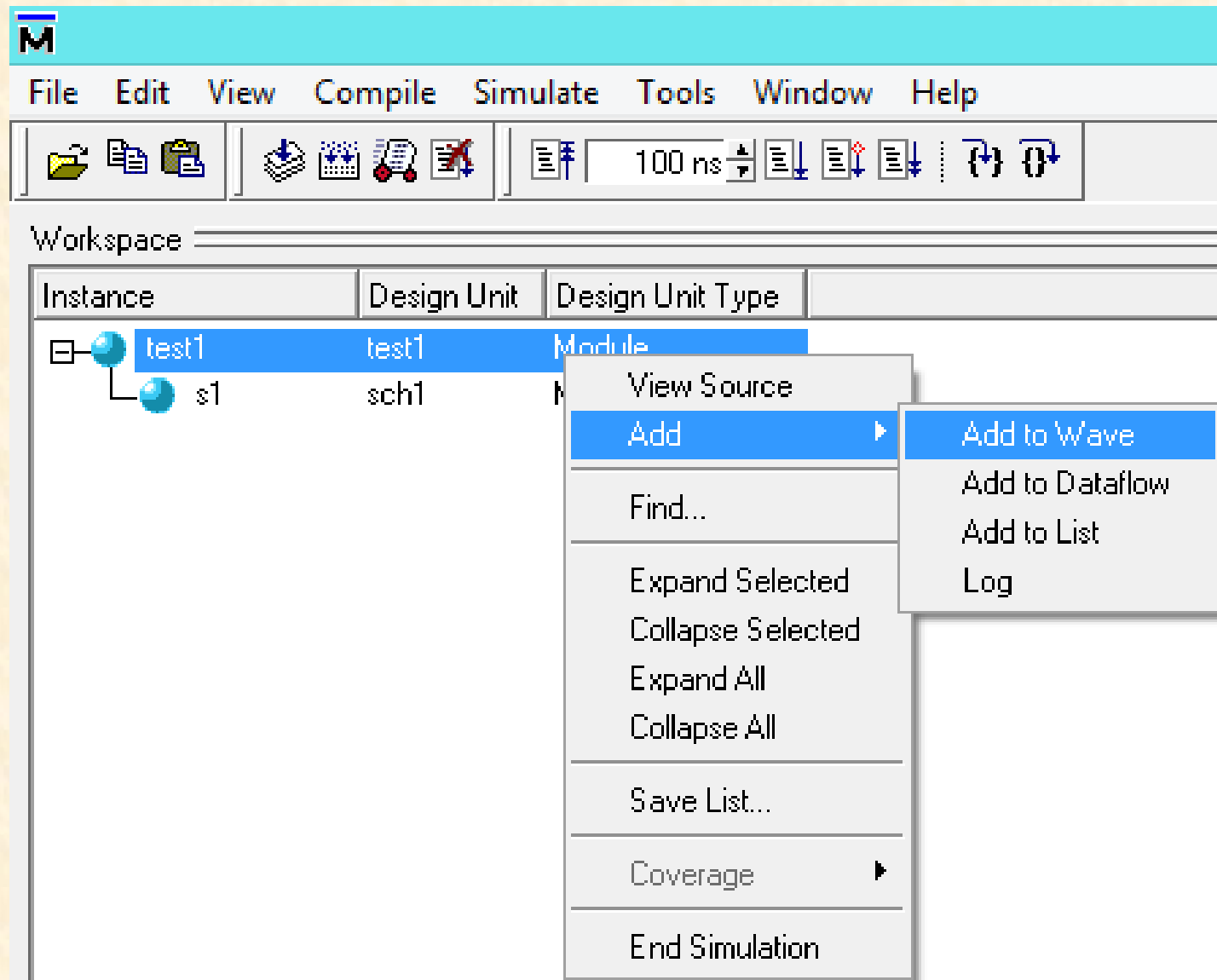
Click simulate



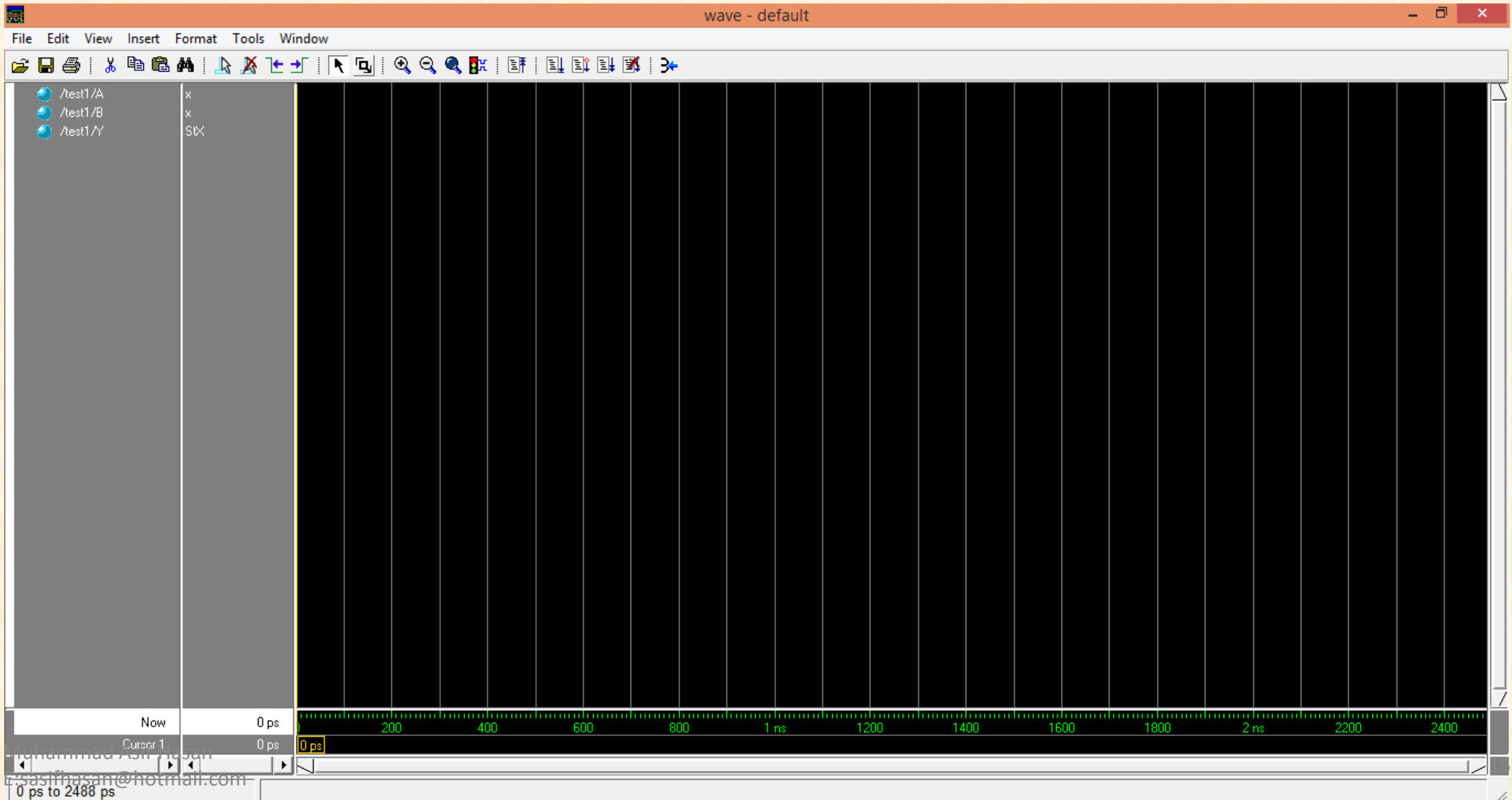
Chose test1



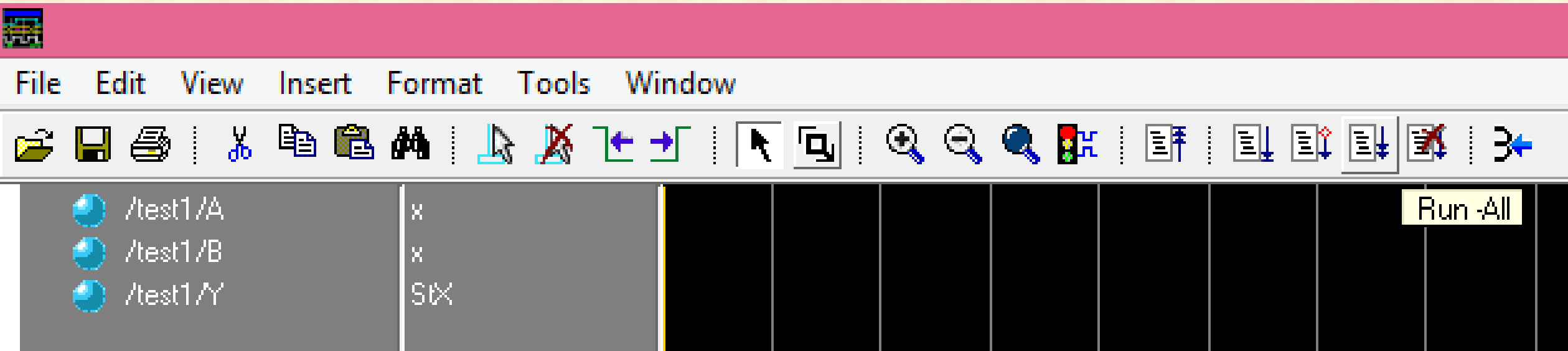
Add to wave



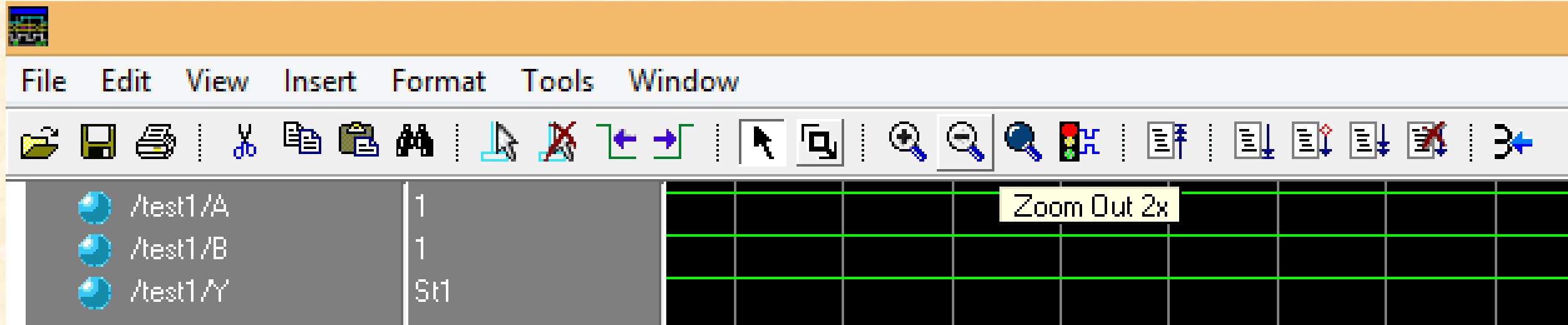
Below window will appear



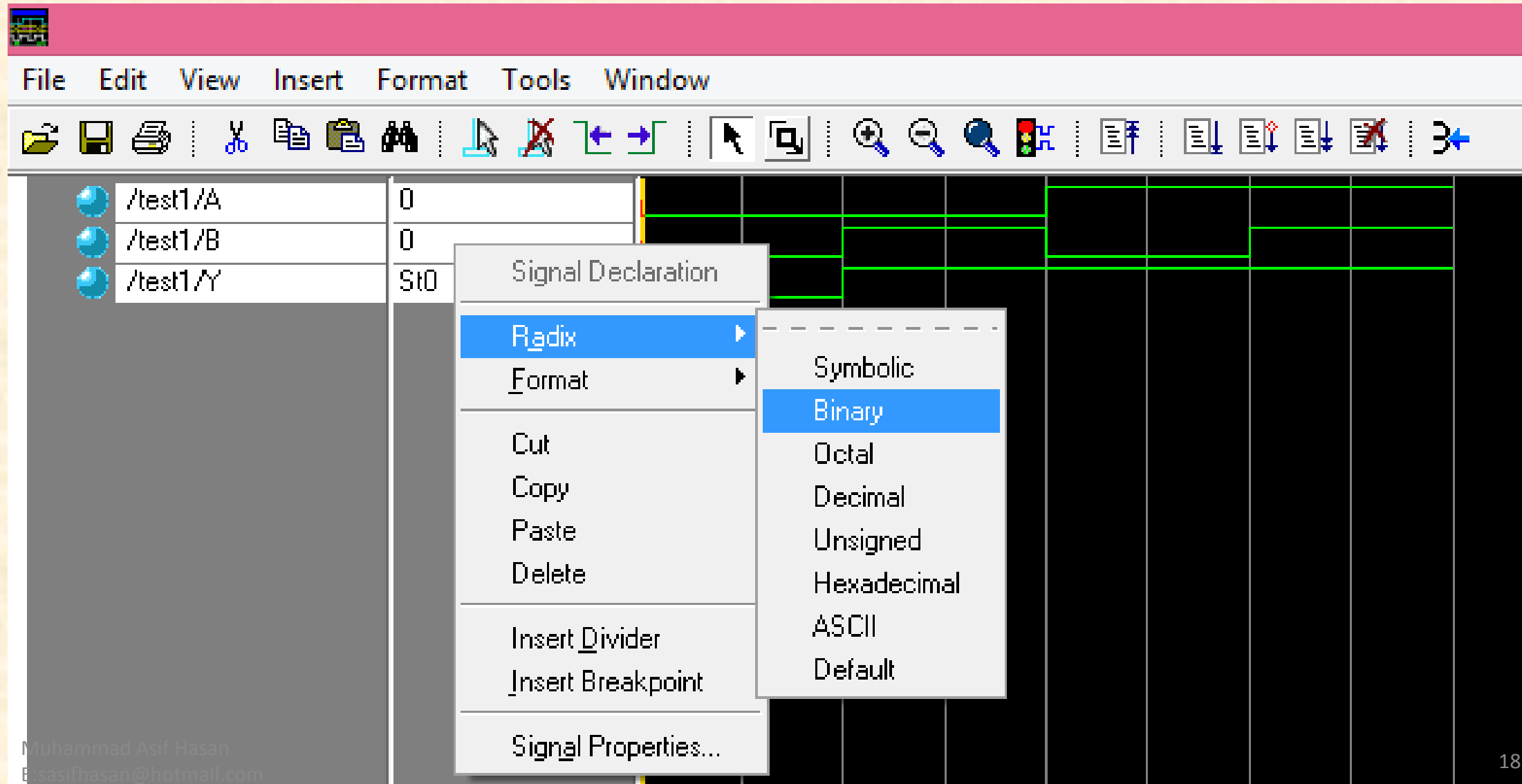
Click Run - All



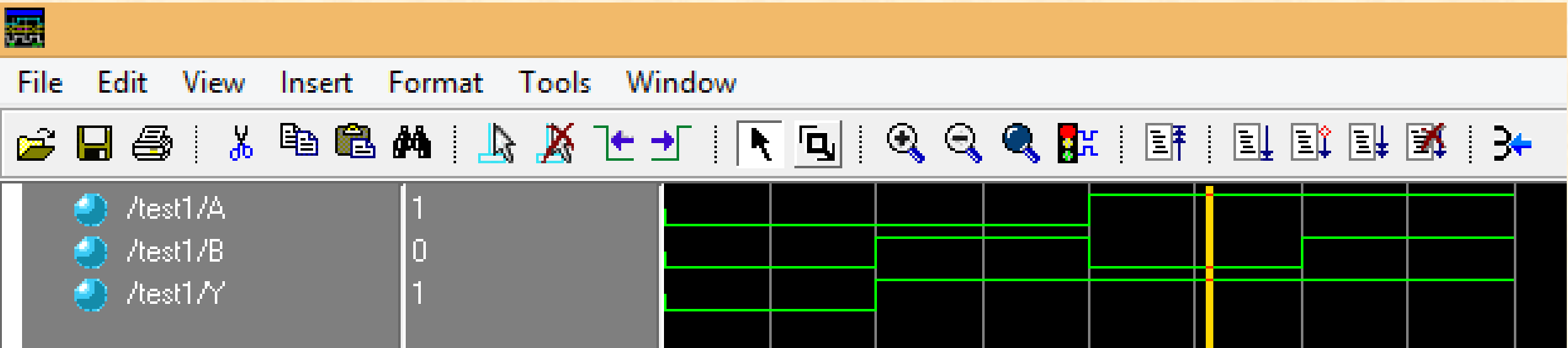
Keep clicking zoom out






Select radix as binary



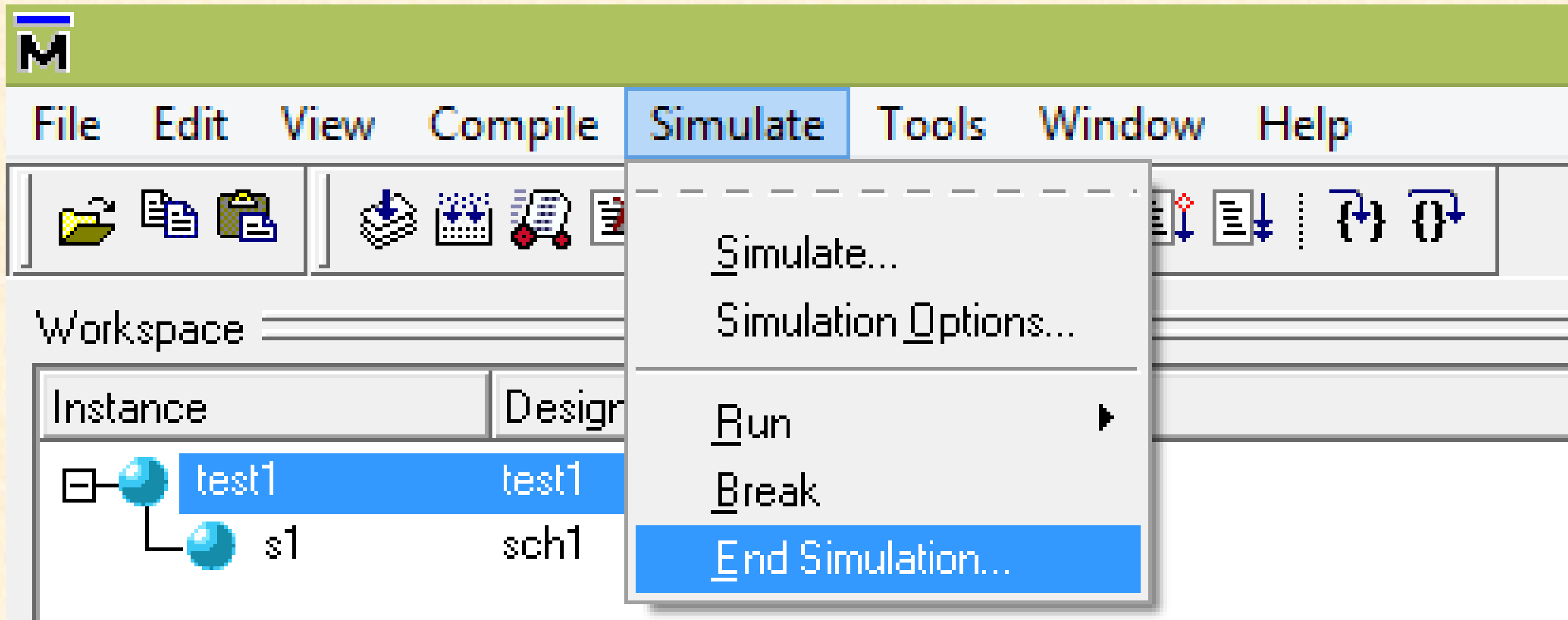
Example result



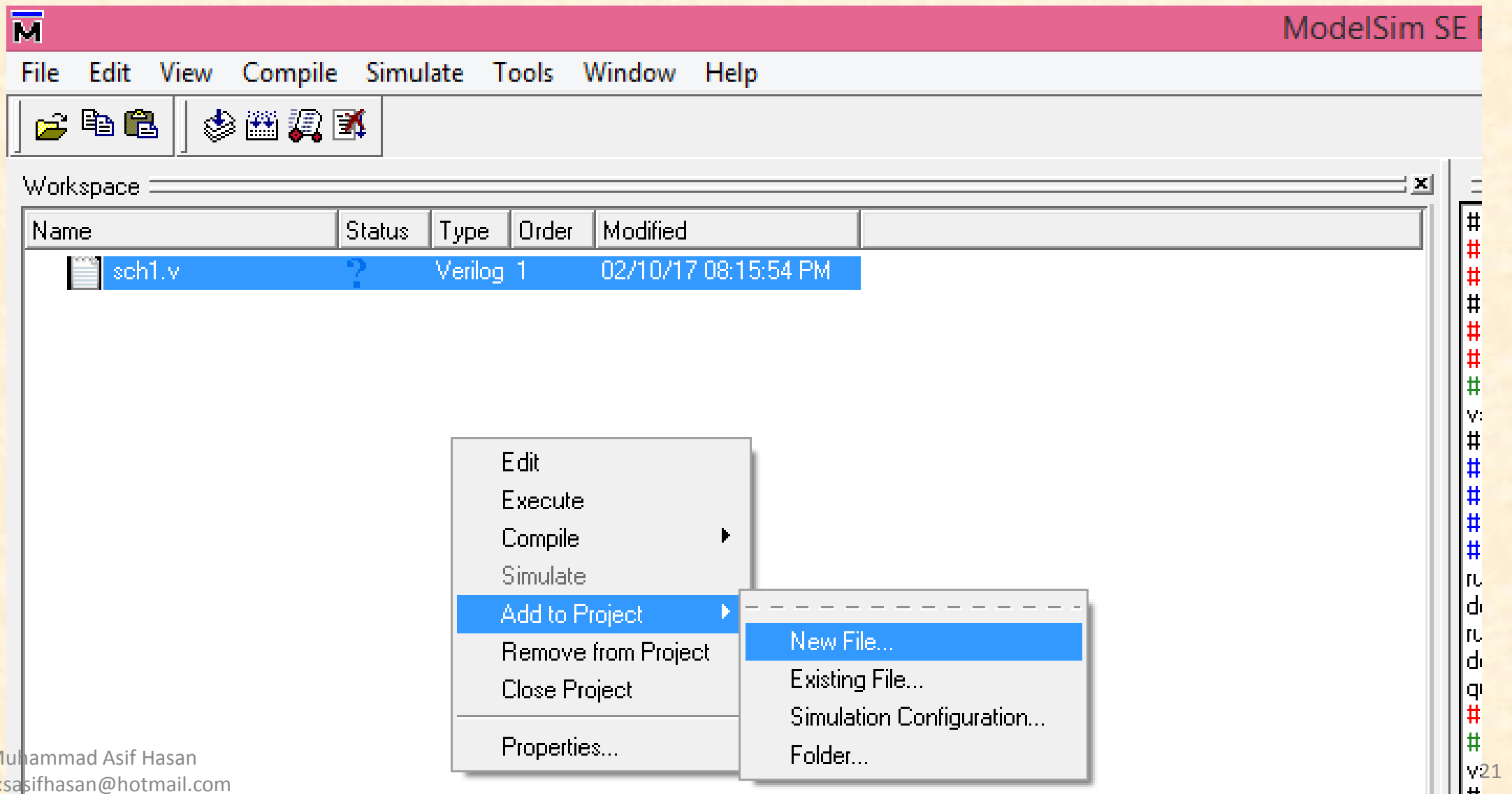
The screenshot shows a software interface with a menu bar (File, Edit, View, Insert, Format, Tools, Window) and a toolbar containing various icons for file operations, editing, and navigation. Below the toolbar is a table with three columns and four rows. The first column contains file paths, the second column contains numerical values, and the third column contains a grid of cells with green borders and a yellow vertical line.

 /test1/A	1	
 /test1/B	0	
 /test1/Y	1	

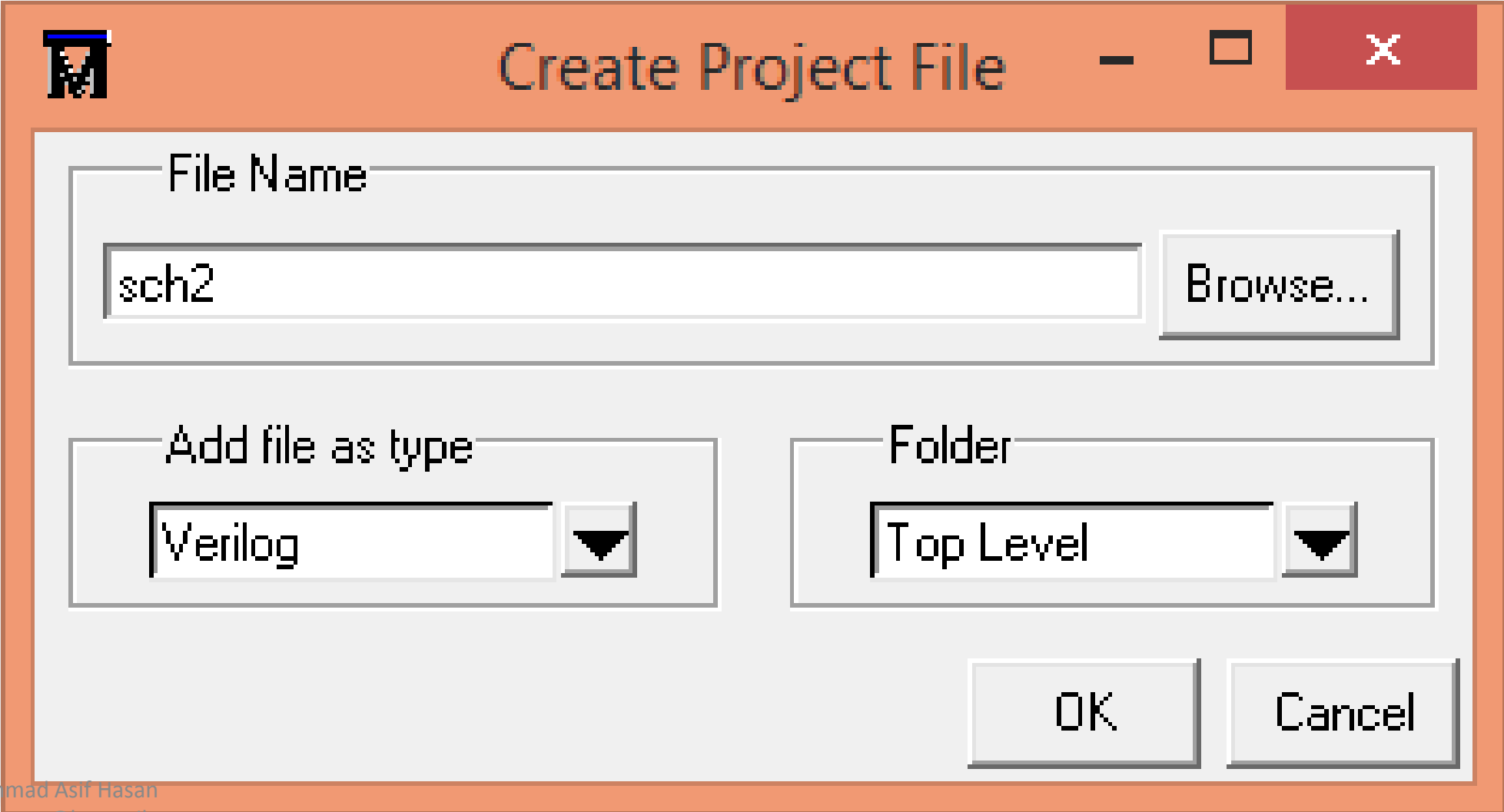
Click End Simulation



Create new file



Give name and chose as below



Create Project File

File Name

sch2

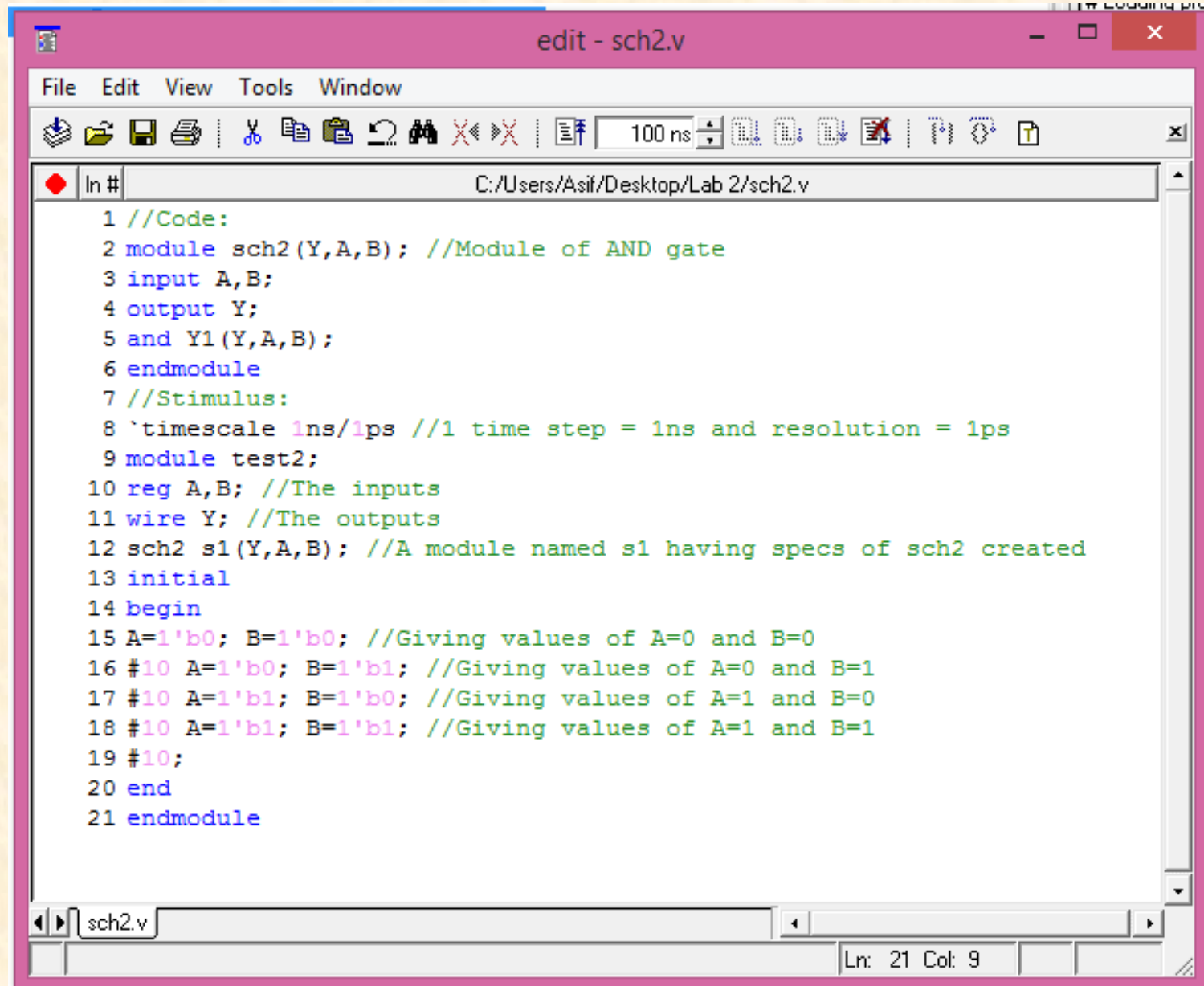
Add file as type

Verilog

Folder

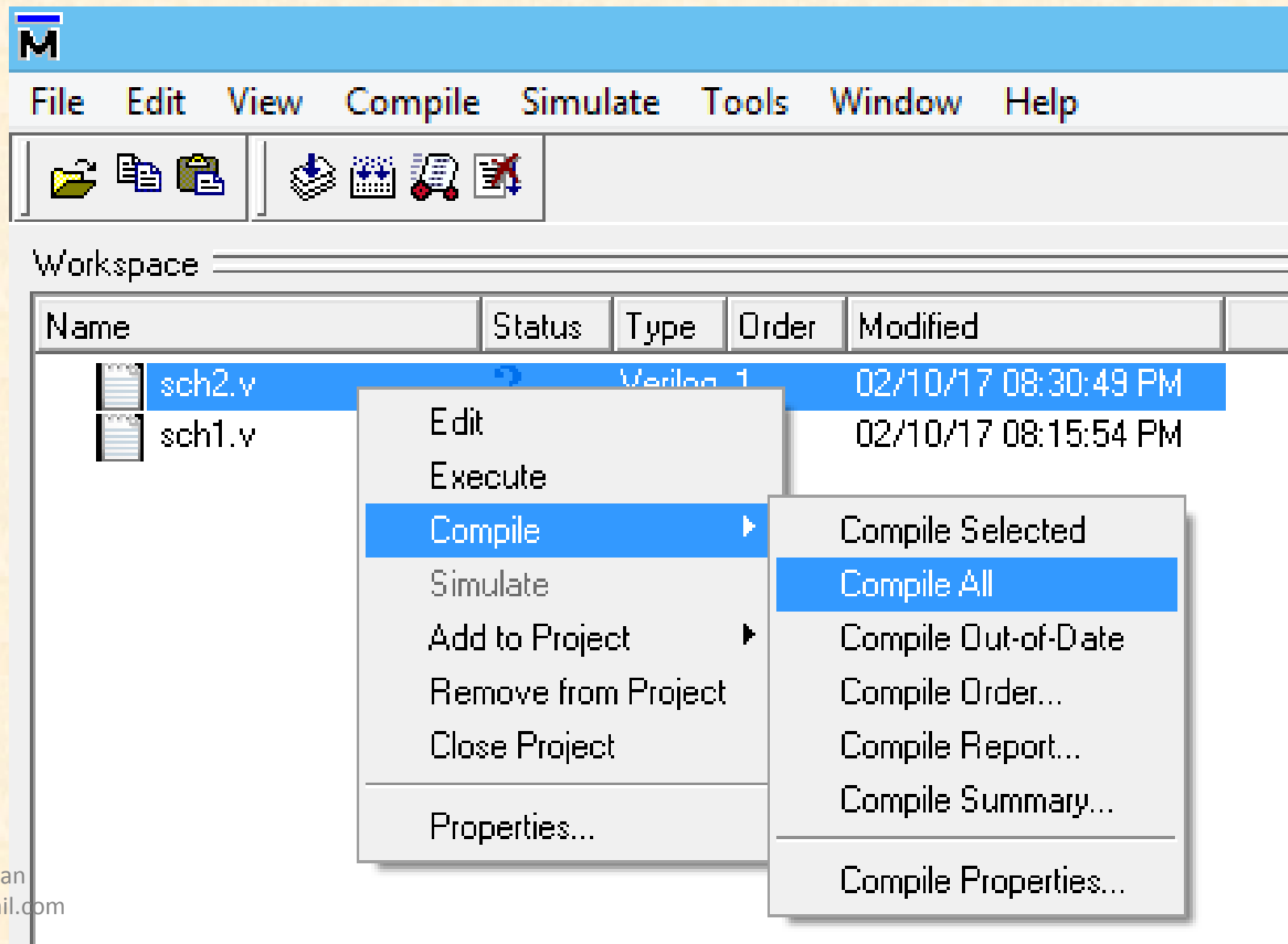
Top Level

Type code as below

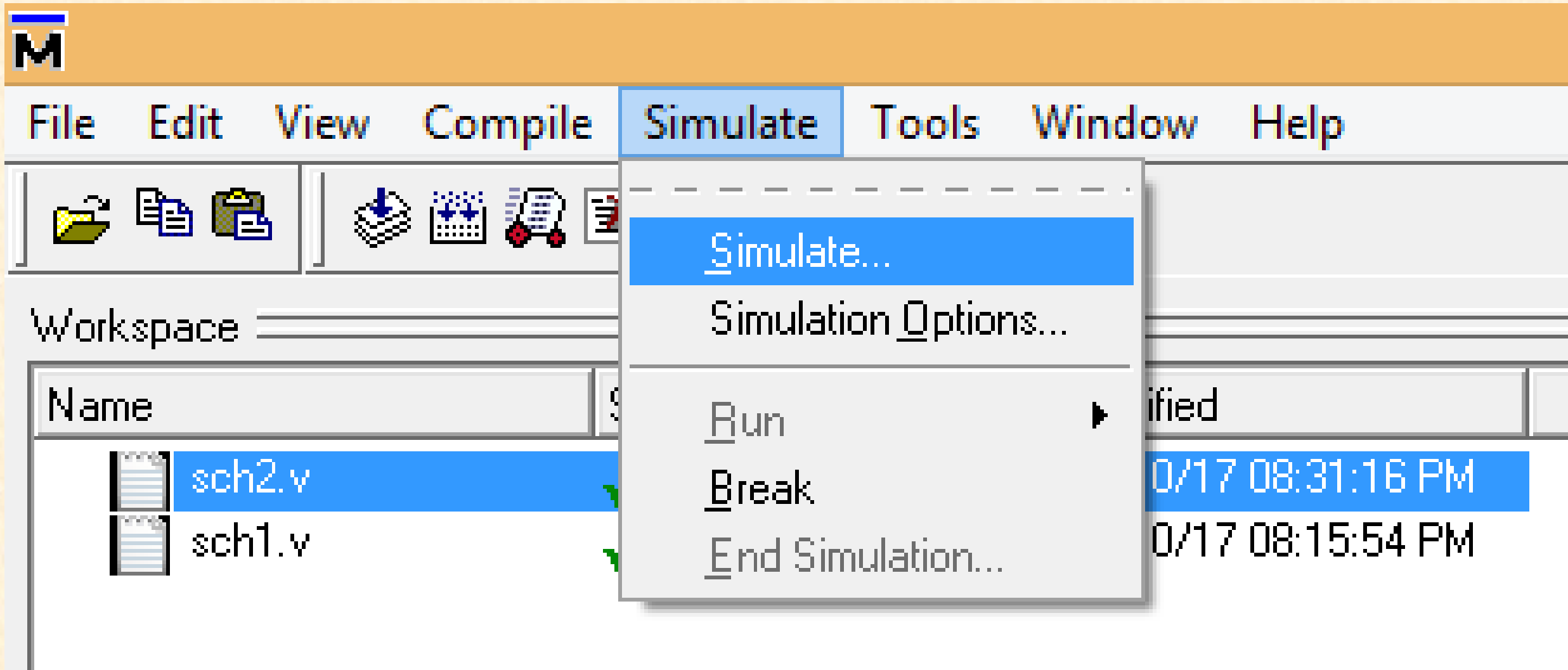


```
1 //Code:
2 module sch2(Y,A,B); //Module of AND gate
3 input A,B;
4 output Y;
5 and Y1(Y,A,B);
6 endmodule
7 //Stimulus:
8 `timescale 1ns/1ps //1 time step = 1ns and resolution = 1ps
9 module test2;
10 reg A,B; //The inputs
11 wire Y; //The outputs
12 sch2 s1(Y,A,B); //A module named s1 having specs of sch2 created
13 initial
14 begin
15 A=1'b0; B=1'b0; //Giving values of A=0 and B=0
16 #10 A=1'b0; B=1'b1; //Giving values of A=0 and B=1
17 #10 A=1'b1; B=1'b0; //Giving values of A=1 and B=0
18 #10 A=1'b1; B=1'b1; //Giving values of A=1 and B=1
19 #10;
20 end
21 endmodule
```

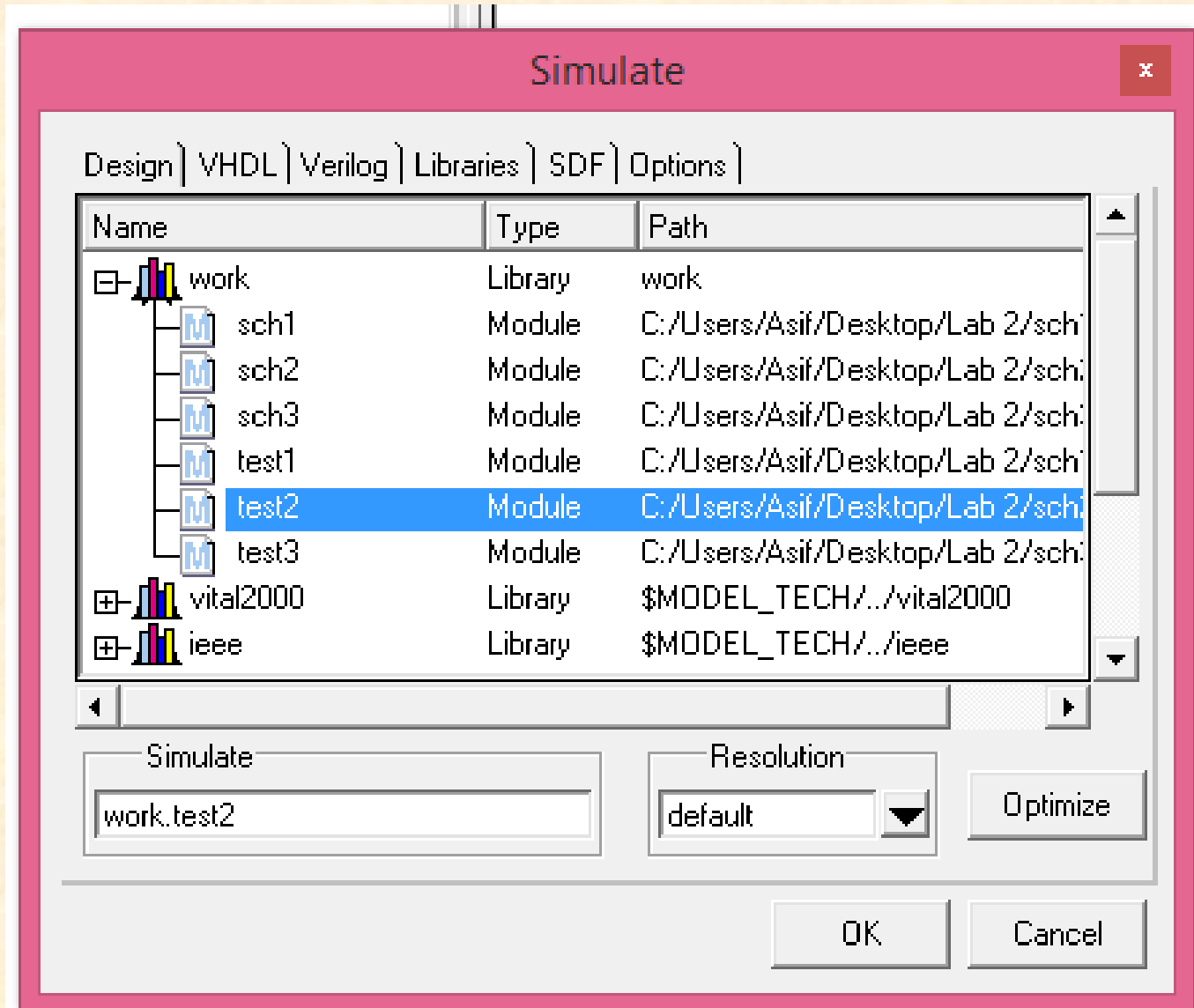
Compile code



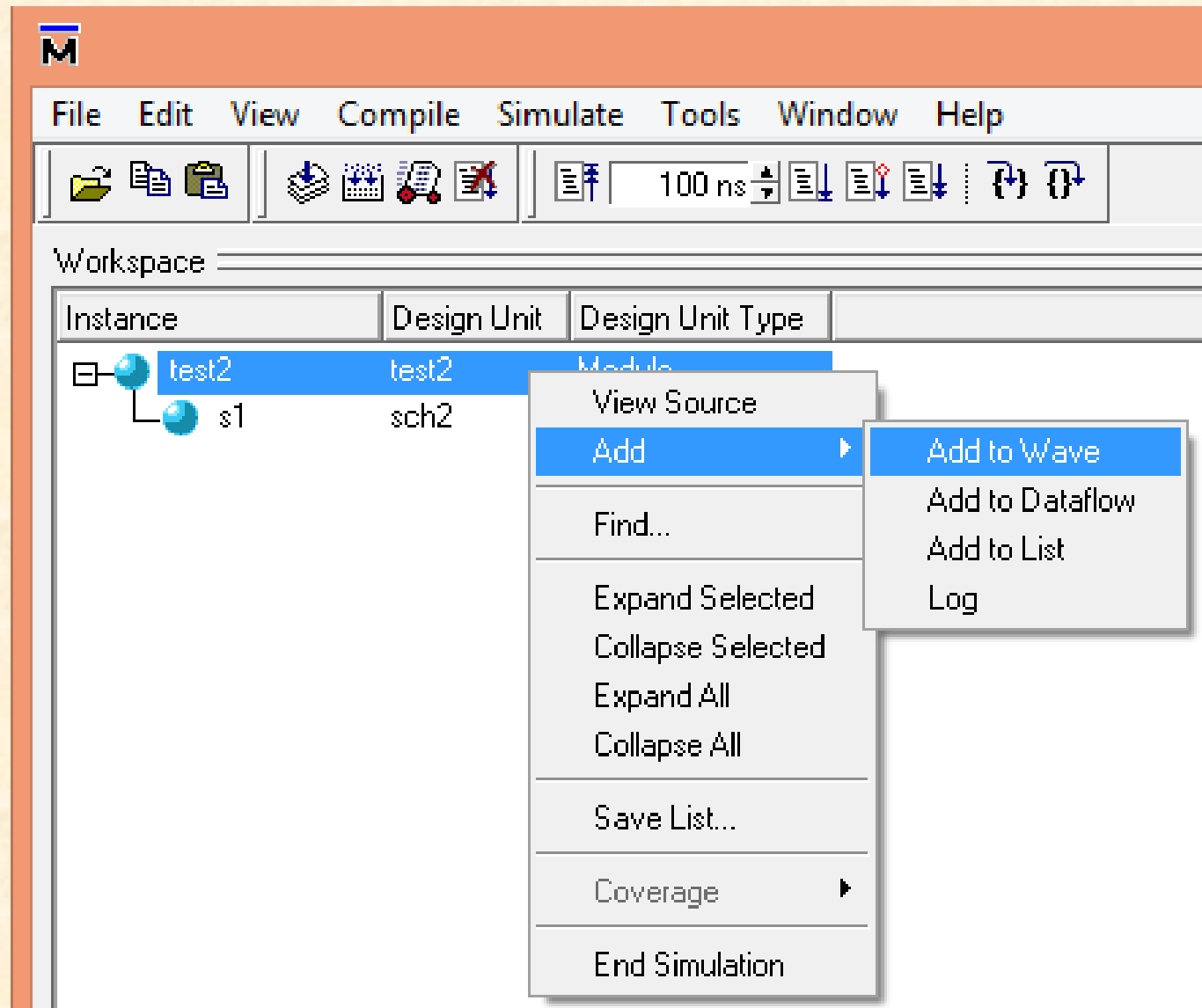
Click simulate



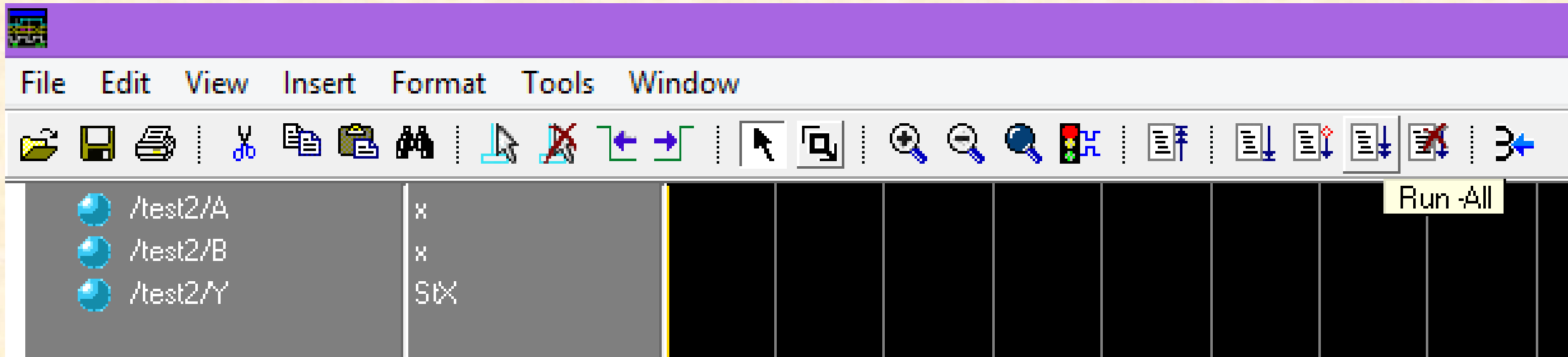
Chose test2



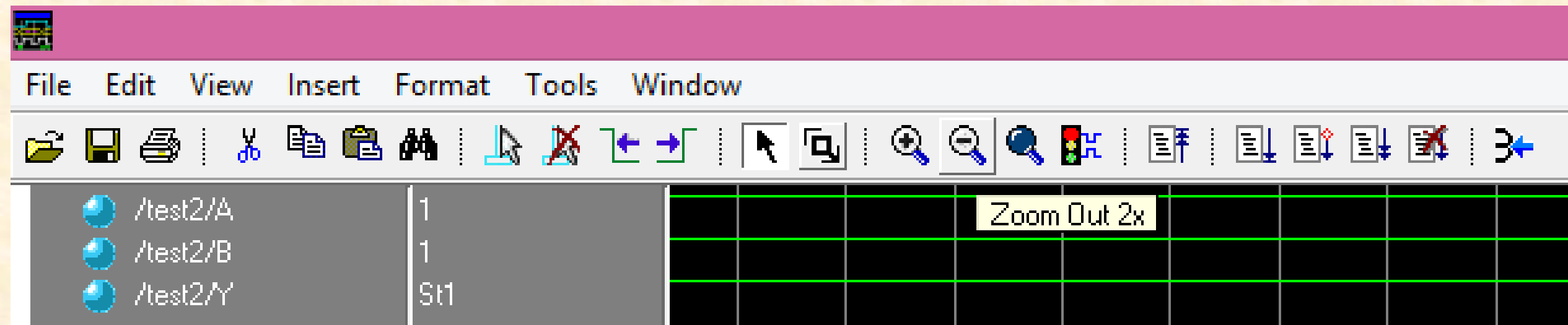
Add to wave



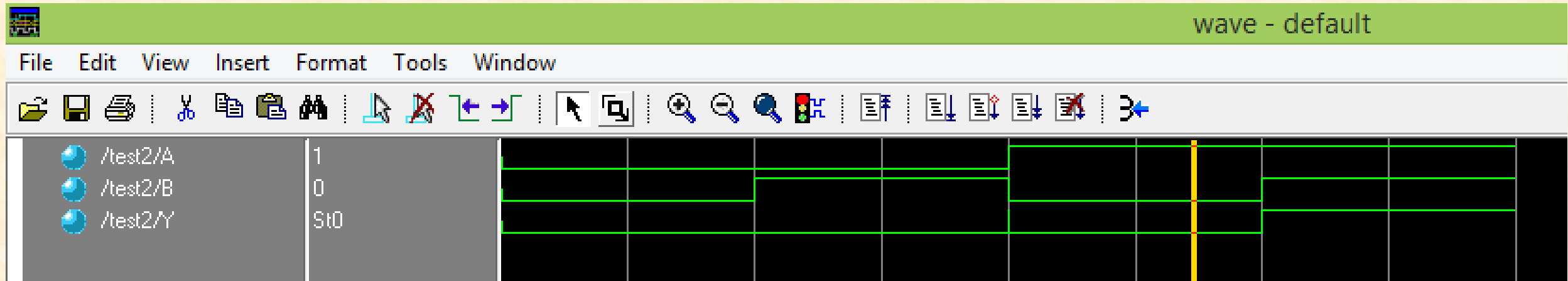
Click Run - All



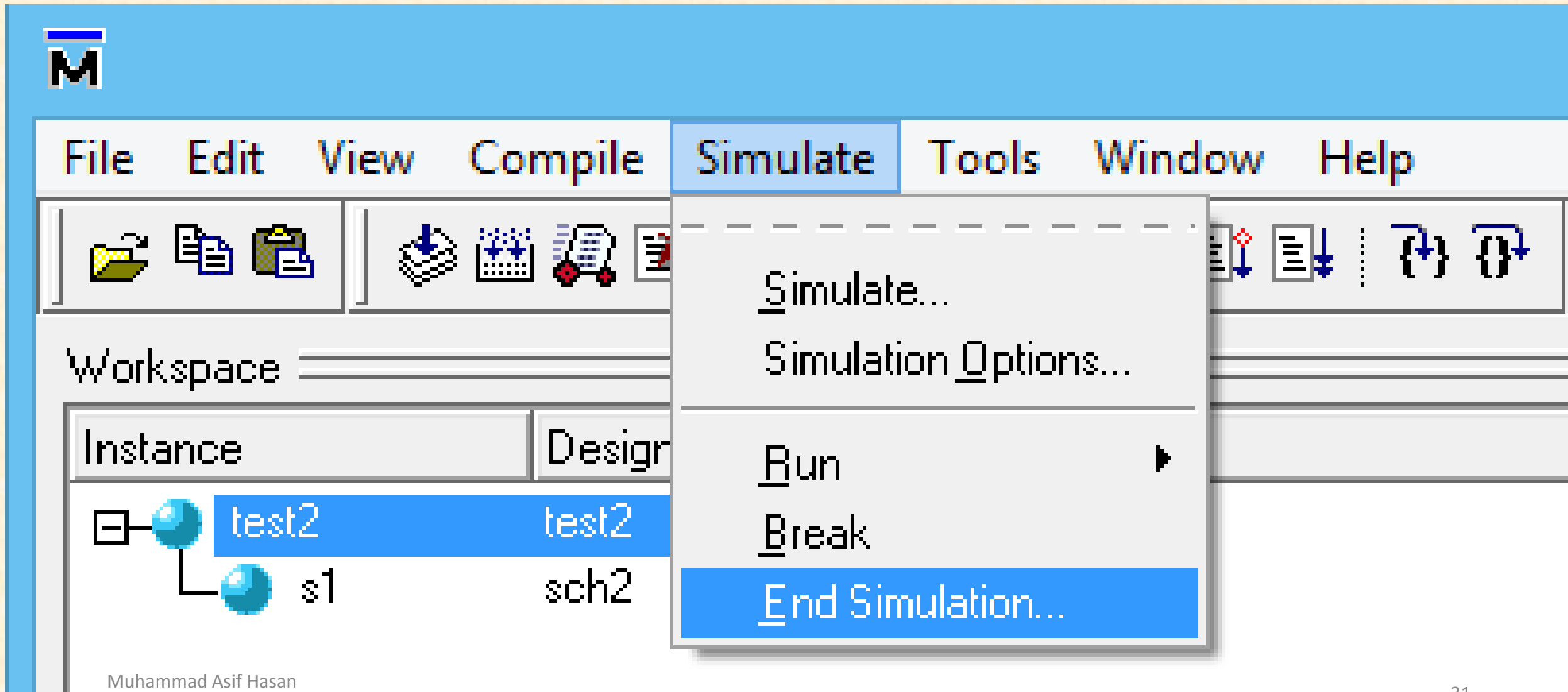
Keep clicking zoom out



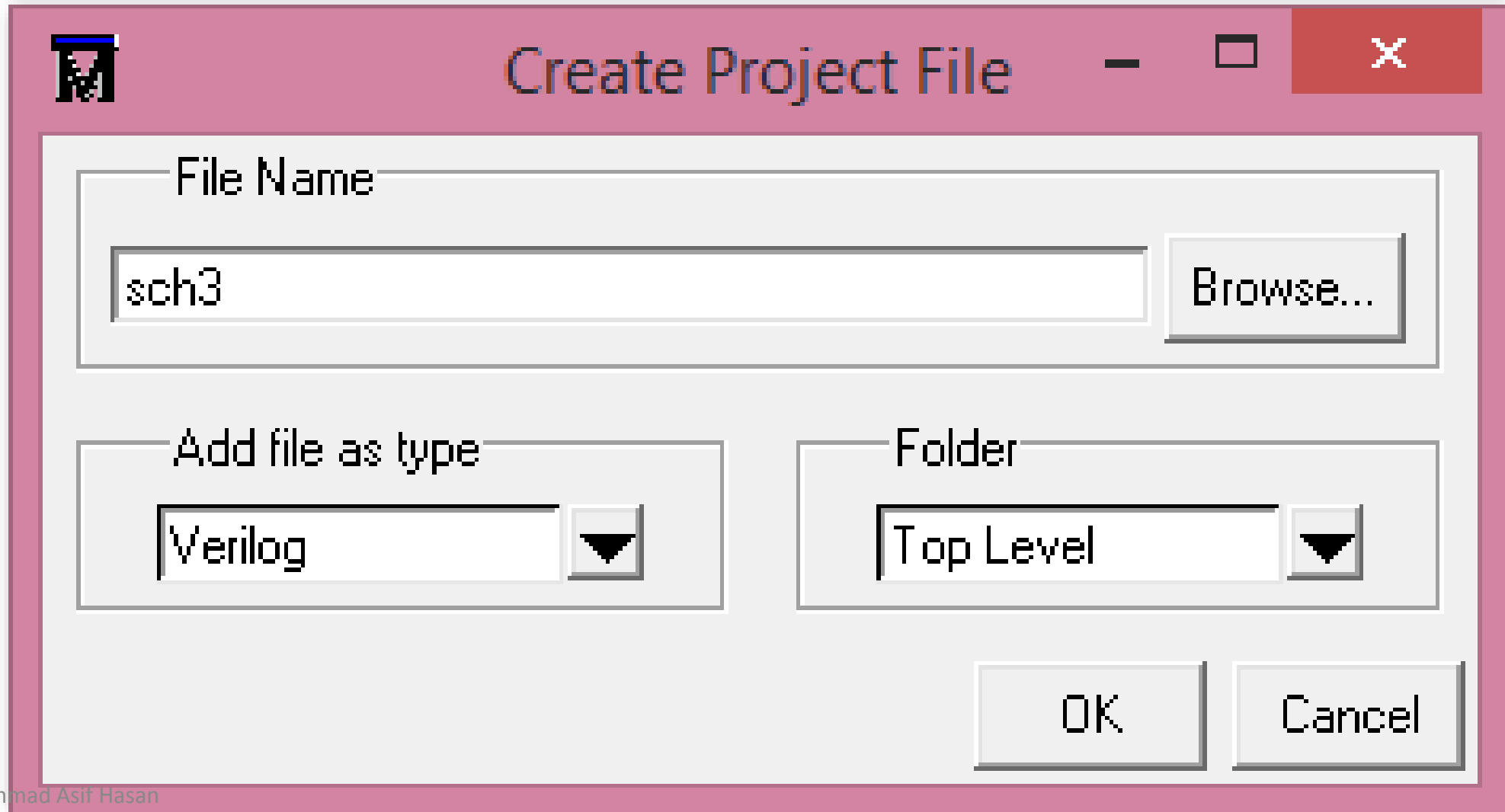
Example result



Click End Simulation



Create new file, Give name and chose as below



Create Project File

File Name

sch3

Browse...

Add file as type

Verilog

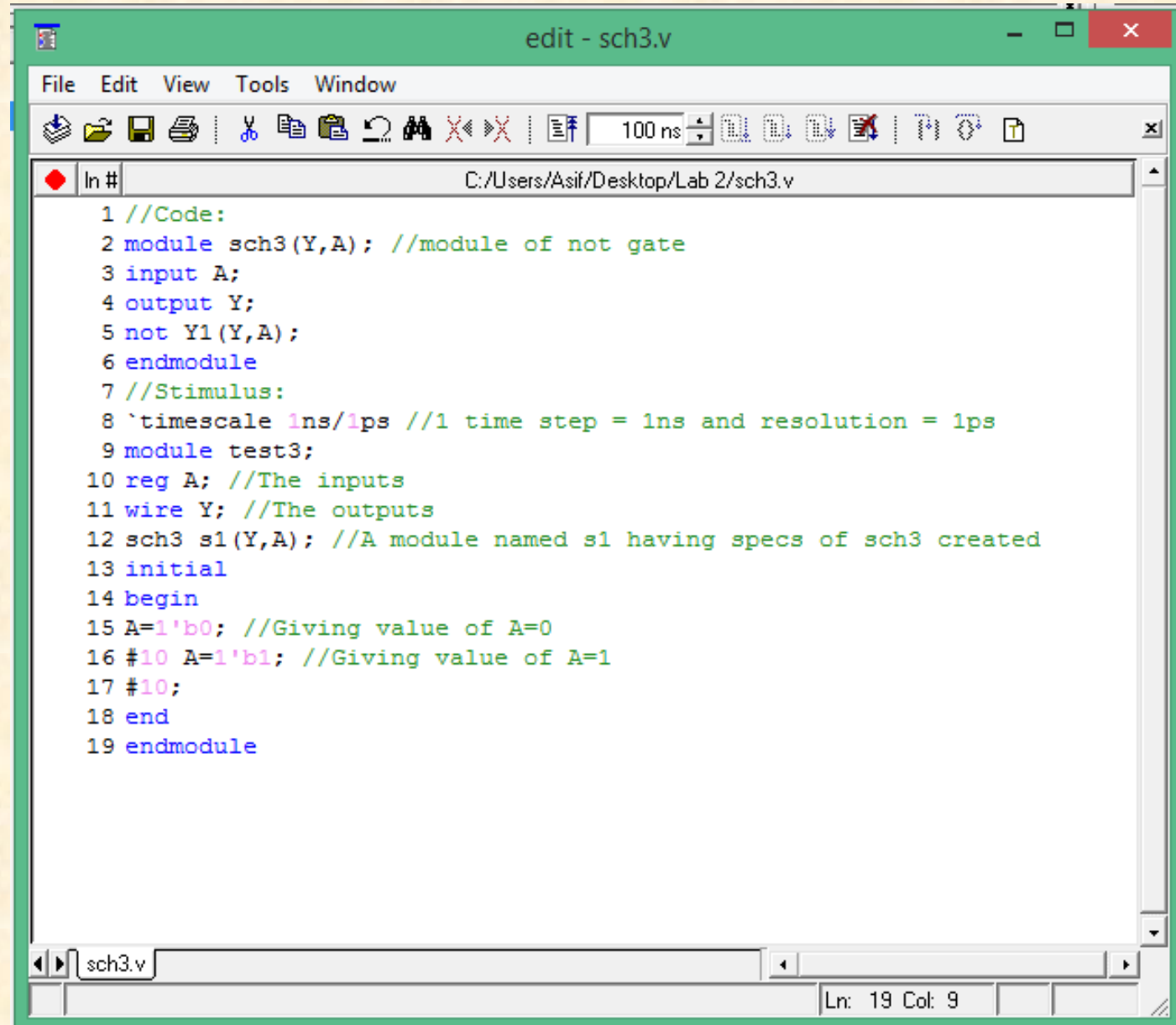
Folder

Top Level

OK

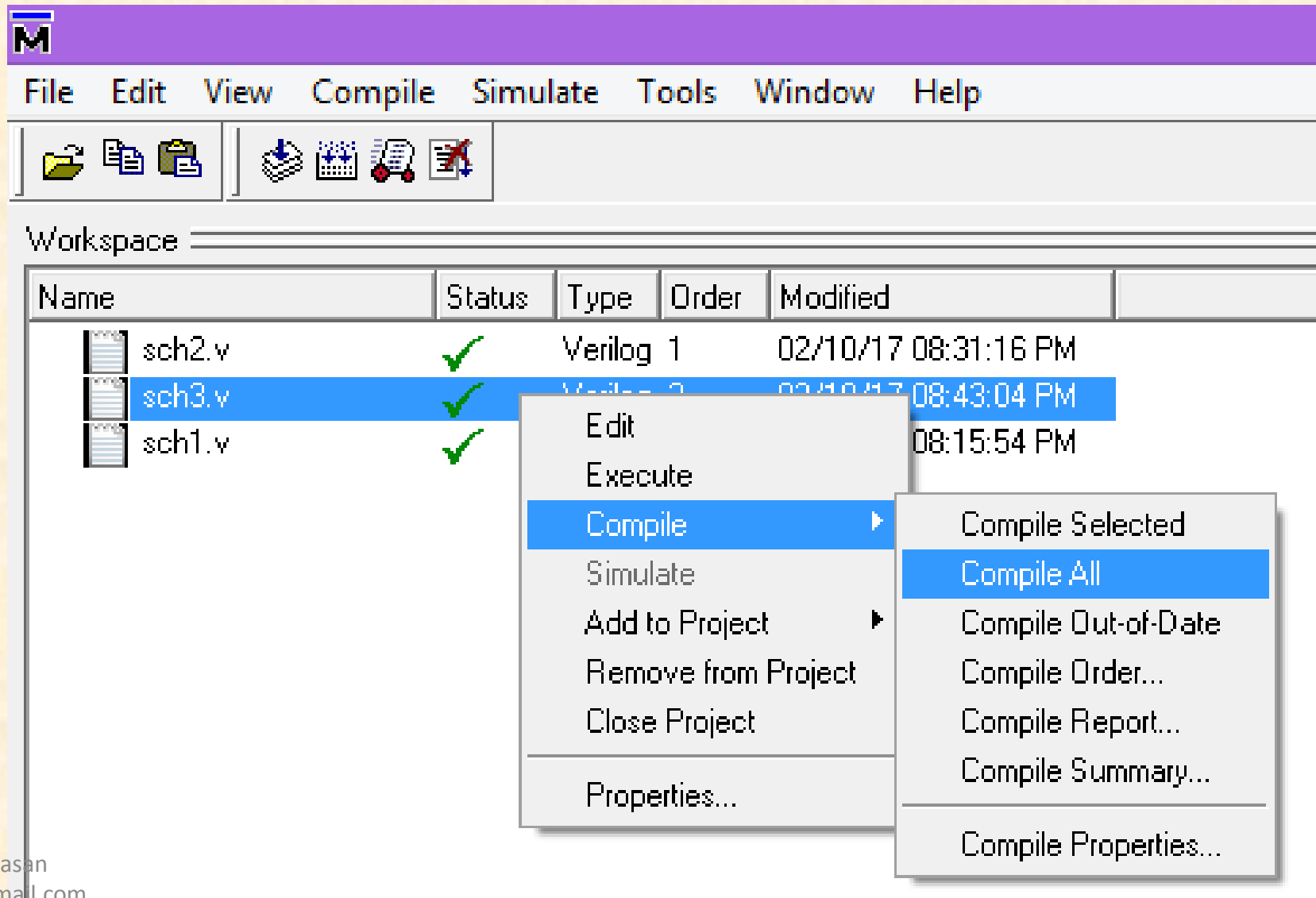
Cancel

Type code as below

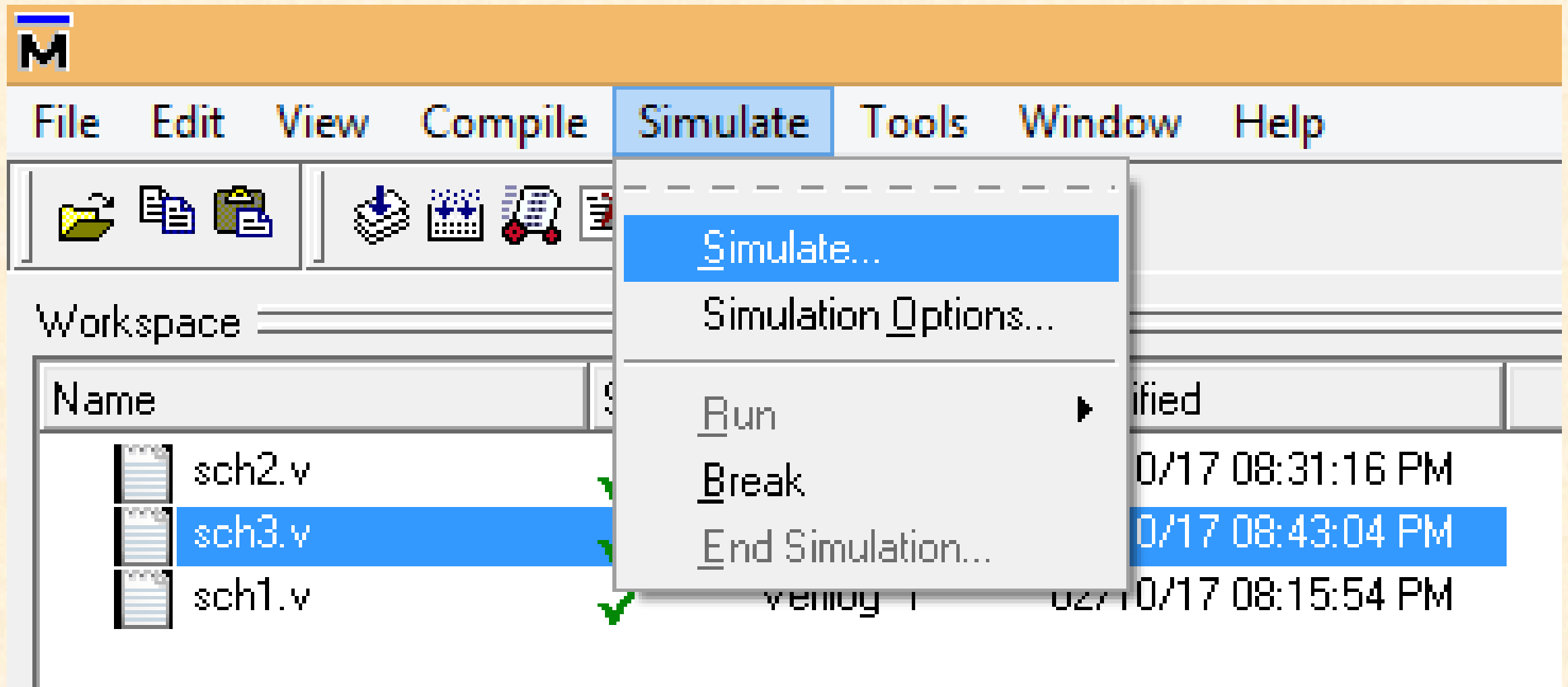


```
1 //Code:
2 module sch3(Y,A); //module of not gate
3 input A;
4 output Y;
5 not Y1(Y,A);
6 endmodule
7 //Stimulus:
8 `timescale 1ns/1ps //1 time step = 1ns and resolution = 1ps
9 module test3;
10 reg A; //The inputs
11 wire Y; //The outputs
12 sch3 s1(Y,A); //A module named s1 having specs of sch3 created
13 initial
14 begin
15 A=1'b0; //Giving value of A=0
16 #10 A=1'b1; //Giving value of A=1
17 #10;
18 end
19 endmodule
```

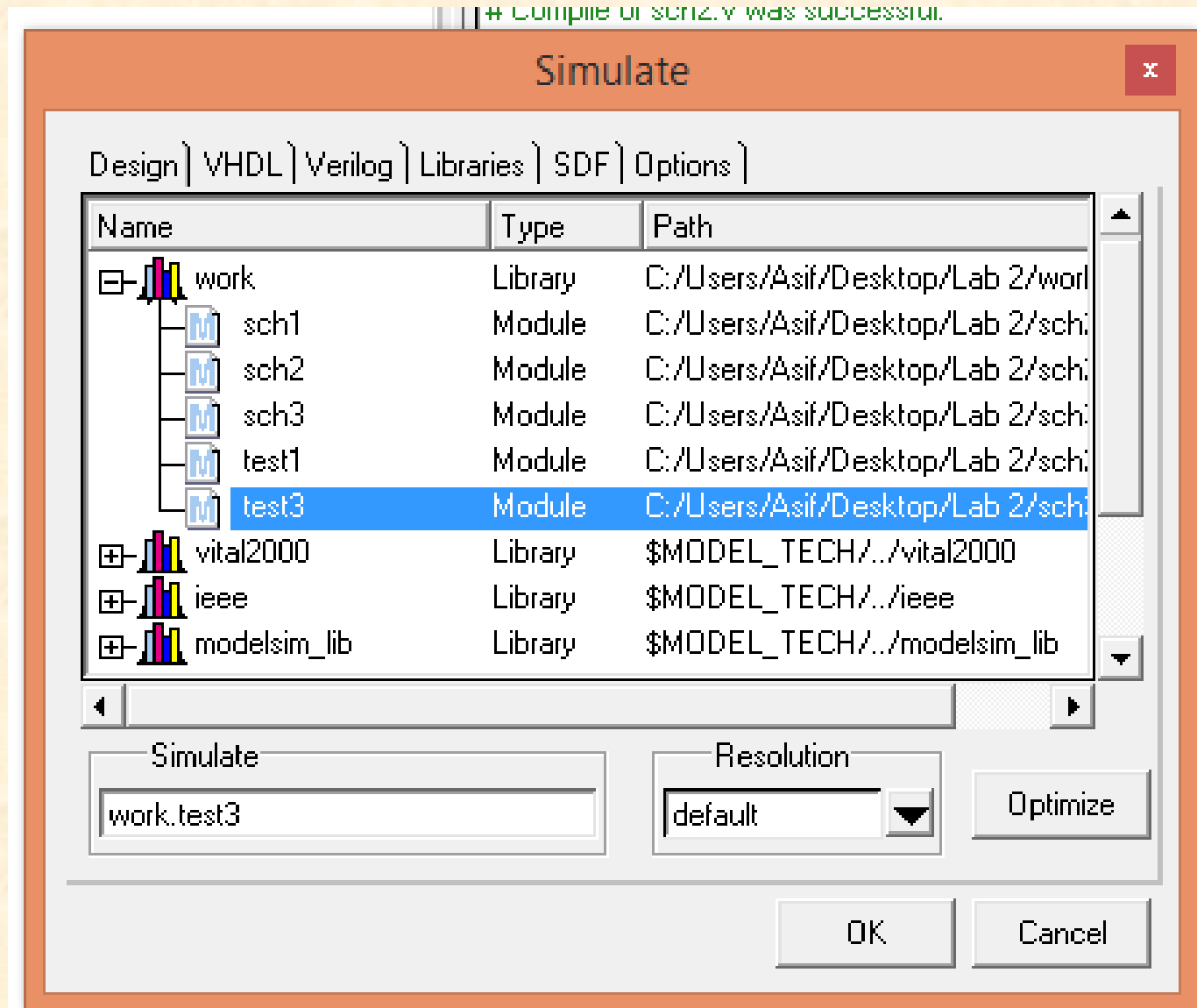
Compile code



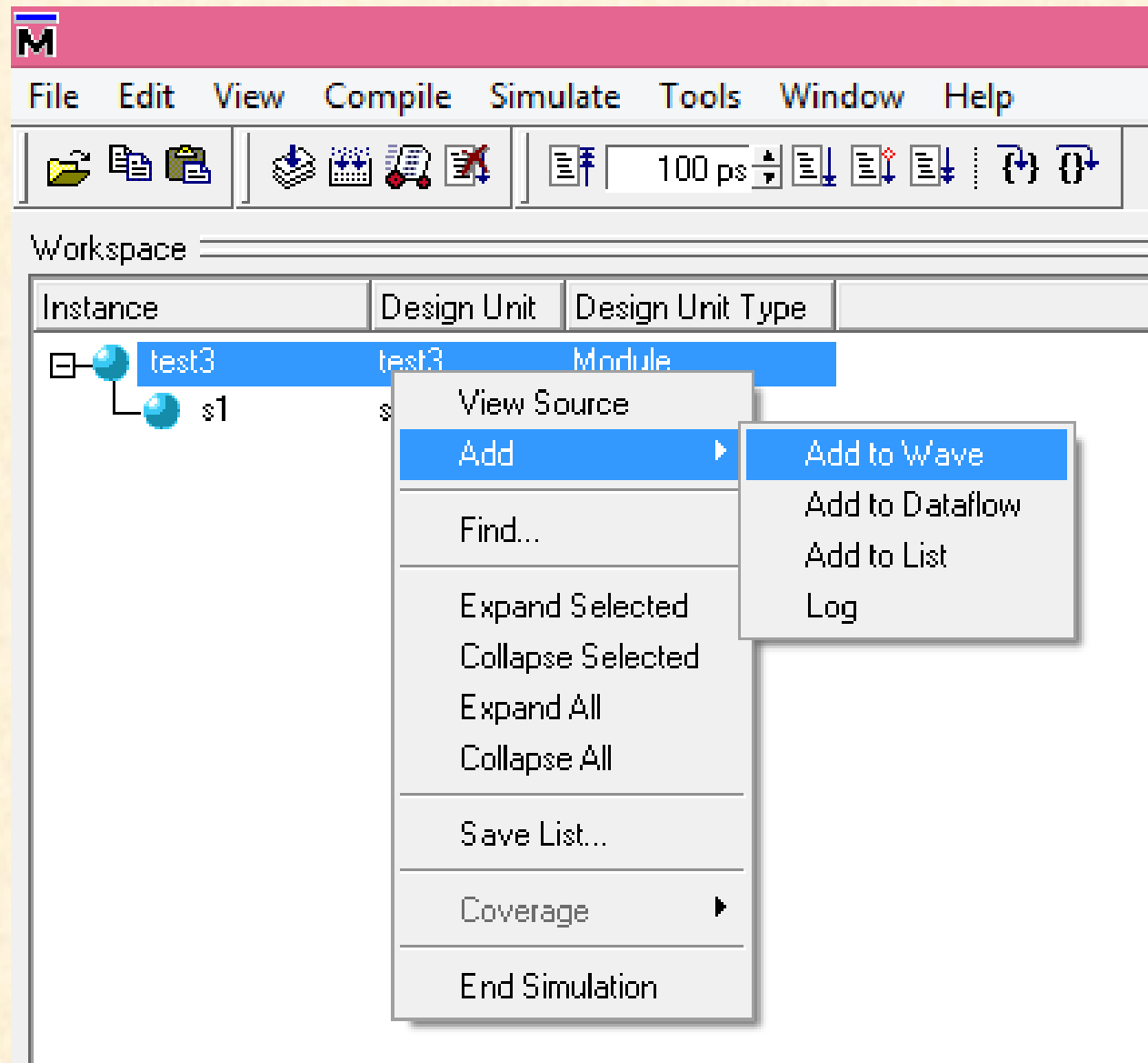
Click simulate



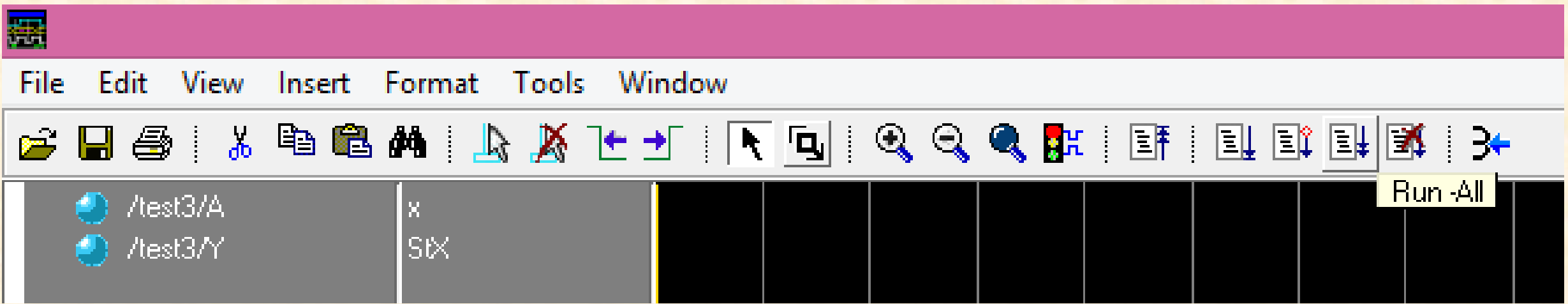
Chose test3



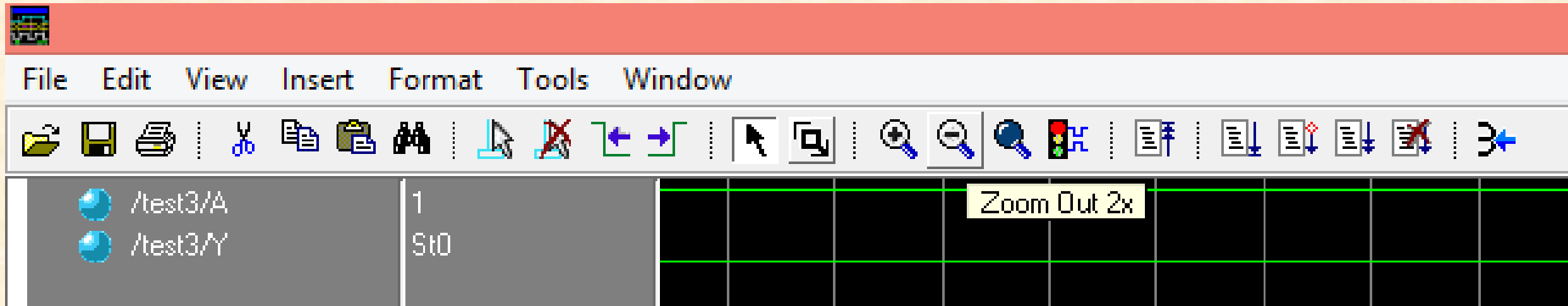
Add to wave



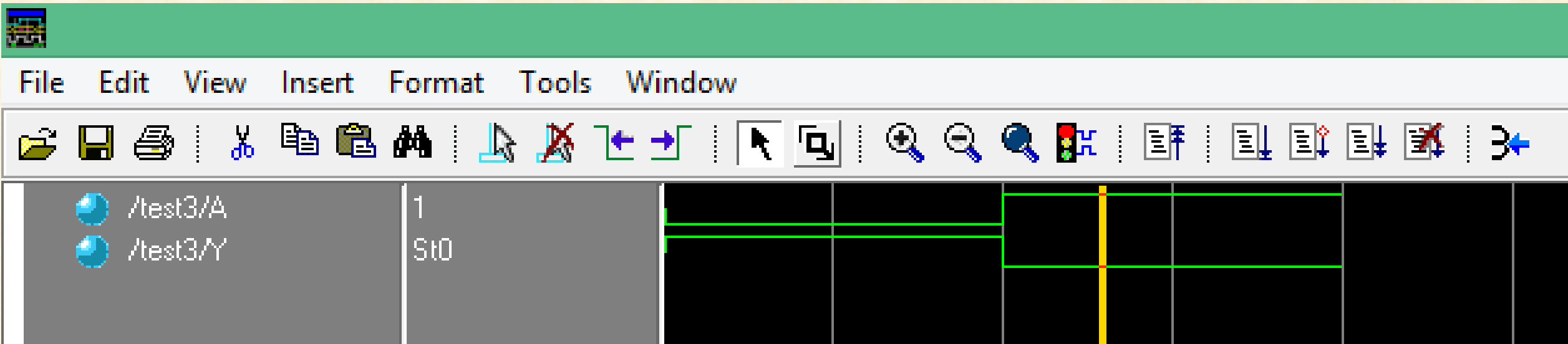
Click Run - All





Keep clicking zoom out



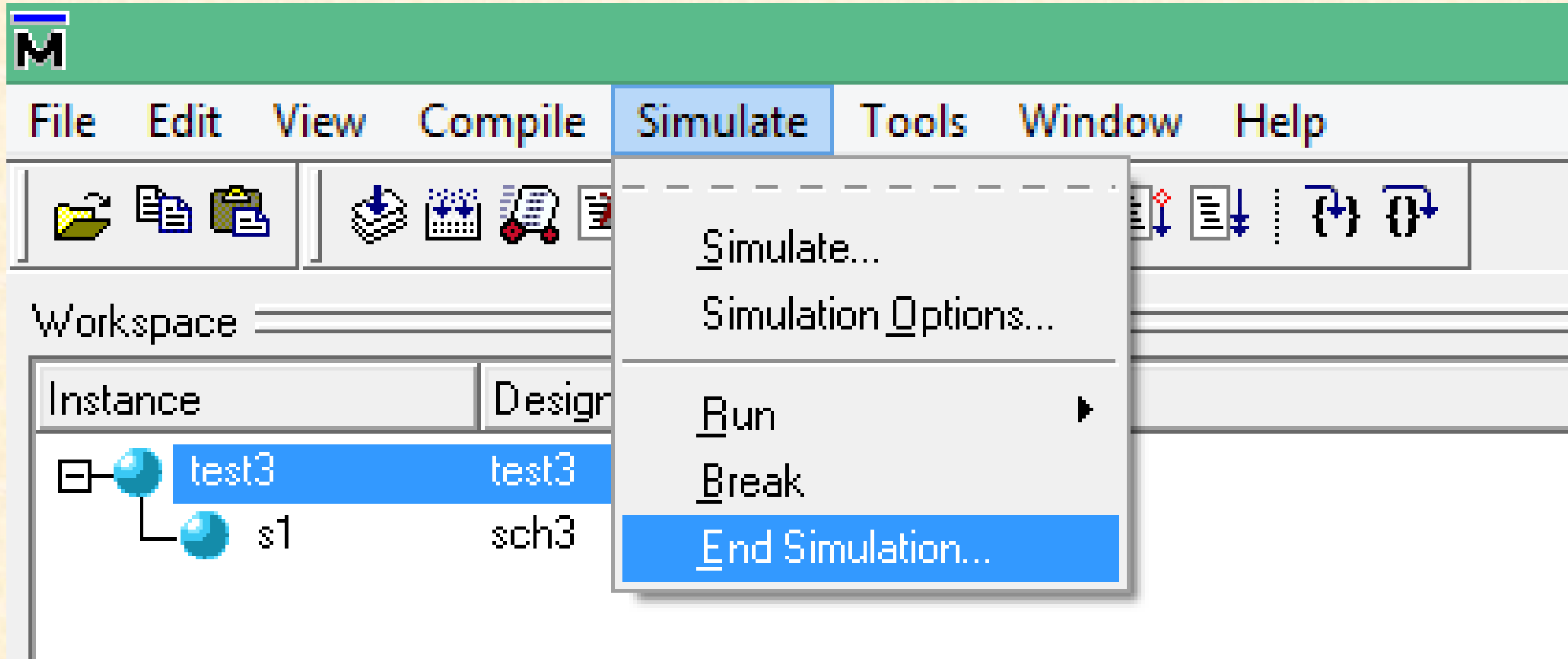
Example result



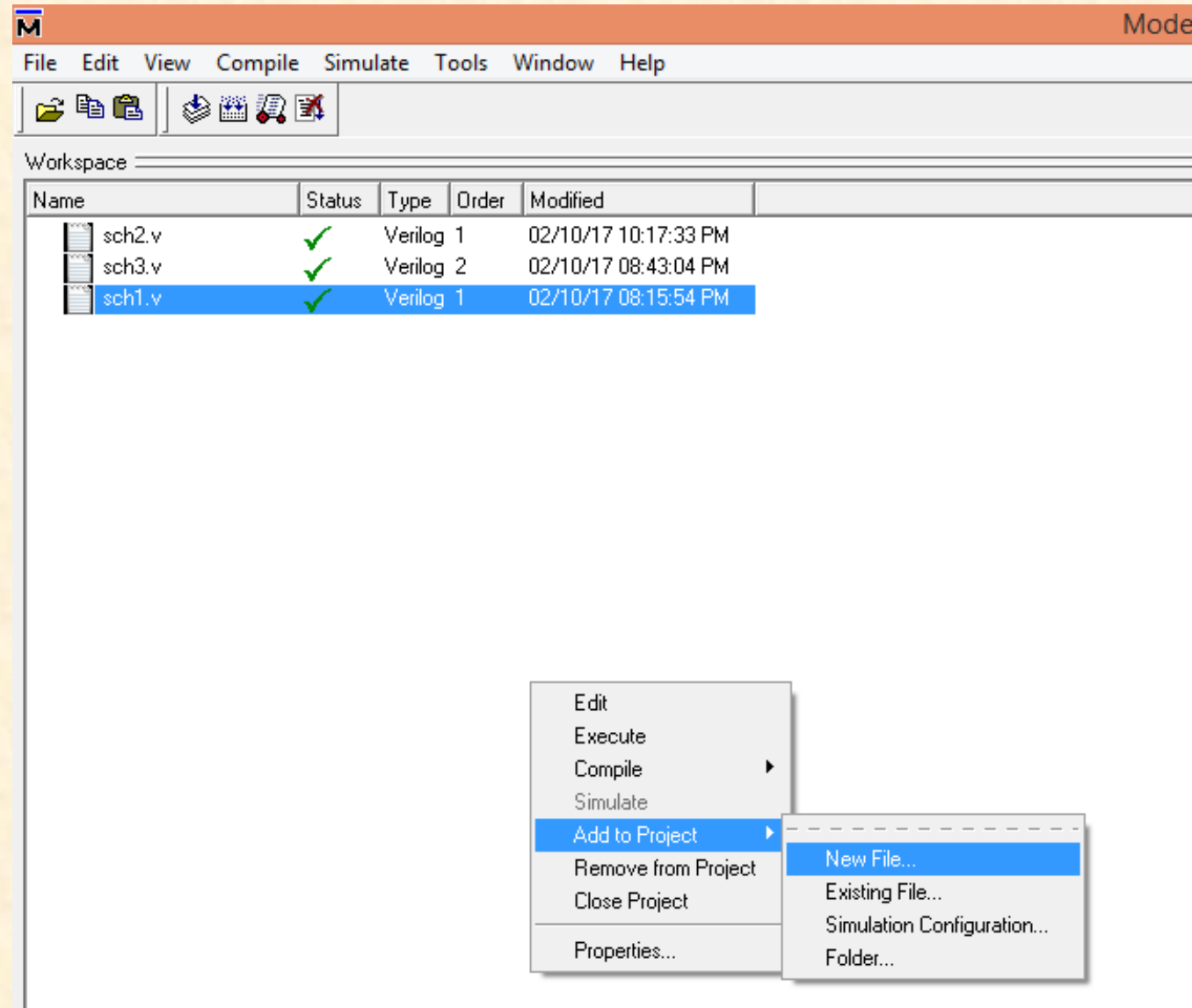
The screenshot displays a spreadsheet application with a menu bar (File, Edit, View, Insert, Format, Tools, Window) and a toolbar containing various icons for file operations, editing, and navigation. The main area shows a table with a light gray header and a black body. The first column contains file paths, the second column contains text, and the remaining columns are empty. A yellow vertical line is positioned at the end of the first data column.

 /test3/A	1						
 /test3/Y	St0						

Click End Simulation

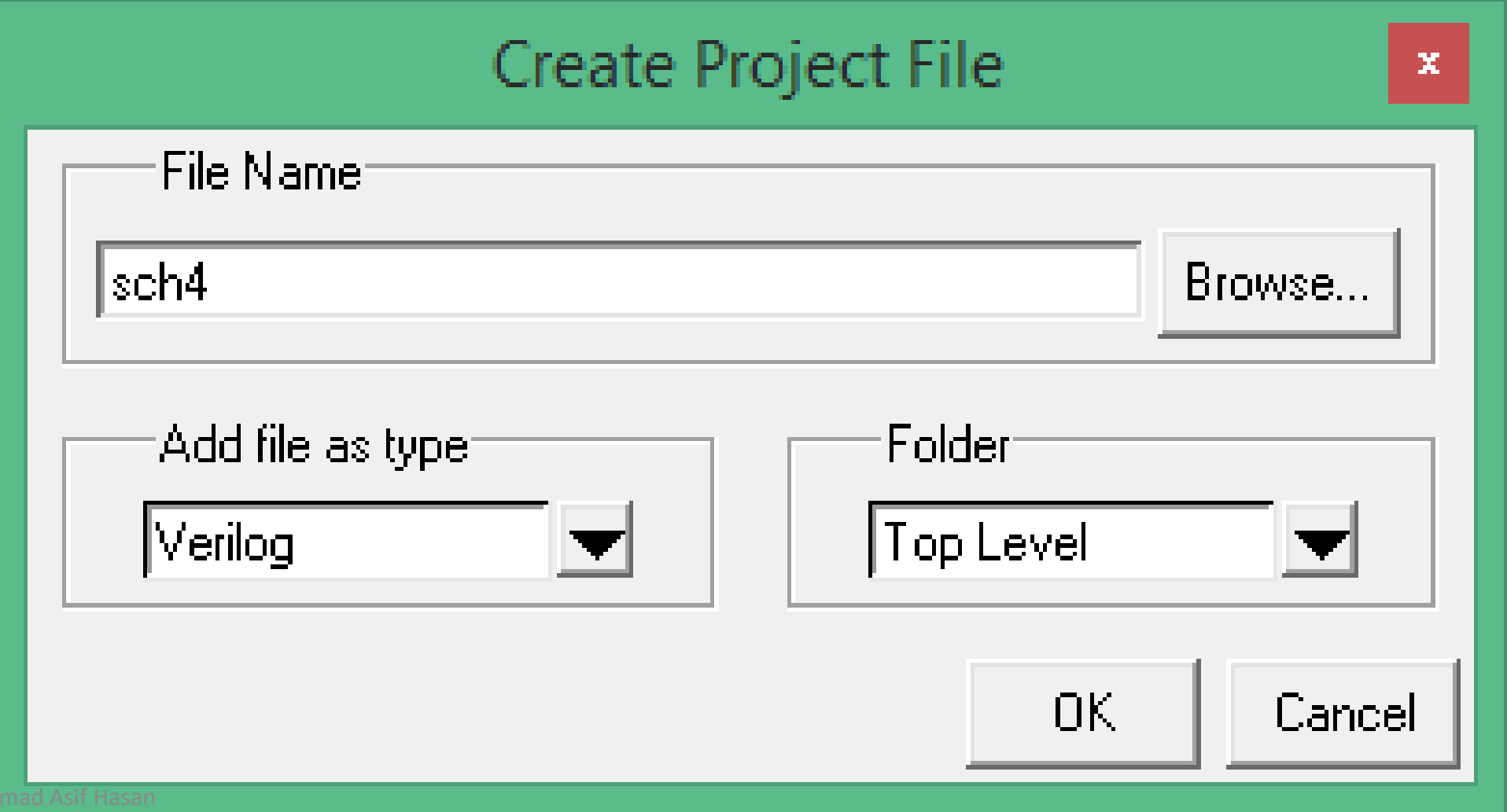


Create new file



Give name and chose as below

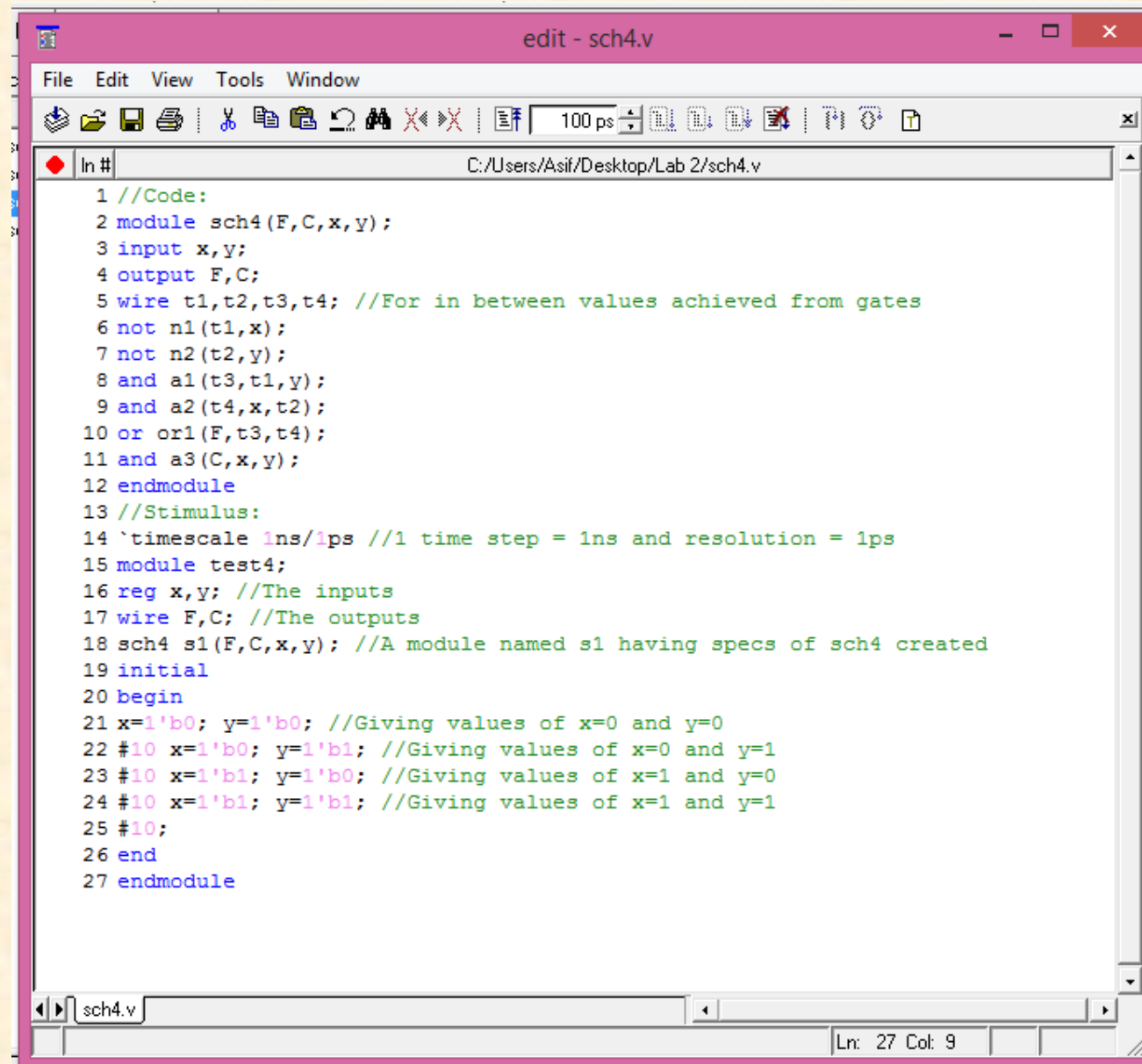
Loading work.sch3



The image shows a 'Create Project File' dialog box with a green title bar. The title bar contains the text 'Create Project File' and a red close button with a white 'X'. The dialog box has a light gray background. It contains the following elements:

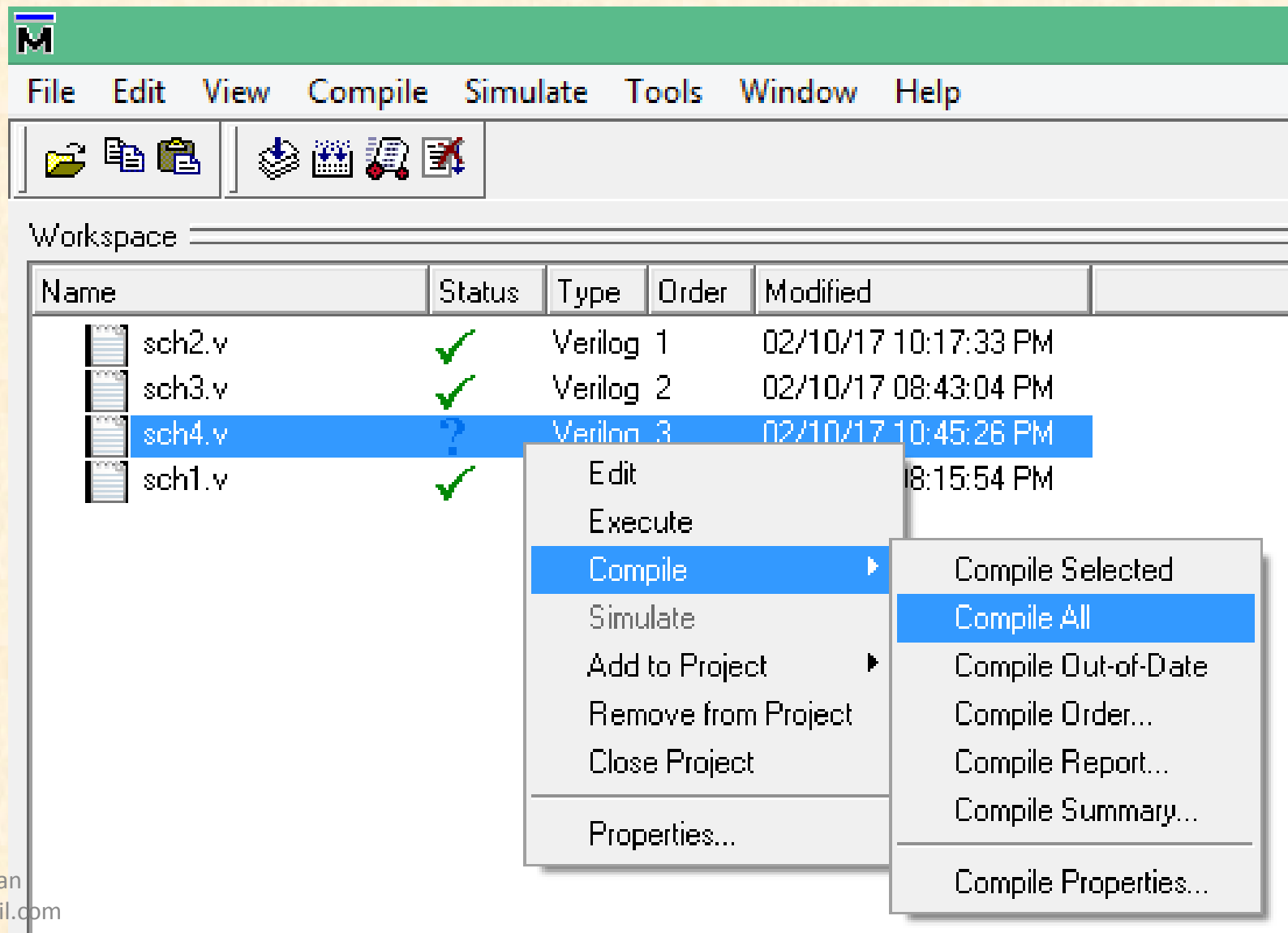
- A 'File Name' label above a text input field containing 'sch4'. To the right of the input field is a 'Browse...' button.
- An 'Add file as type' label above a dropdown menu showing 'Verilog'.
- A 'Folder' label above a dropdown menu showing 'Top Level'.
- 'OK' and 'Cancel' buttons at the bottom right.

Type code as below

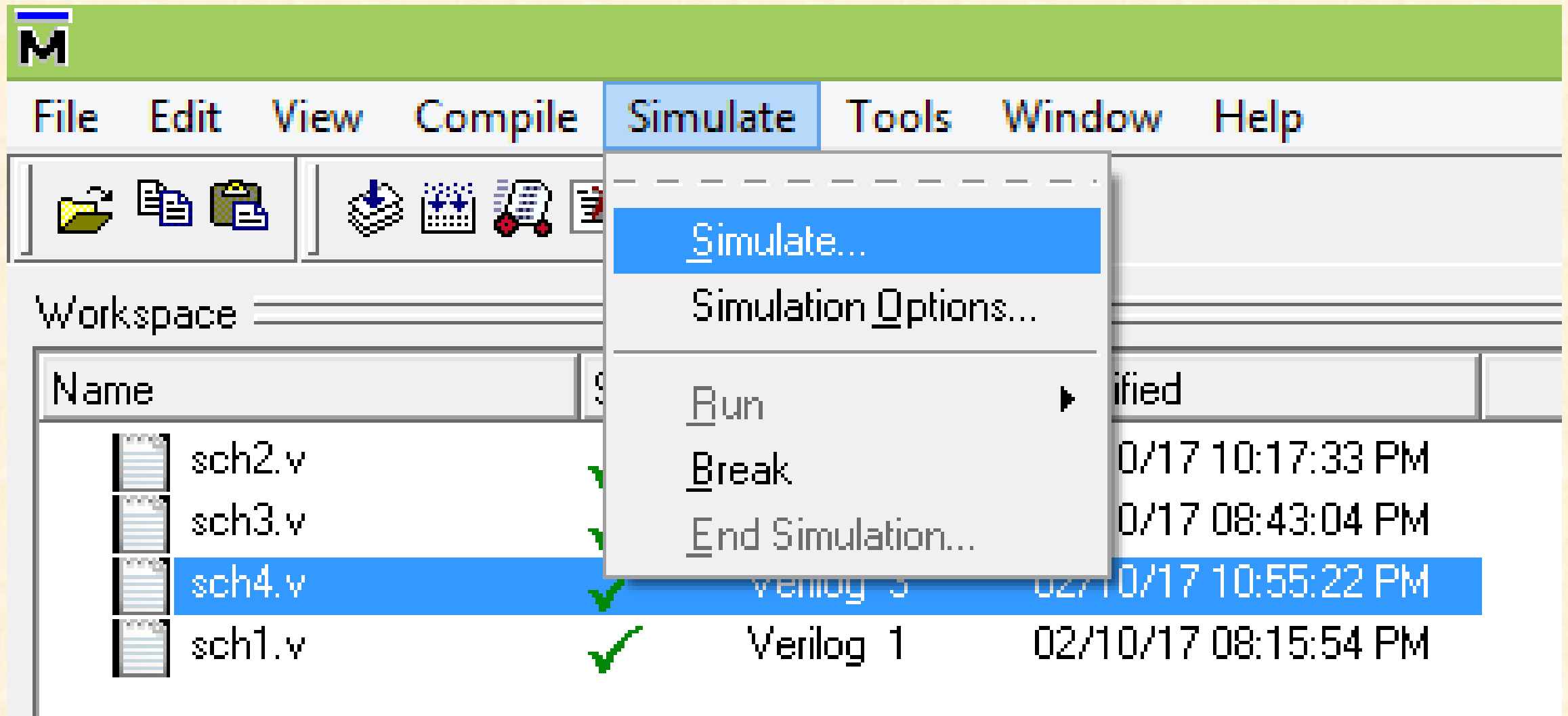


```
1 //Code:
2 module sch4(F,C,x,y);
3 input x,y;
4 output F,C;
5 wire t1,t2,t3,t4; //For in between values achieved from gates
6 not n1(t1,x);
7 not n2(t2,y);
8 and a1(t3,t1,y);
9 and a2(t4,x,t2);
10 or or1(F,t3,t4);
11 and a3(C,x,y);
12 endmodule
13 //Stimulus:
14 `timescale 1ns/1ps //1 time step = 1ns and resolution = 1ps
15 module test4;
16 reg x,y; //The inputs
17 wire F,C; //The outputs
18 sch4 s1(F,C,x,y); //A module named s1 having specs of sch4 created
19 initial
20 begin
21 x=1'b0; y=1'b0; //Giving values of x=0 and y=0
22 #10 x=1'b0; y=1'b1; //Giving values of x=0 and y=1
23 #10 x=1'b1; y=1'b0; //Giving values of x=1 and y=0
24 #10 x=1'b1; y=1'b1; //Giving values of x=1 and y=1
25 #10;
26 end
27 endmodule
```

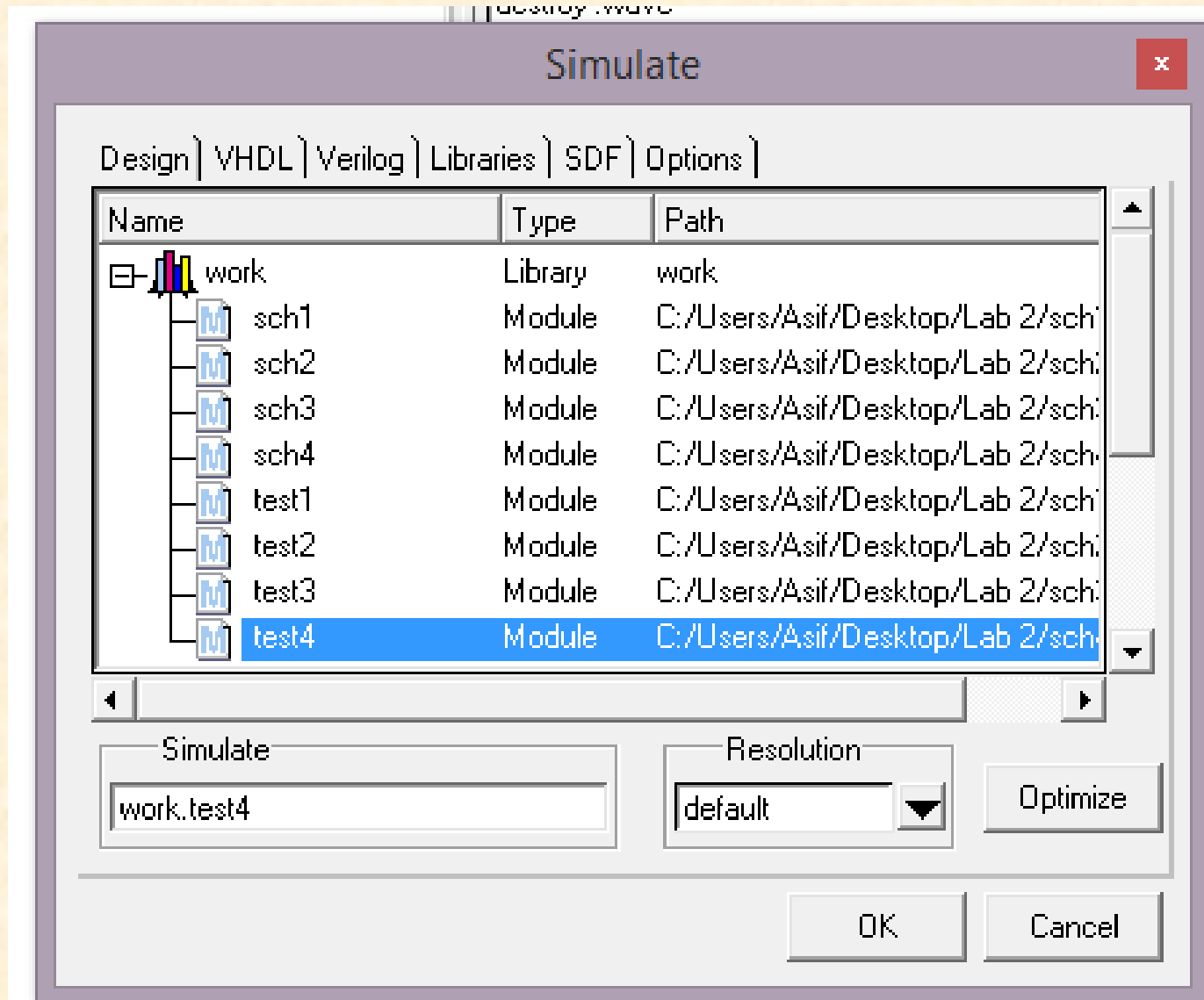
Compile code



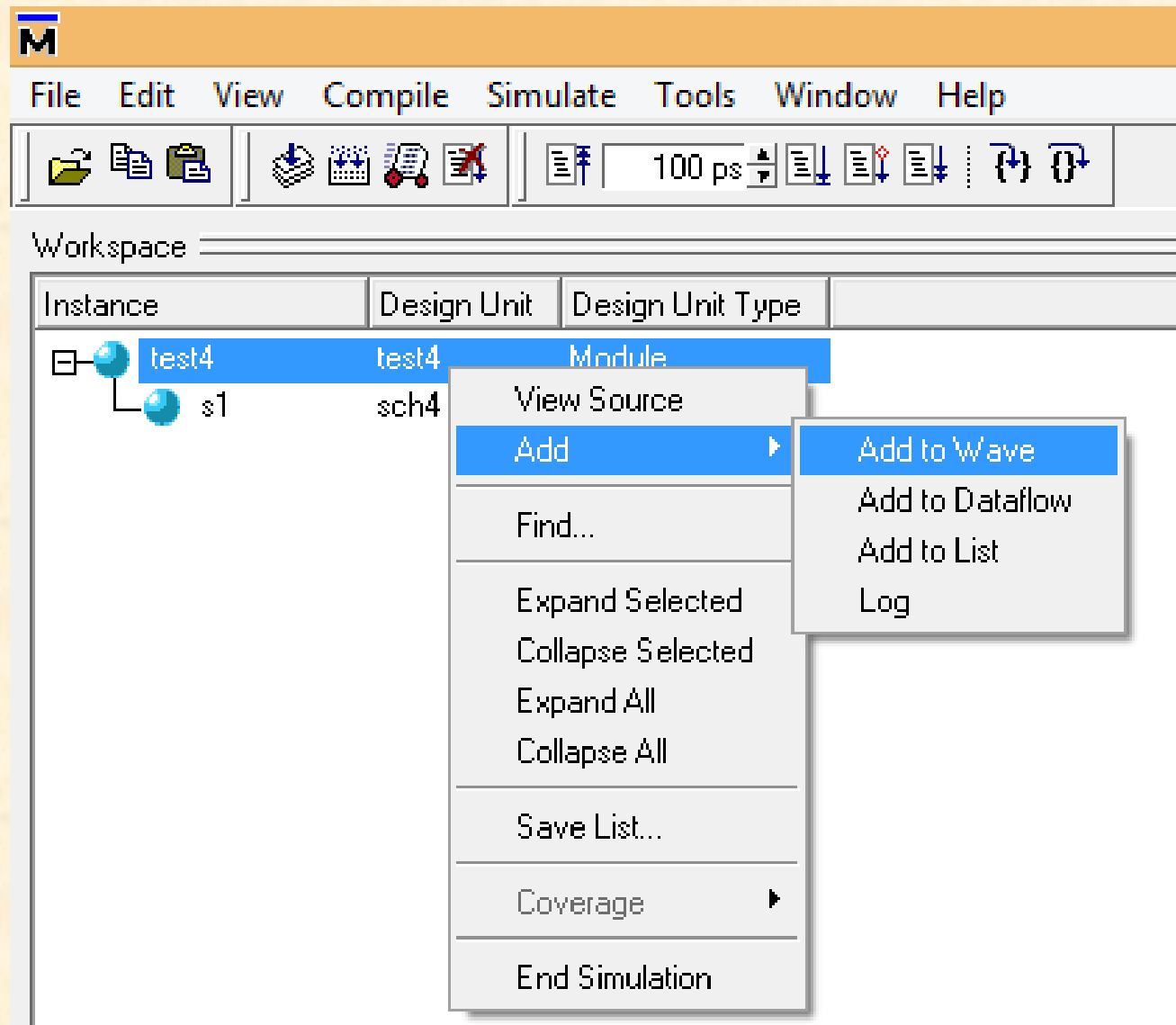
Click simulate



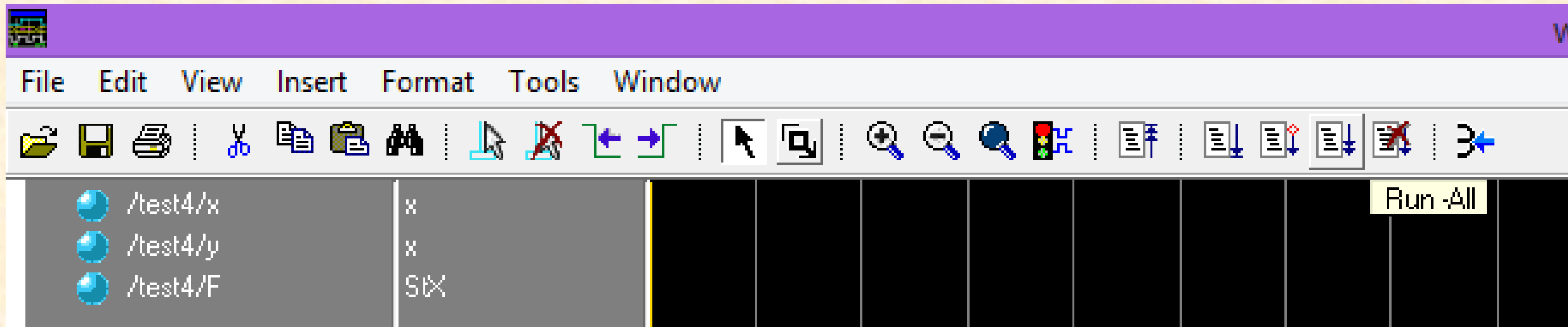
Chose test4



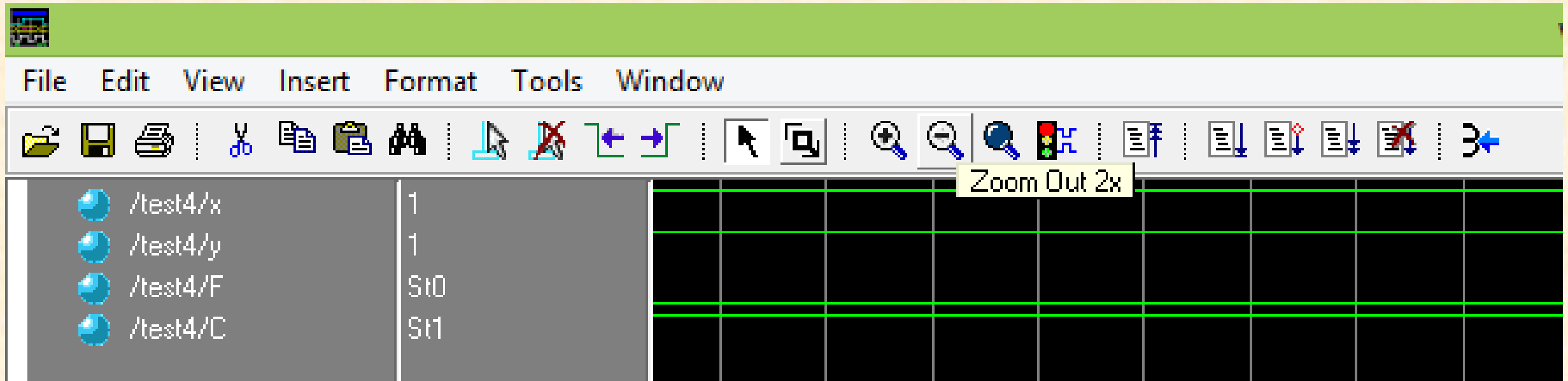
Add to wave



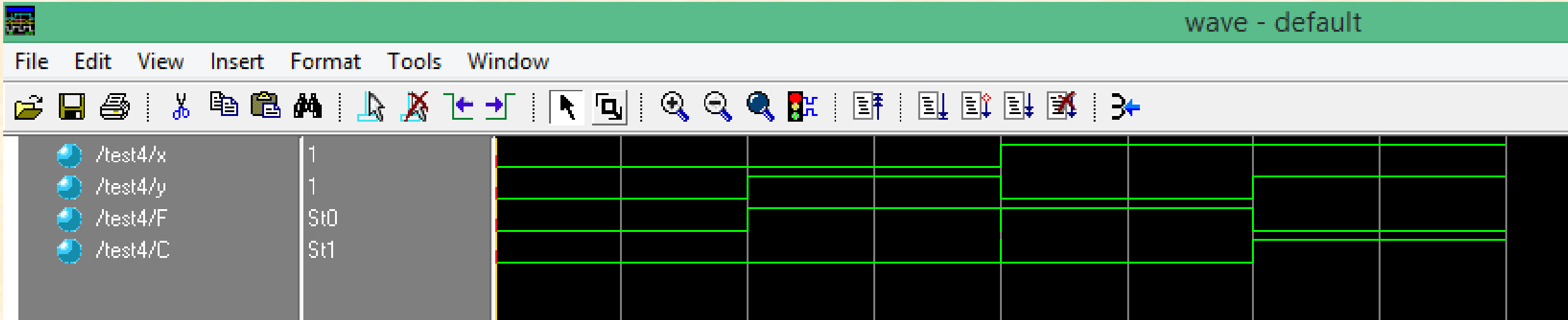
Click Run - All



Keep clicking zoom out

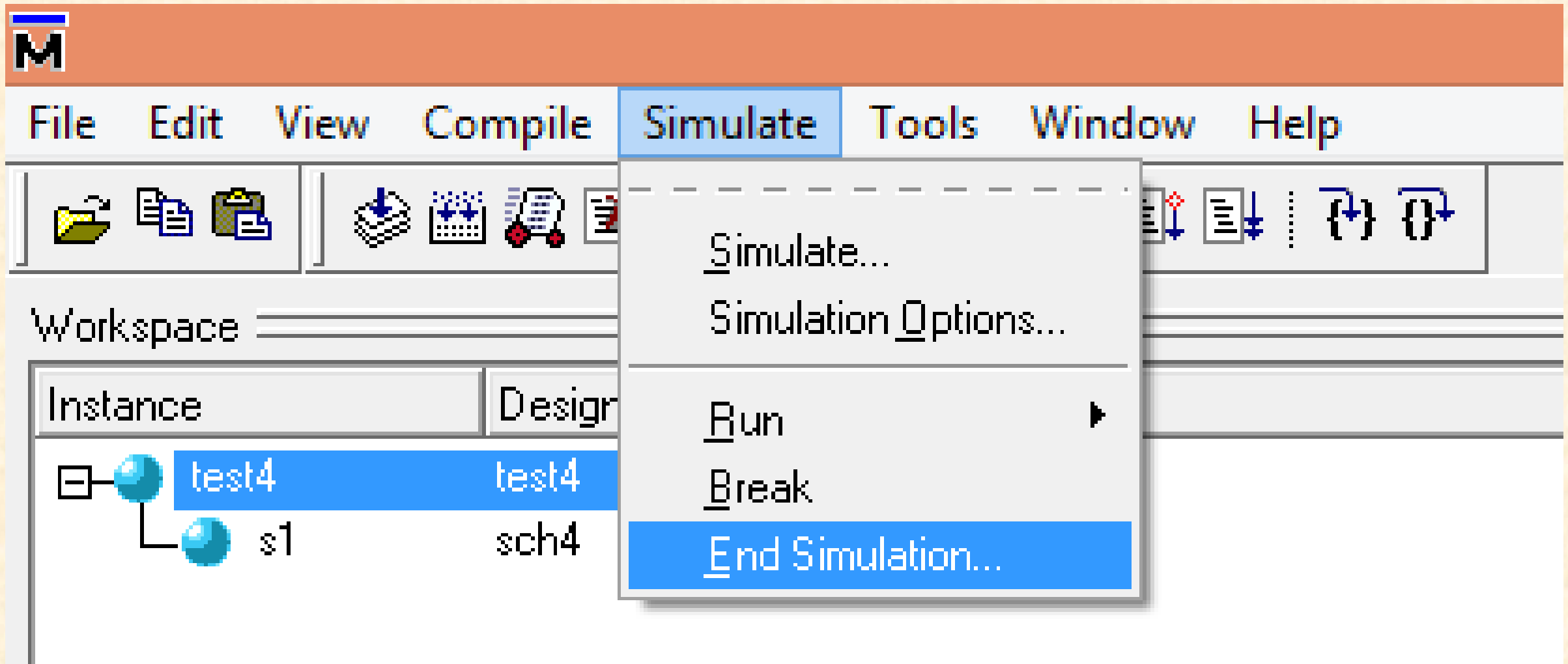


Example result



The screenshot shows a software window titled "wave - default". It features a menu bar with "File", "Edit", "View", "Insert", "Format", "Tools", and "Window". Below the menu is a toolbar with various icons for file operations, editing, and navigation. The main area is divided into two panes. The left pane is a file explorer showing a directory structure with four items: "/test4/x", "/test4/y", "/test4/F", and "/test4/C", each preceded by a blue sphere icon. The right pane displays a table with 10 columns and 5 rows. The first two columns are greyed out and contain the values "1", "1", "St0", and "St1" for the first four rows, respectively. The remaining eight columns are black with green grid lines.

/test4/x	1								
/test4/y	1								
/test4/F	St0								
/test4/C	St1								



End of Lab..!

- Get your handouts signed by instructor
- Submit your lab handouts in next lab for assessment