National University of Sciences and Technology (NUST)
School of Electrical Engineering and Computer Science

Department of Electrical Engineering

Faculty :_____ **Dated:** _____

Semester:_____ **Section:** _____

EE221: Digital Logic Design

Lab 6: Design of a Combinational Circuit (BCD to 7-Segment Decoder)

Name	Reg. No.	Report Marks / 10	Viva Marks / 5	Total Marks / 15

Lab 6: Design of a Combinational Circuit (BCD to 7-Segment Decoder)

This Lab Activity has been designed to familiarize the student with design and working of a BCD to 7-Segment Decoder

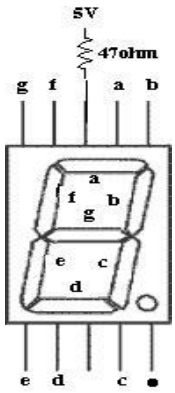
Objectives:

- Apply design steps for the combinational circuits
- Simplify functions with don't cares using map method.
- Design and Implementation of a BCD to 7-Segment Decoder for Selected Digit Display
- Using 7-Segment LED Displays
- Understanding the difference between common cathode and common anode displays

Pre-Lab Tasks:

1. What do you mean by BCD numbers? Explain with Examples.

2. 7-Segment LED Displays are commonly used for displaying decimal Numbers (0 to 9). It can also be used for displaying alphabets. A 7-Segment LED Displays essentially consist of 7 LEDs configured as shown below to display numbers. It comes in two configurations. Common Cathode and Common Anode. Draw the diagram showing connections to drivers and power source and ground for both configurations and highlight differences between the two. Also give signal logic level required to light up the LEDs in the segment in each configuration:



3. Design a BCD-to-Seven Segment Decoder with minimum number of gates that coverts BCD Numbers 0 through 9 in such a way that the display shows 0-9 on the Seven-Segment-Display. The unused input combinations should be taken as don't care conditions. For what configuration are you making truth table?

a) Give Truth Table

Inputs (BCD)				Outputs(7 LEDs on 7-Segment Display)						
A	B	C	D	a	b	c	d	e	f	g

b) K-Map Simplification

c) Draw Hardware Schematic diagram showing pin numbering and connections of each IC.

Lab Tasks:

4. Implement the above circuit in hardware using minimum number of NAND gates.

5. Mention which configuration of 7-Segment Display did you use in Lab? If you were to use the other configuration what change would you need in your circuit?