National University of Sciences and Technology (NUST)
School of Electrical Engineering and Computer Science

Department of Electrical Engineering

Faculty Member:_____ **Date:** _____

Lab Engineer:_____ **Course/Section:**_____

EE-221: Digital Logic Design

Lab 2: Part (a): Introduction to Verilog and Gate-level Modelling
Part (b): Implementation of Basic Logic Circuit

Name	Reg. No.	Report Marks / 10	Viva Marks / 5	Total Marks / 15

Lab 02: Introduction to Verilog, Gate-level Modelling and Hardware

This Lab has been divided into two parts.

In first part you will be introduced to Verilog and Gate - Level Modelling.
The next part is the hardware Implementation of a Boolean function given to you.

Objectives:

- ✓ Understand HDL and compare it with normal programming languages.
- ✓ Simulate Basic Gates using Verilog with ModelSim
- ✓ Write stimulus using Verilog
- ✓ Derive algebraic expression for a Boolean function from the given schematics.
- ✓ Hardware Implementation of Logic Circuit

Pre-Lab Task:

1. Read the manual Getting Started with Verilog and answer the following questions.
   a) HDL stands for
   b) Two standard versions of HDL are
   c) Give the different levels of abstraction in Verilog HDL

2. What do we understand by Simulation of Gates?

Lab Task:

Lab Task 1:

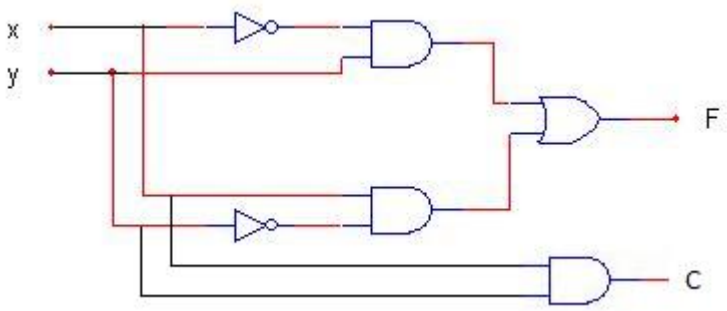
Simulate the code given to you for OR gate and attach the simulation results with your report. Compare the simulation waveform results with the truth table in space provided below.

Lab Task 2:

Model and simulate the AND and NOT gates in Verilog. Compare the simulation waveform results with truth table in space provided below.

Lab Task 3:

Write the Verilog Code for the following circuit. List the code for design as well as stimulus below:



Lab Task 4:

Label each gate output in the above circuit and derive algebraic expressions for SUM and Carry Out. Fill in the following truth table and determine the function performed by the circuit. Also perform hardware implementation of the given circuit.

Truth Table:

x	y	Sum	Carry Out

Schematic: (showing pin numbers)

Observation/Comments: