Quiz 3 master solution for reference

**Q1. Write down the names of the stages of instruction pipelining (experienced in CPU simulator) explain each one of them.**
(Sequence of the stages is important here)
**Fetch**: The next instruction is fetched from the memory address that is currently stored in the program counter and stored into the instruction register.
**Decode**: The encoded instruction present in the instruction register is interpreted by the decoder.
**Read Operands**: This step evaluates which type of operation is to be performed
**Execute**: The function of the instruction is performed. E.g. If the instruction involves arithmetic or logic, the ALU is utilized.
**Write Result**: The result generated by the operation is stored in the main memory or sent to an output device

**Q2 Explain different types of pipelining hazards.**
(Sequence is not important here)

**Structural Hazards**: They arise due to resource conflicts when the hardware is required by multiple instructions at the same time however the hardware cannot support them simultaneously.
**Data Hazards**: When a data required by an instruction is still awaited due to pipelining data hazard occurs i.e. the instruction depend on the result of an instruction not yet executed.
**Control Hazards**: control hazards may occur due to branching in the program for example when jmp or if statement change the program counter to other than its target address.