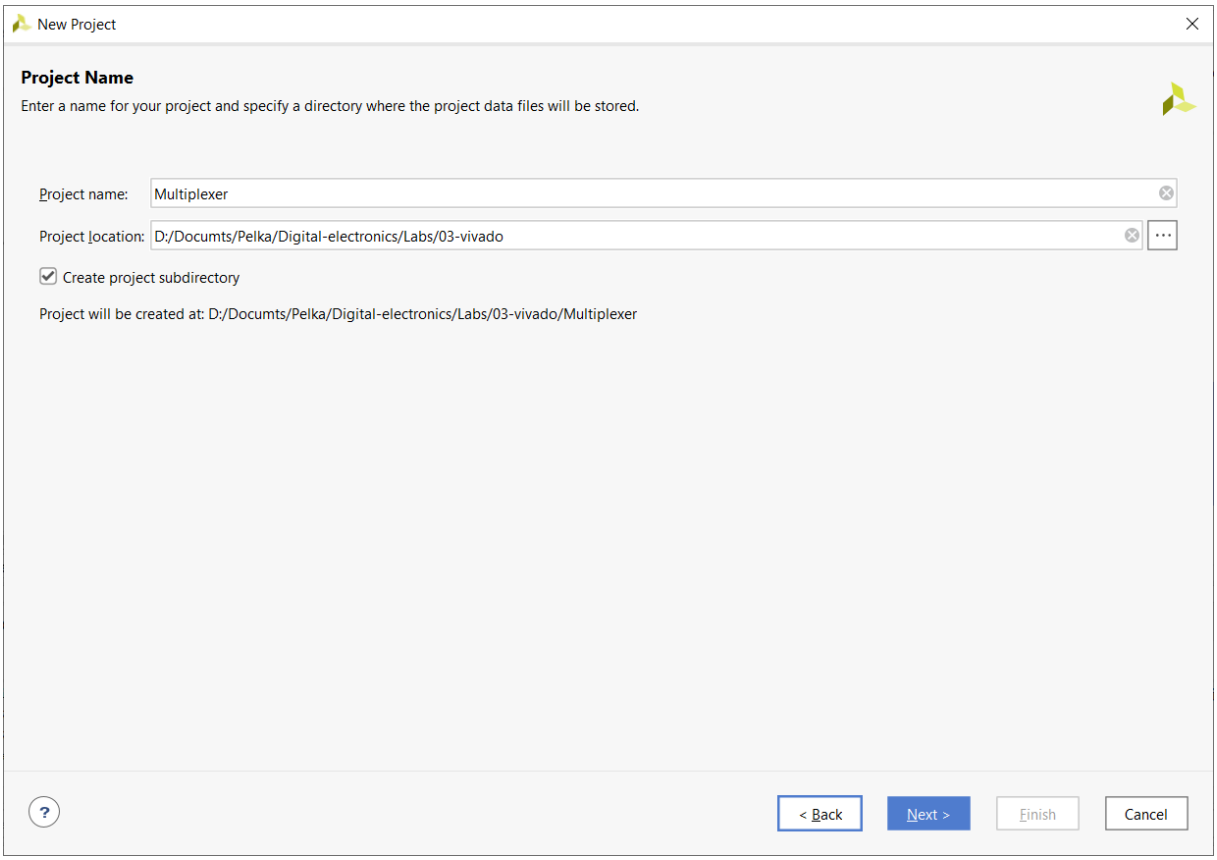
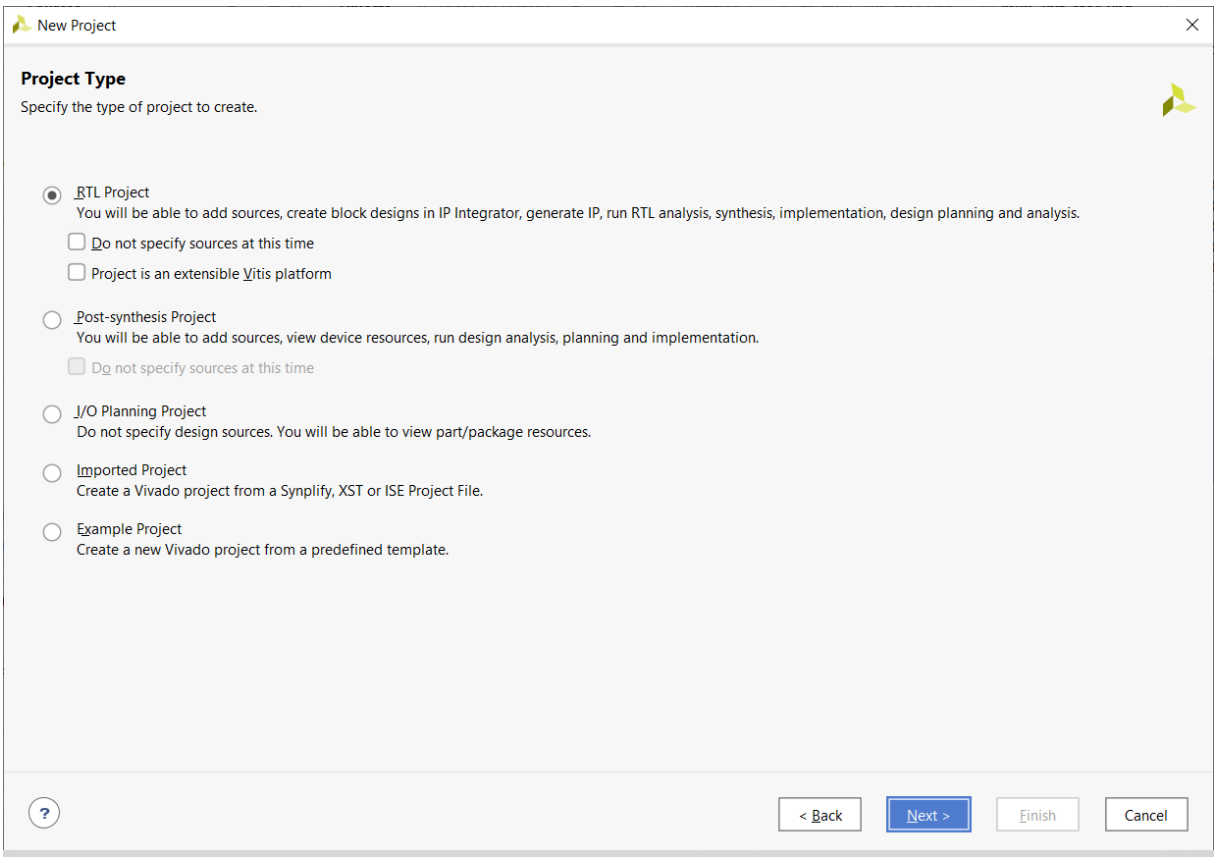
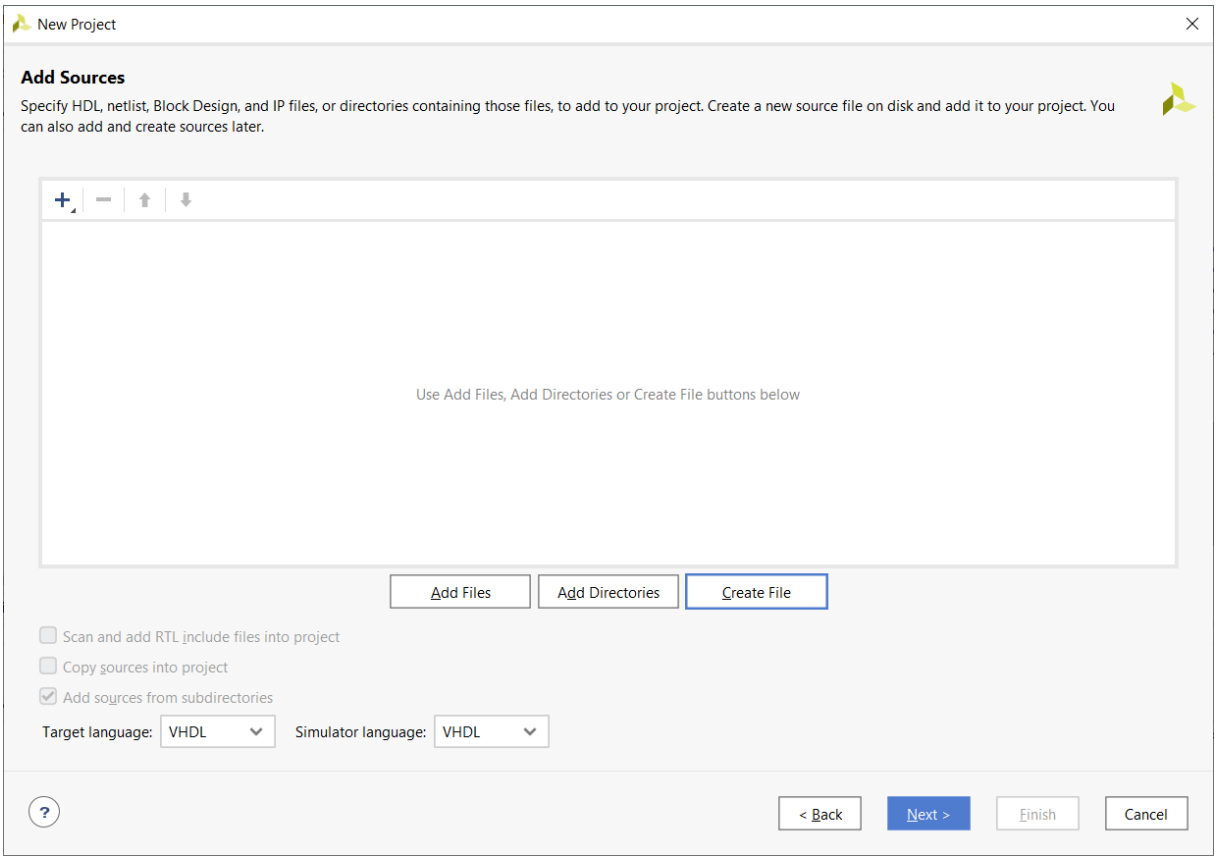
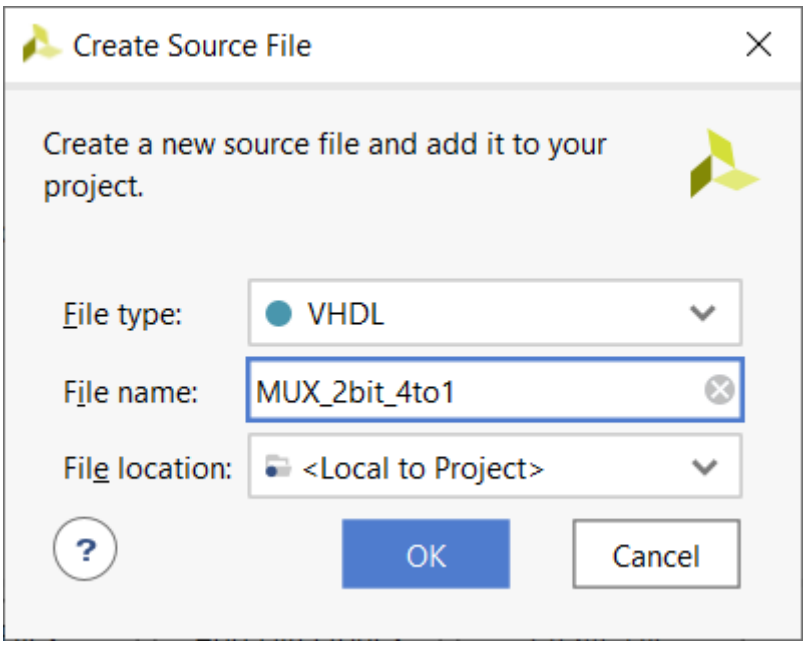
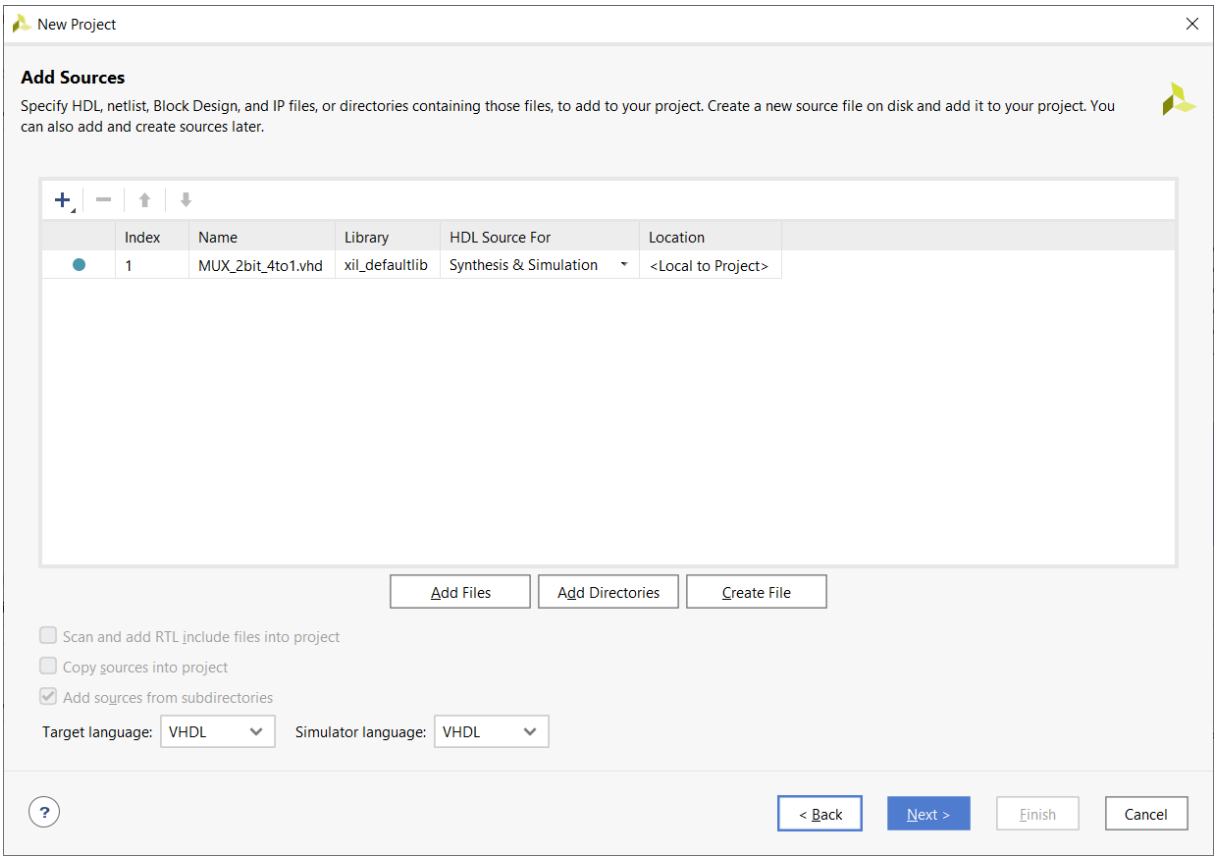
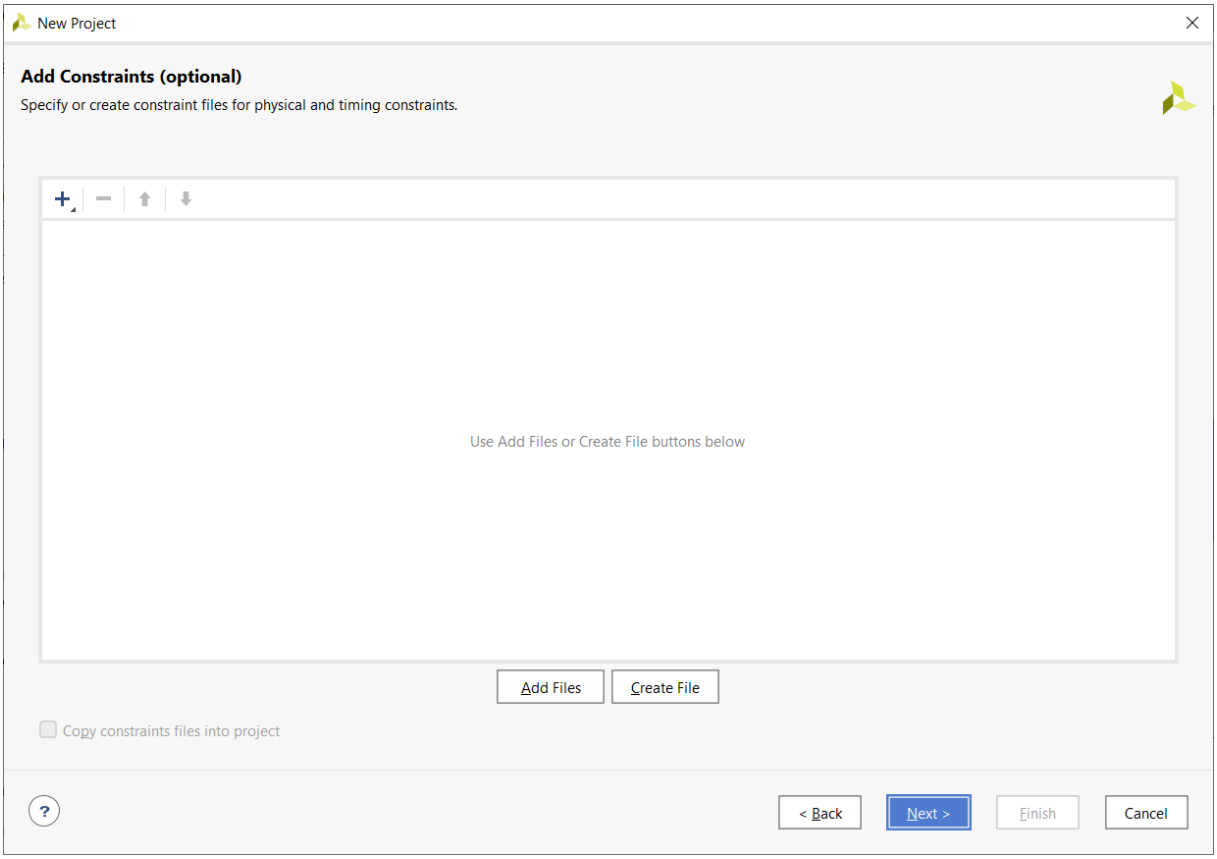

New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
Multiplexer
Project location:
D:/Documts/Pelka/Digital-electronics/Labs/03-vivado
Create project subdirectory
Project will be created at: D:/Documts/Pelka/Digital-electronics/Labs/03-vivado/Multiplexer
?
< Back
Next >
Finish
Cancel

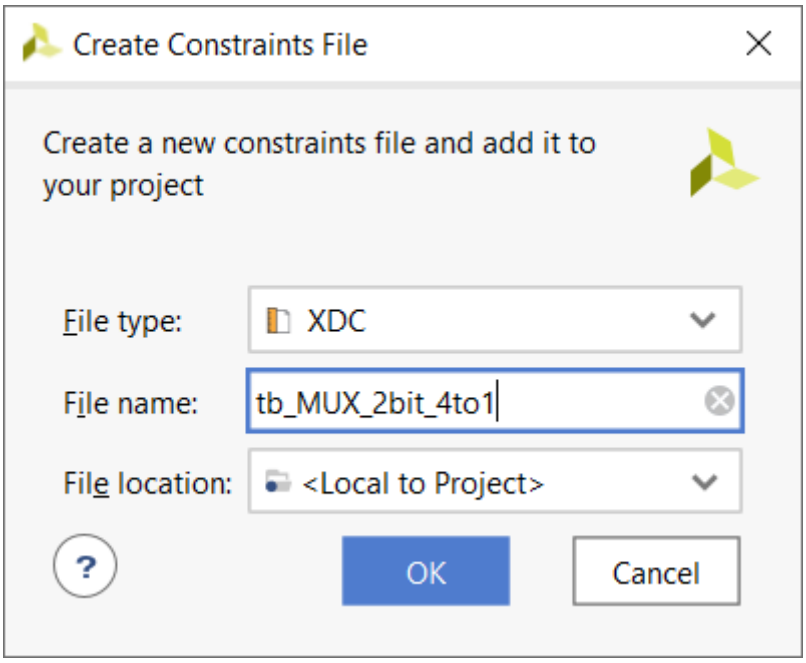

New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Project is an extensible Vitis platform
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
?
< Back
Next >
Finish
Cancel

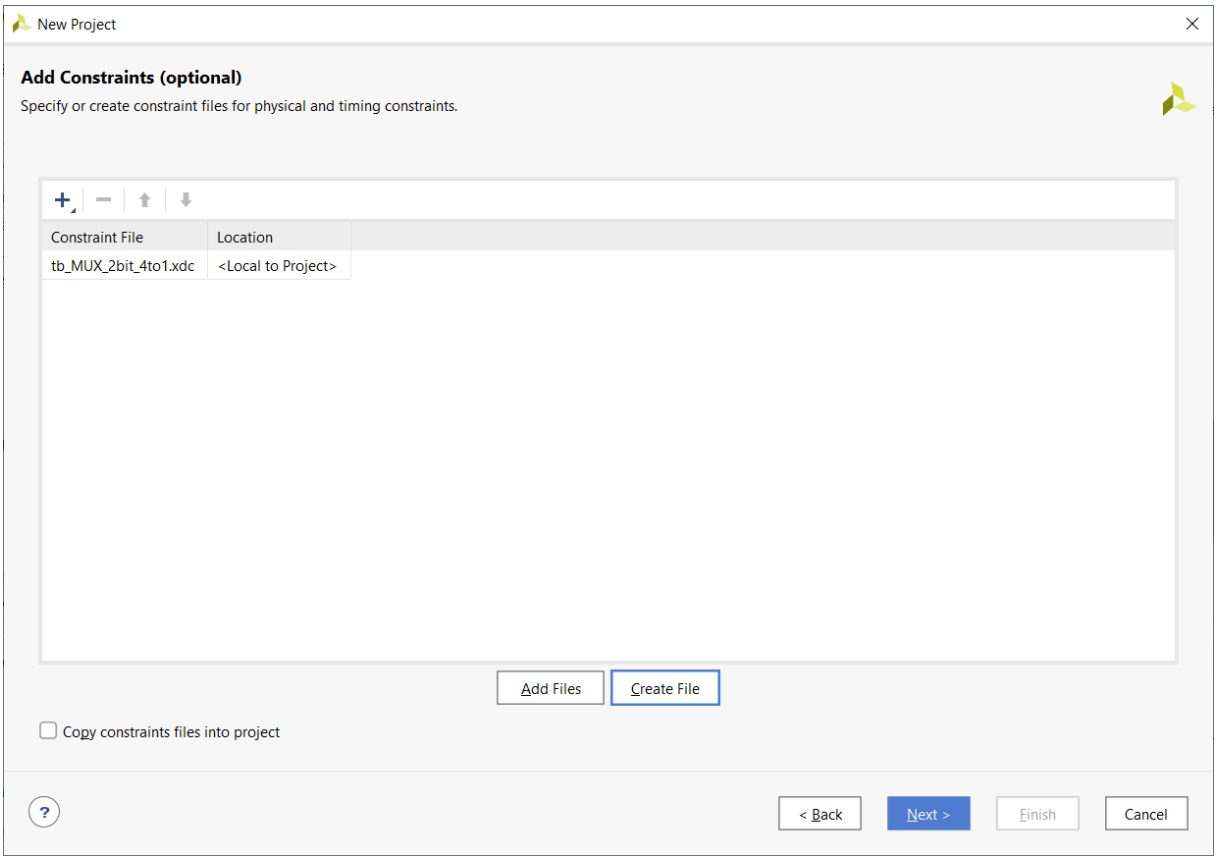

New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: VHDL
Simulator language: VHDL
< Back
Next >
Finish
Cancel

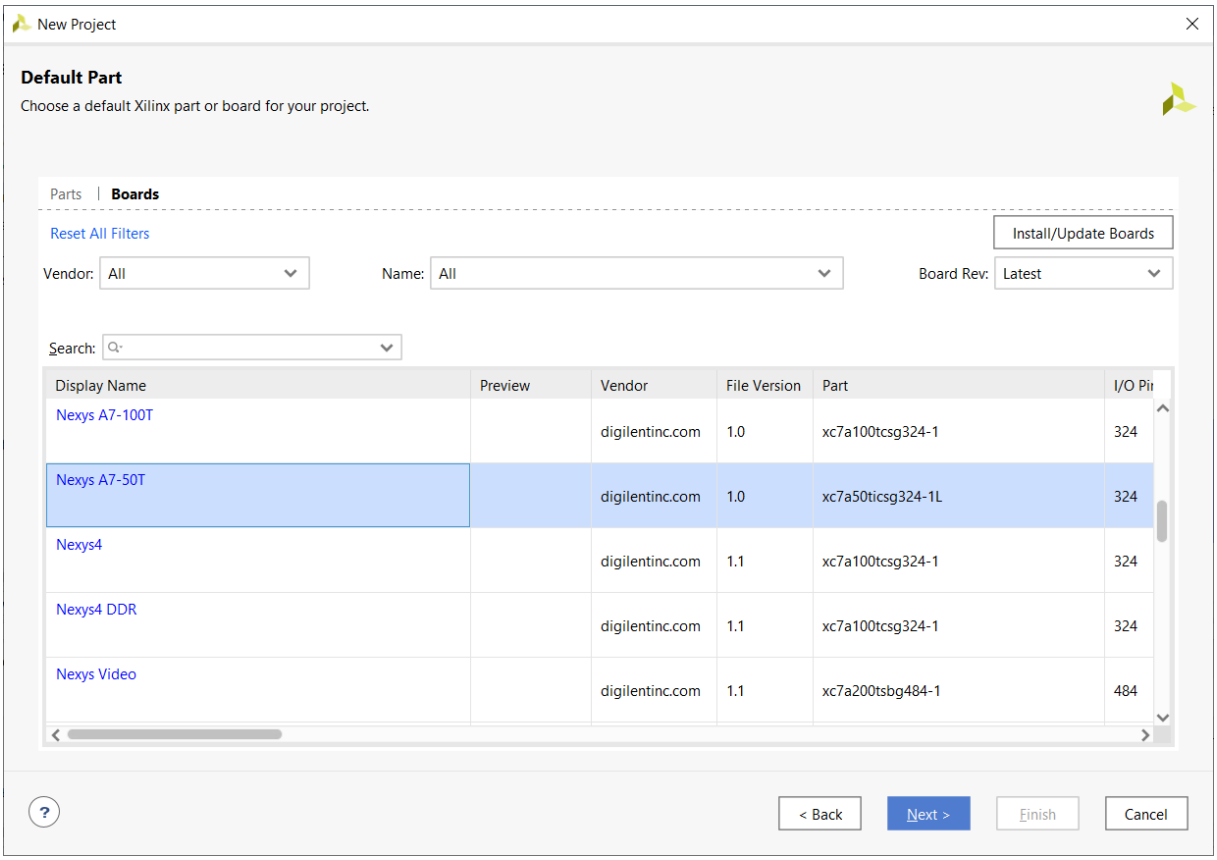

Create Source File
Create a new source file and add it to your project.
File type: VHDL
File name: MUX_2bit_4to1
File location: <Local to Project>
OK
Cancel

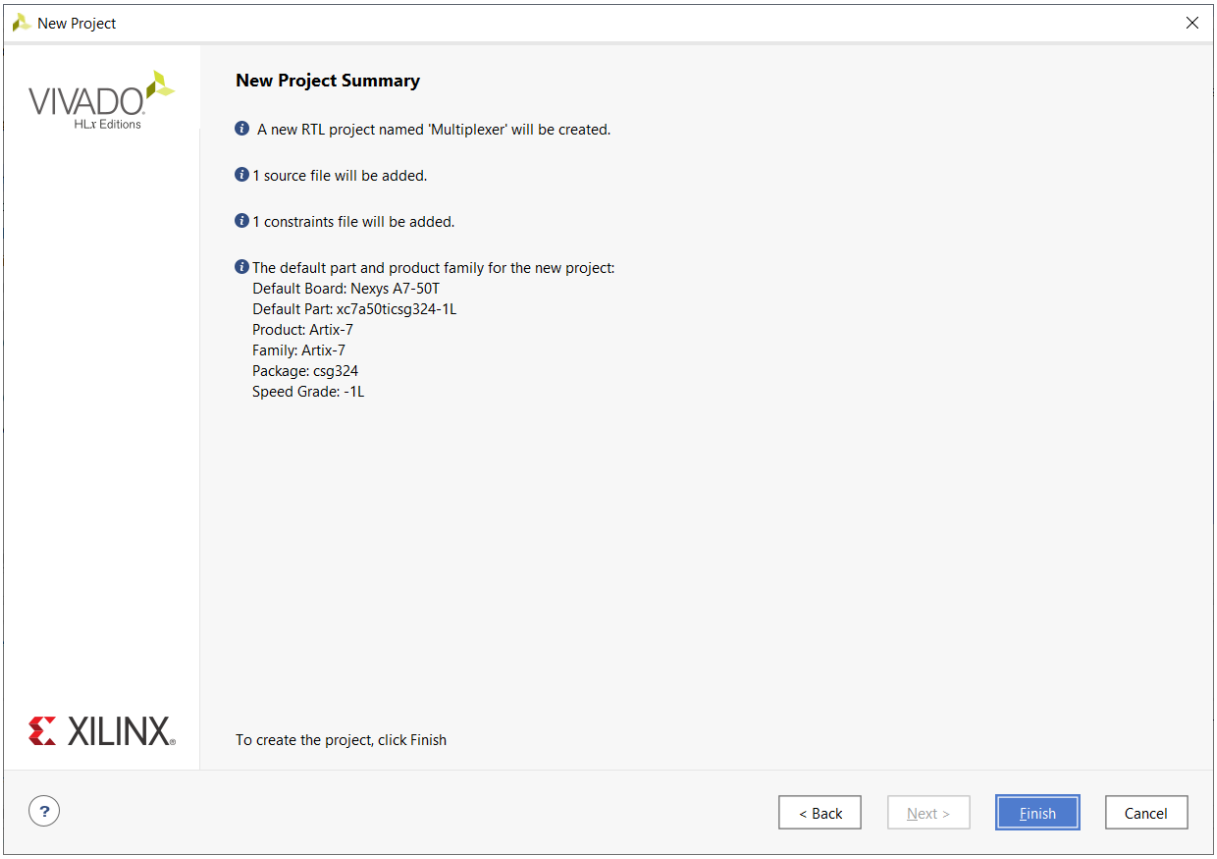

New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Index
Name
Library
HDL Source For
Location
1
MUX_2bit_4to1.vhd
xil_defaultlib
Synthesis & Simulation
<Local to Project>
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language:
VHDL
Simulator language:
VHDL
< Back
Next >
Finish
Cancel

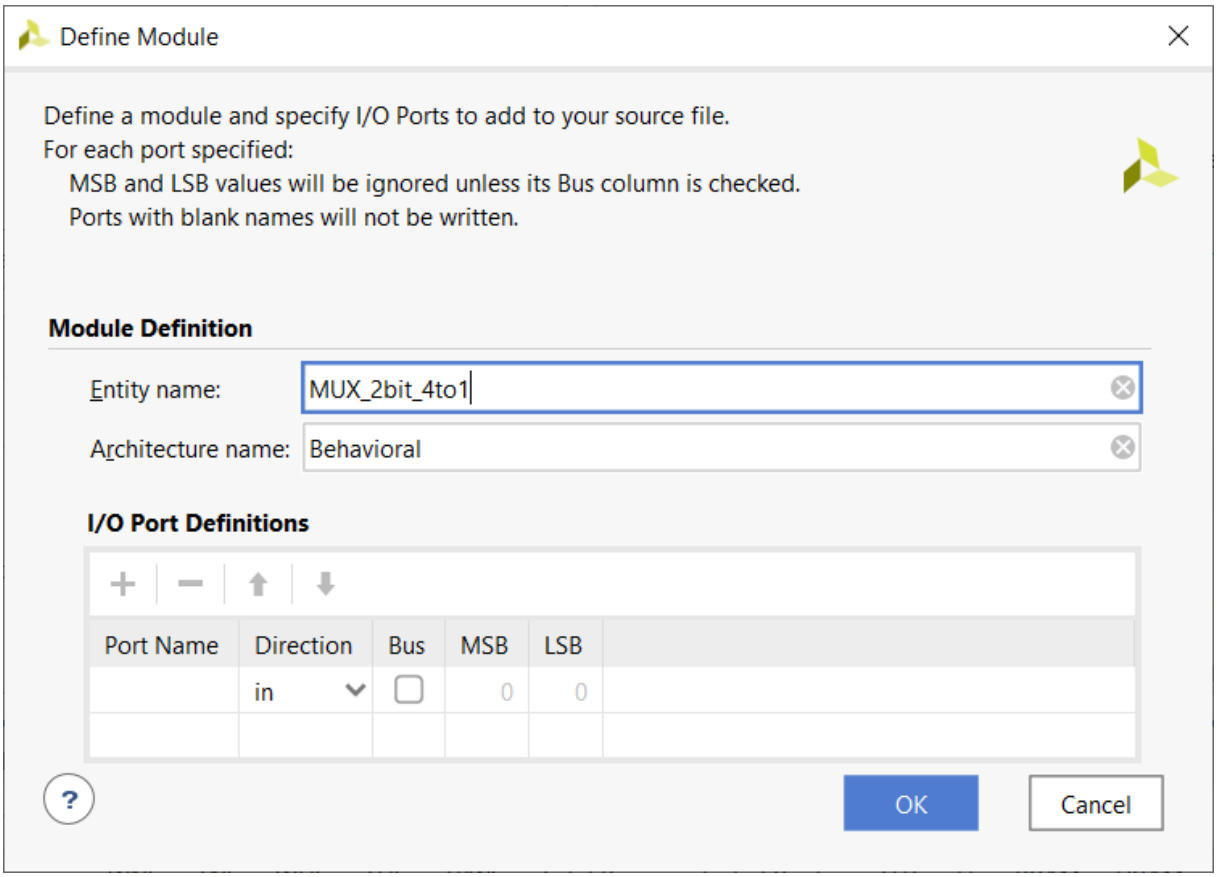

New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

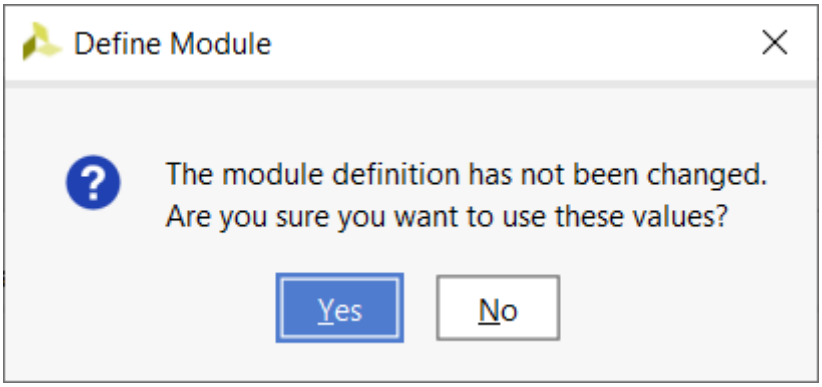

Create Constraints File
Create a new constraints file and add it to your project
File type:
XDC
File name:
tb_MUX_2bit_4to1
File location:
<Local to Project>
OK
Cancel

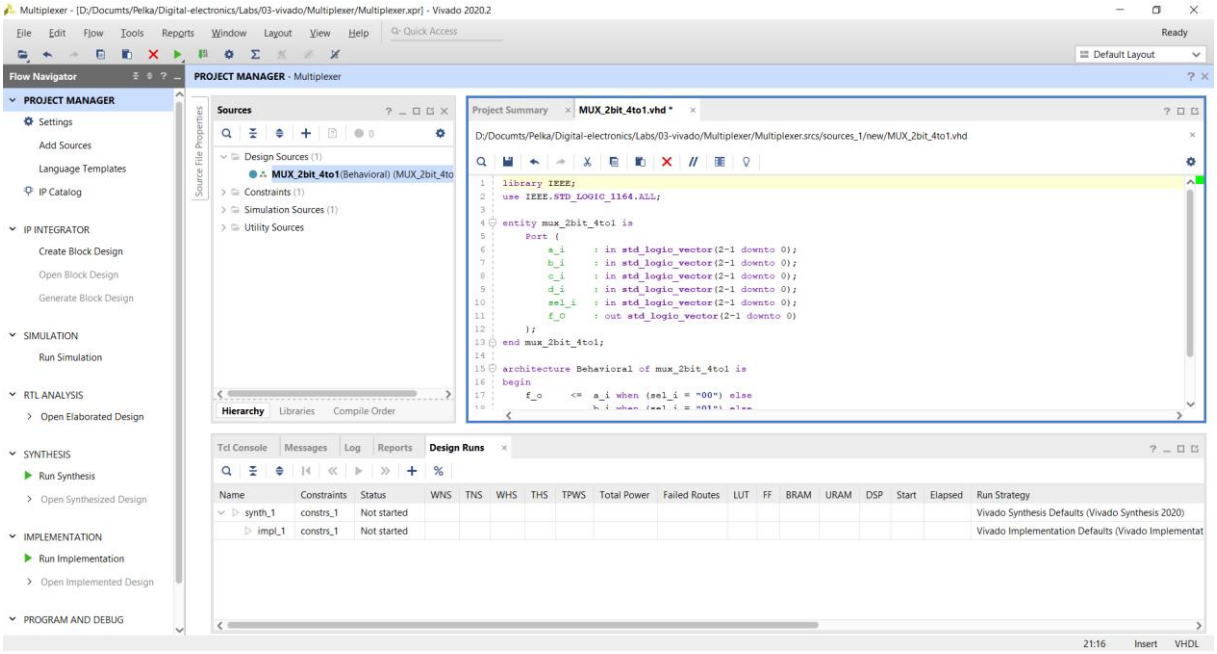

New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Constraint File
Location
tb_MUX_2bit_4to1.xdc
<Local to Project>
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

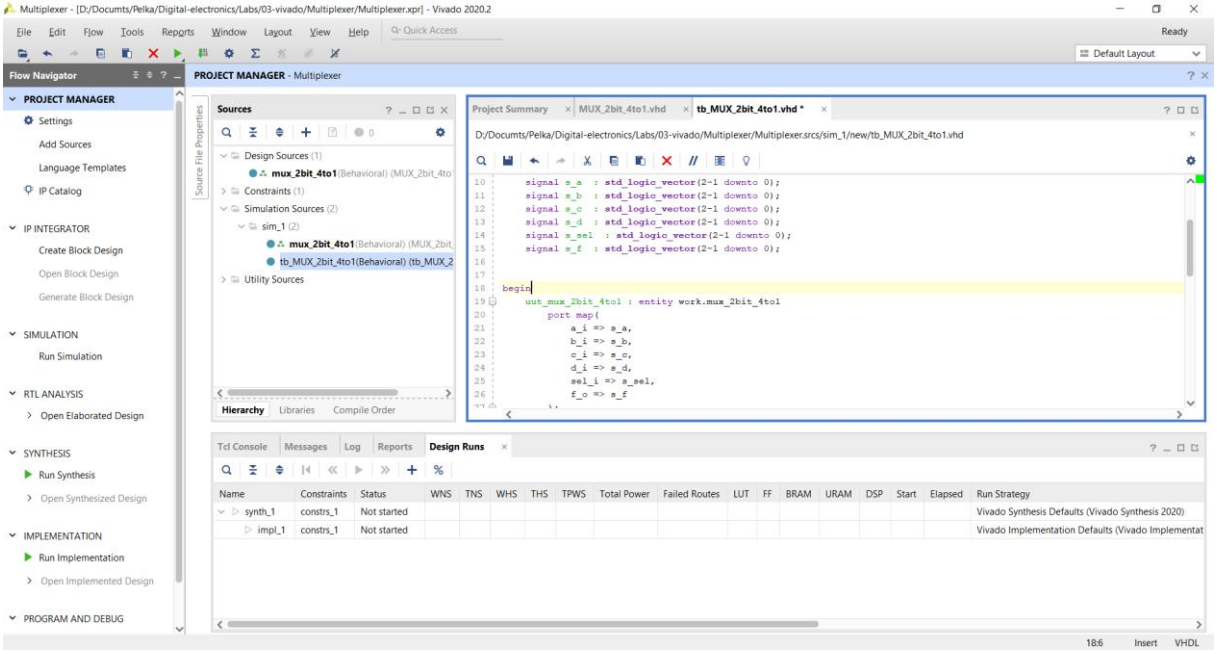

New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Install/Update Boards
Vendor: All
Name: All
Board Rev: Latest
Search:
Display Name
Preview
Vendor
File Version
Part
I/O Pi
Nexys A7-100T
digilentinc.com
1.0
xc7a100tcsg324-1
324
Nexys A7-50T
digilentinc.com
1.0
xc7a50ticsg324-1L
324
Nexys4
digilentinc.com
1.1
xc7a100tcsg324-1
324
Nexys4 DDR
digilentinc.com
1.1
xc7a100tcsg324-1
324
Nexys Video
digilentinc.com
1.1
xc7a200tsbg484-1
484
< Back
Next >
Finish
Cancel

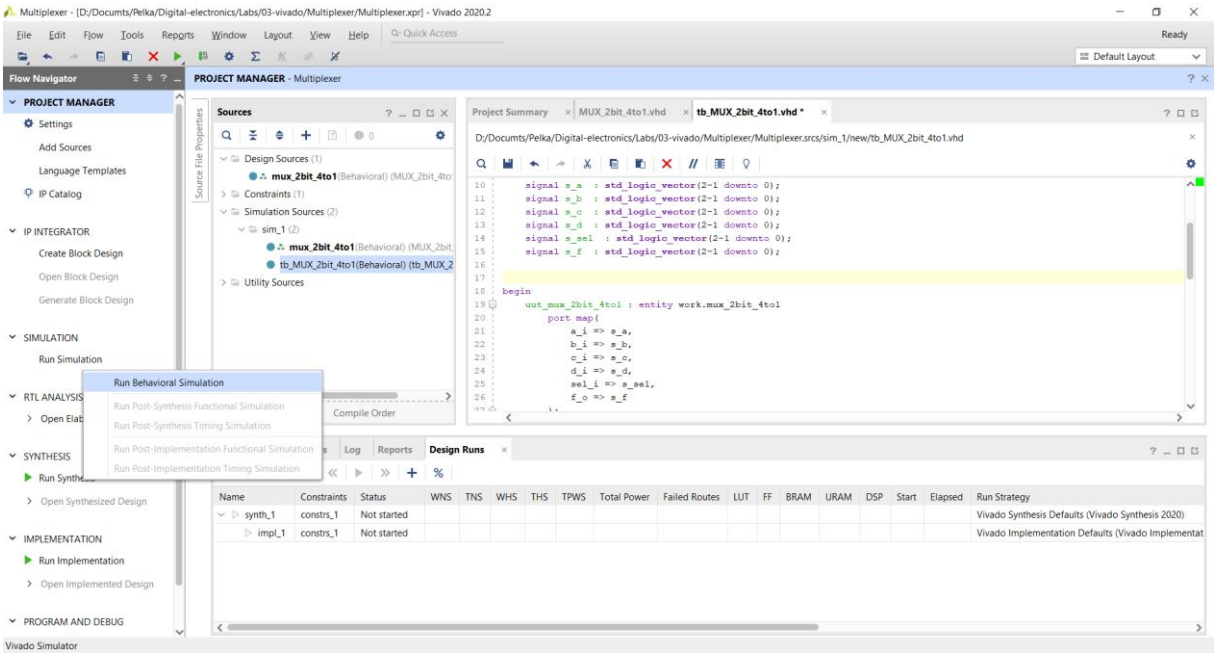

New Project
VIVADO
HLx Editions
New Project Summary
A new RTL project named 'Multiplexer' will be created.
1 source file will be added.
1 constraints file will be added.
The default part and product family for the new project:
Default Board: Nexys A7-50T
Default Part: xc7a50ticsg324-1L
Product: Artix-7
Family: Artix-7
Package: csg324
Speed Grade: -1L
XILINX
To create the project, click Finish
< Back
Next >
Finish
Cancel

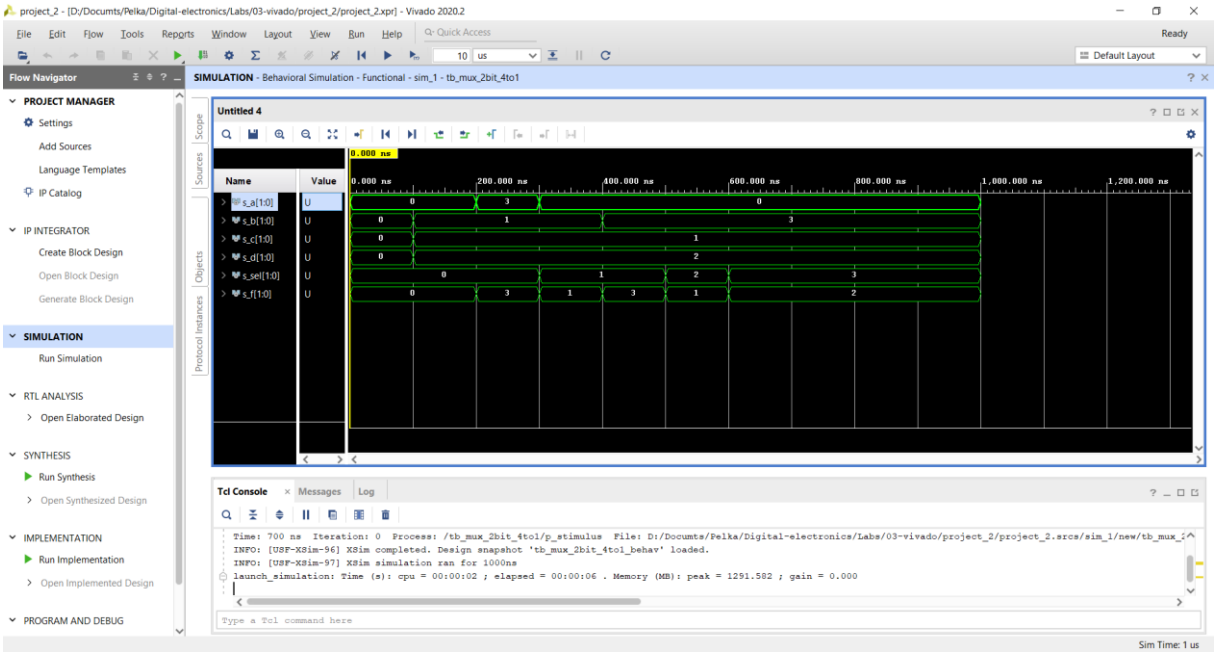

Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Entity name:
MUX_2bit_4to1
Architecture name:
Behavioral
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
in
0
0
OK
Cancel


Define Module
The module definition has not been changed.
Are you sure you want to use these values?
Yes
No


Multiplexer - [D:/Documts/Pelka/Digital-electronics/Labs/03-vivado/Multiplexer/Multiplexer.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
PROJECT MANAGER - Multiplexer
Sources
Design Sources (1)
MUX_2bit_4to1(Behavioral) (MUX_2bit_4to
Constraints (1)
Simulation Sources (1)
Utility Sources
Hierarchy Libraries Compile Order
Project Summary
MUX_2bit_4to1.vhd *
D:/Documts/Pelka/Digital-electronics/Labs/03-vivado/Multiplexer/Multiplexer.srcs/sources_1/new/MUX_2bit_4to1.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity mux_2bit_4to1 is
Port (a_i : in std_logic_vector(2-1 downto 0);
b_i : in std_logic_vector(2-1 downto 0);
c_i : in std_logic_vector(2-1 downto 0);
d_i : in std_logic_vector(2-1 downto 0);
sel_i : in std_logic_vector(2-1 downto 0);
f_o : out std_logic_vector(2-1 downto 0)
);
end mux_2bit_4to1;
architecture Behavioral of mux_2bit_4to1 is
begin
f_o <= a_i when (sel_i = "00") else
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy
synth_1 constrs_1 Not started Vivado Synthesis Defaults (Vivado Synthesis 2020)
impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado Implementat
21:16 Insert VHDL


Multiplexer - [D:/Documts/Pelka/Digital-electronics/Labs/03-vivado/Multiplexer/Multiplexer.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
PROJECT MANAGER - Multiplexer
Sources
Design Sources (1)
mux_2bit_4to1(Behavioral) (MUX_2bit_4to
Constraints (1)
Simulation Sources (2)
sim_1 (2)
mux_2bit_4to1(Behavioral) (MUX_2bit_
tb_MUX_2bit_4to1(Behavioral) (tb_MUX_2
Utility Sources
Hierarchy Libraries Compile Order
Project Summary
MUX_2bit_4to1.vhd
tb_MUX_2bit_4to1.vhd *
D:/Documts/Pelka/Digital-electronics/Labs/03-vivado/Multiplexer/Multiplexer.srcs/sim_1/new/tb_MUX_2bit_4to1.vhd
signal s_a : std_logic_vector(2-1 downto 0);
signal s_b : std_logic_vector(2-1 downto 0);
signal s_c : std_logic_vector(2-1 downto 0);
signal s_d : std_logic_vector(2-1 downto 0);
signal s_sel : std_logic_vector(2-1 downto 0);
signal s_f : std_logic_vector(2-1 downto 0);
begin
uut_mux_2bit_4to1 : entity work.mux_2bit_4to1
port map(
a_i => s_a,
b_i => s_b,
c_i => s_c,
d_i => s_d,
sel_i => s_sel,
f_o => s_f
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy
synth_1 constrs_1 Not started Vivado Synthesis Defaults (Vivado Synthesis 2020)
impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado Implementat
18:6 Insert VHDL


Multiplexer - [D:/Documts/Pelka/Digital-electronics/Labs/03-vivado/Multiplexer/Multiplexer.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elab
SYNTHESIS
Run Synthe
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
PROJECT MANAGER - Multiplexer
Sources
Design Sources (1)
mux_2bit_4to1(Behavioral) (MUX_2bit_4to
Constraints (1)
Simulation Sources (2)
sim_1 (2)
mux_2bit_4to1(Behavioral) (MUX_2bit_
tb_MUX_2bit_4to1(Behavioral) (tb_MUX_2
Utility Sources
Run Behavioral Simulation
Run Post-Synthesis Functional Simulation
Run Post-Synthesis Timing Simulation
Run Post-Implementation Functional Simulation
Run Post-Implementation Timing Simulation
Compile Order
Project Summary
MUX_2bit_4to1.vhd
tb_MUX_2bit_4to1.vhd *
D:/Documts/Pelka/Digital-electronics/Labs/03-vivado/Multiplexer/Multiplexer.srcs/sim_1/new/tb_MUX_2bit_4to1.vhd
signal s_a : std_logic_vector(2-1 downto 0);
signal s_b : std_logic_vector(2-1 downto 0);
signal s_c : std_logic_vector(2-1 downto 0);
signal s_d : std_logic_vector(2-1 downto 0);
signal s_sel : std_logic_vector(2-1 downto 0);
signal s_f : std_logic_vector(2-1 downto 0);
begin
uut_mux_2bit_4to1 : entity work.mux_2bit_4to1
port map(
a_i => s_a,
b_i => s_b,
c_i => s_c,
d_i => s_d,
sel_i => s_sel,
f_o => s_f
Log
Reports
Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy
synth_1 constrs_1 Not started Vivado Synthesis Defaults (Vivado Synthesis 2020)
impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado Implementat
Vivado Simulator


project_2 - [D:/Documts/Pelka/Digital-electronics/Labs/03-vivado/project_2/project_2.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_mux_2bit_4to1
Untitled 4
Name
Value
s_a[1:0]
s_b[1:0]
s_c[1:0]
s_d[1:0]
s_sel[1:0]
s_f[1:0]
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
1,200.000 ns
Tcl Console
Messages
Log
Time: 700 ns Iteration: 0 Process: /tb_mux_2bit_4to1/p_stimulus File: D:/Documts/Pelka/Digital-electronics/Labs/03-vivado/project_2/project_2.srcs/sim_1/new/tb_mux_2
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_mux_2bit_4to1_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:06 . Memory (MB): peak = 1291.582 ; gain = 0.000
Type a Tcl command here
Sim Time: 1 us