nRF24L01
Single Chip 2.4GHz Transceiver

Product Specification

Key Features

- Worldwide 2.4GHz ISM band operation
- Up to 2Mbps on air data rate
- Ultra low power operation
- 11.3mA TX at 0dBm output power
- 12.3mA RX at 2Mbps air data rate
- 900nA in power down
- 22µA in standby-I
- On chip voltage regulator
- 1.9 to 3.6V supply range
- Enhanced ShockBurst™
- Automatic packet handling
- Auto packet transaction handling
- 6 data pipe MultiCeiver™
- Air compatible with nRF2401A, 02, E1 and E2
- Low cost BOM
- ±60ppm 16MHz crystal
- 5V tolerant inputs
- Compact 20-pin 4x4mm QFN package

Applications

- Wireless PC Peripherals
- Mouse, keyboards and remotes
- 3-in-one desktop bundles
- Advanced Media center remote controls
- VoIP headsets
- Game controllers
- Sports watches and sensors
- RF remote controls for consumer electronics
- Home and commercial automation
- Ultra low power sensor networks
- Active RFID
- Asset tracing systems
- Toys

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Objective product specification	This product specification contains target specifications for product development.
Preliminary product specification	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
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Writing Conventions

This product specification follows a set of typographic rules that makes the document consistent and easy to read. The following writing conventions are used:

- Commands, bit state conditions, and register names are written in `Courier`.
- Pin names and pin signal conditions are written in **`Courier bold`**.
- Cross references are underlined and highlighted in blue.

Revision History

Date	Version	Description
July 2007	2.0	• Restructured layout in a new template • Added details of the following features: ▸ Dynamic Payload Length (DPL) ▸ Acknowledgement Payload (`ACK_PLD`) ▸ Feature register ▸ ACTIVATE SPI command ▸ Selective Auto Acknowledgement (`NO_ACK`)

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1 Introduction

The nRF24L01 is a single chip 2.4GHz transceiver with an embedded baseband protocol engine (Enhanced ShockBurst™), designed for ultra low power wireless applications. The nRF24L01 is designed for operation in the world wide ISM frequency band at 2.400 - 2.4835GHz. An MCU (microcontroller) and very few external passive components are needed to design a radio system with the nRF24L01.

The nRF24L01 is configured and operated through a Serial Peripheral Interface (SPI.) Through this interface the register map is available. The register map contains all configuration registers in the nRF24L01 and is accessible in all operation modes of the chip.

The embedded baseband protocol engine (Enhanced ShockBurst™) is based on packet communication and supports various modes from manual operation to advanced autonomous protocol operation. Internal FIFOs ensure a smooth data flow between the radio front end and the system's MCU. Enhanced ShockBurst™ reduces system cost by handling all the high-speed link layer operations.

The radio front end uses GFSK modulation. It has user configurable parameters like frequency channel, output power and air data rate.

The air data rate supported by the nRF24L01 is configurable to 2Mbps. The high air data rate combined with two power saving modes makes the nRF24L01 very suitable for ultra low power designs.

Internal voltage regulators ensure a high Power Supply Rejection Ratio (PSRR) and a wide power supply range.

1.1 Features

Features of the nRF24L01 include:

- Radio
  - Worldwide 2.4GHz ISM band operation
  - 126 RF channels
  - Common RX and TX pins
  - GFSK modulation
  - 1 and 2Mbps air data rate
  - 1MHz non-overlapping channel spacing at 1Mbps
  - 2MHz non-overlapping channel spacing at 2Mbps
- Transmitter
  - Programmable output power: 0, -6, -12 or -18dBm
  - 11.3mA at 0dBm output power
- Receiver
  - Integrated channel filters
  - 12.3mA at 2Mbps
  - -82dBm sensitivity at 2Mbps
  - -85dBm sensitivity at 1Mbps
  - Programmable LNA gain
- RF Synthesizer
  - Fully integrated synthesizer
  - No external loop filer, VCO varactor diode or resonator
  - Accepts low cost ±60ppm 16MHz crystal
- Enhanced ShockBurst™
  - 1 to 32 bytes dynamic payload length
  - Automatic packet handling
  - Auto packet transaction handling
  - 6 data pipe MultiCeiver™ for 1:6 star networks
- Power Management
  - Integrated voltage regulator
  - 1.9 to 3.6V supply range
  - Idle modes with fast start-up times for advanced power management
  - 22uA Standby-I mode, 900nA power down mode
  - Max 1.5ms start-up from power down mode
  - Max 130us start-up from standby-I mode
- Host Interface
  - 4-pin hardware SPI
  - Max 8Mbps
  - 3 separate 32 bytes TX and RX FIFOs
  - 5V tolerant inputs
- Compact 20-pin 4x4mm QFN package

1.2 Block diagram

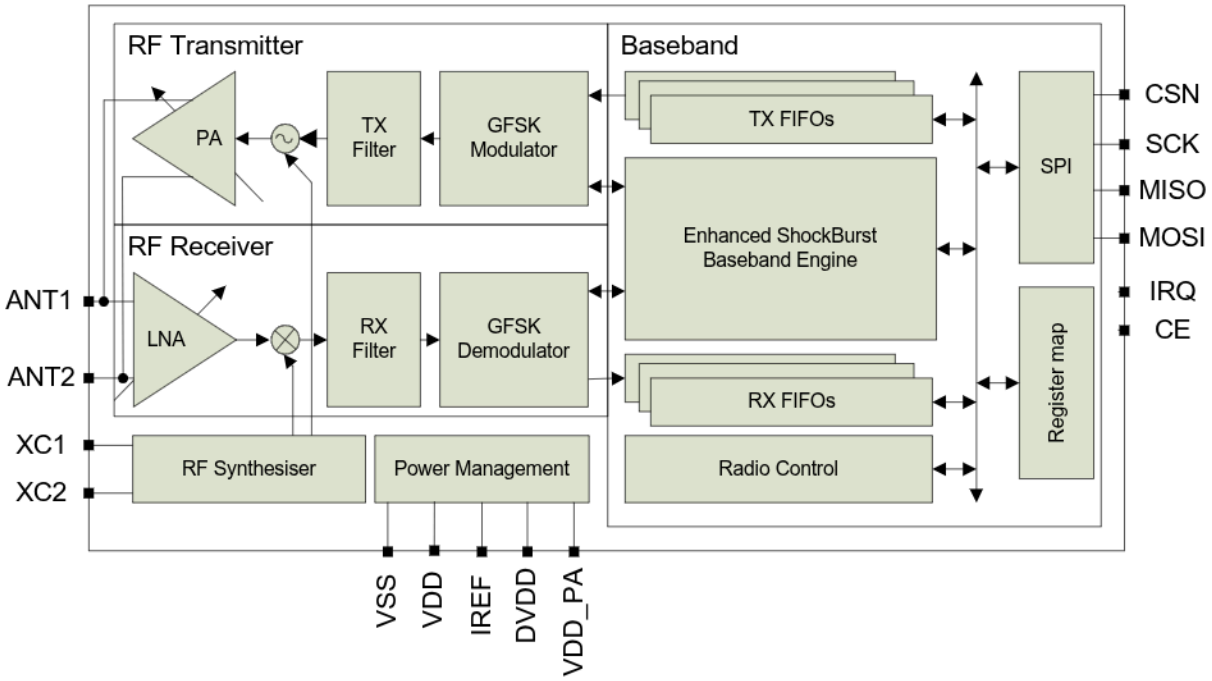


Figure 1. nRF24L01 block diagram

2 Pin Information

2.1 Pin assignment

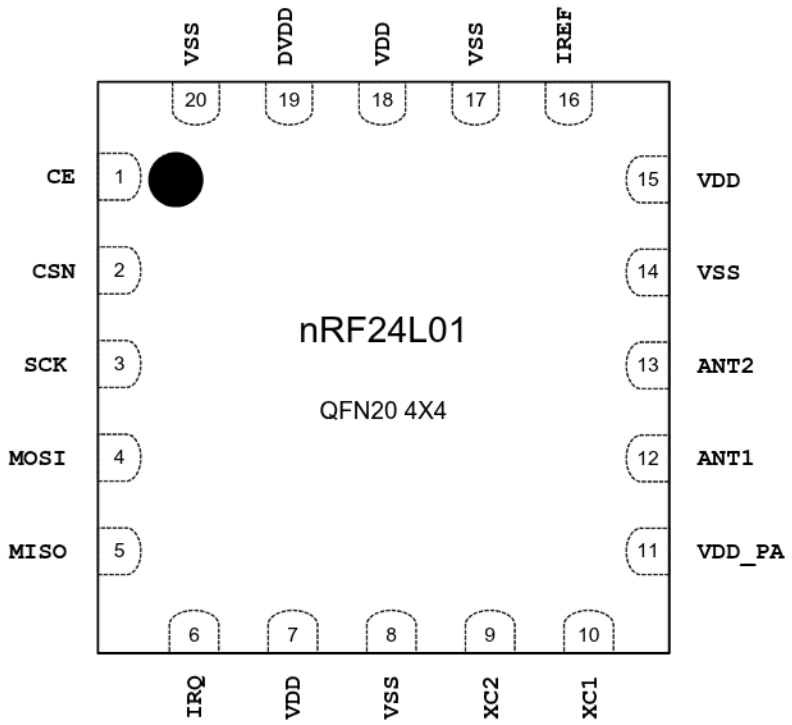


Figure 2. nRF24L01 pin assignment (top view) for the QFN20 4x4 package

2.2 Pin functions

Pin	Name	Pin function	Description
1	CE	Digital Input	Chip Enable Activates RX or TX mode
2	CSN	Digital Input	SPI Chip Select
3	SCK	Digital Input	SPI Clock
4	MOSI	Digital Input	SPI Slave Data Input
5	MISO	Digital Output	SPI Slave Data Output, with tri-state option
6	IRQ	Digital Output	Maskable interrupt pin. Active low
7	VDD	Power	Power Supply (+1.9V - +3.6V DC)
8	VSS	Power	Ground (0V)
9	XC2	Analog Output	Crystal Pin 2
10	XC1	Analog Input	Crystal Pin 1
11	VDD_PA	Power Output	Power Supply Output(+1.8V) for the internal nRF24L01 Power Amplifier. Must be connected to ANT1 and ANT2 as shown in Figure 30.
12	ANT1	RF	Antenna interface 1
13	ANT2	RF	Antenna interface 2
14	VSS	Power	Ground (0V)
15	VDD	Power	Power Supply (+1.9V - +3.6V DC)
16	IREF	Analog Input	Reference current. Connect a 22kΩ resistor to ground. See: Figure 30.
17	VSS	Power	Ground (0V)
18	VDD	Power	Power Supply (+1.9V - +3.6V DC)
19	DVDD	Power Output	Internal digital supply output for de-coupling purposes. See: Figure 30.
20	VSS	Power	Ground (0V)

Table 1. nRF24L01 pin function

3 Absolute maximum ratings

Note: Exceeding one or more of the limiting values may cause permanent damage to nRF24L01.

Operating conditions	Minimum	Maximum	Units
Supply voltages			
VDD	-0.3	3.6	V
VSS		0	V
Input voltage			
V_I	-0.3	5.25	V
Output voltage			
V_O	VSS to VDD	VSS to VDD	
Total Power Dissipation			
P_D (T_A=85°C)		60	mW
Temperatures			
Operating Temperature	-40	+85	°C
Storage Temperature	-40	+125	°C

Table 2. Absolute maximum ratings

4 Operating conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
VDD	Supply voltage		1.9	3.0	3.6	V
VDD	Supply voltage if input signals >3.6V		2.7	3.0	3.3	V
TEMP	Operating Temperature		-40	+27	+85	ºC

Table 3. Operating conditions

5 Electrical specifications

Conditions: VDD = +3V, VSS = 0V, T_A = - 40ºC to + 85ºC

5.1 Power consumption

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
	Idle modes					
I_{VDD_PD}	Supply current in power down			900		nA
I_{VDD_ST1}	Supply current in standby-I mode	a		22		µA
I_{VDD_ST2}	Supply current in standby-II mode			320		µA
I_{VDD_SU}	Average current during 1.5ms crystal oscillator startup			285		µA
	Transmit					
I_{VDD_TX0}	Supply current @ 0dBm output power	b		11.3		mA
I_{VDD_TX6}	Supply current @ -6dBm output power	b		9.0		mA
I_{VDD_TX12}	Supply current @ -12dBm output power	b		7.5		mA
I_{VDD_TX18}	Supply current @ -18dBm output power	b		7.0		mA
I_{VDD_AVG}	Average Supply current @ -6dBm output power, Enhanced ShockBurst™	c		0.12		mA
I_{VDD_TXS}	Average current during TX settling	d		8.0		mA
	Receive					
I_{VDD_2M}	Supply current 2Mbps			12.3		mA
I_{VDD_LC}	Supply current 2Mbps LNA low current			11.5		mA
I_{VDD_1M}	Supply current 1Mbps			11.8		mA
I_{VDD_LC}	Supply current 1Mbps LNA low current			11.1		mA
I_{VDD_RXS}	Average current during RX settling	e		8.4		mA

a. Current is given for a 12pF crystal. Current when using external clock is dependent on signal swing.
b. Antenna load impedance = 15Ω+j88Ω.
c. Antenna load impedance = 15Ω+j88Ω. Average data rate 10kbps and full packets
d. Average current consumption for TX startup (130µs) and when changing mode from RX to TX (130µs).
e. Average current consumption for RX startup (130µs) and when changing mode from TX to RX (130µs).

Table 4.Power consumption

5.2 General RF conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
f_{OP}	Operating frequency	a	2400		2525	MHz
PLL_{res}	PLL Programming resolution			1		MHz
f_{XTAL}	Crystal frequency			16		MHz
Δf_{1M}	Frequency deviation @ 1Mbps			±160		kHz
Δf_{2M}	Frequency deviation @ 2Mbps			±320		kHz
R_{GFSK}	Air Data rate	b	1000		2000	kbps
$F_{CHANNEL\ 1M}$	Non-overlapping channel spacing @ 1Mbps	c		1		MHz
$F_{CHANNEL\ 2M}$	Non-overlapping channel spacing @ 2Mbps	c		2		MHz

a. Usable band is determined by local regulations
b. Data rate in each burst on-air
c. The minimum channel spacing is 1Mhz

Table 5. General RF conditions

5.3 Transmitter operation

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
P_{RF}	Maximum Output Power	a		0	+4	dBm
P_{RFC}	RF Power Control Range		16	18	20	dB
P_{RFCR}	RF Power Accuracy				±4	dB
P_{BW2}	20dB Bandwidth for Modulated Carrier (2Mbps)			1800	2000	kHz
P_{BW1}	20dB Bandwidth for Modulated Carrier (1Mbps)			900	1000	kHz
P_{RF1}	1st Adjacent Channel Transmit Power 2MHz				-20	dBm
P_{RF2}	2nd Adjacent Channel Transmit Power 4MHz				-50	dBm

a. Antenna load impedance = 15Ω+j88Ω

Table 6.Transmitter operation

5.4 Receiver operation

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
RX_{max}	Maximum received signal at <0.1% BER			0		dBm
RX_{SENS}	Sensitivity (0.1%BER) @2Mbps			-82		dBm
RX_{SENS}	Sensitivity at (0.1%BER) @1Mbps			-85		dBm
RX selectivity according to ETSI EN 300 440-1 V1.3.1 (2001-09) page 27						
C/I_{CO}	C/I Co-channel (@2Mbps)	a		7		dB
C/I_{1ST}	1st Adjacent Channel Selectivity C/I 2MHz			1		dB
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I 4MHz			-21		dB
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I 6MHz			-27		dB
C/I_{CO}	C/I Co-channel (@1Mbps)	b		9		dB
C/I_{1ST}	1st Adjacent Channel Selectivity C/I 1MHz			8		dB
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I 2MHz			-22		dB
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I 3MHz			-30		dB
RX selectivity with nRF24L01 equal modulation on interfering signal						
C/I_{CO}	C/I Co-channel (@2Mbps) (Modulated carrier)	a		11		dB
C/I_{1ST}	1st Adjacent Channel Selectivity C/I 2MHz			4		dB
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I 4MHz			-20		dB
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I 6MHz			-27		dB
C/I_{CO}	C/I Co-channel (@1Mbps)	b		12		dB
C/I_{1ST}	1st Adjacent Channel Selectivity C/I 1MHz			8		dB
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I 2MHz			-21		dB
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I 3MHz			-30		dB

a. Data rate is 2Mbps for the following C/I measurements
b. Data rate is 1Mbps for the following C/I measurements

Table 7. Receiver operation

5.5 Crystal specifications

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
Fxo	Crystal Frequency			16		MHz
ΔF	Tolerance	a b		±60		ppm
C_0	Equivalent parallel capacitance			1.5	7.0	pF
C_L	Load capacitance		8	12	16	pF
ESR	Equivalent Series Resistance				100	Ω

a. Frequency accuracy including; tolerance at 25ºC, temperature drift, aging and crystal loading.
b. Frequency regulations in certain regions sets tighter requirements to frequency tolerance (Ex: Japan and Korea max. +/- 50ppm)

Table 8. Crystal specifications

5.6 DC characteristics

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
V_{IH}	HIGH level input voltage		0.7VDD		5.25[a]	V
V_{IL}	LOW level input voltage		VSS		0.3VDD	V

a. If the input signal >3.6V, the VDD of the nRF24L01 must be between 2.7V and 3.3V (3.0V±10%)

Table 9. Digital input pin

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
V_{OH}	HIGH level output voltage (I_{OH}=-0.25mA)		VDD -0.3		VDD	V
V_{OL}	LOW level output voltage (I_{OL}=0.25mA)				0.3	V

Table 10. Digital output pin

5.7 Power on reset

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
T_{PUP}	Power ramp up time	a			100	ms
T_{POR}	Power on reset	b	1.6	5.3	10.3	ms

a. From 0V to 1.9V
b. Measured when the VDD reaches 1.9V to when the reset finishes

Table 11. Power on reset

6 Radio Control

This chapter describes the different modes the nRF24L01 radio transceiver can operate in and the parameters used to control the radio.

The nRF24L01 has a built-in state machine that controls the transitions between the different operating modes of the chip. The state machine takes input from user defined register values and internal signals.

6.1 Operational Modes

The nRF24L01 can be configured in four main modes of operation. This section describes these modes.

6.1.1 State diagram

The state diagram (Figure 3.) shows the modes the nRF24L01 can operate in and how they are accessed. The nRF24L01 is undefined until the **VDD** becomes 1.9V or higher. When this happens nRF24L01 enters the Power on reset state where it remains in reset until it enters the Power Down mode. Even when the nRF24L01 enters Power Down mode the MCU can control the chip through the SPI and the Chip Enable (**CE**) pin Three types of states are used in the state diagram. “Recommended operating mode” is a state that is used during normal operation. “Possible operating mode” is a state that is allowed to use, but it is not used during normal operation. “Transition state” is a time limited state used during start up of the oscillator and settling of the PLL.

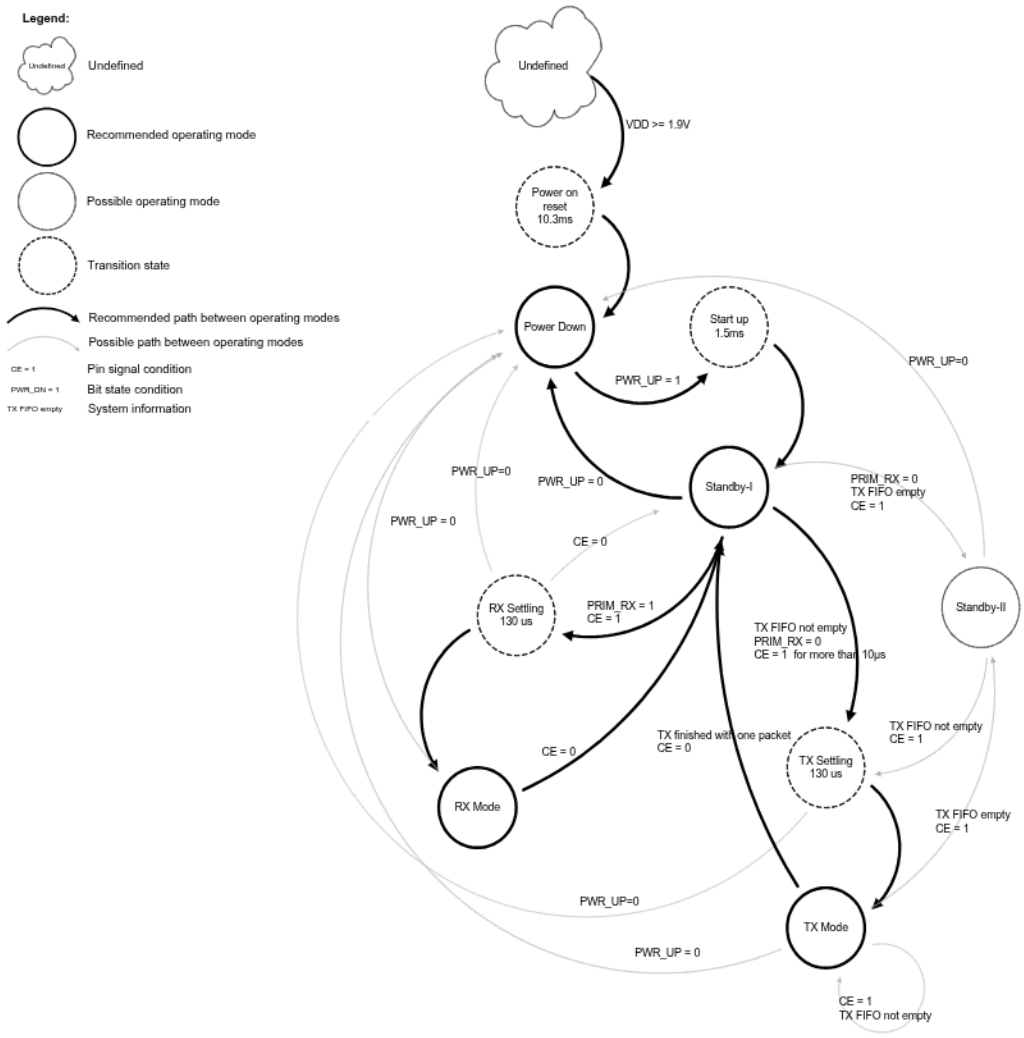


Figure 3. Radio control state diagram

6.1.2 Power Down Mode

In power down mode nRF24L01 is disabled with minimal current consumption. In power down mode all the register values available from the SPI are maintained and the SPI can be activated. For start up time see Table 13. on page 22. Power down mode is entered by setting the `PWR_UP` bit in the `CONFIG` register low.

6.1.3 Standby Modes

By settting the `PWR_UP` bit in the `CONFIG` register to 1, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start up times. In this mode part of the crystal oscillator is active. This is the mode the nRF24L01 returns to from TX or RX mode when **`CE`** is set low.

In standby-II mode extra clock buffers are active compared to standby-I mode and much more current is used compared to standby-I mode. Standby-II occurs when **`CE`** is held high on a PTX device with empty TX FIFO. If a new packet is uploaded to the TX FIFO, the PLL starts and the packet is transmitted.

The register values are maintained during standby modes and the SPI may be activated. For start up time see Table 13. on page 22.

6.1.4 RX mode

The RX mode is an active mode where the nRF24L01 radio is a receiver. To enter this mode, the nRF24L01 must have the `PWR_UP` bit set high, `PRIM_RX` bit set high and the **`CE`** pin set high.

In this mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the baseband protocol engine. The baseband protocol engine constantly searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFO. If the RX FIFO is full, the received packet is discarded.

The nRF24L01 remains in RX mode until the MCU configures it to standby-I mode or power down mode. If the automatic protocol features (Enhanced ShockBurst™) in the baseband protocol engine are enabled, the nRF24L01 can enter other modes in order to execute the protocol.

In RX mode a carrier detect signal is avaliable. The carrier detect is a signal that is set high when a RF signal is detected inside the receiving frequency channel. The signal must be FSK modulated for a secure detection. Other signals can also be detected. The Carrier Detect (`CD`) is set high when an RF signal is detected in RX mode, otherwise `CD` is low. The internal `CD` signal is filtered before presented to `CD` register. The RF signal must be present for at least 128µs before the `CD` is set high. How to use the `CD` is described in Appendix E on page 74.

6.1.5 TX mode

The TX mode is an active mode where the nRF24L01 transmits a packet. To enter this mode, the nRF24L01 must have the `PWR_UP` bit set high, `PRIM_RX` bit set low, a payload in the TX FIFO and, a high pulse on the **`CE`** for more than 10µs.

The nRF24L01 stays in TX mode until it finishes transmitting a current packet. If **`CE`** = 0 nRF24L01 returns to standby-I mode. If **`CE`** = 1, the next action is determined by the status of the TX FIFO. If the TX FIFO is not empty the nRF24L01 remains in TX mode, transmitting the next packet. If the TX FIFO is empty the nRF24L01 goes into standby-II mode.The nRF24L01 transmitter PLL operates in open loop when in TX mode. It is important to never keep the nRF24L01 in TX mode for more than 4ms at a time. If the auto retransmit is enabled, the nRF24L01 is never in TX mode long enough to disobey this rule.

6.1.6 Operational modes configuration

The following table (Table 12.) describes how to configure the operational modes.

Mode	**`PWR_UP`** register	**`PRIM_RX`** register	**`CE`**	FIFO state
RX mode	1	1	1	-
TX mode	1	0	1	Data in TX FIFO. Will empty all levels in TX FIFO[a].
TX mode	1	0	minimum 10µs high pulse	Data in TX FIFO.Will empty one level in TX FIFO[b].
Standby-II	1	0	1	TX FIFO empty
Standby-I	1	-	0	No ongoing packet transmission
Power Down	0	-	-	-

a. In this operating mode if the **CE** is held high the TX FIFO is emptied and all necessary ACK and possible retransmits are carried out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when the **CE** is still high, nRF24L01 enters standby-II mode. In this mode the transmission of a packet is started as soon as the **CSN** is set high after a upload (UL) of a packet to TX FIFO.
b. This operating mode pulses the **CE** high for at least 10µs. This allows one packet to be transmitted. This is the normal operating mode. After the packet is transmittet, the nRF24L01 enters standby-I mode.

Table 12. nRF24L01 main modes

6.1.7 Timing Information

The timing information in this section is related to the transitions between modes and the timing for the **CE** pin. The transition from TX mode to RX mode or vice versa is the same as the transition from standby-I to TX mode or RX mode,Tstby2a.

Name	nRF24L01	Max.	Min.	Comments
Tpd2stby	Power Down ➔ Standby mode	1.5ms		Internal crystal oscillator
Tpd2stby	Power Down ➔ Standby mode	150µs		With external clock
Tstby2a	Standby modes ➔ TX/RX mode	130µs		
Thce	Minimum **CE** high		10µs	
Tpece2csn	Delay from **CE** pos. edge to **CSN** low		4µs	

Table 13. Operational timing of nRF24L01

When nRF24L01 is in power down mode it must settle for 1.5ms before it can enter the TX or RX modes. If an *external clock* is used this delay is reduced to 150µs, see Table 13. on page 22. The settling time must be controlled by the MCU.

Note: The register value is lost if **VDD** is turned off. In this case, nRF24L01 must be configured before entering the TX or RX modes.

6.2 Air data rate

The air data rate is the modulated signaling rate the nRF24L01 uses when transmitting and receiving data.

The air data rate can be 1Mbps or 2Mbps. The 1Mbps data rate gives 3dB better receiver sensitivity compared to 2Mbps. High air data rate means lower average current consumption and reduced probability of on-air collisions.

The air data rate is set by the `RF_DR` bit in the `RF_SETUP` register.

A transmitter and a receiver must be programmed with the same air data rate to be able to communicate with each other.

For compatibility with nRF2401A, nRF24E1, nRF2402 and nRF24E2 the air data rate must be set to 1Mbps.

6.3 RF channel frequency

The RF channel frequency determines the center of the channel used by the nRF24L01. The channel occupies a bandwidth of 1MHz at 1Mbps and 2MHz at 2Mbps. nRF24L01 can operate on frequencies from 2.400GHz to 2.525GHz. The resolution of the RF channel frequency setting is 1MHz.

At 2Mbps the channel occupies a bandwidth wider than the resolution of the RF channel frequency setting. To ensure non-overlapping channels in 2Mbps mode, the channel spacing must be 2MHz or more. At 1Mbps the channel bandwidth is the same as the resolution of the RF frequency setting.

The RF channel frequency is set by the `RF_CH` register according to the following formula:

F_0= 2400 + `RF_CH` [MHz]

A transmitter and a receiver must be programmed with the same RF channel frequency to be able to communicate with each other.

6.4 PA control

The PA control is used to set the output power from the nRF24L01 power amplifier (PA). In TX mode PA control has four programmable steps, see Table 14.

The PA control is set by the `RF_PWR` bits in the `RF_SETUP` register.

SPI RF-SETUP (`RF_PWR`)	RF output power	DC current consumption
11	0dBm	11.3mA
10	-6dBm	9.0mA
01	-12dBm	7.5mA
00	-18dBm	7.0mA

Conditions: **VDD** = 3.0V, **VSS** = 0V, T_A = 27ºC, Load impedance = 15Ω+j88Ω.

Table 14. RF output power setting for the nRF24L01

6.5 LNA gain

The gain in the Low Noise Amplifier (LNA) in the nRF24L01 receiver is controlled by the LNA gain setting. The LNA gain makes it possible to reduce the current consumption in RX mode with 0.8mA at the cost of 1.5dB reduction in receiver sensitivity.

The LNA gain has two steps and is set by the `LNA_HCURR` bit in the `RF_SETUP` register.

6.6 RX/TX control

The RX/TX control is set by `PRIM_RX` bit in the `CONFIG` register and sets the nRF24L01 in transmit/receive.

7 Enhanced ShockBurst™

Enhanced ShockBurst™ is a packet based data link layer. It features automatic packet assembly and timing, automatic acknowledgement and re-transmissions of packets. Enhanced ShockBurst™ enables the implementation of ultra low power, high performance communication with low cost host microcontrollers. The features enable significant improvements of power efficiency for bi-directional and uni-directional systems, without adding complexity on the host controller side.

7.1 Features

The main features of Enhanced ShockBurst™ are:

- 1 to 32 bytes dynamic payload length
- Automatic packet handling
- Auto packet transaction handling
  - Auto Acknowledgement
  - Auto retransmit
- 6 data pipe MultiCeiver™ for 1:6 star networks

7.2 Enhanced ShockBurst™ overview

Enhanced ShockBurst™ uses ShockBurst™ for automatic packet handling and timing. During transmit, ShockBurst™ assembles the packet and clocks the bits in the data packet into the transmitter for transmission. During receive, ShockBurst™ constantly searches for a valid address in the demodulated signal. When ShockBurst™ finds a valid address, it processes the rest of the packet and validates it by CRC. If the packet is valid the payload is moved into the RX FIFO. The high speed bit handling and timing is controlled by ShockBurst™.

Enhanced ShockBurst™ features automatic packet transaction handling that enables the implementation of a reliable bi-directional data link. An Enhanced ShockBurst™ packet transaction is a packet exchange between to transceivers, where one transceiver is the Primary Receiver (PRX) and the other is the Primary Transmitter (PTX). An Enhanced ShockBurst™ packet transaction is always initiated by a packet transmission from the PTX, the transaction is complete when the PTX has received an acknowledgment packet (ACK packet) from the PRX.

The automatic packet transaction handling works as follows:

- The user initiates the transaction by transmitting a data packet from the PTX to the PRX. Enhanced ShockBurst™ automatically sets the PTX in receive mode to wait for the ack packet.
- If the packet is received by the PRX, Enhanced ShockBurst™ automatically assembles and transmits an acknowledgment packet (ACK packet) to the PTX before returning to receive mode
- If the PTX does not receive the ACK packet within a set time, Enhanced ShockBurst™ will automatically retransmit the original data packet and set the PTX in receive mode to wait for the ACK packet

The PRX can attach user data to the ACK packet enabling a bi-directional data link. The Enhanced ShockBurst™ is highly configurable; it is possible to configure parameters such as maximum number of retransmits and the delay from one transmission to the next retransmission. All automatic handling is done without involvement of the MCU.

Section 7.3 on page 25 gives a description of the Enhanced ShockBurst packet format, section 7.4 on page 26 describes autmatic packet handling, section 7.5 on page 28 describes automatic packet transaction handling, section 7.6 on page 31 provides flowcharts for PTX and PRX operation.

7.3 Enhanced Shockburst™ packet format

The format of the Enhanced ShockBurst™ packet is described in this chapter. The Enhanched Shock-Burst™ packet contains a preamble field, address field, packet control field, payload field and a CRC field. Figure 4. on page 25 shows the packet format with MSB to the left.

Preamble 1 byte	Address 3-5 byte	Packet Control Field 9 bit	Payload 0 - 32 byte	CRC 1-2 byte

Figure 4. An Enhanced ShockBurst™ packet with payload (0-32 bytes)

7.3.1 Preamble

The preamble is a bit sequence used to detect 0 and 1 levels in the receiver. The preamble is one byte long and is either 01010101 or 10101010. If the first bit in the address is 1 the preamble is automatically set to 10101010 and if the first bit is 0 the preamble is automatically set to 01010101. This is done to ensure there are enough transitions in the preamble to stabilize the receiver.

7.3.2 Address

This is the address for the receiver. An address ensures that the correct packet are detected by the receiver. The address field can be configured to be 3, 4 or, 5 bytes long with the `AW` register.

Note: Addresses where the level shifts only one time (that is, 000FFFFFFF) can often be detected in noise and can give a false detection, which may give a raised Packet-Error-Rate. Addresses as a continuation of the preamble (hi-low toggling) raises the Packet-Error-Rate.

7.3.3 Packet Control Field

Figure 5 shows the format of the 9 bit packet control field, MSB to the left.

Payload length 6bit	PID 2bit	NO_ACK 1bit

Figure 5. Packet control field

The packet control field contains a 6 bit payload length field, a 2 bit PID (Packet Identity) field and, a 1 bit `NO_ACK` flag.

7.3.3.1 Payload length

This 6 bit field specifies the length of the payload in bytes. The length of the payload can be from 0 to 32 bytes.

Coding: 000000 = 0 byte (only used in empty ACK packets.) 100000 = 32 byte, 100001 = Don't care.

This field is only used if the Dynamic Payload Length function is enabled.

7.3.3.2 PID (Packet identification)

The 2 bit PID field is used to detect if the received packet is new or retransmitted. PID prevents the PRX device from presenting the same payload more than once to the MCU. The PID field is incremented at the TX side for each new packet received through the SPI. The PID and CRC fields (see section 7.3.5 on page 26) are used by the PRX device to determine if a packet is retransmitted or new. When several data packets are lost on the link, the PID fields may become equal to the last received PID. If a packet has the same PID as the previous packet, nRF24L01 compares the CRC sums from both packets. If the CRC sums are also equal, the last received packet is considered a copy of the previously received packet and discarded.

7.3.3.3 No Acknowledgment flag(`NO_ACK`)

The Selective Auto Acknowledgement feature controls the `NO_ACK` flag.

This flag is only used when the auto acknowledgement feature is used. Setting the flag high, tells the receiver that the packet is not to be auto acknowledged.

7.3.4 Payload

The payload is the user defined content of the packet. It can be 0 to 32 bytes wide and is transmitted on-air as it is uploaded (unmodified) to the device.

7.3.5 CRC (Cyclic Redundancy Check)

The CRC is the error detection mechanism in the packet. It may either be 1 or 2 bytes and is calculated over the address, Packet Control Field, and Payload.

The polynomial for 1 byte CRC is $X^8 + X^2 + X + 1$. Initial value 0xFF

The polynomial for 2 byte CRC is $X^{16} + X^{12} + X^5 + 1$. Initial value 0xFFFF

No packet is accepted by Enhanced ShockBurst™ if the CRC fails.

7.4 Automatic packet handling

Enhanced ShockBurst™ uses ShockBurst™ for automatic packet handling. The functions are static and dynamic payload length, automatic packet assembly, automatic packet validation and automatic packet disassembly.

7.4.1 Static and Dynamic Payload Length

The Enhanced ShockBurst™ provides two alternatives for handling payload lengths, static and dynamic.

The default alternative is static payload length. With static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by the `RX_PW_Px` registers on the receiver side. The payload length on the transmitter side is set by the number of bytes clocked into the TX_FIFO and must equal the value in the `RX_PW_Px` register on the receiver side

Dynamic Payload Length(DPL) is an alternative to static payload length.DPL enables the transmitter to send packets with variabel payload length to the receiver. This means for a system with different payload lenghts it is not necessary to scale the packet length to the longest payload.

With DPL feature the nRF24L01 can decode the payload length of the received packet automatically instead of using the RX_PW_Px registers. The MCU can read the length of the received payload by using the R_RX_PL_WID command.

In order to enable DPL the EN_DPL bit in the FEATURE register must be set. In RX mode the DYNPD register has to be set. A PTX that transmits to a PRX with DPL enabled must have the DPL_P0 bit in DYNPD set.

7.4.2 Automatic packet assembly

The automatic packet assembly assembles the preamble, address, packet control field, payload and CRC to make a complete packet before it is transmitted.

7.4.2.1 Preamble

The preamble is automaticly generated based on the address field.

7.4.2.2 Address

The address is fetched from the TX_ADDR register. The address field can be configured to be 3, 4 or 5 bytes long with the AW register.

7.4.2.3 Packet control field

For the static packet lenght option the payload length field is not used. With DPL enabled, the value in the payload length field is automaticly set to the number of bytes in the payload clocked into the TX FIFO.

The transmitter increments the PID field each time it generates a new packet and uses the same PID on packets that are retransmitted. Refer to the left flow chart in Figure 6. on page 28

The PTX can set the NO_ACK flag bit in the Packet Control Field with this command:

```
W_TX_PAYLOAD_NOACK
```

However, the function must first be enabled in the FEATURE register by setting the EN_DYN_ACK bit. When you use this option the PTX goes directly to standby-I mode after transmitting the packet and the PRX does not transmit an ACK packet when it receives the packet.

7.4.2.4 Payload

The payload is fetched from the TX FIFO.

7.4.2.5 CRC

The CRC is automaticly calculated based on the packet content with the polynomials in 7.3.5 on page 26.

The number of bytes in the CRC is set by the CRCO bit in the CONFIG register.

7.4.3 Automatic packet validation

Enhanced ShockBurst™ features automatic packet validation. In receive mode the nRF24L01 is constanly searching for a valid address (given in the RX_ADDR registers.) If a valid address is detected the Enhanced ShockBurst™ will start to validate the packet.

With static packet length the Enhanced ShockBurst™ will capture the packet according to the length given by the RX_PW register. With DPL Enhanced ShockBurst™ captures the packet according to the payload lenght field in the packet control field. After capturing the packet Enhanced ShockBurst™ will perform CRC.

If the CRC is valid, Enhanced ShockBurst™ will check PID. The received PID is compared with the previous received PID. If the PID fields are different, the packet is considered new. If the PID fields are equal the receiver must check if the received CRC is equal to the previous CRC. If the CRCs are equal, the packet is defined as equal to the previous packet and is discarded. Refer to the right flow chart in Figure 6. on page 28

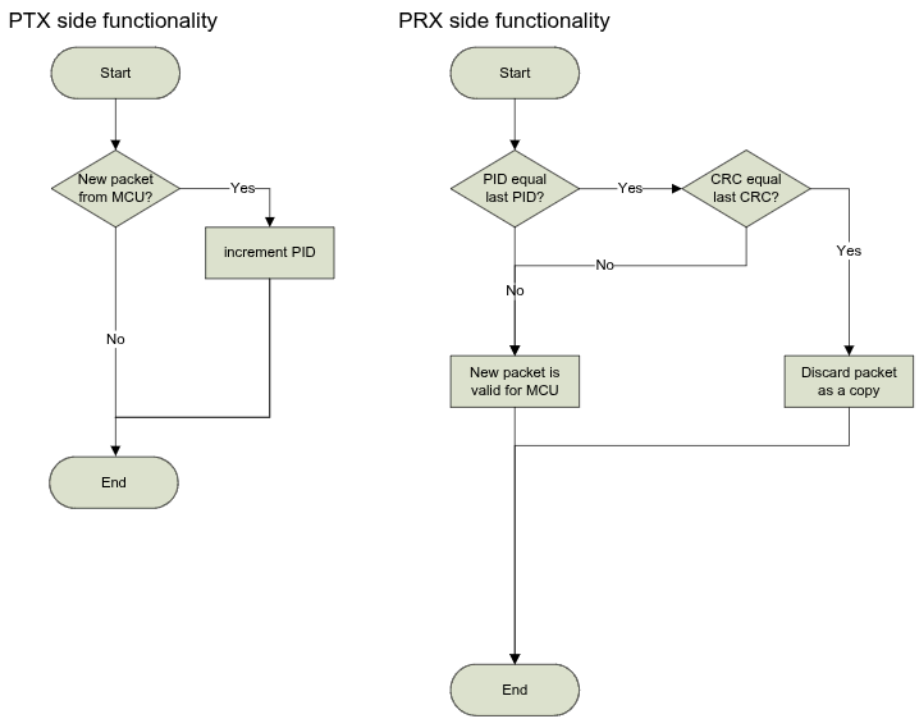


Figure 6. PID generation/detection

7.4.4 Automatic packet disassembly

After the packet is validated,Enhanched ShockBurst™ disassembles the packet and loads the payload into the RX FIFO, and assert the RX_DR IRQ

7.5 Automatic packet transaction handling

Enhanced ShockBurst™ features two functions for automatic packet transaction handling; auto acknowledgement and auto re-transmit.

7.5.1 Auto Acknowledgement

Auto acknowledgment is a function that automatically transmits an ACK packet to the PTX after it has received and validated a packet. The auto acknowledgement function reduces the load of the system MCU and can remove the need for dedicated SPI hardware. This also reduces cost and average current consumption. The Auto Acknowledgement feature is enabled by setting the `EN_AA` register.

Note: If the received packet has the `NO_ACK` flag set, the auto acknowledgement is not executed.

An ACK packet can contain an optional payload from PRX to PTX. In order to use this feature, the dynamic payload length feature mus be enabled. The MCU on the PRX side has to upload the payload by clocking it into the TX FIFO by using the `W_ACK_PAYLOAD` command. The payload is pending in the TX FIFO (PRX) until a new packet is received from the PTX. nRF24L01 can have three ACK packet payloads pending in the TX FIFO (PRX) at the same time.

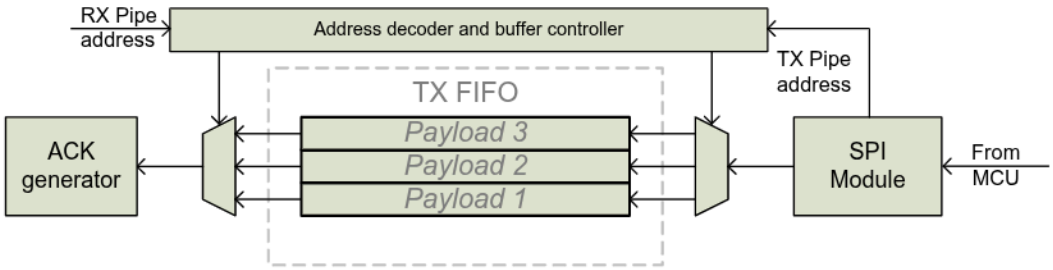


Figure 7. TX FIFO (PRX) with pending payloads

Figure 7. shows how the TX FIFO (PRX) is operated when handling pending ACK packet payloads. From the MCU the payload is clocked in with the `W_ACK_PAYLOAD` command. The address decoder and buffer controller ensure that the payload is stored in a vacant slot in the TX FIFO (PRX). When a packet is received, the address decoder and buffer controller are notified with the PTX address. This ensures that the right payload is presented to the ACK generator.

If the TX FIFO (PRX) contains more than one payload to a PTX, payloads are handled using the first in – first out principle. The TX FIFO (PRX) is blocked if all pending payloads are addressed to a PTX where the link is lost. In this case, the MCU can flush the TX FIFO (PRX) by using the `FLUSH_TX` command.

In order to enable Auto Acknowledgement with payload the `EN_ACK_PAY` bit in the `FEATURE` register must be set.

7.5.2 Auto Retransmission (ART)

The auto retransmission is a function that retransmits a packet if an ACK packet is not received. It is used at the PTX side in an auto acknowledgement system. You can set up the number of times a packet is allowed to be retransmitted if a packet is not acknowledged with the ARC bits in the `SETUP_RETR` register. PTX enters RX mode and waits a time period for an ACK packet each time a packet is transmitted. The time period the PTX is in RX mode is based on the following conditions:

- Auto Retransmit Delay (ARD) elapsed or
- No address match within 250µs or
- After received packet (CRC correct or not) if address match within 250µs

nRF24L01 asserts the `TX_DS` IRQ when the ACK packet is received

nRF24L01 enters standby-I mode if there is no more untransmitted data in the TX FIFO and the **CE** pin is low. If the ACK packet is not received, nRF24L01 goes back to TX mode after a delay defined by ARD and retransmits the data. This continues until acknowledgment is received, or the maximum number of retransmits is reached. Set `PWR_UP` =0 to abort auto retransmission. Two packet loss counters are incremented each time a packet is lost, ARC_CNT and PLOS_CNT in the `OBSERVE_TX` register. The ARC_CNT counts the number of retransmissions for the current transaction. The PLOS_CNT counts the total number of retransmissions since the last channel change. You reset ARC_CNT by initiating a new transaction. You reset `PLOS_CNT` by writing to the `RF_CH` register. It is possible to use the information in the `OBSERVE_TX` register to make a overall assessment of the channel quality.

The ARD defines the time from the end of a transmitted packet to a retransmit starts on the PTX side. ARD is set in `SETUP_RETR` register in steps of 250µs. A retransmit is made if no ACK packet is received by the PTX.

There is a restriction for the length of ARD when using ACK packets with payload. The ARD time must never be shorter than the sum of the startup time and the time on-air for the ACK packet.

For 1Mbps data rate and 5 byte address; 5 byte is maximum ACK packet payload length for ARD=250µs (reset value).

For 2Mbps data rate and 5 byte address; 15 byte is maximum ACK packet payload length for ARD=250µs (reset value).

ARD=500µs will be long enough for any payload length.

As an alternative to Auto Retransmit it is possible to manually set the nRF24L01 to retransmit a packet a number of times. This is done by the `REUSE_TX_PL` command. The MCU must initiate each transmission of the packet with the **CE** pin after this command has been used.

7.6 Enhanced ShockBurst flowcharts

This section shows flowcharts for PTX and PRX operation in Enhanced ShockBurst™. ShockBurst™ operation is marked with a dashed square in the flow charts.

7.6.1 PTX operation

The flowchart in Figure 8. shows how a nRF24L01 configured as a PTX behaves after entering standby-I mode.

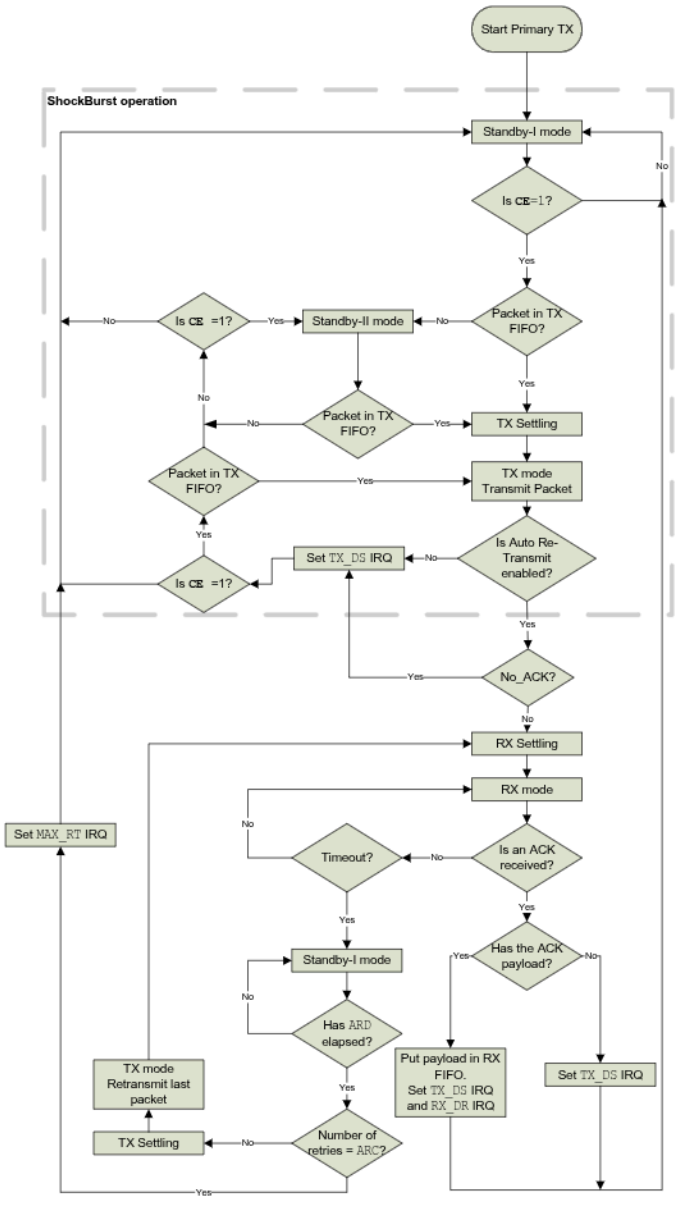


Figure 8. PTX operations in Enhanced ShockBurst™

You activate PTX mode by setting the **CE** pin high. If there is a packet present in the TX FIFO the nRF24L01 enters TX mode and transmits the packet. If Auto Retransmit is enabled, the state machine

checks if the NO_ACK flag is set. If it is not set, the nRF24L01 enters RX mode to receive an ACK packet. If the received ACK packet is empty, only the TX_DS IRQ is asserted. If the ACK packet contains a payload, both TX_DS IRQ and RX_DR IRQ are asserted simultaneously before nRF24L01 returns to standby-I mode.

If the ACK packet is not received before timeout occurs, the nRF24L01 returns to standby-I mode. It stays in standby-I mode until the ARD has elapsed. If the number of retransmits has not reached the ARC, the nRF24L01 enters TX mode and transmits the last packet once more.

While executing the Auto Retransmit feature, the number of retransmits can reach the maximum number defined in ARC. If this happens, the nRF24L01 asserts the MAX_RT IRQ and returns to standby-I mode.

If the **CE** is high and the TX FIFO is empty, the nRF24L01 enters Standby-II mode.

7.6.2 PRX operation

The flowchart in Figure 9. shows how a nRF24L01 configured as a PRX behaves after entering standby-I mode.

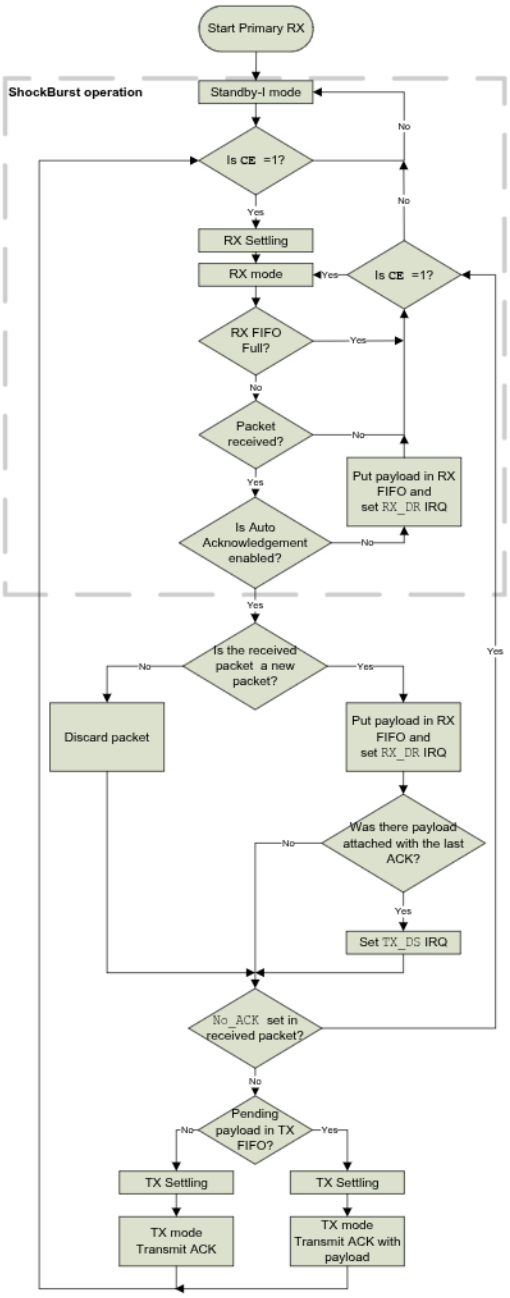


Figure 9. PRX operations in Enhanced ShockBurst™

You activate PRX mode by setting the **CE** pin high. The nRF24L01 enters RX mode and starts searching for packets. If a packet is received and Auto Acknowledgement is enabled the nRF24L01 decides if this is a new packet or a copy of a previously received packet. If the packet is new the payload is made available in the RX FIFO and the `RX_DR` IRQ is asserted. If the last received packet from the transmitter is acknowledged with an ACK packet with payload, the `TX_DS` IRQ indicates that the PTX received the ACK packet

with payload. If the `No_ACK` flag is not set in the received packet, the PRX enters TX mode. If there is a pending payload in the TX FIFO it is attached to the ACK packet. After the ACK packet is transmitted, the nRF24L01 returns to RX mode.

A copy of a previously received packet might be received if the ACK packet is lost. In this case, the PRX discards the received packet and transmits an ACK packet before it returns to RX mode.

7.7 Multiceiver

Multiceiver is a feature used in RX mode that contains a set of 6 parallel data pipes with unique addresses. A data pipe is a logical channel in the physical RF channel. Each data pipe has its own physical address decoding in the nRF24L01.

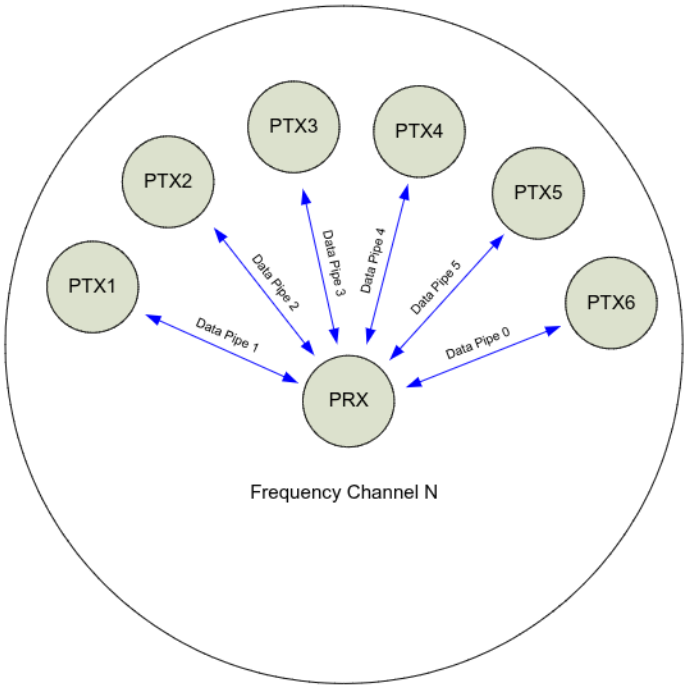


Figure 10. PRX using multiceiver

nRF24L01 configured as PRX (primary receiver) can receive data addressed to six different data pipes in one frequency channel as shown in Figure 10. Each data pipe has its own unique address and can be configured for individual behavior.

Up to six nRF24L01s configured as PTX can communicate with one nRF24L01 configured as PRX. All data pipe addresses are searched for simultaneously. Only one data pipe can receive a packet at a time. All data pipes can perform Enhanced ShockBurst™ functionality.

The following settings are common to all data pipes:

- CRC enabled/disabled (CRC always enabled when Enhanced ShockBurst™ is enabled)
- CRC encoding scheme
- RX address width
- Frequency channel
- Air data rate
- LNA gain

The data pipes are enabled with the bits in the `EN_RXADDR` register. By default only data pipe 0 and 1 are enabled.

Each data pipe address is configured in the `RX_ADDR_PX` registers.

Note: Always ensure that none of the data pipes have the same address.

Each pipe can have up to 5 byte configurable address. Data pipe 0 has a unique 5 byte address. Data pipes 1-5 share the 4 most significant address bytes. The LSByte must be unique for all 6 pipes. Figure 11. is an example of how data pipes 0-5 are addressed.

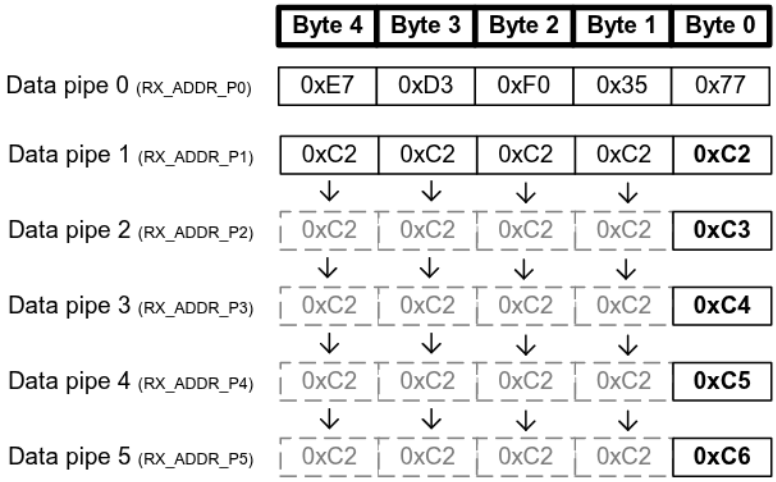


Figure 11. Addressing data pipes 0-5

The PRX, using multiceiver and Enhanced ShockBurst™, receives packets from more than one PTX. To ensure that the ACK packet from the PRX is transmitted to the correct PTX, the PRX takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet. Figure 12. is an example of how address configuration could be for the PRX and PTX. On the PRX the `RX_ADDR_Pn`, defined as the pipe address, must be unique. On the PTX the `TX_ADDR` must be the same as the `RX_ADDR_P0` and as the pipe address for the designated pipe.

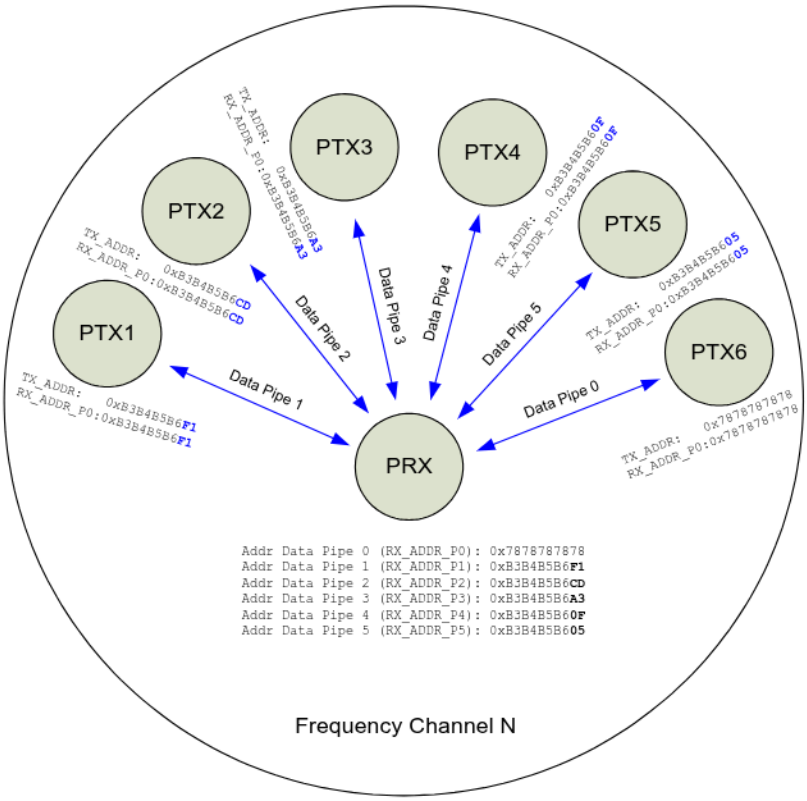
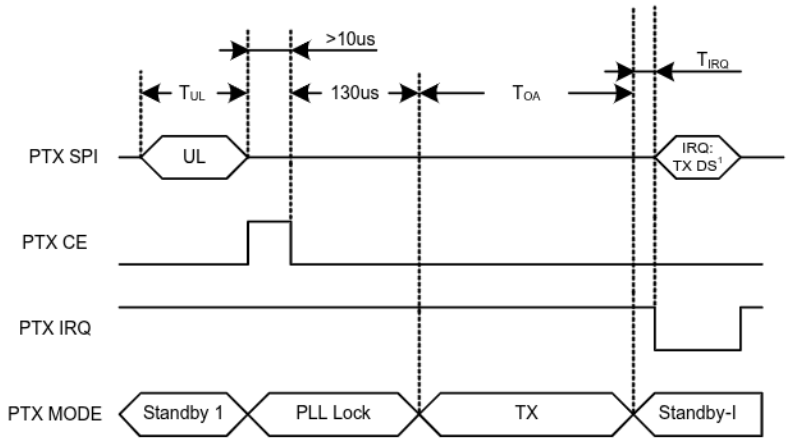


Figure 12. Example of data pipe addressing in multiceiver

No other data pipe can receive data until a complete packet is received by a data pipe that has detected its address. When multiple PTXs are transmitting to a PRX, the ARD can be used to skew the auto retransmission so that they only block each other once.

7.8 Enhanced ShockBurst™ timing

This section describes the timing sequence of Enhanced ShockBurst™ and how all modes are initiated and operated. The Enhanced ShockBurst™ timing is controlled through the Data and Control interface. The nRF24L01 can be set to static modes or autonomous modes where the internal state machine controls the events. Each autonomous mode/sequence is ended with an interrupt at the **IRQ** pin. All the interrupts are indicated as IRQ events in the timing diagrams.



1 IRQ if No Ack is on.

T_{IRQ} = 8.2ηs @ 1Mbps, T_{IRQ} = 6.0ηs @ 2Mbps

Figure 13. Transmitting one packet with NO_ACK *on*

The following equations calculate various timing measurements:

Symbol	Description	Equation
T_{OA}	Time on-air	$T_{OA} = \frac{packet\ length}{air\ data\ rate} = \frac{8\left[bit/byte\right]\cdot\left(1[byte]_{preamble} + 3,4\ or\ 5[bytes]_{address} + N[bytes]_{payload} + 1\ or\ 2[bytes]_{CRC}\right) + 9[bit]_{packet\ control\ field}}{air\ data\ rate\left[bit/s\right]}$
T_{ACK}	Time on-air Ack	$T_{ACK} = \frac{packet\ length}{air\ data\ rate} = \frac{8\left[bit/byte\right]\cdot\left(1[byte]_{preamble} + 3,4\ or\ 5[bytes]_{address} + N[bytes]_{payload} + 1\ or\ 2[bytes]_{CRC}\right) + 9[bit]_{packet\ control\ field}}{air\ data\ rate\left[bit/s\right]}$
T_{UL}	Time Upload	$T_{UL} = \frac{payload\ length}{SPI\ data\ rate} = \frac{8\left[bit/byte\right]\cdot N[bytes]_{payload}}{SPI\ data\ rate\left[bit/s\right]}$
T_{ESB}	Time Enhanced Shock-Burst™ cycle	$T_{ESB} = T_{UL} + 2\cdot T_{stby2a} + T_{ACK} + T_{IRQ}$

Table 15. Timing equations

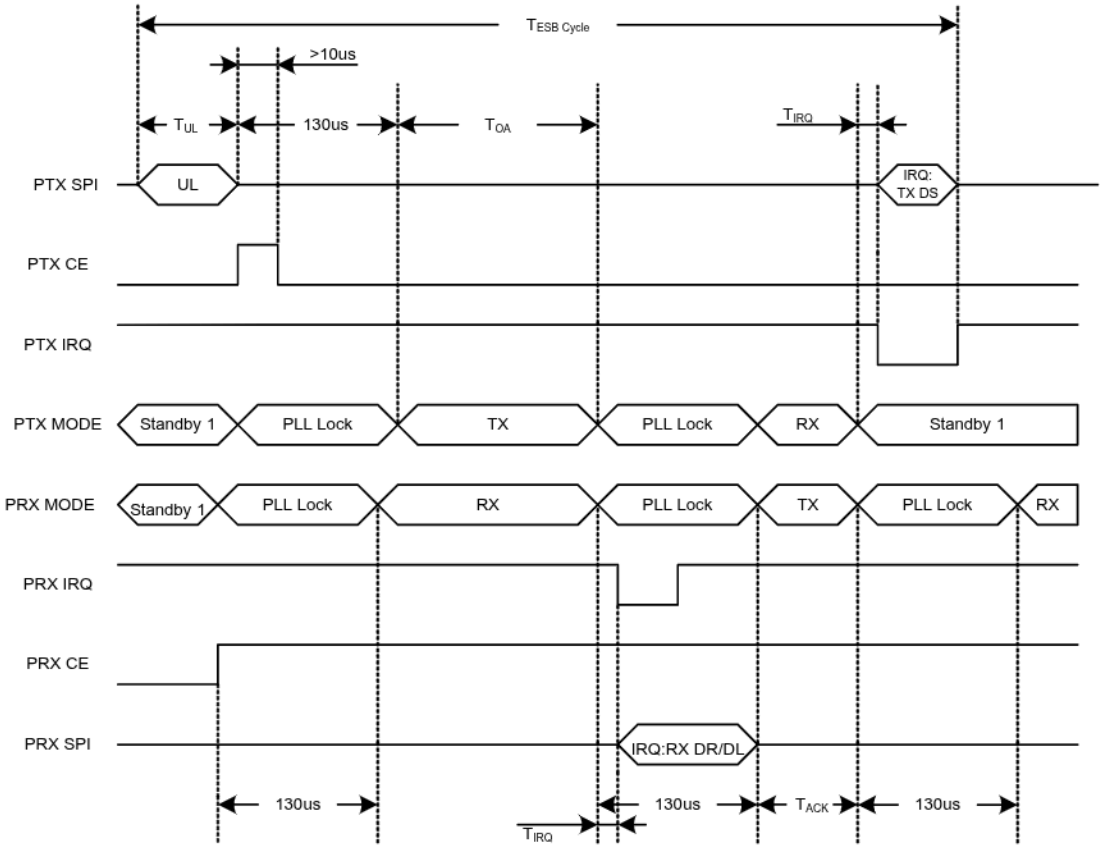


Figure 14. Timing of Enhanced ShockBurst™ for one packet upload (2Mbps)

In Figure 14. the transmission and acknowledgement of a packet are shown. The PRX device is turned into RX mode (**CE**=1), and the PTX device is set to TX mode (**CE**=1 for minimum 10µs). After 130µs the transmission starts and finishes after the elapse of T_{OA}.

When the transmission ends the PTX device automatically switches to RX mode to wait for the ACK packet from the PRX device. After the PTX device receives the ACK packet it responds with an interrupt to the MCU. When the PRX device receives the packet it responds with an interrupt to the MCU.

7.9 Enhanced ShockBurst™ transaction diagram

This section describes how several scenarios for the Enhanced ShockBurst™ automatic transaction handling. The call outs in this section's figures indicate the IRQs and other events. For MCU activity the event may be placed at a different timeframe.

Note: The figures in this section indicate the earliest possible download (DL) of the packet to the MCU and the latest possible upload (UL) of payload to the transmitter.

7.9.1 Single transaction with ACK packet and interrupts

In Figure 15. the basic auto acknowledgement is shown. After the packet is transmitted by the PTX and received by the PRX the ACK packet is transmitted from the PRX to the PTX. The `RX_DR` IRQ is asserted after the packet is received by the PRX, whereas the `TX_DS` IRQ is asserted when the packet is acknowledged and the ACK packet is received by the PTX.

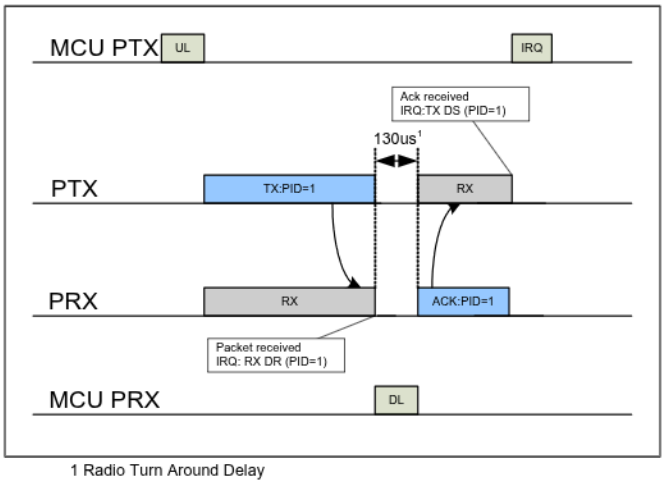


Figure 15. TX/RX cycles with ACK and the according interrupts

7.9.2 Single transaction with a lost packet

Figure 16. is a scenario where a retransmission is needed due to loss of the first packet transmit. After the packet is transmitted, the PTX enters RX mode to receive the ACK packet. After the first transmission, the PTX waits a specified time for the ACK packet, if it is not in the specific time slot the PTX retransmits the packet as shown in Figure 16.

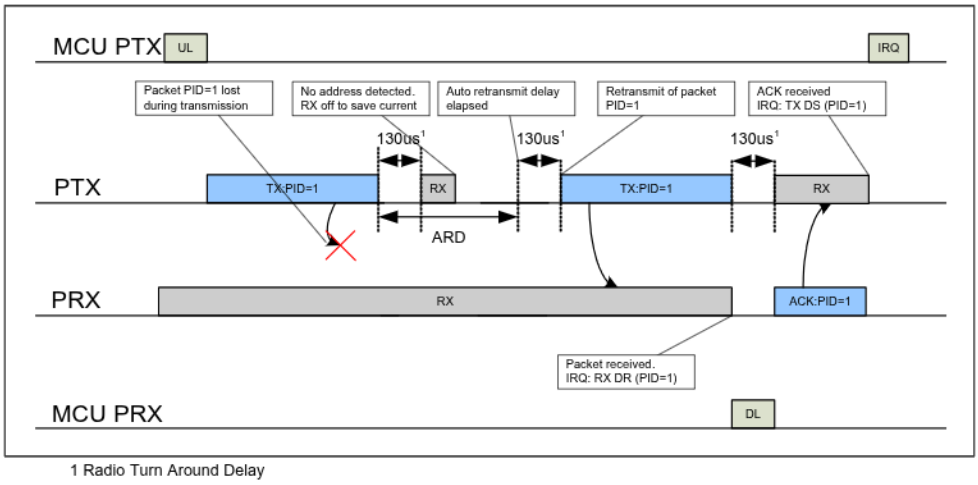


Figure 16. TX/RX cycles with ACK and the according interrupts when the first packet transmit fails

When an address is detected the PTX stays in RX mode until the packet is received. When the retransmitted packet is received by the PRX (see Figure 16.), the `RX_DR` IRQ is asserted and an ACK is transmitted back to the PTX. When the ACK is received by the PTX, the `TX_DS` IRQ is asserted.

7.9.3 Single transaction with a lost ACK packet

Figure 17. is a scenario where a retransmission is needed after a loss of the ACK packet. The corresponding interrupts are also indicated.

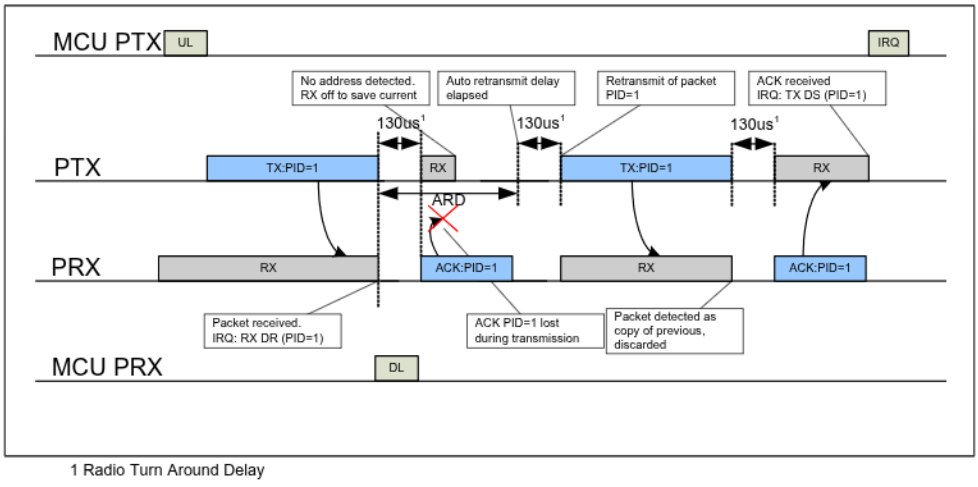
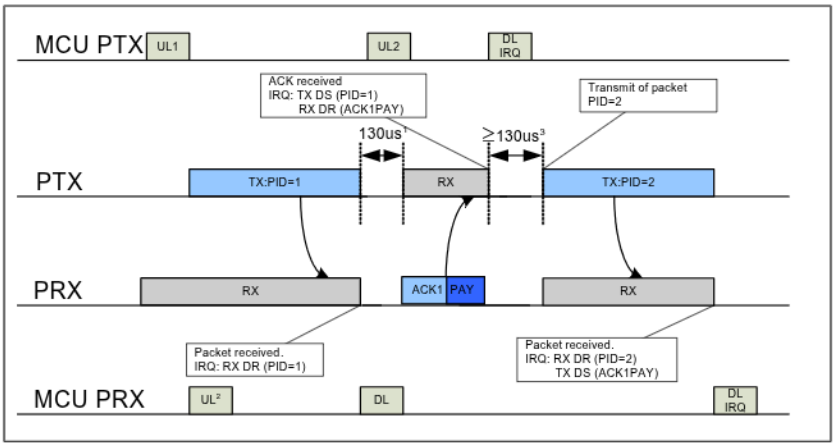


Figure 17. TX/RX cycles with ACK and the according interrupts when the ACK packet fails

7.9.4 Single transaction with ACK payload packet

Figure 18. is a scenario of the basic auto acknowledgement with payload. After the packet is transmitted by the PTX and received by the PRX the ACK packet with payload is transmitted from the PRX to the PTX. The `RX_DR` IRQ is asserted after the packet is received by the PRX, whereas on the PTX side the `TX_DS` IRQ is asserted when the ACK packet is received by the PTX. On the PRX side, the `TX_DS` IRQ for the ACK packet payload is asserted after a new packet from PTX is received. The position of the IRQ in Figure 18. shows where the MCU can respond to the interrupt.

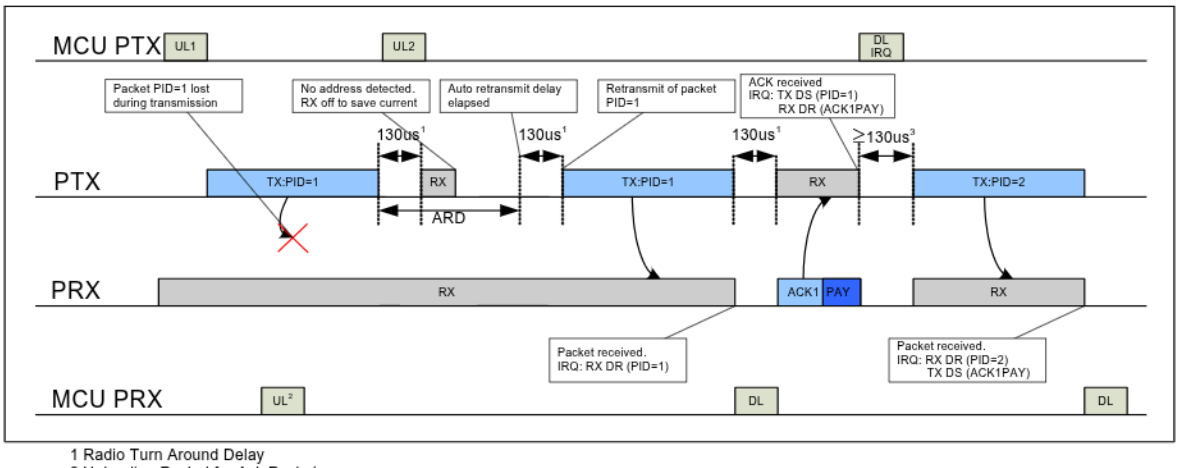


1 Radio Turn Around Delay
2 Uploading Paylod for Ack Packet
3 Delay defined by MCU on PTX side, ≥ 130us

Figure 18. TX/RX cycles with ACK Payload and the according interrupts

7.9.5 Single transaction with ACK payload packet and lost packet

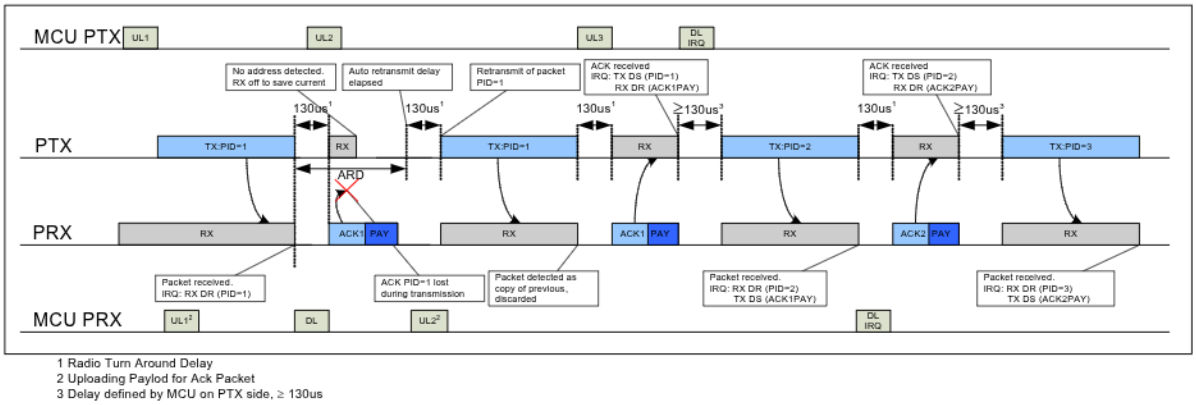
Figure 19. is a scenario where the first packet is lost and a retransmission is needed before the `RX_DR` IRQ on the PRX side is asserted. For the PTX both the `TX_DS` and `RX_DR` IRQ are asserted after the ACK packet is received. After the second packet (PID=2) is received on the PRX side both the `RX_DR` (PID=2) and `TX_DS` (ACK packet payload) IRQ are asserted.



1 Radio Turn Around Delay
2 Uploading Paylod for Ack Packet
3 Delay defined by MCU on PTX side, ≥ 130us

Figure 19. TX/RX cycles and the according interrupts when the packet transmission fails

7.9.6 Two transactions with ACK payload packet and the first ACK packet lost.

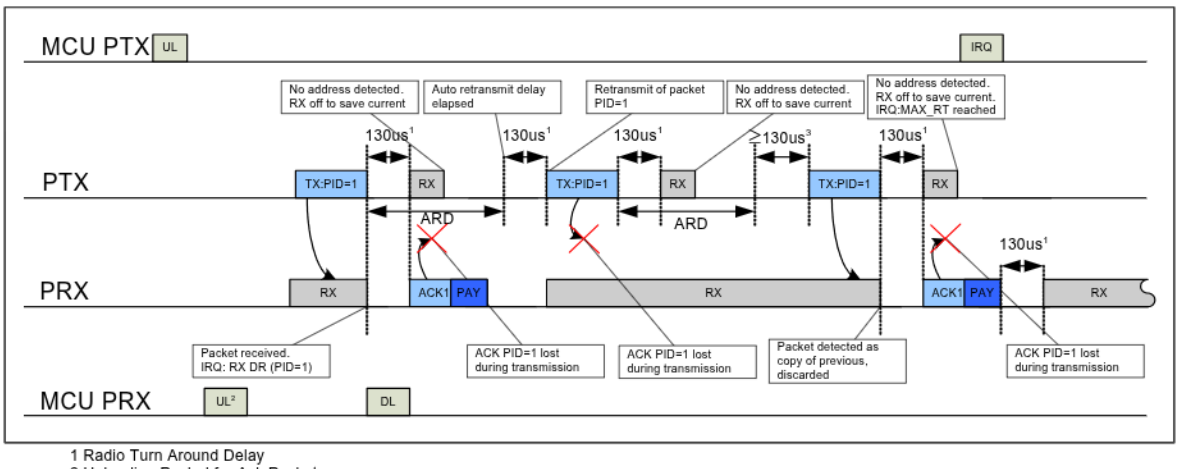


1 Radio Turn Around Delay
2 Uploading Paylod for Ack Packet
3 Delay defined by MCU on PTX side, ≥ 130us

Figure 20. TX/RX cycles with ACK Payload and the according interrupts when the ACK packet fails

In Figure 20. the ACK packet is lost and a retransmission is needed before the `TX_DS` IRQ is asserted, but the `RX_DR` IRQ is asserted immediately. The retransmission of the packet (PID=1) results in a discarded packet. For the PTX both the `TX_DS` and `RX_DR` IRQ are asserted after the second transmission of ACK, which is received. After the second packet (PID=2) is received on the PRX both the `RX_DR` (PID=2) and `TX_DS` (ACK1PAY) IRQ is asserted. The callouts explains the different events and interrupts.

7.9.7 Two transactions where max retransmissions is reached



1 Radio Turn Around Delay
2 Uploading Paylod for Ack Packet
3 Delay defined by MCU on PTX side, ≥ 130us

Figure 21. TX/RX cycles with ACK Payload and the according interrupts when the transmission fails. ARC is set to 2.

If the auto retransmit counter (`ARC_CNT`) exceeds the programmed maximum limit (ARC), the `MAX_RT` IRQ is asserted. In Figure 21. the packet transmission ends with a `MAX_RT` IRQ. The payload in TX FIFO is NOT removed and the MCU decides the next step in the protocol. A toggle of the **`CE`** starts a new sequence of transmitting the same packet. The payload can be removed from the TX FIFO using the `FLUSH_TX` command.

7.10 Compatibility with ShockBurst™

The nRF24L01 can have the Enhanced ShockBurst™ feature disabled in order to be backward compatible with the nRF2401A, nRF24E1, nRF2402 and nRF24E2.

Disabling the Enhanced ShockBurst™ features is done by setting register `EN_AA`=0x00 and the `ARC` = 0.

In addition, the nRF24L01 air data rate must be set to 1Mbps.

7.10.1 ShockBurst™ packet format

The ShockBurst™ packet format is described in this chapter. MSB to the left.

Preamble 1 byte	Address 3-5 byte	Payload 1 - 32 byte	CRC 1-2 byte

Figure 22. A ShockBurst™ packet compatible with nRF2401/nRF2402/nRF24E1/nRF24E2 devices.

The ShockBurst™ packet format has a preamble, address, payload and CRC field that is the same as in the Enhanced ShockBurst™ packet format described in section 7.3 on page 25.

The differences between the ShockBurst™ packet and the Enhanced ShockBurst™ packet are:

- The 9 bit Packet Control Field is not present in the ShockBurst™ packet format.
- The CRC is optional in the ShockBurst™ packet format and is controled by the `EN_CRC` bit in the `CONFIG` register.

8 Data and Control Interface

The data and control interface gives you access to all the features in the nRF24L01. The data and control interface consists of the following six 5Volt tolerant digital signals:

- **IRQ** (this signal is active low and is controlled by three maskable interrupt sources)
- **CE** (this signal is active high and is used to activate the chip in RX or TX mode)
- **CSN** (SPI signal)
- **SCK** (SPI signal)
- **MOSI** (SPI signal)
- **MISO** (SPI signal)

You can use the SPI to activate the nRF24L01 data FIFOs or the register map by 1 byte SPI commands during all modes of operation.

8.1 Features

- Special SPI commands for quick access to the most frequently used features
- 0-8Mbps 4-wire SPI serial interface
- 8 bit command set
- Easily configurable register map
- Full three level FIFO for both TX and RX direction

8.2 Functional description

The SPI is a standard SPI with a maximum data rate of 8Mbps.

8.3 SPI operation

This chapter describes the SPI commands and SPI timing.

8.3.1 SPI Commands

The SPI commands are shown in Table 16.. Every new command must be started by a high to low transition on **CSN**.

In parallel to the SPI command word applied on the **MOSI** pin, the STATUS register is shifted serially out on the **MISO** pin.

The serial shifting SPI commands is in the following format:

<**Command word**: MSBit to LSBit (one byte)>

<**Data bytes**: LSByte to MSByte, MSBit in each byte first>

See Figure 23. on page 47 and Figure 24. on page 48 for timing information.

Command name	Command word (binary)	# Data bytes	Operation
R_REGISTER	000A AAAA	1 to 5 LSByte first	Read command and status registers. AAAAA = 5 bit Register Map Address
W_REGISTER	001A AAAA	1 to 5 LSByte first	Write command and status registers. AAAAA = 5 bit Register Map Address Executable in power down or standby modes only.
R_RX_PAYLOAD	0110 0001	1 to 32 LSByte first	Read RX-payload: 1 – 32 bytes. A read operation always starts at byte 0. Payload is deleted from FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32 LSByte first	Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0 used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode Should not be executed during transmission of acknowledge, that is, acknowledge package will not be completed.
REUSE_TX_PL	1110 0011	0	Used for a PTX device Reuse last transmitted payload. Packets are repeatedly retransmitted as long as **CE** is high. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX payload reuse must not be activated or deactivated during package transmission
ACTIVATE	0101 0000	1	This write command followed by data 0x73 activates the following features: • R_RX_PL_WID • W_ACK_PAYLOAD • W_TX_PAYLOAD_NOACK A new ACTIVATE command with the same data deactivates them again. *This is executable in power down or stand by modes only.* The R_RX_PL_WID, W_ACK_PAYLOAD, and W_TX_PAYLOAD_NOACK features registers are initially in a deactivated state; a write has no effect, a read only results in zeros on **MISO**. To activate these registers, use the ACTIVATE command followed by data 0x73. Then they can be accessed as any other register in nRF24L01. Use the same command and data to deactivate the registers again.
R_RX_PL_WID[a]	0110 0000		Read RX-payload width for the top R_RX_PAYLOAD in the RX FIFO.
W_ACK_PAYLOAD[a]	1010 1PPP	1 to 32 LSByte first	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled using first in - first out principle. Write payload: 1– 32 bytes. A write operation always starts at byte 0.

Command name	Command word (binary)	# Data bytes	Operation
W_TX_PAYLOAD_NOACK[a]	1011 000	1 to 32 LSByte first	Used in TX mode. Disables AUTOACK on this specific packet.
NOP	1111 1111	0	No Operation. Might be used to read the STATUS register

a. To activate this feature use the ACTIVATE SPI command followed by data 0x73. The corresponding bits in the FEATURE register shown in Table 24. on page 58 have to be set.

Table 16. Command set for the nRF24L01 SPI

The W_REGISTER and R_REGISTER commands can operate on single or multi-byte registers. When accessing multi-byte registers you read or write to the MSBit of LSByte first. You can terminate the writing before all bytes in a multi-byte register are written, leaving the unwritten MSByte(s) unchanged. For example, the LSByte of RX_ADDR_P0 can be modified by writing only one byte to the RX_ADDR_P0 register. The content of the status register is always read to **MISO** after a high to low transition on **CSN**.

Note: The 3 bit pipe information in the STATUS register is updated during the **IRQ** pin high to low transition. If the STATUS register is read during an **IRQ** pin high to low transition, the pipe information is unreliable.

8.3.2 SPI timing

SPI operation and timing is shown in Figure 23. on page 47 to Figure 25. on page 48 and in Table 18. on page 49 to Table 23. on page 50. nRF24L01 must be in one of the standby modes or in power down mode before writing to the configuration registers.

In Figure 23. on page 47 to Figure 25. on page 48 the following abbreviations are used:

Abbreviation	Description
Cn	SPI command bit
Sn	STATUS register bit
Dn	Data Bit (**Note:** LSByte to MSByte, MSBit in each byte first)

Table 17. Abbreviations used in Figure 23. to Figure 25.

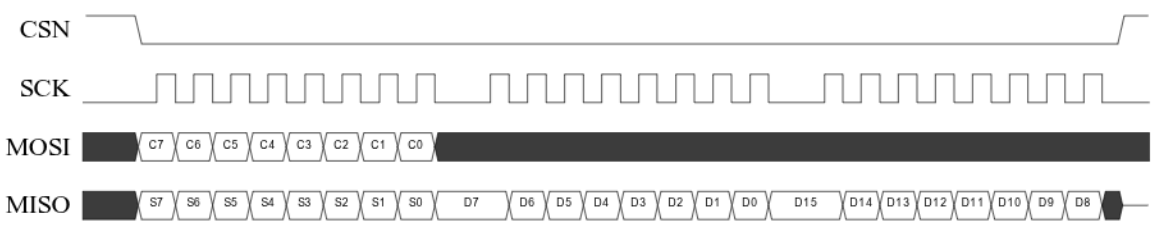


Figure 23. SPI read operation

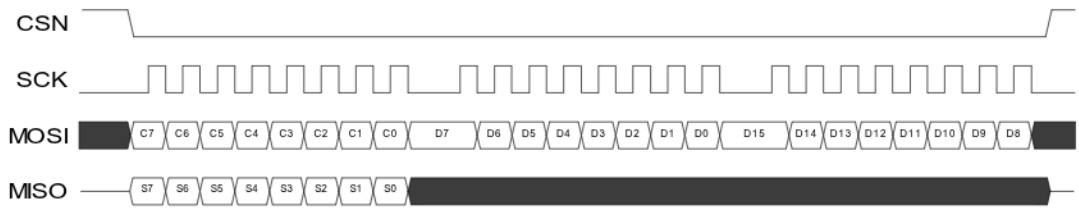


Figure 24. SPI write operation

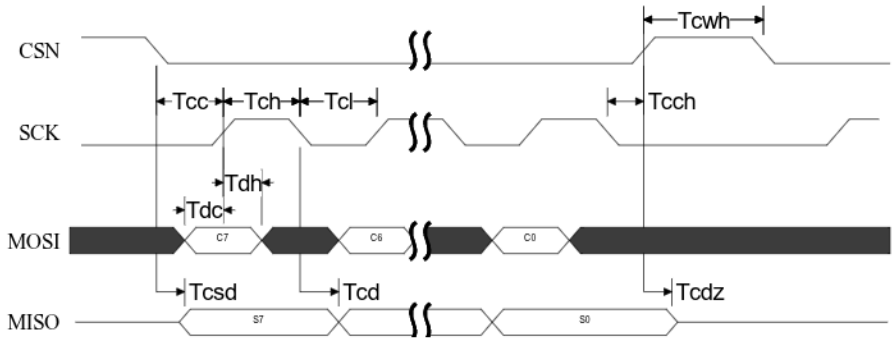


Figure 25. SPI NOP timing diagram

Figure 26. shows the R_{pull} and C_{load} that are referenced in Table 18. to Table 23.

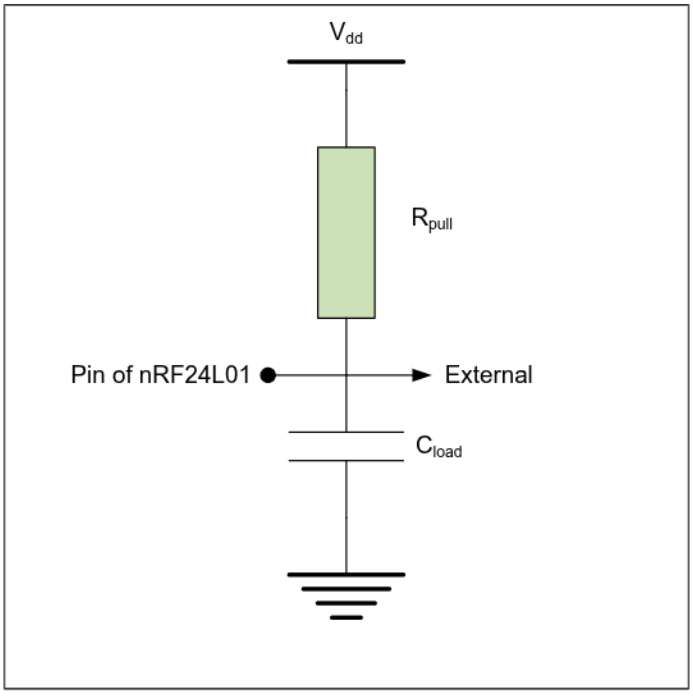


Figure 26. R_{pull} and C_{load}

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		38	ns
Tcd	SCK to Data Valid		55	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	8	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		38	ns

Table 18. SPI timing parameters (C_{load} = 5pF)

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		42	ns
Tcd	SCK to Data Valid		58	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	8	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		42	ns

Table 19. SPI timing parameters (C_{load} = 10pF)

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		75	ns
Tcd	SCK to Data Valid		86	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	5	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		75	ns

Table 20. SPI timing parameters (R_{pull} = 10kΩ, C_{load} = 50pF)

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		116	ns
Tcd	SCK to Data Valid		123	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	4	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		116	ns

Table 21. SPI timing parameters (R_{pull} = 10kΩ, C_{load} = 100pF)

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		75	ns
Tcd	SCK to Data Valid		85	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	5	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		75	ns

Table 22. SPI timing parameters (R_{pull} = 50kΩ, C_{load} = 50pF)

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		116	ns
Tcd	SCK to Data Valid		121	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	4	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		116	ns

Table 23. SPI timing parameters (R_{pull} = 50kΩ, C_{load} = 100pF)

8.4 Data FIFO

The data FIFOs are used to store payload that is transmitted (TX FIFO) or payload that is received and ready to be clocked out (RX FIFO). The FIFOs are accessible in both PTX mode and PRX mode.

The following FIFOs are present in nRF24L01:

- TX three level, 32 byte FIFO
- RX three level, 32 byte FIFO

Both FIFOs have a controller and are accessible through the SPI by using dedicated SPI commands. A TX FIFO in PRX can store payload for ACK packets to three different PTX devices. If the TX FIFO contains more than one payload to a pipe, payloads are handled using the first in - first out principle. The TX FIFO in a PRX is blocked if all pending payloads are addressed to pipes where the link to the PTX is lost. In this case, the MCU can flush the TX FIFO by using the `FLUSH_TX` command.

The RX FIFO in PRX may contain payload from up to three different PTX devices.

A TX FIFO in PTX can have up to three payloads stored.

The TX FIFO can be written to by three commands, `W_TX_PAYLOAD` and `W_TX_PAYLOAD_NO_ACK` in PTX mode and `W_ACK_PAYLOAD` in PRX mode. All three commands give access to the `TX_PLD` register.

The RX FIFO can be read by the command `R_RX_PAYLOAD` in both PTX and PRX mode. This command gives access to the `RX_PLD` register.

The payload in TX FIFO in a PTX is NOT removed if the `MAX_RT` IRQ is asserted. Figure 27. is a block diagram of the TX FIFO and the RX FIFO.

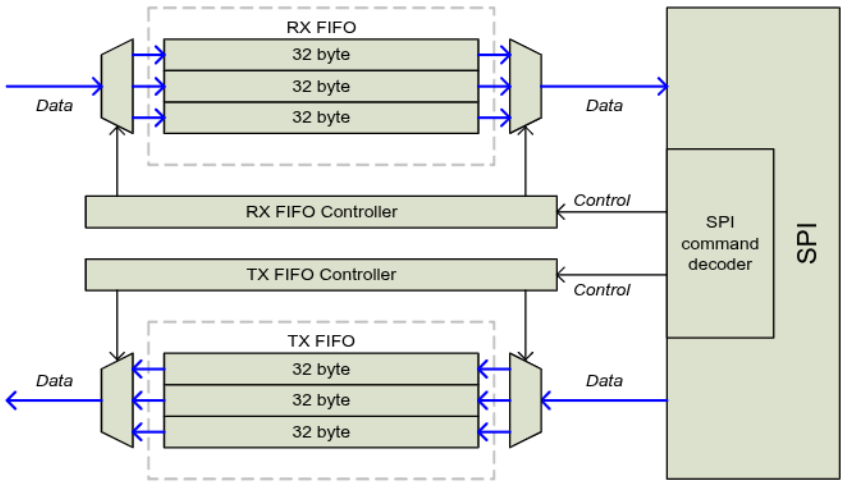


Figure 27. FIFO block diagram

In the `FIFO_STATUS` register it is possible to read if the TX and RX FIFO is full or empty. The `TX_REUSE` bit is also available in the `FIFO_STATUS` register. `TX_REUSE` is set by the SPI command `REUSE_TX_PL`, and is reset by the SPI commands `W_TX_PAYLOAD` or `FLUSH TX`.

8.5 Interrupt

The nRF24L01 has an active low interrupt (**IRQ**) pin. The **IRQ** pin is activated when TX_DS IRQ, RX_DR IRQ or MAX_RT IRQ are set high by the state machine in the STATUS register. The **IRQ** pin resets when MCU writes '1' to the IRQ source bit in the STATUS register. The IRQ mask in the CONFIG register is used to select the IRQ sources that are allowed to assert the **IRQ** pin. By setting one of the MASK bits high, the corresponding IRQ source is disabled. By default all IRQ sources are enabled.

Note: The 3 bit pipe information in the STATUS register is updated during the **IRQ** pin high to low transition. If the STATUS register is read during an **IRQ** pin high to low transition, the pipe information is unreliable.

9 Register Map

You can configure and control the radio chip by accessing the register map through the SPI by using read and write commands.

9.1 Register map table

All undefined bits in the table below are redundant. They are read out as '0'.

Note: Addresses 18 to 1B are reserved for test purposes, altering them will make the chip malfunction.

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
00	CONFIG				Configuration Register
	Reserved	7	0	R/W	Only '0' allowed
	MASK_RX_DR	6	0	R/W	Mask interrupt caused by RX_DR 1: Interrupt not reflected on the **IRQ** pin 0: Reflect RX_DR as active low interrupt on the **IRQ** pin
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS 1: Interrupt not reflected on the **IRQ** pin 0: Reflect TX_DS as active low interrupt on the **IRQ** pin
	MASK_MAX_RT	4	0	R/W	Mask interrupt caused by MAX_RT 1: Interrupt not reflected on the **IRQ** pin 0: Reflect MAX_RT as active low interrupt on the **IRQ** pin
	EN_CRC	3	1	R/W	Enable CRC. Forced high if one of the bits in the EN_AA is high
	CRCO	2	0	R/W	CRC encoding scheme '0' - 1 byte '1' – 2 bytes
	PWR_UP	1	0	R/W	1: POWER UP, 0:POWER DOWN
	PRIM_RX	0	0	R/W	RX/TX control 1: PRX, 0: PTX
01	EN_AA Enhanced ShockBurst™				Enable 'Auto Acknowledgment' Function Disable this functionality to be compatible with nRF2401, see page 65
	Reserved	7:6	00	R/W	Only '00' allowed
	ENAA_P5	5	1	R/W	Enable auto acknowledgement data pipe 5
	ENAA_P4	4	1	R/W	Enable auto acknowledgement data pipe 4
	ENAA_P3	3	1	R/W	Enable auto acknowledgement data pipe 3
	ENAA_P2	2	1	R/W	Enable auto acknowledgement data pipe 2
	ENAA_P1	1	1	R/W	Enable auto acknowledgement data pipe 1
	ENAA_P0	0	1	R/W	Enable auto acknowledgement data pipe 0
02	EN_RXADDR				Enabled RX Addresses
	Reserved	7:6	00	R/W	Only '00' allowed
	ERX_P5	5	0	R/W	Enable data pipe 5.
	ERX_P4	4	0	R/W	Enable data pipe 4.

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
	ERX_P3	3	0	R/W	Enable data pipe 3.
	ERX_P2	2	0	R/W	Enable data pipe 2.
	ERX_P1	1	1	R/W	Enable data pipe 1.
	ERX_P0	0	1	R/W	Enable data pipe 0.
03	SETUP_AW				Setup of Address Widths (common for all data pipes)
	Reserved	7:2	000000	R/W	Only '000000' allowed
	AW	1:0	11	R/W	RX/TX Address field width '00' - Illegal '01' - 3 bytes '10' - 4 bytes '11' – 5 bytes LSByte is used if address width is below 5 bytes
04	SETUP_RETR				Setup of Automatic Retransmission
	ARD	7:4	0000	R/W	Auto Retransmit Delay ‘0000’ – Wait 250µS ‘0001’ – Wait 500µS ‘0010’ – Wait 750µS …….. ‘1111’ – Wait 4000µS (Delay defined from end of transmission to start of next transmission)[a]
	ARC	3:0	0011	R/W	Auto Retransmit Count ‘0000’ –Re-Transmit disabled ‘0001’ – Up to 1 Re-Transmit on fail of AA …… ‘1111’ – Up to 15 Re-Transmit on fail of AA
05	RF_CH				RF Channel
	Reserved	7	0	R/W	Only '0' allowed
	RF_CH	6:0	0000010	R/W	Sets the frequency channel nRF24L01 operates on
06	RF_SETUP				RF Setup Register
	Reserved	7:5	000	R/W	Only '000' allowed
	PLL_LOCK	4	0	R/W	Force PLL lock signal. Only used in test
	RF_DR	3	1	R/W	Air Data Rate ‘0’ – 1Mbps ‘1’ – 2Mbps
	RF_PWR	2:1	11	R/W	Set RF output power in TX mode '00' – -18dBm '01' – -12dBm '10' – -6dBm '11' – 0dBm
	LNA_HCURR	0	1	R/W	Setup LNA gain

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
07	STATUS				Status Register (In parallel to the SPI command word applied on the **MOSI** pin, the STATUS register is shifted serially out on the **MISO** pin)
	Reserved	7	0	R/W	Only '0' allowed
	RX_DR	6	0	R/W	Data Ready RX FIFO interrupt. Asserted when new data arrives RX FIFO[b]. Write 1 to clear bit.
	TX_DS	5	0	R/W	Data Sent TX FIFO interrupt. Asserted when packet transmitted on TX. If AUTO_ACK is activated, this bit is set high only when ACK is received. Write 1 to clear bit.
	MAX_RT	4	0	R/W	Maximum number of TX retransmits interrupt Write 1 to clear bit. If MAX_RT is asserted it must be cleared to enable further communication.
	RX_P_NO	3:1	111	R	Data pipe number for the payload available for reading from RX_FIFO 000-101: Data Pipe Number 110: Not Used 111: RX FIFO Empty
	TX_FULL	0	0	R	TX FIFO full flag. 1: TX FIFO full. 0: Available locations in TX FIFO.
08	OBSERVE_TX				Transmit observe register
	PLOS_CNT	7:4	0	R	Count lost packets. The counter is overflow protected to 15, and discontinues at max until reset. The counter is reset by writing to RF_CH. See page 65 and page 74.
	ARC_CNT	3:0	0	R	Count retransmitted packets. The counter is reset when transmission of a new packet starts. See page 65.
09	CD				
	Reserved	7:1	000000	R	
	CD	0	0	R	Carrier Detect. See page page 74.
0A	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	Receive address data pipe 0. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)
0B	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	Receive address data pipe 1. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)
0C	RX_ADDR_P2	7:0	0xC3	R/W	Receive address data pipe 2. Only LSB. MSBytes is equal to RX_ADDR_P1[39:8]
0D	RX_ADDR_P3	7:0	0xC4	R/W	Receive address data pipe 3. Only LSB. MSBytes is equal to RX_ADDR_P1[39:8]
0E	RX_ADDR_P4	7:0	0xC5	R/W	Receive address data pipe 4. Only LSB. MSBytes is equal to RX_ADDR_P1[39:8]
0F	RX_ADDR_P5	7:0	0xC6	R/W	Receive address data pipe 5. Only LSB. MSBytes is equal to RX_ADDR_P1[39:8]

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
10	TX_ADDR	39:0	0xE7E7E7E7E7	R/W	Transmit address. Used for a PTX device only. (LSByte is written first) Set RX_ADDR_P0 equal to this address to handle automatic acknowledge if this is a PTX device with Enhanced ShockBurst™ enabled. See page 65.
11	RX_PW_P0				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P0	5:0	0	R/W	Number of bytes in RX payload in data pipe 0 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
12	RX_PW_P1				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P1	5:0	0	R/W	Number of bytes in RX payload in data pipe 1 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
13	RX_PW_P2				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P2	5:0	0	R/W	Number of bytes in RX payload in data pipe 2 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
14	RX_PW_P3				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P3	5:0	0	R/W	Number of bytes in RX payload in data pipe 3 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
15	RX_PW_P4				
	Reserved	7:6	00	R/W	Only '00' allowed

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
	RX_PW_P4	5:0	0	R/W	Number of bytes in RX payload in data pipe 4 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
16	RX_PW_P5				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P5	5:0	0	R/W	Number of bytes in RX payload in data pipe 5 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
17	FIFO_STATUS				FIFO Status Register
	Reserved	7	0	R/W	Only '0' allowed
	TX_REUSE	6	0	R	Reuse last transmitted data packet if set high. The packet is repeatedly retransmitted as long as CE is high. TX_REUSE is set by the SPI command REUSE_TX_PL, and is reset by the SPI commands W_TX_PAYLOAD or FLUSH_TX
	TX_FULL	5	0	R	TX FIFO full flag. 1: TX FIFO full. 0: Available locations in TX FIFO.
	TX_EMPTY	4	1	R	TX FIFO empty flag. 1: TX FIFO empty. 0: Data in TX FIFO.
	Reserved	3:2	00	R/W	Only '00' allowed
	RX_FULL	1	0	R	RX FIFO full flag. 1: RX FIFO full. 0: Available locations in RX FIFO.
	RX_EMPTY	0	1	R	RX FIFO empty flag. 1: RX FIFO empty. 0: Data in RX FIFO.
N/A	ACK_PLD[c]	255:0	X	W	Written by separate SPI command ACK packet payload to data pipe number PPP given in SPI command Used in RX mode only Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled first in first out.
N/A	TX_PLD	255:0	X	W	Written by separate SPI command TX data payload register 1 - 32 bytes. This register is implemented as a FIFO with three levels. Used in TX mode only

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
N/A	RX_PLD	255:0	X	R	Read by separate SPI command RX data payload register. 1 - 32 bytes. This register is implemented as a FIFO with three levels. All RX channels share the same FIFO
1C	DYNPD[c]				Enable dynamic payload length
	Reserved	7:6	0	R/W	Only '00' allowed
	DPL_P5	5	0	R/W	Enable dyn. payload length data pipe 5. (Requires EN_DPL and ENAA_P5)
	DPL_P4	4	0	R/W	Enable dyn. payload length data pipe 4. (Requires EN_DPL and ENAA_P4)
	DPL_P3	3	0	R/W	Enable dyn. payload length data pipe 3. (Requires EN_DPL and ENAA_P3)
	DPL_P2	2	0	R/W	Enable dyn. payload length data pipe 2. (Requires EN_DPL and ENAA_P2)
	DPL_P1	1	0	R/W	Enable dyn. payload length data pipe 1. (Requires EN_DPL and ENAA_P1)
	DPL_P0	0	0	R/W	Enable dyn. payload length data pipe 0. (Requires EN_DPL and ENAA_P0)
1D	FEATURE[c]			R/W	Feature Register
	Reserved	7:3	0	R/W	Only '00000' allowed
	EN_DPL	2	0	R/W	Enables Dynamic Payload Length
	EN_ACK_PAY[d]	1	0	R/W	Enables Payload with ACK
	EN_DYN_ACK	0	0	R/W	Enables the W_TX_PAYLOAD_NOACK command

a. This is the time the PTX is waiting for an ACK packet before a retransmit is made. The PTX is in RX mode for a minimum of 250µS, but it stays in RX mode to the end of the packet if that is longer than 250µS. Then it goes to standby-I mode for the rest of the specified ARD. After the ARD it goes to TX mode and then retransmits the packet.

b. The RX_DR IRQ is asserted by a new packet arrival event. The procedure for handling this interrupt should be: 1) read payload through SPI, 2) clear RX_DR IRQ, 3) read FIFO_STATUS to check if there are more payloads available in RX FIFO, 4) if there are more data in RX FIFO, repeat from 1)

c. To activate this feature use the ACTIVATE SPI command followed by data 0x73. The corresponding bits in the FEATURE register must be set.

d. If ACK packet payload is activated, ACK packets have dynamic payload lengths and the Dynamic Payload Length feature should be enabled for pipe 0 on the PTX and PRX. This is to ensure that they receive the ACK packets with payloads. If the payload in ACK is more than 15 byte in 2Mbps mode the ARD must be 500µS or more, and if the payload is more than 5byte in 1Mbps mode the ARD must be 500µS or more.

Table 24. Register map of nRF24L01

10 Peripheral RF Information

This chapter describes peripheral circuitry and PCB layout requirements that are important for achieving optimum RF performance from the nRF24L01.

10.1 Antenna output

The **ANT1** and **ANT2** output pins provide a balanced RF output to the antenna. The pins must have a DC path to **VDD_PA**, either through a RF choke or through the center point in a balanced dipole antenna. A load of 15Ω+j88Ω is recommended for maximum output power (0dBm). Lower load impedance (for instance 50Ω) can be obtained by fitting a simple matching network between the load and **ANT1** and **ANT2**. A recommended matching network for 50Ω load impedance is described in Appendix D on page 69.

10.2 Crystal oscillator

A crystal being used with the nRF24L01 must fulfil the specifications given in Table 8. on page 17.

To achieve a crystal oscillator solution with low power consumption and fast start-up time a crystal with a low load capacitance specification must be used. A lower C_0 also gives lower current consumption and faster start-up time, but may increase the cost of the crystal. Typically C_0=1.5pF at a crystal specified for C_{0max}=7.0pF.

The crystal load capacitance, C_L, is given by:

$C_L = \frac{C_1' \cdot C_2'}{C_1' + C_2'}$, where $C_1' = C_1 + C_{PCB1} + C_{I1}$ and $C_2' = C_2 + C_{PCB2} + C_{I2}$

C_1 and C_2 are SMD capacitors as shown in the application schematics, see Figure 30. on page 69. C_{PCB1} and C_{PCB2} are the layout parasitic on the circuit board. C_{I1} and C_{I2} are the capacitance seen into the **XC1** and **XC2** pins respectively; the value is typically 1pF for each of these pins.

10.3 nRF24L01 sharing crystal with an MCU

When using an MCU to drive the crystal reference input **XC1** of the nRF24L01 transceiver the rules described in the following sections (10.3.1 and 10.3.2) must be followed.

10.3.1 Crystal parameters

The requirement of load capacitance C_L is only set by the MCU when the MCU drives the nRF24L01 clock input. The frequency accuracy of ±60ppm is still required to get a functional radio link. The nRF24L01 loads the crystal by 1pF in addition to the PCB routing.

10.3.2 Input crystal amplitude and current consumption

The input signal should not have amplitudes exceeding any rail voltage. Exceeding rail voltage excites the ESD structure and the radio performance is degraded below specification. You must use an external DC block if you are testing the nRF24L01 with a reference source that has no DC offset (which is often the case with a RF source).

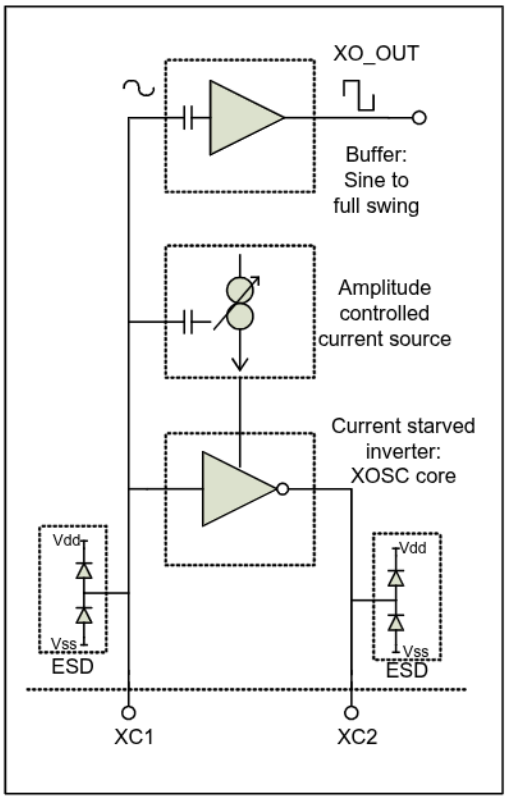


Figure 28. Principle of crystal oscillator

The nRF24L01 crystal oscillator is amplitude regulated. It is recommended to use an input signal larger than 0.4V-peak to achieve low current consumption and good signal-to-noise ratio when using an external clock. **XC2** is not used and can be left as an open pin when clocked externally.

10.4 PCB layout and decoupling guidelines

A well designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss of performance or functionality. A fully qualified RF-layout for the nRF24L01 and its surrounding components, including matching networks, can be downloaded from www.nordicsemi.no.

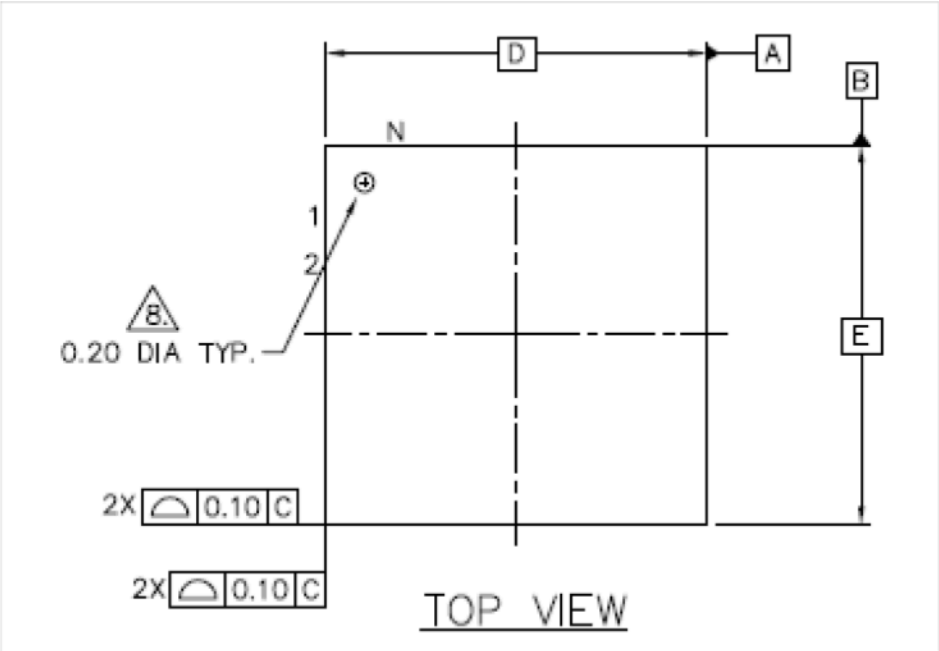
A PCB with a minimum of two layers including a ground plane is recommended for optimum performance. The nRF24L01 DC supply voltage should be decoupled as close as possible to the **VDD** pins with high performance RF capacitors, see Table 26. on page 69. It is preferable to mount a large surface mount capacitor (for example, 4.7µF ceramic) in parallel with the smaller value capacitors. The nRF24L01 supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

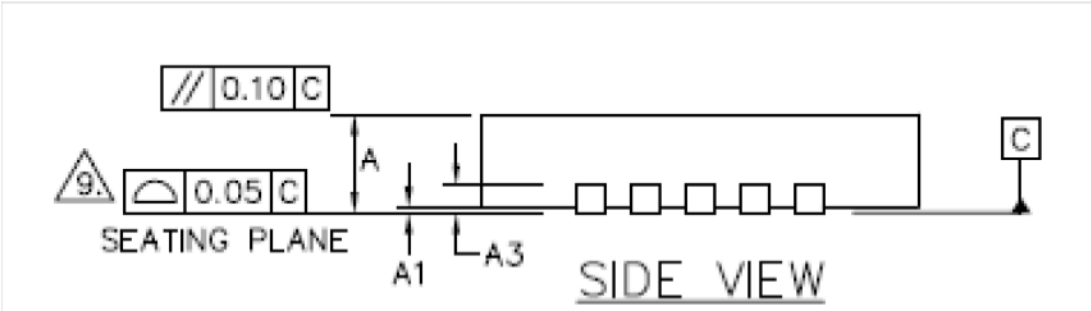
Long power supply lines on the PCB should be avoided. All device grounds, **VDD** connections and **VDD** bypass capacitors must be connected as close as possible to the nRF24L01 IC. For a PCB with a topside RF ground plane, the **VSS** pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the **VSS** pads. A minimum of one via hole should be used for each **VSS** pin.

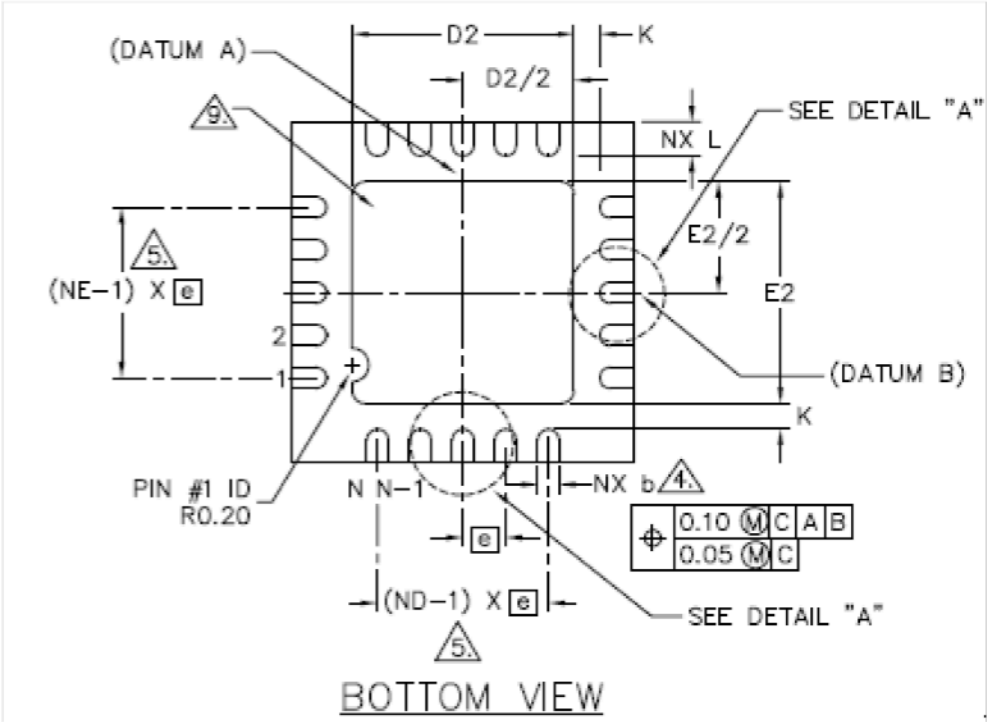
Full swing digital data or control signals should not be routed close to the crystal or the power supply lines. The exposed die attach pad is a ground pad connected to the IC substrate die ground and is intentionally not used in our layouts. It is recommended to keep it unconnected.

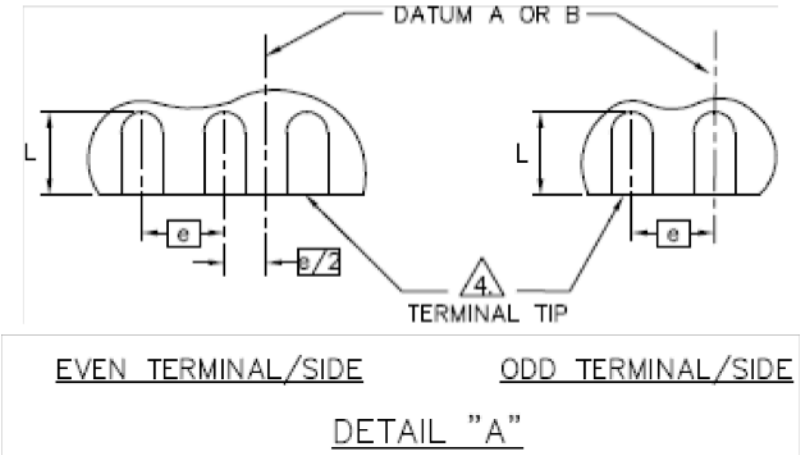
11 Mechanical specifications

nRF24L01 uses the QFN20 4x4 package, with matt tin plating.









Package Type		A	A1	A3	K	D/E	e	D2/E2	L	L1	b
Saw QFN20	**Min**	0.80	0.00					2.50	0.35		0.18
(4x4 mm)	**Typ.**	0.85	0.02	0.20	0.20 min	4.0	0.5 BSC	2.60	0.40	0.15	0.25
	Max	0.95	0.05	REF.		BSC[a]		2.70	0.45	max	0.30

a. BSC: Basic Spacing between Centers, ref. JEDEC standard 95, page 4.17-11/A

Figure 29. nRF24L01 Package Outline

12 Ordering information

Ordering code	Description	Package	Container	MOQ[a]
nRF24L01-REEL	2/1Mbps Transceiver	20 pin QFN 4x4	Tape and reel[b]	4000
nRF24L01-REEL7	2/1Mbps Transceiver	20 pin QFN 4x4	Tape and reel	1500
nRF24L01	2/1Mbps Transceiver	20 pin QFN 4x4	Tray	490
nRF24L01-EVKIT	2 node evaluation	N/A	N/A	1

a. MOQ = Minimum order quantity
b. **Moisture Sensitivity Level:** MSL2@260ºC, three times reflow

12.1 Package marking

n	R	F		*B*	*X*
2	4	L	0	1	
Y	*Y*	*W*	*W*	*L*	*L*

12.2 Abbreviations

Abbreviation	Definition
nRF	Fixed text
B	Variable Build Code, that is, unique code for production sites, package type and test platform
X	“X" grade, i.e. Engineering Samples (optional)
YY	2 digit Year number
WW	2 digit Week number
LL	2 letter wafer lot number code

Attention!

Observe precaution for handling Electrostatic Sensitive Device.

13 Glossary of Terms

Term	Description
ACK	Acknowledgement
ART	Auto Re-Transmit
CE	Chip Enable
CLK	Clock
CRC	Cyclic Redundancy Check
CSN	Chip Select NOT
ESB	Enhanced ShockBurst™
GFSK	Gaussian Frequency Shift Keying
IRQ	Interrupt Request
ISM	Industrial-Scientific-Medical
LNA	Low Noise Amplifier
LSB	Least Significant Bit
LSByte	Least Significant Byte
Mbps	Megabit per second
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
MSByte	Most Significant Byte
PCB	Printed Circuit Board
PID	Packet Identity Bits
PLD	Payload
PRX	Primary RX
PTX	Primary TX
PWR_DWN	Power Down
PWR_UP	Power Up
RoHS	Restriction of use of Certain Hazardous Substances
RX	Receive
RX_DR	Receive Data Ready
SPI	Serial Peripheral Interface
TX	Transmit
TX_DS	Transmit Data Sent

Table 25. Glossary

Appendix A - Enhanced ShockBurst™ - Configuration and Communication Example

Enhanced ShockBurst™ Transmitting Payload

1. The configuration bit PRIM_RX has to be low.
2. When the application MCU has data to transmit, the address for the receiving node (TX_ADDR) and payload data (TX_PLD) has to be clocked into nRF24L01 through the SPI. The width of TX-payload is counted from number of bytes written into the TX FIFO from the MCU. TX_PLD must be written continuously while holding **CSN** low. TX_ADDR does not have to be rewritten if it is unchanged from last transmit. If the PTX device shall receive acknowledge, data pipe 0 has to be configured to receive the ACK packet. The RX address for data pipe 0 (RX_ADDR_P0) has to be equal to the TX address (TX_ADDR) in the PTX device. For the example in Figure 12. on page 37 the following address settings have to be performed for the TX5 device and the RX device:
   TX5 device: TX_ADDR = 0xB3B4B5B605
   TX5 device: RX_ADDR_P0 = 0xB3B4B5B605
   RX device: RX_ADDR_P5 = 0xB3B4B5B605
3. A high pulse on **CE** starts the transmission. The minimum pulse width on **CE** is 10µs.
4. nRF24L01 ShockBurst™:
   - Radio is powered up.
   - 16MHz internal clock is started.
   - RF packet is completed (see the packet description).
   - Data is transmitted at high speed (1Mbps or 2Mbps configured by MCU).
5. If auto acknowledgement is activated (ENAA_P0=1) the radio goes into RX mode immediately, unless the NO_ACK bit is set in the received packet. If a valid packet has been received in the valid acknowledgement time window, the transmission is considered a success. The TX_DS bit in the STATUS register is set high and the payload is removed from TX FIFO. If a valid ACK packet is not received in the specified time window, the payload is retransmitted (if auto retransmit is enabled). If the auto retransmit counter (ARC_CNT) exceeds the programmed maximum limit (ARC), the MAX_RT bit in the STATUS register is set high. The payload in TX FIFO is NOT removed. The **IRQ** pin is active when MAX_RT or TX_DS is high. To turn off the **IRQ** pin, the interrupt source must be reset by writing to the STATUS register (see Interrupt chapter). If no ACK packet is received for a packet after the maximum number of retransmits, no further packets can be transmitted before the MAX_RT interrupt is cleared. The packet loss counter (PLOS_CNT) is incremented at each MAX_RT interrupt. That is, ARC_CNT counts the number of retransmits that was required to get a single packet through. PLOS_CNT counts the number of packets that did not get through after maximum number of retransmits.
6. nRF24L01 goes into standby-I mode if **CE** is low. Otherwise next payload in TX FIFO is transmitted. If TX FIFO is empty and **CE** is still high, nRF24L01 enters standby-II mode.
7. If nRF24L01 is in standby-II mode, it goes to standby-I mode immediately if **CE** is set low.

Enhanced ShockBurst™ Receive Payload

1. RX is selected by setting the PRIM_RX bit in the CONFIG register to high. All data pipes that receive data must be enabled (EN_RXADDR register), auto acknowledgement for all pipes running Enhanced ShockBurst™ has to be enabled (EN_AA register), and the correct payload widths must be set (RX_PW_Px registers). Addresses have to be set up as described in item 2 in the Enhanced ShockBurst™ transmit payload chapter above.
2. Active RX mode is started by setting **CE** high.
3. After 130µs nRF24L01 is monitoring the air for incoming communication.
4. When a valid packet has been received (matching address and correct CRC), the payload is stored in the RX-FIFO, and the RX_DR bit in STATUS register is set high. The **IRQ** pin is active

when RX_DR is high. RX_P_NO in STATUS register indicates what data pipe the payload has been received in.

5. If auto acknowledgement is enabled, an ACK packet is transmitted back, unless the NO_ACK bit is set in the received packet. If there is a payload in the TX_PLD FIFO, this payload is added to the ACK packet.
6. MCU sets the **CE** pin low to enter standby-I mode (low current mode).
7. MCU can clock out the payload data at a suitable rate through the SPI.
8. nRF24L01 is now ready for entering TX or RX mode or power down mode.

Appendix B - Configuration for compatibility with nRF24XX

How to setup nRF24L01 to receive from an nRF2401/nRF2402/nRF24E1/nRF24E2:

1. Use the same CRC configuration as the nRF2401/nRF2402/nRF24E1/nRF24E2
2. Set the `PWR_UP` and `PRIM_RX` bit to 1
3. Disable auto acknowledgement on the data pipe that is addressed
4. Use the same address width as the PTX device
5. Use the same frequency channel as the PTX device
6. Select data rate 1Mbps on both nRF24L01 and nRF2401/nRF2402/nRF24E1/nRF24E2
7. Set correct payload width on the data pipe that is addressed
8. Set **`CE`** high

How to setup nRF24L01 to transmit to an nRF2401/nRF24E1:

1. Use the same CRC configuration as the nRF2401/nRF2402/nRF24E1/nRF24E2
2. Set the `PRIM_RX` bit to 0
3. Set the Auto Retransmit Count to 0 to disable the auto retransmit functionality
4. Use the same address width as the nRF2401/nRF2402/nRF24E1/nRF24E2 uses
5. Use the same frequency channel as the nRF2401/nRF2402/nRF24E1/nRF24E2 uses
6. Select data rate 1Mbps on both nRF24L01 and nRF2401/nRF2402/nRF24E1/nRF24E2
7. Set `PWR_UP` high
8. Clock in a payload that has the same length as the nRF2401/nRF2402/nRF24E1/nRF24E2 is configured to receive
9. Pulse **`CE`** to transmit the packet

Appendix C - Carrier wave output power

The output power of a radio is a critical factor for achieving wanted range. Output power is also the first test criteria needed to qualify for all telecommunication regulations.

Configuration

1. Set `PWR_UP` = 1 in the `CONFIG` register
2. Wait 1.5ms `PWR_UP`->standby
3. Clear the `PRIM_RX` in the `CONFIG` register
4. Set all auto acknowledgement functionality in the `EN_AA` register and the `SETUP_RETR` register to 0
5. Set output power
6. Set `PLL_LOCK` to 1
7. Configure TX address as 5 bytes with all 0xFF
8. Fill the TX payload with 32 bytes of 0xFF
9. Turn off CRC
10. Set the wanted RF channel
11. Transmit the packet by pulsing **`CE`** (minimum 10µs)
12. Wait until the transmission ends (indicated by IRQ going active, a fixed delay of 1ms can also be used)
13. Set **`CE`** high
14. Use the SPI command for re-use of last sent packet (`REUSE_TX_PL`)
15. Keep **`CE`** high as long as the carrier is needed

The nRF24L01 should now output a carrier.

> **Note:** This is not a clean carrier but is slightly modulated by the preamble.

Appendix D - Application example

nRF24L01 with single ended matching network crystal, bias resistor, and decoupling capacitors.

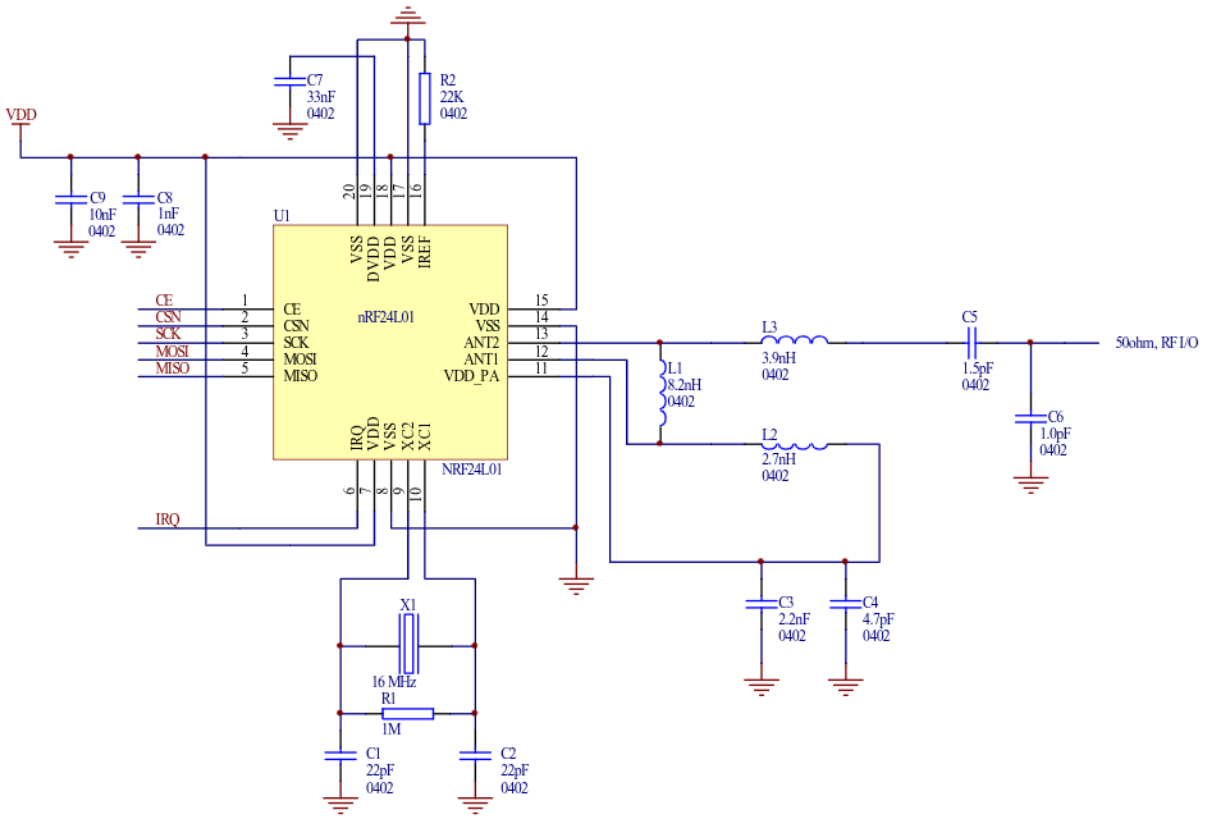


Figure 30. nRF24L01 schematic for RF layouts with single ended 50Ω RF output

Part	Designator	Footprint	Description
22pF[a]	C1	0402	NPO, +/- 2%
22pF[a]	C2	0402	NPO, +/- 2%
2.2nF	C3	0402	X7R, +/- 10%
4.7pF	C4	0402	NPO, +/- 0.25pF
1.5pF	C5	0402	NPO, +/- 0.1pF
1,0pF	C6	0402	NPO, +/- 0.1pF
33nF	C7	0402	X7R, +/- 10%
1nF	C8	0402	X7R, +/- 10%
10nF	C9	0402	X7R, +/- 10%
8,2nH	L1	0402	chip inductor +/- 5%
2.7nH	L2	0402	chip inductor +/- 5%
3,9nH	L3	0402	chip inductor +/- 5%
1MΩ	R1	0402	+/-10%
22kΩ	R2	0402	+/-1%
nRF24L01	U1	QFN20 4x4	
16MHz	X1		+/-60ppm, C_L=12pF

a. C1 and C2 must have values that match the crystals load capacitance, C_L.

Table 26. Recommended components (BOM) in nRF24L01 with antenna matching network

PCB layout examples

Figure 31. on page 70, Figure 32. on page 71 and Figure 33. on page 71 show a PCB layout example for the application schematic in Figure 30. on page 69.

A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane.

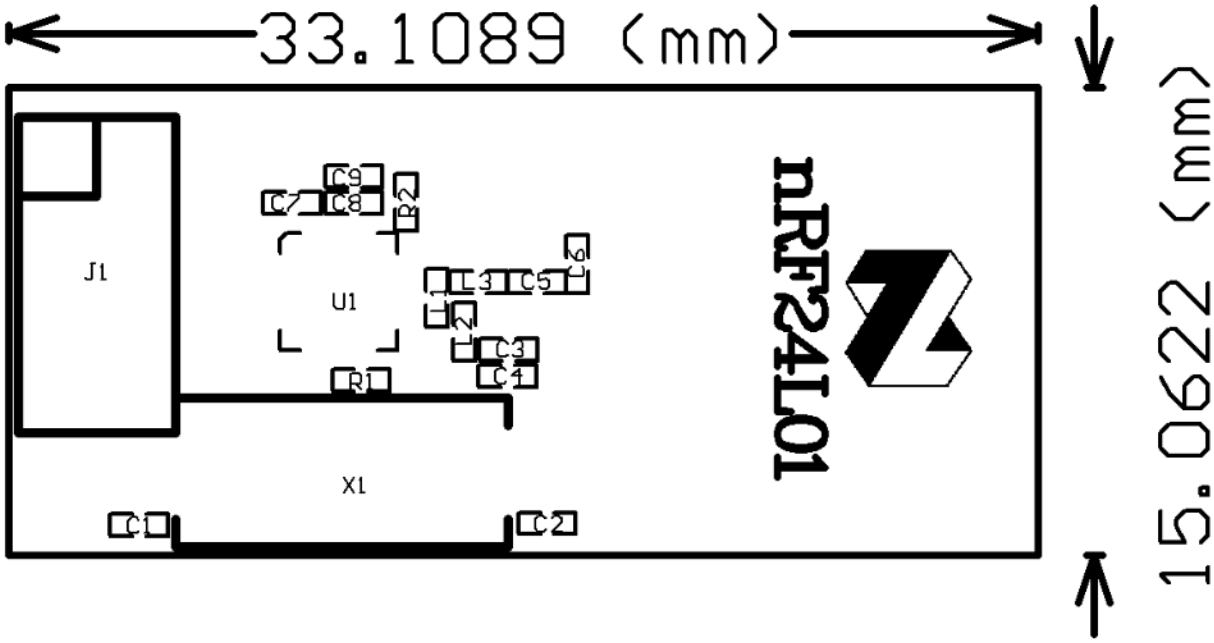


Figure 31. Top overlay (nRF24L01 RF layout with single ended connection to PCB antenna and 0402 size passive components)

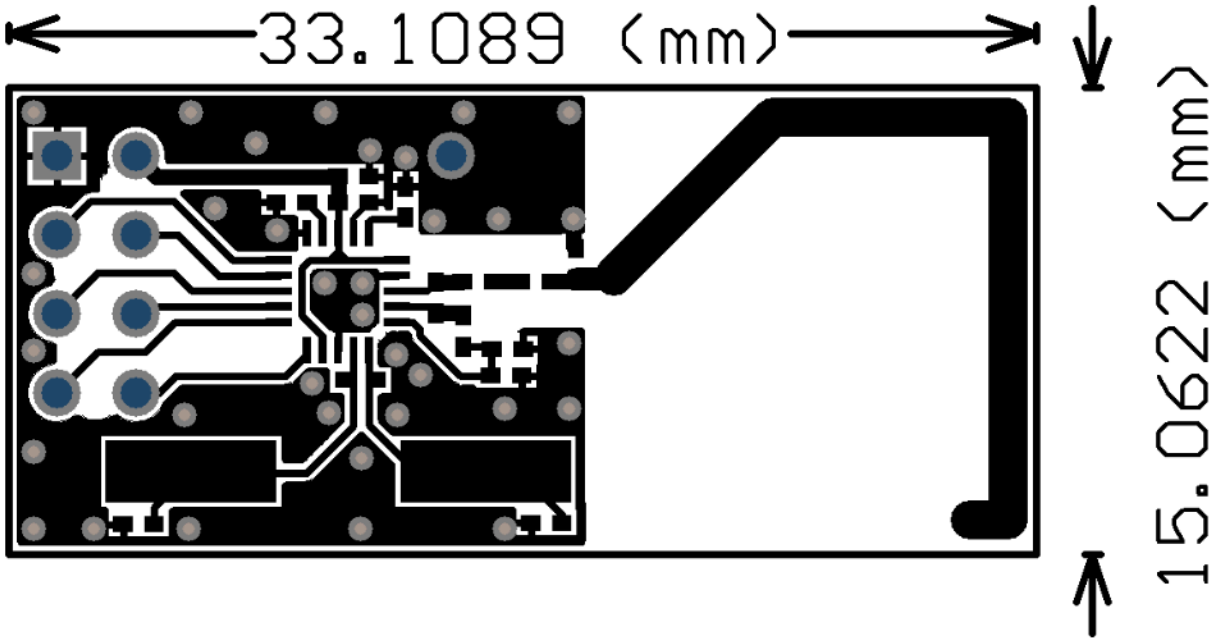


Figure 32. Top layer (nRF24L01 RF layout with single ended connection to PCB antenna and 0402 size passive components)

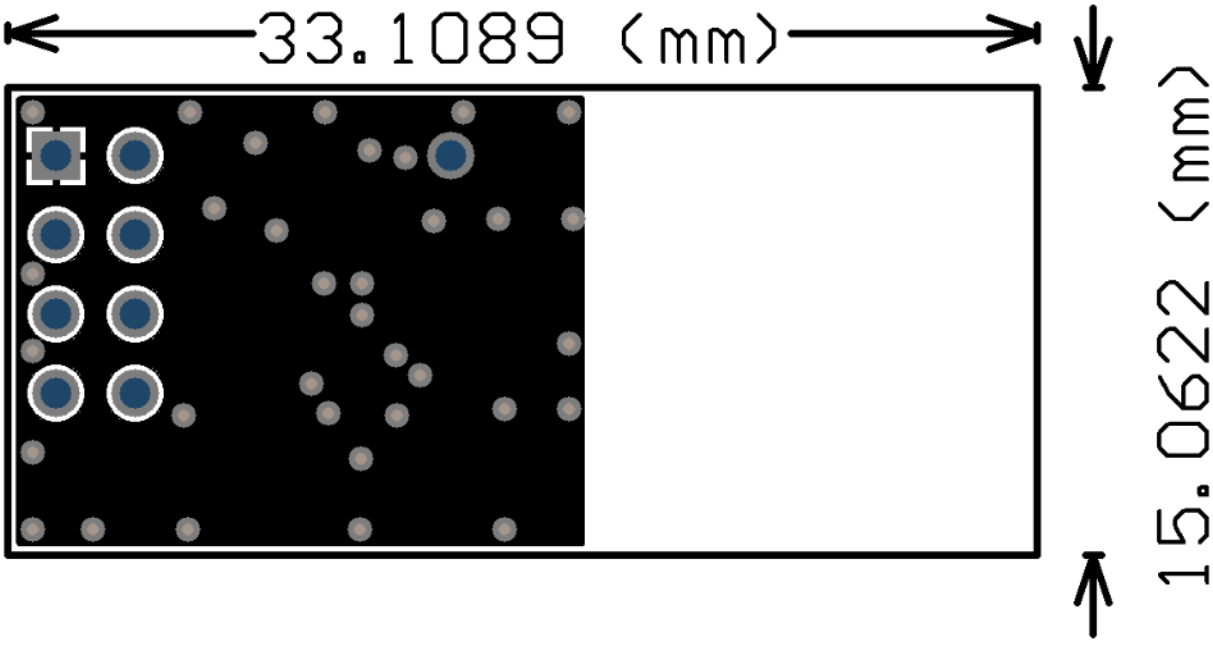


Figure 33. Bottom layer (nRF24L01 RF layout with single ended connection to PCB antenna and 0402 size passive components

The nest figure (Figure 34. on page 72, Figure 35. on page 72 and Figure 36. on page 73) is for the SMA output to have a board for direct measurements at a 50Ω SMA connector.

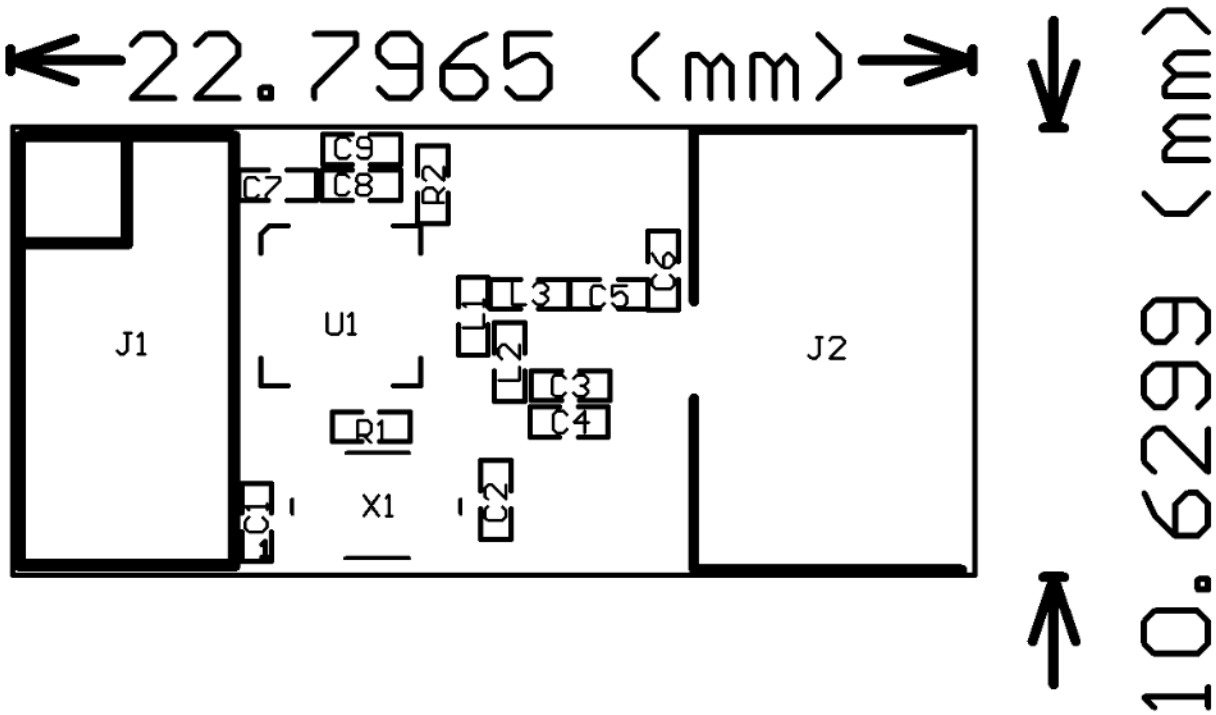


Figure 34. Top Overlay (Module with OFM crystal and SMA connector)

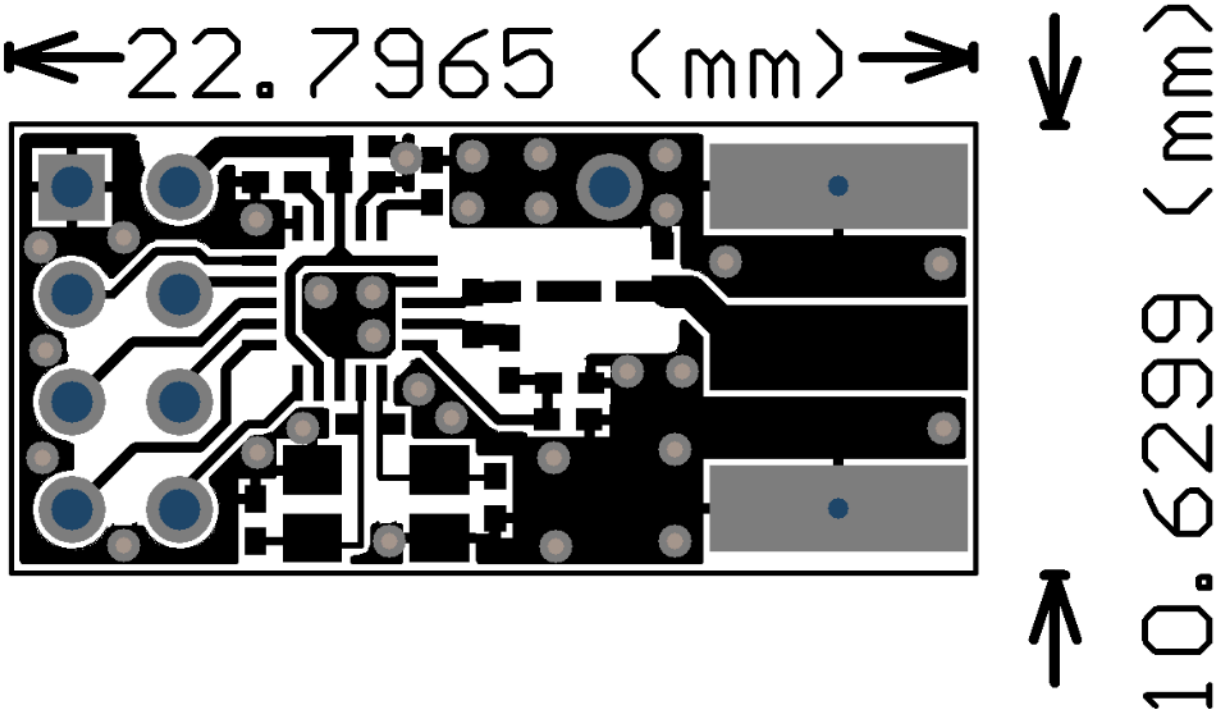


Figure 35. Top Layer (Module with OFM crystal and SMA connector)

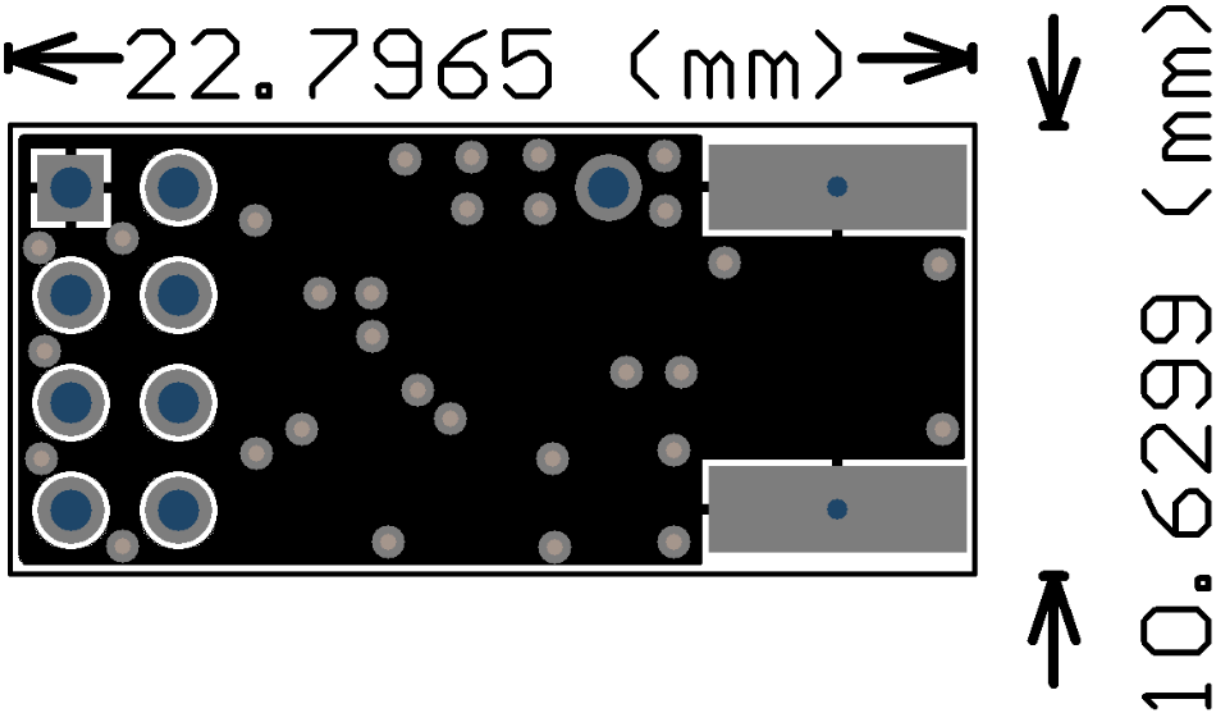


Figure 36. Bottom Layer (Module with OFM crystal and SMA connector)

Appendix E - Stationary disturbance detection

In Enhanced ShockBurst™ it is recommended to use the Carrier Detect functionality only when the PTX device does not succeed to get packets through, as indicated by the `MAX_RT` IRQ for single packets and by the packet loss counter (`PLOS_CNT`) if several packets are lost. If the `PLOS_CNT` in the PTX device indicates a high rate of packet losses, the device can be configured to a PRX device for a short time (T_{stbt2a} + `CD`-filter delay = 130µs+128µs = 258µs) to check `CD`. If `CD` was high (jam situation), the frequency channel should be changed. If `CD` was low (out of range or jammed by broadband signals like WLAN), it may continue on the same frequency channel, but you must perform other adjustments (a dummy write to the `RF_CH` clears the `PLOS_CNT`).