JANAK SHARDA

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Ph.D. Student, Electrical and Computer Engineering

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EDUCATION

Year	Degree/Exam	Institute	CGPA
2021-Now	**Ph.D., Electrical Engineering**	**Georgia Institute of Technology, Atlanta**	**3.54/4**
2017-2021	B.Tech, Electrical Engineering	Indian Institute of Technology, Delhi	9.034/10

PUBLICATIONS

[1] J. Sharda*, W. Li*, *et. al.*, IEEE TCAS-I, 2023. [2] J. Sharda, *et. al.*, IEEE EDTM, 2023. [3] W. Li, *et. al.*, IEEE AICAS, 2022. [4] J. Sharda, *et. al.*, IEEE ISCAS, 2021. [5] V. Desai, *et. al.*, IOP Science NCE, 2022. [6] J. Sharda, *et. al.*, ACM ICONS, 2020. [7] D. Kaushik, *et. al.*, IOP Science Nanotechnology, 2020. [8] N. Dey*, J. Sharda* *et. al.*, IEEE BioCAS, 2019.   *these authors equally contributed in the paper

EXPERIENCE

Graduate Research Assistant(Jan'21-Now):   Prof. Shimeng Yu, Dept. of ECE, Georgia Tech
- Designed **Thermal-aware 3D stacked CMOS Image Sensor** for multi-object tracking for **autonomous driving**.
- Explored 2.5D/3D integration of CIS and accelerator for accurate inference of Resnet-50 based QDTrack network.
- Designed **heterogenous 3D integration** of photodiodes with **IWO-FETs** based buffer memory and near-pixel compute circuits using **Cu-Cu hybrid bonding** and obtained **global shutter** operation of CIS.
- Simulated different components and obtained **45.8 TOPS/W** energy efficiency and **0.12 TOPS/mm^2** area efficiency.
- Modelled complete system in **ANSYS mechanical** for thermal simulations to obtain the peak temperature.

Graduate Teaching Assistant(Sep'21-Dec'21):   Prof. Nivedita Bhattacharya, Dept. of ECE, Georgia Tech
- Teaching Assistant for a course on VLSI Design(ECE3150), responsible for grading and conducting office hours.

PROJECTS

B.Tech Thesis: Compute-in-Memory based Hardware Accelerator using Transistors and Spintronics (Feb'19-May'21):   Prof. D. Bhowmik, Dept. of EE, IIT Delhi
- Implemented hardware accelerators for CNNs using **transistors** and **spintronics** based analog crossbars.
- Designed seperate crossbars for MSBs and LSBs, to efficiently implement and got **70% accuracy** on CIFAR10 dataset.
- Devised a thresholding scheme and synapse cell based on MOSFETs for Analog crossbar based deep neural networks.
- Improved speed, area, power, decay rate and done mismatch analysis of volatile synapses, trained it on MNIST.
- Designed transistor based circuit for Spintronic based Non-Volatile Synapse Cell and tested it on MNIST Dataset.
- Recieved **Best Thesis Award** and **Summer Undergraduate Research Award** in EE Department, IIT Delhi.

Other Projects:
- Designed a **12-bit pipelined SAR ADC** using an 8-bit and 5-bit SAR ADC in the first and second stage respectively. Designed various components like high-gain cascode OTA, SAR logic, DAC with power consumption of **1mW**.
- **Fabricating and characterizing an IC** consisting of individual MOSFETs, inverters, resistors and ring oscillators.
- **UNet based Image segmentation** of X-Ray images of Vertebral Column and obtained 0.7 Dice Score.
- Implemented a **5-stage pipeline processor** for SimpleRisc Assembly language instructions with forwarding.

TECHNICAL SKILLS

Computer Languages C/C++, Python, MATLAB, Java, Assembly Language(SimpleRisc), Verilog HDL
Software & Tools   Cadence Virtuoso, Cadence Allegro, Ansys Mechanical APDL, Ansys HFSS, SUPREM

RELEVANT COURSES

Electrical: Microelectronic System Packaging(ECE6776), Analog Integrated System Design(ECE6414), Memory Devices and Technology(ECE8803), Advance Machine Learning(ELL888), Advanced VLSI systems(ECE6130)
Computer Science: Data Structures and Algorithms(COL106), Systems in Machine Learning(CS8803)
Mathematics: Math. Foundations for Machine Learning(ECE7750), Probability and Stochastic Processes(MTL106)
Laboratories: IC Fabrication Lab(ECE4452)