JANAK SHARDA

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EDUCATION

Year	Degree/Exam	Institute	CGPA
2021-Now	Ph.D., Electrical Engineering	Georgia Institute of Technology, Atlanta	3.54/4
2017-2021	B.Tech, Electrical Engineering	Indian Institute of Technology, Delhi	9.034/10

PUBLICATIONS

- J. Sharda*, W. Li* et. al., Temporal Frame Filtering for Autonomous Driving Using 3D-Stacked Global Shutter CIS With IWO Buffer Memory and Near-Pixel Compute, IEEE TCAS-I, 2023.
- J. Sharda et. al., Thermal Modeling of 2.5D Integrated Package of CMOS Image Sensor and FPGA for Autonomous Driving, IEEE EDTM, 2023.
- W. Li, et. al., Temporal Frame Filtering with Near-Pixel Compute for Autonomous Driving, IEEE AICAS, 2022.
- J. Sharda, et. al., A Crossbar Array of Analog-Digital-Hybrid Volatile Memory Synapse Cells for Energy-Efficient On-Chip Learning, IEEE ISCAS, 2021.
- V. Desai, et. al., On-chip learning of a domain-wall-synapse crossbar-array-based convolutional neural network, IOP Science Neuromorphic Computing and Engineering, 2022.
- D. Kaushik, et. al. Synapse cell optimization and back-propagation algorithm implementation in a domain wall synapse based crossbar Neural Network for scalable on-chip learning, IOP Science Nanotechnology, 2020.
- N. Dey*, J. Sharda* et. al., On-chip Learning In A Conventional Silicon MOSFET Based Analog Hardware Neural Network, IEEE Biomedical Circuits and Systems, 2019.

*these authors equally contributed in the paper

EXPERIENCE

Graduate Research Assistant(Jan'21-Now):

Prof. Shimeng Yu, Dept. of ECE, Georgia Tech

- · Designed Thermal-aware 3D stacked CMOS Image Sensor for multi-object tracking for autonomous driving.
- · Explored 2.5D/3D integration of CIS and accelerator for accurate inference of Resnet-50 based QDTrack network.
- · Designed **heterogenous 3D integration** of photodiodes with **IWO-FETs** based buffer memory and near-pixel compute circuits using **Cu-Cu hybrid bonding** and obtained **global shutter** operation of CIS.
- · Simulated different components and obtained 45.8 TOPS/W energy efficiency and 0.12 TOPS/mm² area efficiency.
- · Modelled complete system in ANSYS mechanical for thermal simulations to obtain the peak temperature.

Graduate Teaching Assistant(Sep'21-Dec'21): Prof. Nivedita Bhattacharya, Dept. of ECE, Georgia Tech

· Teaching Assistant for a course on VLSI Design(ECE3150), responsible for grading and handling project doubts.

ACADEMIC ACHIEVEMENTS

- · Awarded Best Bachelor's thesis award in Electrical Engineering Department, IIT Delhi.
- · Awarded Summer Undergraduate Research Award for the work done under Prof. Debanjan Bhowmik.

- · Won IIT Delhi Semester Merit Award in both 1st and 2nd semester 2017-18 (given to top 7% of all the students).
- · Secured an All India Rank 410 in Joint Entrance Exam Advanced 2017 among 200 thousand candidates.
- · Qualified KVPY exam, by Indian Institute of Science, Bangalore by securing an All India Rank 126.
- · Ranked in top 0.01% among 2 million candidates appearing in JEE mains 2017.
- · Ranked in top 1% in India in NSEC 2017 (National Standard Examination in Chemistry) and NSEP 2017 (National Standard Examination in Physics).

PROJECTS

In-Memory Computation based Hardware Accelerator using Transistors and Spintronics(Feb'19-May'21): Prof. D. Bhowmik, Dept. of EE, IIT Delhi

- · Implemented hardware accelerators for CNNs using **transistors** and **spintronics** synapse based analog crossbars.
- · Designed seperate crossbars for MSBs and LSBs, to efficiently implement and got 70% accuracy on CIFAR10 dataset.
- $\cdot \ \, \text{Devised a thresholding scheme and synapse cell based on MOSFETs for Analog crossbar based deep neural networks}.$
- · Improved speed, area, power, decay rate and done mismatch analysis of volatile synapses, trained it on MNIST.
- · Designed transistor based circuit for Spintronic based Non-Volatile Synapse Cell and tested it on MNIST Dataset.

12-bit Pipelined SAR ADC(Jan'22-Apr'22):

Prof. S. Li, Dept. of ECE, Georgia Tech

- · Designed a 12-bit pipelined SAR ADC using an 8-bit SAR ADC in the first stage and 5-bit SAR ADC in second stage.
- · Designed various components like high-gain cascode OTA, SAR logic, DAC and obtained power consumption of 1mW.

Fabricating an IC in Cleanroom(May'22-Aug'22):

Prof. A. Frazier, Dept. of ECE, Georgia Tech

- · Fabricating and characterizing an IC consisting of individual MOSFETs, inverters, resistors and ring oscillators .
- · Cleanroom experience of various processes such as photolithography, diffusion, oxidation, etching, metallization etc...

Characterization of Railway Track Vibration(Sept'18-Jan'19): Prof. S.D.Joshi, Dept. of EE, IIT Delhi

- · Designed and employed a sensor capable of collecting **real time data** of track vibrations for normal running of train.
- · Characterized different types of vibrations for different track conditions using standard signal processing like autocorrelation, power spectral density and machine learning techniques like Neural Network, SVM etc.

Detecting damages in vertebral column(Jan'20-Mar'20): Prof. A.P. Prathosh, Dept. of EE, IIT Delhi

- · UNet based Image segmentation of X-Ray images of different regions of Vertebral Column and obtained 0.7 Dice Score.
- · Trained a squeezenet based classifier and classified X-Ray images as damaged or normal with validation score of 72%.

SimpleRisc processor with 5 stage pipeline(Sep'19-Nov'19): Prof. Smruti R.Sarangi, Dept. of CS, IIT Delhi

- · Implemented a 5-stage pipeline processor for SimpleRisc Assembly language instructions.
- · Implemented forwarding, data locks and branch locks to check for control and data hazards.

Small Search Engine (Sept'18-Oct'18):

Prof. Amitabha Bagchi, Dept. of CS, IIT Delhi

- · Implemented Search Engine using **Inverted Indexing** for a set of webpages using **Hash Table**.
- · Devised connector words skipping mechanism for faster search.

RELEVANT COURSES

Electrical: Microelectronic System Packaging(ECE6776), Analog Integrated System Design(ECE6414), Memory Devices and Technology(ECE8803), Advance Machine Learning(ELL888), Advanced VLSI systems(ECE6130)

Computer Science: Data Structures and Algorithms(COL106), Systems in Machine Learning(CS8803)

 $\textbf{Mathematics:} \ \ \text{Math.} \ \ \text{Foundations for Machine Learning} (ECE7750), \ Probability \ and \ Stochastic \ Processes (MTL106)$

Laboratories: IC Fabrication Lab(ECE4452)

TECHNICAL SKILLS

Computer Languages C/C++, Python, MATLAB, JAVA, Assembly Language(SimpleRisc), Verilog HDL Software & Tools Cadence Virtuoso, Cadence Allegro, Ansys Mechanical APDL, Ansys HFSS, SUPREM