Level-Crossing ADCs and Their Applications in Biomedical Readout Systems

Yongjia LI

Level-Crossing ADCs and Their Applications in Biomedical Readout Systems

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Yongjia LI

Master of Science in Electrical Engineering, Southeast University, China
geboren te Sichuan, China

This dissertation has been approved by the:
Promotor: Prof.dr.ir. W.A. Serdijn
Promotor: Prof.dr. E. Charbon

Composition of the doctoral committee:

Rector Magnificus,	voorzitter
Prof.dr.ir. W.A. Serdijn,	Technische Universiteit Delft, promotor
Prof.dr. E. Charbon,	Technische Universiteit Delft, promotor
Independent members:	
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Printed in the Netherlands.

To my family

Contents

Chapter 1

Introduction

Wearable and implantable medical devices with signal acquisition and wireless transmission are nowadays drawing more and more attention from medical and consumer electronics industries. In such systems, the signal acquisition front-end plays a key role in the definition of signal fidelity, transmitted data size and power consumption. Conventional readout interfaces, utilizing uniform sampling, constantly generate samples and consume power during data transmission regardless of the acquired sparse biomedical signals. To decrease the data size and power consumption of the transmitter from the sensor side, data compression and non-uniform sampling have been applied [1-13]. Level-crossing sampling is an attractive solution among these options as samples are generated only when the input signal crosses predefined threshold levels. In other words, there is no sampling if the input signal remains constant, reducing data size and power consumption [1-4].

Data acquisition chains are indispensable blocks in wireless wearable and implantable biomedical systems, in which analog-to-digital converters (ADCs) play an important role. Therefore, this thesis mainly focuses on the design and realization of level-crossing (LC) sampling based ADCs and biomedical data acquisition interfaces that are dedicated to energy-constrained applications. This work aims to develop proof-of-concept

circuits and systems for level-crossing sampling based biomedical read-out systems.

In this chapter, the background knowledge on level-crossing sampling is introduced and the design challenges and motivation are described. At the end of this chapter, the highlights and structure of the thesis are listed.

1.1 Background

As is commonly known, conventional uniform-sampling based analog-to-digital converters quantize the signal at a constant rate. However, as is shown in Fig. 1.1, contrary to uniform sampling (Fig. 1.1 (b)), in level-crossing sampling (Fig. 1.1 (a)), samples are generated only when the input signal crosses the threshold levels, while the time in between two consecutive samples is measured by a timer. The conversion results of a LC-ADC are thus composed of digital codes for the voltage magnitude and the time intervals. It is even possible to process the non-uniform samples by a continuous-time DSP without a synchronous clock to record the time interval [1].

For level-crossing ADCs, under the condition that the timer frequency is much higher than the signal frequency and the quantization levels are without any error, ideally, we expect a resolution of [2, 3]

$$SNR = 20logOSR - 11.2, \tag{1.1}$$

in which SNR is the signal-to-noise ratio and OSR is the clock over-sampling ratio (i.e. the ratio of the timer frequency to the input signal frequency), respectively. Unlike level-crossing sampling, SNR of uniform sampling is expressed as a function of the number of bits n in the amplitude domain

$$SNR = 6.02 * n + 1.76. \tag{1.2}$$

Note that the number of quantization levels in amplitude determines the SNR in uniform sampling systems while the OSR in time defines the

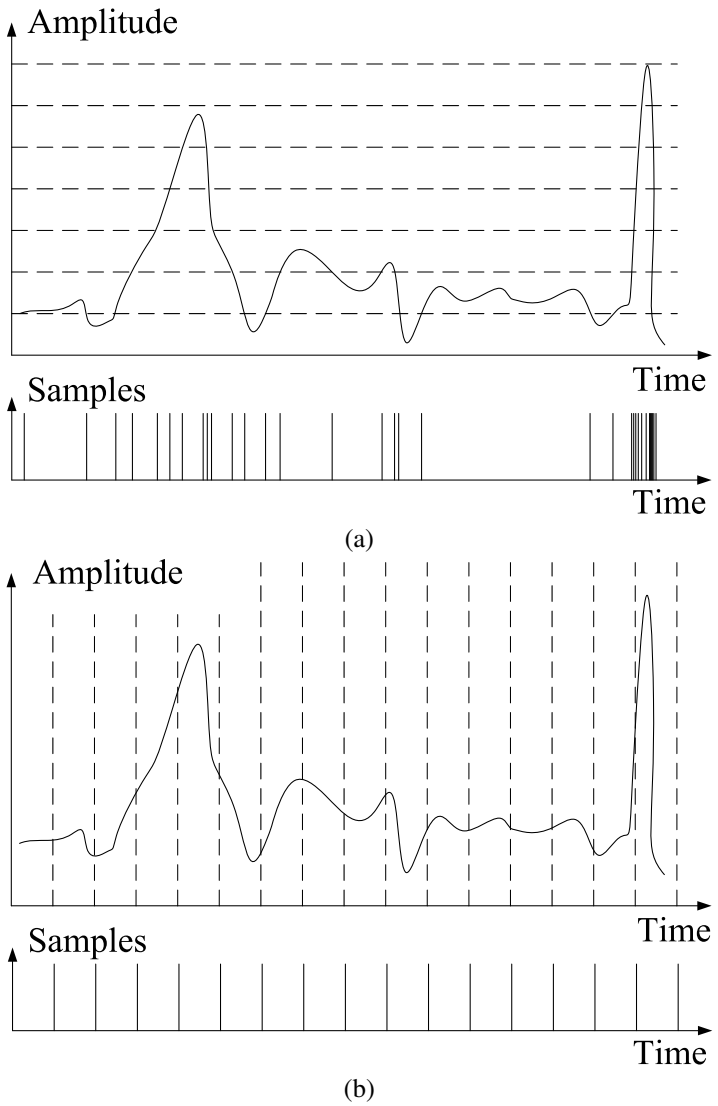


Figure 1.1: (a) LC sampling (b) Uniform sampling

SNR in LC sampling systems. Detailed analysis of how the time and the amplitude resolution affect the resolution of LC-ADCs can be found in [1-5]. Indeed, it was shown in some previous works [1-5, 16, 19] that with lower resolution in amplitude, LC-ADCs can still exceed the related theoretical limit defined in (1.2). In other words, in order to obtain n-bit resolution in LC-ADCs, it is not necessary to set the number of quantization levels as 2^n. It can be 2^{n-1} or even lower as long as the OSR of the timer can meet the resolution requirement.

Since LC sampling and uniform sampling are different sampling mechanisms, it is worthwhile to compare the generated number of samples for

both of them with the same resolution for the same input signal. Simulations and calculations of different signals in MATLAB were conducted as follows. Typical biomedical signals, i.e. ECG, EEG, ECoG and EMG, were chosen for the simulations in MATLAB [4]. The original transient signals were normalized in the range from 0 to 1 V for the sake of clarity.

As the original signals were sampled at particular frequencies (the ECG, EEG, EMG, and ECoG were sampled at 1kHz, 2.048kHz, 4kHz and 1kHz, respectively) and thus were not suitable for LC sampling, linear interpolation is used to add more samples to the original signals. Their OSR was set to 1000 to reach the targeted 8-bit overall resolution in this work, so the size of the input signal after interpolation was 1000 times the original one.

In a uniform-sampling system, samples are constantly generated. By multiplying the original sampling frequency and sampling duration we obtain the number of samples. For LC-ADCs, we set the amplitude resolution from 3 to 8 bits to do the comparison with uniform-sampling ADCs.

The normalized original transient input signals and the number of samples for comparison are depicted in Fig. 1.2. "US" represents uniform sampling; "LC" means level-crossing sampling. As can be seen from Fig. 1.2, US and LC sampling reveal two different trends for the generated number of samples when the resolution varies from 3 to 8 bits. As expected, US remains constant for all input signals and all resolutions while LC sampling shows an exponentially rising trend. For the various ExG signals the results are slightly different. Basically, the sparser the signal is, the more the LC-ADC can benefit from that. Furthermore, the number of samples goes up exponentially when the resolution in LC sampling increases. For 8-bit resolution applications, if the amplitude resolution of LC-ADCs is 8 bits, more samples than for US-ADCs are expected according to the bars in the bottom four graphs. Generally, fewer samples are acquired for LC sampling than for uniform sampling for amplitude resolutions lower than 6 bits.

The above discussion is based on a comparison of the numbers of the samples. If we further include the number of bits, level-crossing sampling will show a greater potential as the output of the uniform sampling is

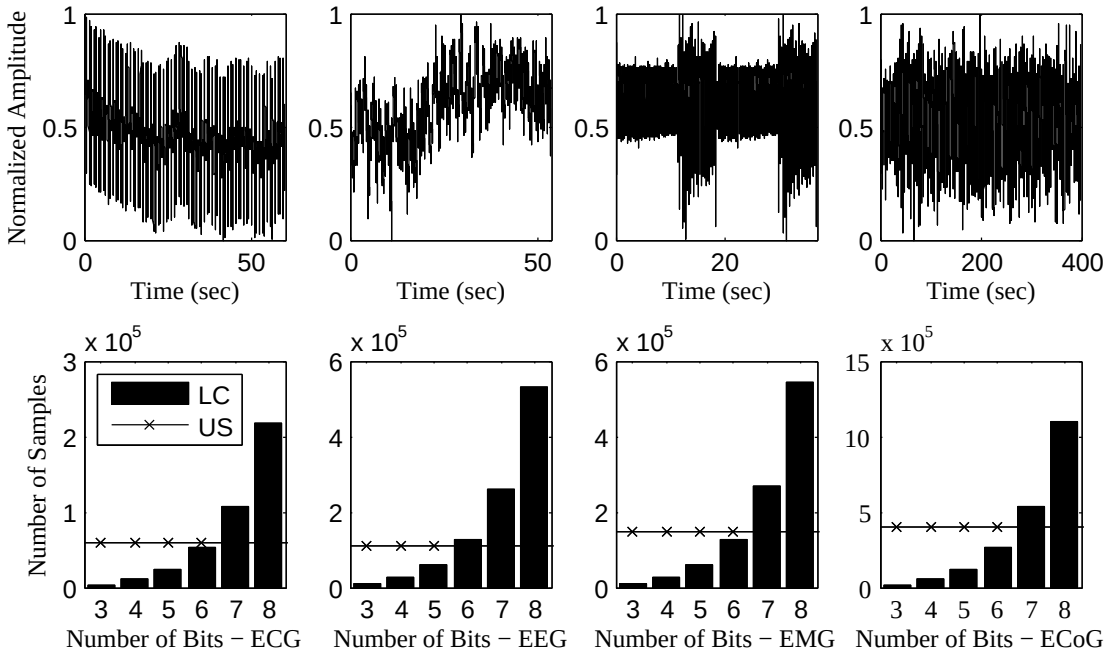


Figure 1.2: The normalized input transient signal and the corresponding number of samples for comparison: ECG, EEG, EMG and ECoG. The amplitude of the original signals were normalized for clarity. The number of bits denotes the accuracy in the amplitude domain. "US" denotes uniform sampling while "LC" represents level-crossing sampling.

represented by multiple bits while level-crossing sampling only needs two bits (up or down). A similar discussion can be found in [5].

1.2 Challenges and Motivation

There is a growing demand to integrate wearable health monitoring systems into telemedicine systems, which makes early detection of abnormal conditions from patients possible [6, 7]. A simplified system diagram of a typical wireless data acquisition system is shown in Fig. 1.3. AFE denotes the analog front-end and TX denotes the transmitter. In such systems, the power consumed from the wireless transmission usually dominates and is proportional to the overall data rate [6, 7]. Although state-of-the-art SAR-ADC already achieved a figure of merit (FoM) down to sub-fJ/conversion [8], the bottleneck of realizing a lower system power still relies on wireless transmission power and related data rate.

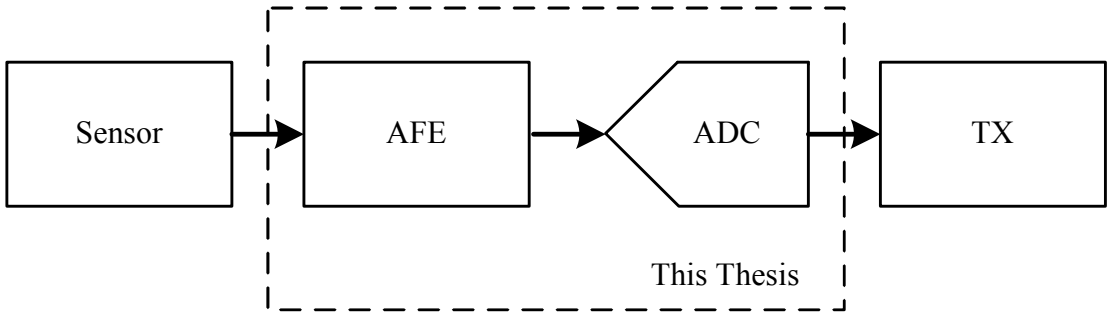


Figure 1.3: A simplified system diagram of a typical wireless data acquisition system.

To realize low-power wireless biomedical sensors, new concepts and IC implementations for biomedical signal readout front-ends are necessary. With the event-driven LC-ADC, data compression can be realized in the analog front-end. This potentially allows the power consumption of future systems to be lowered to a new level while offering the same or even better performance. Most of the previously reported works regarding level-crossing sampling are either theoretical analyses or standalone LC-ADC designs with relatively high-power consumption. As there are only a few fully integrated systems with level-crossing sampling for biomedical applications, this inspired us to design low-power LC-ADCs and an entire readout front-end and apply them to a wearable ECG autonomous wireless sensor [9].

1.3 Thesis Organization

There are five remaining chapters in this thesis, organized as follows.

Chapter 2 gives an overview and classification of previously reported LC-ADCs. Various circuits and techniques in LC-ADCs are discussed, including the window detecting method, feedback DACs and offset calibration. Furthermore, applications and integrations of LC-ADCs at system level are discussed.

Chapter 3 presents a low-power LC-ADC with a single-bit feedback DAC. The operation principle of the proposed offset injection mechanism and the single-bit DAC are discussed in detail. A single-ended asymmetrical

window-detector is proposed to further decrease the power consumption. Measurement results of the fabricated LC-ADC are given.

Chapter 4 presents the implementation of a low-power LC-ADC with a programmable window comparator. A differential asymmetrical window detecting method is described. A comparator with a deliberately introduced imbalance in the input pair is used. Measurement results are given, followed by a performance comparison with other LC-ADCs.

Chapter 5 explores the system integration of a current-mode LC-ADC in a readout front-end and its application in ECG recording. The front-end includes a low-noise amplifier (LNA), a programmable voltage-to-current converter (PVCC), a 7-bit level-crossing ADC with 4-bit calibrating DACs and an RC oscillator to generate the required calibrating clock. Measurement results are shown at the end of the chapter. The proposed system is also very suitable for other biomedical applications where the input signals are sparse.

Chapter 6 concludes the thesis and gives recommendations for future work.

Chapter 2

Level-Crossing ADCs: An Overview

The background, challenge and motivation of the thesis have been discussed in the previous chapter. To obtain a comprehensive understanding of LC-ADCs, this chapter gives an overview and classification of all previously reported LC-ADCs. Window detecting methods, feedback DACs and offset calibration from the block level of LC-ADCs are investigated. Discussions on system integration and applications are presented as well.

2.1 Introduction

The proof-of-concept circuit of a level-crossing (or delta modulation) ADC was originally introduced in 1966 [10]. Conceptually, the working principle of LC-ADCs is similar to that of flash ADCs. However, there are some differences between them. One major difference is that LC-ADCs work with closed-loop feedback while a flash ADC does not. Further, there are only two continuous-time comparators with asynchronous logic circuits in LC-ADCs while there are 2^n-1 comparators with synchronous logic circuits for an n-bit flash ADC. There are loop delays for either input signals or reference levels to be refreshed in the feedback loops of LC-ADCs, but flash ADCs do not have such loop delay as they work in open loop.

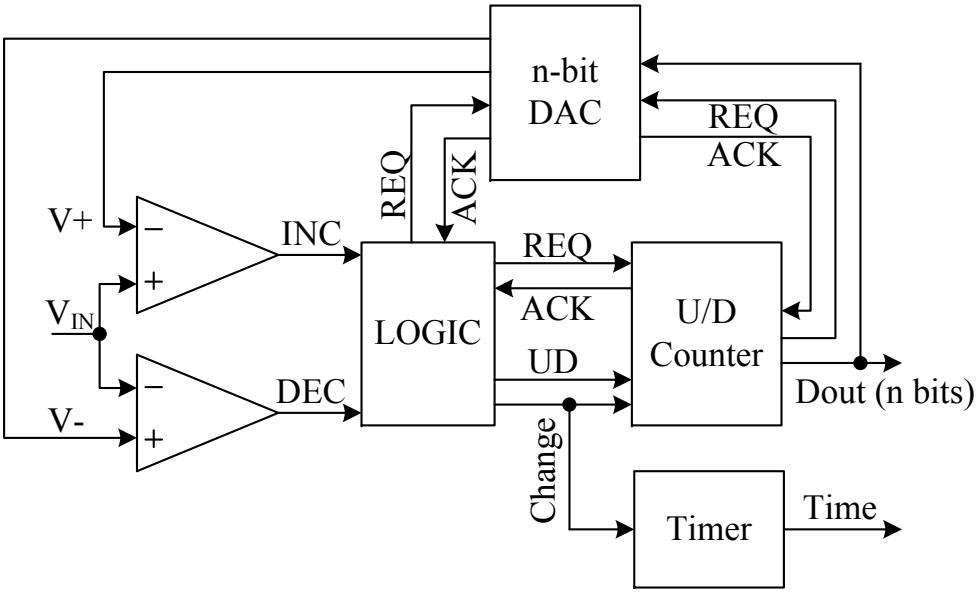


Figure 2.1: Block diagram of a typical LC-ADC.

From the way the feedback loops work, LC-ADCs are similar to SAR-ADCs but with different search algorithms. The successive approximation register (SAR) ADC is the most popular type of ADC in biomedical data acquisition due to its power efficiency. Assuming both ADCs consume the same amount of power in their respective digital circuits, a LC-ADC is less power efficient than a SAR-ADC as there is one more comparator in a typical LC-ADC than there is in a SAR-ADC. However, LC-ADCs do have some advantages over SAR-ADCs: the digital output code is continuously available for feature extraction [11, 12], and less samples are generated for sparse biomedical signals.

The block diagram of a conventional LC-ADC is shown in Fig. 2.1. The comparators operate in the continuous-time domain. The feedback loop forces the comparison window to stay around V_{IN}. The up/down counter functions as the digital integrator and the time in between two samples is recorded by the timer. Whenever V_{IN} crosses the upper level or the lower level, the output of the comparators toggles and the control logic in the next stage starts to update the up/down counter to refresh the comparison window. Such an ADC operates continuously thanks to a handshake protocol. The detailed operation of the conventional LC-ADC was summarized in [1, 2, 13].

Although LC-ADCs are still in the research phase, some LC-ADCs al-

ready have been realized in silicon. For a better understanding and to allow for better system integration of LC-ADCs, the previously reported LC-ADCs will be discussed and summarized in the following sections.

2.2 Window Detection in LC-ADCs

Reference levels are critical to quantize the input analog signal. A window with one or two reference levels that follow the input signal is able to implement the level-crossing algorithm. The static inaccuracy of comparison windows results in differential nonlinearity (DNL) while the settling inaccuracy of comparison windows leads to dynamic errors. The static and dynamic inaccuracy of the window can stem from non-idealities of either DACs or comparators or both. There are various window detection methods for level-crossing detections. Each has its own advantages and disadvantages. We classify them into two categories: 1) whether the windows operate with a clock or without a clock; 2) whether the windows are floating or fixed. These two categories will be discussed in the following subsections.

2.2.1 Clocked and Clockless Window

For a continuous-time system without any clock, there are an upper level and a lower level composing the comparison window in LC-ADCs as discussed above. So the clockless window detector needs two continuous-time (CT) comparators for level-crossing detection. It thus consumes static power. On the other hand, a clocked window (CW) works slightly different. As is shown in Fig. 2.2, a comparison "window" with a toggled reference level works in a clocked fashion. This is also the principle of a tracking ADC [14, 15]. In other words, as shown in 2.2(b), the reference level alternates by 1 LSB from just above the previous value to just below it with a certain frequency, and vice versa (depending on whether the input signal is above or below the reference level). Similar to the CT LC-ADC, the feedback loop here in the CW LC-ADC forces the DAC output to follow the analog input signal. But the LC-ADC with clocked window

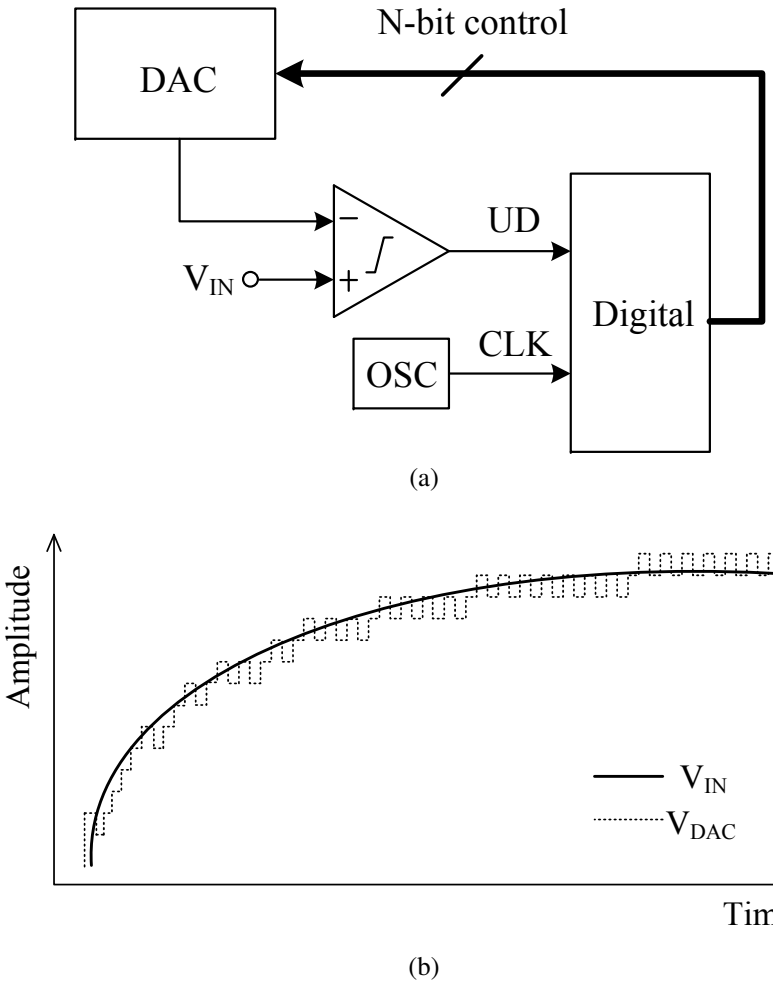


Figure 2.2: (a) LC-ADC with a clocked window detector. (b) Example waveform.

has the problem of a flickered output digital code as the reference level always toggles according to the clock frequency.

At block diagram level, LC-ADCs with clocked windows become SAR-ADCs if the up/down counter is replaced by the SAR logic. So CW LC-ADCs can be considered to be a result of a compromise between a CT LC-ADC and a SAR ADC. Dynamic comparators can be adopted in CW LC-ADCs. So CW LC-ADCs have lower power consumption and less design complexity than CT LC-ADCs. However, a certain over-sampling ratio need to be guaranteed in order to follow the input analog signal well, which may result in even more samples than that happen in a SAR-ADC. Furthermore, considering potential problems due to clock

feedthrough and charge injection, it is difficult for the dynamic comparator in a CW LC-ADC to accurately resolve the 1 LSB difference between the reference level and the input signal. So we focus our discussion on CT LC-ADCs in this thesis.

2.2.2 Floating and Fixed Window

During the data conversion of LC-ADCs, the comparison window can be following the input signal or be fixed, resulting in so-called floating-window detection and fixed-window detection, respectively. They are analyzed in the following two subsections.

2.2.2.1 Floating-Window Detection

An LC-ADC with floating-window detection and its example waveform are shown in Fig. 2.3. It works as follows: as long as the input signal is between the two levels (V_H, V_L), the outputs of both comparators are low and no sample is generated. When the input signal moves outside this range, one of the comparators will detect the level crossing, outputs a logic "1" on INC (increment) or DEC (decrement) and a conversion is triggered. The following digital control logic generates corresponding signals to control the DAC to update the comparison window, which is fed back to the inputs of the comparators. The input signal is then between the refreshed two levels again. Since the comparison window floats up or down according to the movement of the input signal, we call it floating-window detection.

Floating-window detection requires comparators to have a large operating common-mode range to accommodate the input signal range. Worst case of a rail-to-rail input in the design of comparators should be considered. Such a feature requires the design of power hungry comparators (20 μW per comparator in [1]), which is not practical in a large variety of biomedical applications. Furthermore, the offset voltages of comparators at various common-mode levels are most likely different. Hence, from these different offset voltages distortion results. Since the purpose of this thesis is to design LC-ADCs that can be applied in biomedical readout

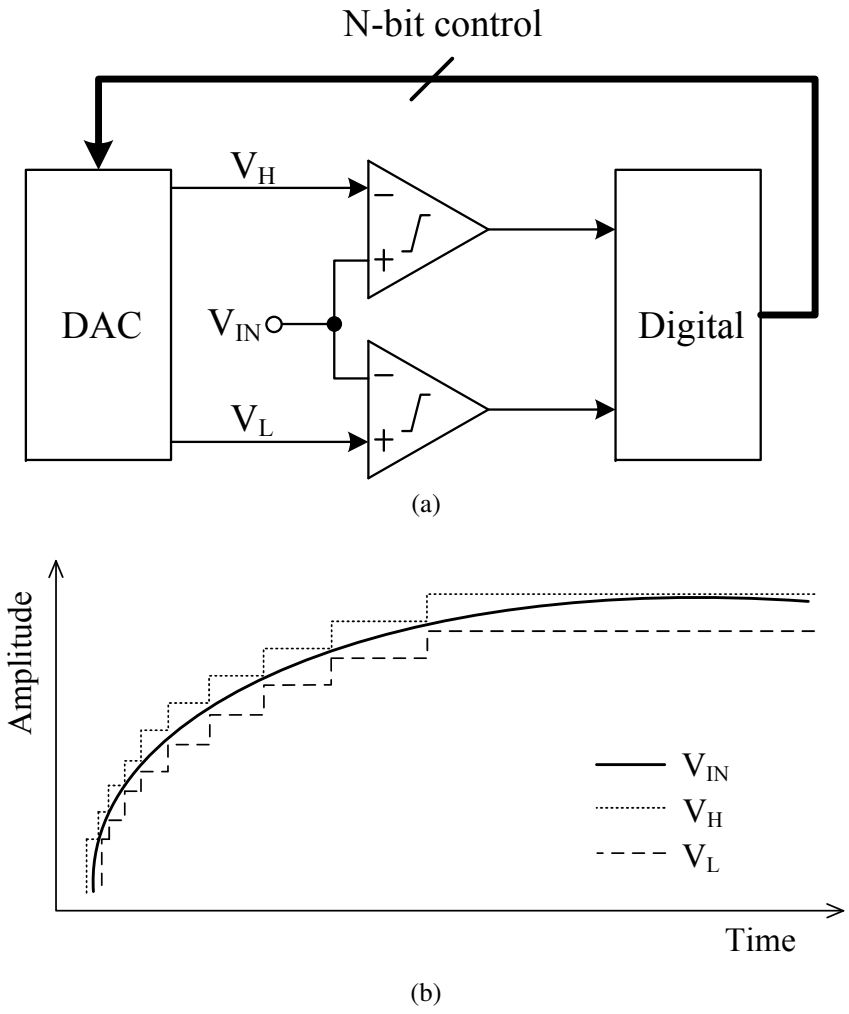


Figure 2.3: (a) LC-ADC with a floating-window detector. (b) Example waveform.

systems, the floating window structure may not be applicable due to its large power consumption.

2.2.2.2 Fixed-Window Detection

Instead of refreshing the comparison window to move up and down to track the input signal, the fixed-window detection fixes the comparison window and injects a corresponding offset to the input signal. An LC-ADC with fixed-window detection is shown in Fig. 2.4. The comparison window is fixed at reference levels (V_H, V_L). The input signal V_{IN} and the

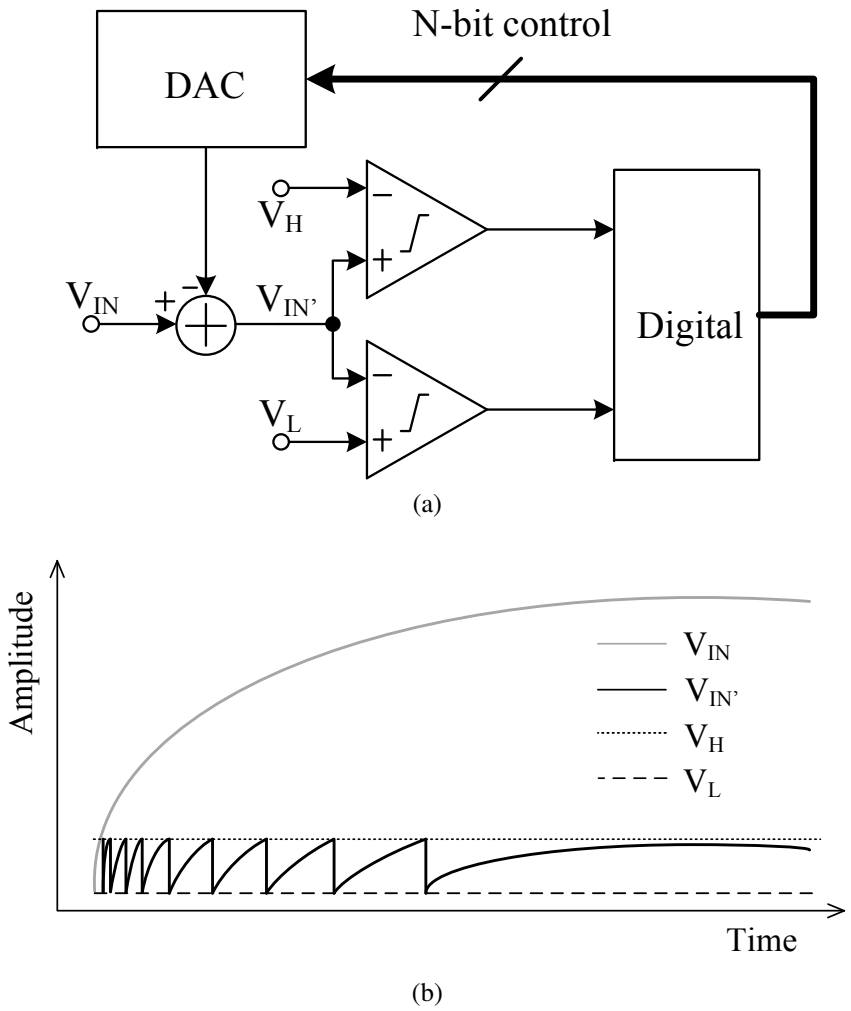


Figure 2.4: (a) LC-ADC with a fixed-window detector. (b) Example waveform.

output of the feedback DAC are summed at the subtractor and the residue voltage (or charge, or current) $V_{IN'}$ is then fed to the input of the comparators. As we can see from the example waveform (Fig. 2.4(b)), the comparator common-mode range is reduced dramatically, and optimization of the comparators targeting at a specific reference level can be done. The related effects that result from comparator offset and distortion are thus reduced. More importantly, similar performance is achievable for the comparators with lower power consumption.

The subtraction prior to window comparison makes the difference between the floating-window detection and fixed-window detection. As the fixed-window detection shows higher power efficiency and less design

complexity, this thesis will be focusing on the fixed-window detection method. From now onwards, all the discussions assume that the two window comparators are exactly the same, but some interesting features of employing two comparators with different bandwidths and power consumption will be proposed and discussed in the next chapter.

2.3 Feedback DACs in LC-ADCs

Digital-to-analog converters are used in the feedback loop of LC-ADCs. They convert the output of the digital integrator (up/down counter) to analog reference levels to form a comparison window to compare with the input signals. Depending on the different requirements on power consumption, accuracy and bandwidth, different structures can be used in the feedback loop. They will be discussed in the following subsections.

2.3.1 Unary, Binary and Segmented DACs

From a structure point of view, there are unary (thermometer), binary and segmented DACs. They are different as they accomplish D/A conversion by dividing (or multiplying) the reference voltage (or current or charge) differently. An n-bit unary DAC divides the reference into 2^n equal values. It is inherently monotonic, simple for analog blocks and good for matching. However, there are 2^n-1 outputs from the digital encoder side, and thus its associated area and routing need to be considered. On the other hand, an n-bit binary weighted DAC divides the reference into n values using a dichotomous method. It does not need an encoder but monotonicity is an issue as the matching between the least-significant bit (LSB) and the most-significant bit (MSB) degrades for increasing resolution. Segmented DACs form a combination of both unary and binary DACs. Different designs can be optimized according to the trade-off among accuracy, area, power and complexity.

In level-crossing ADCs, monotonicity is a critical aspect as the DACs in LC-ADCs are required to increase (or decrease) the output by only 1 LSB for each level crossing. Unary DACs seem to be better in this case.

But since loop delay results in possible overloading of LC-ADCs, higher amplitude resolution requires shorter loop delay to avoid that. So the amplitude resolution of LC-ADCs is usually set between 4 bits and 8 bits. In this range, matching is not difficult to accomplish for any technology. Unary, binary and segmented DACs were indeed all adopted in previously reported works. We will discuss the details of previously reported LC-ADCs with various feedback DACs in the next subsection.

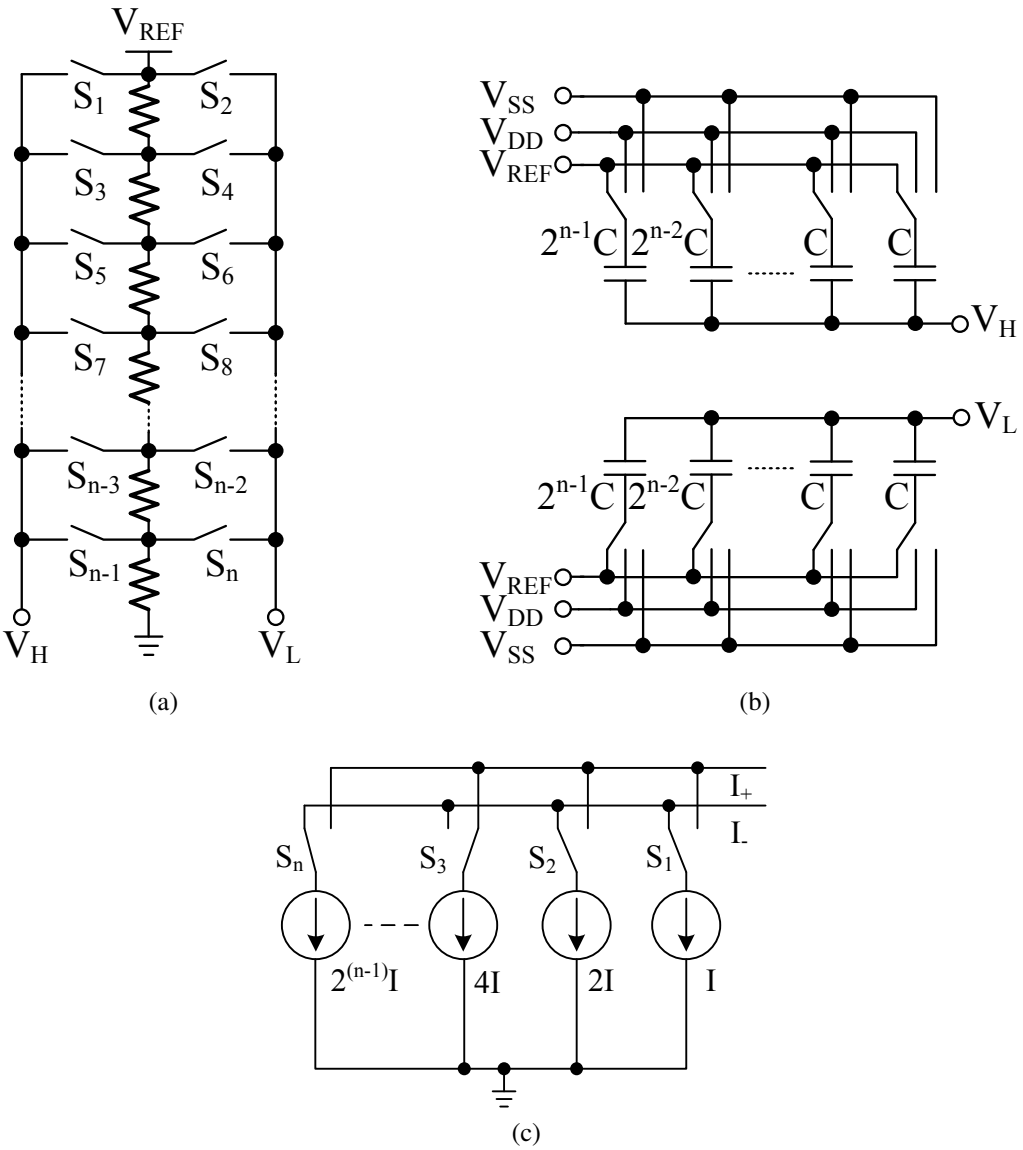


Figure 2.5: DACs that have been adopted in previously reported LC-ADCs: (a) a resistive unary DAC [1], (b) a capacitive binary DAC [16], (c) a current-steering binary DAC [13].

2.3.2 Resistive, Capacitive and Current-Steering DACs

Commonly, signals carry information in the voltage, charge and current domain. The same holds for the feedback DAC in the LC-ADC. Three typical DAC structures that have been used in previously reported LC-ADCs are shown in Fig. 2.5(a), Fig. 2.5(b) and Fig. 2.5(c), respectively. Needless to say, the resistive DAC in Fig. 2.5(a) is an unary DAC, which is simple and monotonic but consumes static power while its capacitive counterpart in Fig. 2.5(b) is a binary DAC, which is more power efficient but suffers from charge leakage. Similar to a capacitive DAC, the current-steering DAC in Fig. 2.5(c) can be either unary or binary or segmented. However, current-steering DACs do not suffer from leakage. Furthermore, current summation is compatible with fixed-window detection as the common-mode voltage of the summation node can be fixed by means of feedback [17].

From the discussion in Section 2.2, it is known that the fixed-window detection differs from its floating-window counterpart as fixed-window detection LC-ADCs perform a subtraction on the input signals before the window comparison. In the circuit realization of the subtractor and the DAC, a capacitive DAC array is a good candidate to combine both the tracking and subtracting function as charge sharing happens naturally on the capacitor. In other words, capacitive DACs have a built-in subtractor. So LC-ADCs with capacitive DACs are able to combine the fixed-window detection without additional power consumption. However, an extra block for the subtractor needs to be added to the resistive DAC in the voltage domain if fixed-window detection is aimed for. Despite leakage, it is still worth exploring further the charge-domain capacitive DAC because of its power efficiency. So far, current-steering DACs have not been adopted in previous works yet. Current-steering DACs consume static power but current summation at the output node is favourable for fixed-window detection. However, the entire signal chain need to be in the current domain or a voltage-to-current converter should be designed in front of the current-domain LC-ADC. We will show more interesting features of a current-domain LC-ADC in Chapter 5.

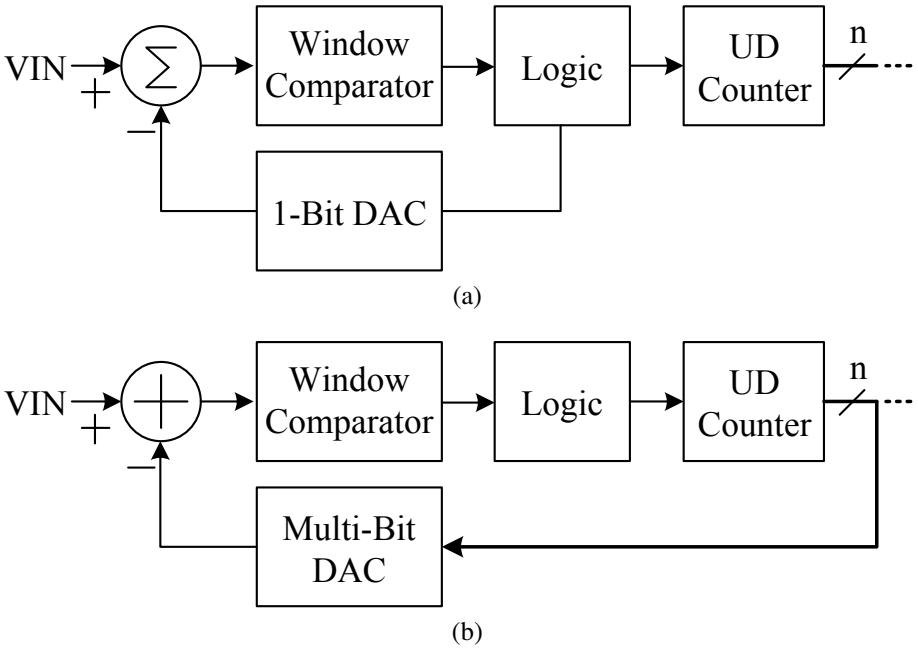


Figure 2.6: (a) A single-bit LC-ADC. (b) A multi-bit LC-ADC.

2.3.3 Multi-Bit and Single-Bit DACs

In the operation of standard LC-ADCs, the multi-bit DAC outputs change by only 1 LSB for each sample, and hence it is not very power-efficient to refresh the entire DAC array. Requirements on higher power efficiency inspired the idea of using 1-bit DACs [4, 18] that are similar to charge pumps. Basically, single-bit DACs subtract or add 1 LSB offset oppositely to the input signal movement when there is a level crossing. A single-bit LC-ADC and a multi-bit LC-ADC are shown in Fig. 2.6 (a) and (b), respectively. They differ in their UD counters configuration. The UD counter is in the feedback loop for the multi-bit LC-ADC while it is not for the single-bit LC-ADC. Note that the 1-bit DAC here is different from the 1-bit DAC in a sigma-delta ADC. The former one represents 1 LSB while the latter one stands for the full reference range.

The implementation of 1-bit feedback DACs reduces the power consumption of LC-ADCs further. However, just like charge pumps in phase-lock loops (PLL), the 1-bit DAC in the LC-ADC also suffers from asymmetry, leakage and so on. Since the current levels are accumulated from the previous levels in level-crossing ADC (also called delta modulation). So at each level-crossing point the single-bit DAC introduces a DC inaccu-

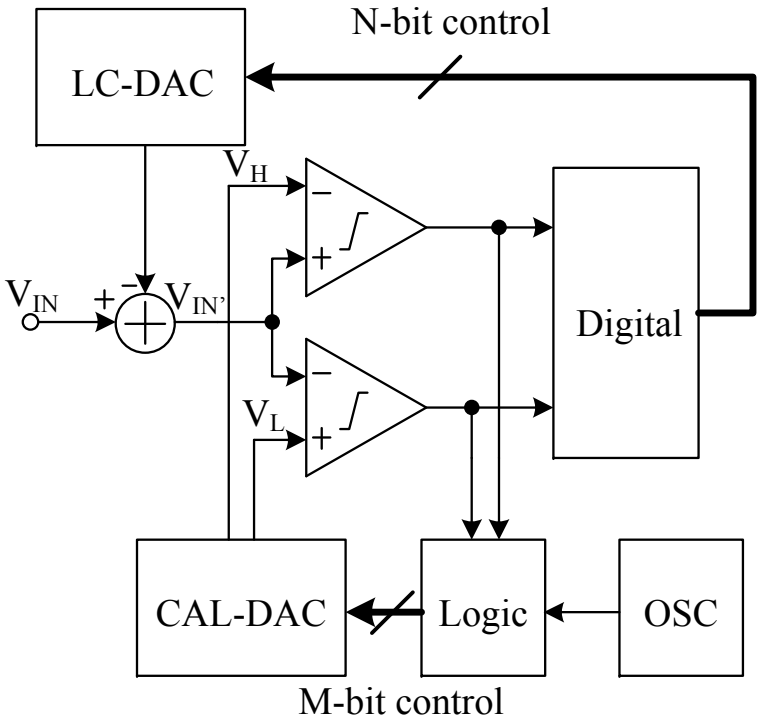


Figure 2.7: LC-ADC with on-chip offset calibration.

racy in the 1 LSB addition (or subtraction) of the input. Consequently, the inaccuracies are accumulated, resulting in a small drift (in the order of 1, 2 LSBs or even more) at the output after a certain number of cycles. The drift can be resolved by introducing either a pseudo resistor or a mixed-signal feedback loop [19].

Consequently, for the 1-bit LC-ADC, advantages include: 1) low-power operation; 2) design flexibility; 3) that the dynamic range is not limited by the power rail. Major disadvantage is offset accumulation. For the multi-bit LC-ADC, advantages include: 1) higher accuracy; 2) easy to achieve an adaptive resolution operation [2, 16]. The disadvantage is apparent: a higher power consumption.

2.4 Offset Calibration in LC-ADCs

Offset is unavoidable in comparators and is of major concern for improving the accuracy of LC-ADCs. Since comparators in LC-ADCs work

in the continuous-time domain, it is impossible to introduce autozeroing. In previous works, offset was compensated by either applying a compensating DC level at the input [1], or DACs to calibrate the offset [2, 16, 20]. A simplified diagram (from [16]) of an LC-ADC with an n-bit level-crossing DAC (LC-DAC) and an m-bit calibration DAC (CAL-DAC) in the feedback loop is shown in Fig. 2.7. Note that the LC-DAC and the CAL-DAC do not necessarily have the same resolution. The resolution of the CAL-DAC depends on the desired calibration accuracy. The calibration loop consists of comparators, an oscillator, control logic and the CAL-DAC. A successive approximation algorithm has been used in the control logic. During the calibration phase, the LC-DAC output is fixed to virtual ground and the calibration loop controls the m-bit digital signal to minimize the comparator offset. Note that the calibration loop and the LC feedback loop do not work simultaneously, as offset of the comparator needs to be compensated before the LC-ADC starts to work [16]. A level-crossing algorithm can also be applied in the calibrating loop. Since the calibration step of the level-crossing algorithm is only 1 LSB, the calibrating speed is lower than that of the SAR calibrating loop. However, this is not an issue as calibration happens only once and before the signal conversion starts [17].

2.5 System Integration of LC-ADCs

Although the research on level-crossing ADCs is relatively new, there are some systems that integrate a LC-ADC on chip. In [21], an LC-ADC based continuous-time digital signal processing (CT-DSP) algorithm was proposed and implemented as a controller in a DC-DC converter. The LC-ADC there detects the output voltage and converts any deviation from the analog representation into a digital control code. The advantage over a conventional DSP system is that any output voltage deviation can be instantaneously sensed by the LC-ADC without waiting for a clock signal. The control logic detects the deviation and outputs the control digital code to adjust the DC-DC converter [21]. On the other hand, the conventional clocked system samples and processes each sample even when there is little activity of the DC-DC output voltage. So another advantage of the LC-ADC based CT-DSP is that the processor is active only when

the input signal changes, resulting in less spikes from the power supply in steady state when the output voltage remains constant.

Another system application can be found in [1, 22], where the full system integrates ADC, DSP and DAC in one chip, targeting voice band or GHz range applications, respectively. These are highly integrated continuous-time systems that convert their analog input into a continuous-time digital representation, process the information digitally in a CT-DSP without the aid of a clock, and then convert the digital signal back to the analog domain by the CT-DAC. The systems potentially take advantage of both analog and digital signal processing. The digital signal processors are active only when there is signal activity, so the computation power is adaptive according to the signal variation. A similar work of a CT-DSP can also be found in [23]. Furthermore, since the entire signal chain processes the signal continuously without any clock, there is no aliasing in the signal band, resulting in higher in band signal-to-noise and distortion ratio (SNDR) when compared to conventional clocked systems.

Two unique advantages of LC-ADCs over other ADCs are that the output digital code is continuously available and the output digital code always follows the input within 1 LSB inaccuracy. This can be crucial in biomedical applications. For example, LC-ADCs play key roles in analog-to-information converters (AICs) [11, 12] for signal feature extraction. These AICs are indeed LC-ADCs combined with some digital blocks with certain feature-extraction algorithms to process the raw digital codes from the LC-ADCs. These AICs achieve high accuracy in QRS detection in ECG applications. Note that one major difference between the LC-ADCs in the AICs and the LC-ADCs in CT-DSP mentioned above is the time code. The duration between two samples is not coded in the CT-DSP while the time is coded in the AICs. In other words, the LC-ADCs in AICs also need to quantize time. But an obvious advantage is that then the LC-ADC is compatible with discrete-time DSPs.

2.6 Conclusions

In this chapter, previously reported LC-ADCs were reviewed and analyzed from different aspects. The system applications show very promis-

ing potential for LC-ADCs. Meanwhile, the performance of LC-ADCs at circuit level is not yet suitable for biomedical application due to a relatively high power consumption. For this reason, the fixed-window detection method will be chosen in this thesis due to its power efficiency. Furthermore, the associated capacitive and current-steering DACs will be explored in the following chapters. In the next chapter, a low-power LC-ADC based on offset injection in the charge domain is proposed and implemented to improve the power efficiency of LC-ADCs.

Chapter 3

Low-Power LC-ADC with 1-Bit DAC

Chapter 2 analyzed and classified the previously reported LC-ADCs. System integration aspects for different applications were discussed as well. As can be seen from the previous discussion, LC-ADCs hold the potential to compress the sampled data and save energy at the system level. However, the reported LC-ADCs still consume too much power when compared to their discrete-time counterparts (e.g. SAR ADC). Since LC-ADCs are signal specific ADCs, this chapter will first analyze signal movement and its influence on the power consumption of LC-ADCs. An offset injection mechanism for the DAC and an asymmetrical window detection method for the comparators are proposed to lower the power consumption of LC-ADCs. A low-power single-bit LC-ADC has been designed in AMS 0.18μm CMOS technology. This chapter is dedicated to the design, implementation and measurement of the proposed single-bit LC-ADC.

3.1 Introduction

The power consumption of previously reported LC-ADCs [1, 2, 13] is usually ranging from a few to tens of microwatts. In order to investigate the possibility of reducing the power consumption, an analysis from a

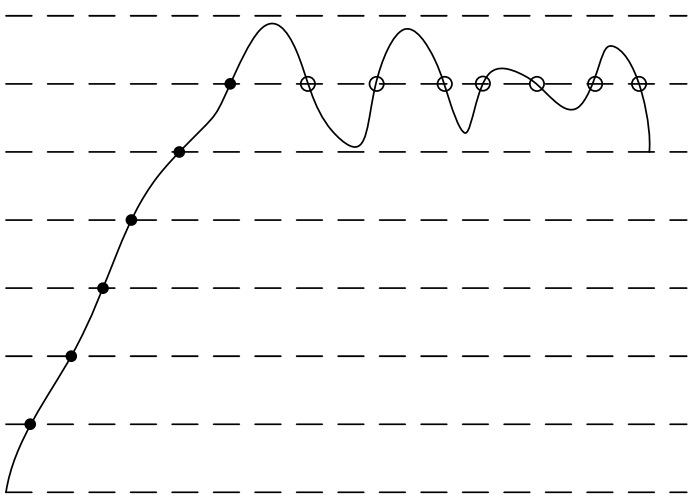


Figure 3.1: Different level crossings: consecutive level crossings (CLC; solid dots) and repeated level crossings (RLC; hollow circles)

system level perspective is necessary. Since the power consumption in LC-ADCs is event related, we start with the fluctuation characteristics of the input signal.

First of all, from the input signal side, we assume that any unwanted level crossings due to noise are suppressed by introducing hysteresis in the DACs or the comparators [1, 2, 24]. Let's assume that the input signal is varying as in Fig. 3.1. We hereby define two types of level-crossing points: one is called consecutive level crossing (CLC) and represented by solid dots; the signal crosses the upper (or lower) levels consecutively. The other type is named repeated level crossing (RLC) and represented by hollow circles; the signal moves up and down around one level within 2 LSB. Apparently, it is not power efficient to update the whole system if the conversion is triggered by repeated level crossings, as the signal variation is indeed only within 2 LSB.

Secondly, the comparison window between the upper and lower levels in previous works was set by two identical comparators, one of which is always idle in the case of consecutive level crossings. As a result, half of the power consumed by these two comparators is wasted. It is possible to lower the power consumption of the idle comparator or even shut it down, but additional circuits are needed [25].

Thirdly, the up/down counter outputs digital codes, which are then converted by the n-bit DAC to analog voltages to track the input voltage.

Nevertheless, the n-bit DAC conveys the delta information of only 1 LSB for each sample. According to the operation of an LC-ADC, a 1 bit DAC should be enough.

Fourthly, the output voltages of the DAC track the input voltage over the full-scale range, which means the operating common-mode voltage of the comparators changes a lot. In order to accommodate this large common-mode voltage range, the comparators need to consume quite some power but input common-mode voltage related offsets still generate different time offsets and hence distortion. Related discussions on how to fix the common-mode voltage can also be found in [2, 5, 16, 20, 25, 26]

3.2 Operating Principle of the Offset Injection Mechanism for a Single-Ended DAC

The system structure of the proposed LC-ADC is shown in Fig. 3.2 (a). An example waveform is depicted in Fig. 3.2 (b). The comparison window is fixed by introducing a 1 bit DAC with offset injection to the input. The 1 bit DAC tracks the input signal V_{IN}, performs subtraction or addition on the tracked input when there is a level crossing, and outputs V_{ON}. The comparison windows of 1 LSB in previous designs are widened to 2 LSB (V_H-V_L=2 LSB) in this work. V_M, V_H and V_L are voltage references. V_M is equal to (V_H+V_L)/2. The MUX is controlled by the logic output from the lower comparator, which only compares the output of the DAC (V_{ON}) with V_M. In other words, the lower comparator is only for detecting the varying direction of the signal. The MUX switches between (V_H, V_{ON}) and (V_L, V_{ON}), namely, V_{ON} is only compared with V_H (or V_L) by the upper comparator. Therefore, the comparison window is now set by V_M and V_H (or V_L). Depending on the signal-crossing direction detected by the lower comparator, V_{ON} and V_H (or V_{ON} and V_L) are then fed to the input of the upper comparator. Consequently, adding an analog multiplexer and one more level (V_M) allows the two comparators to operate individually while still functioning as a comparison window of 1 LSB. Therefore, the level-crossing detection window is asymmetrical, with the upper comparator for consecutive level crossings and the lower comparator for repeated level crossings.

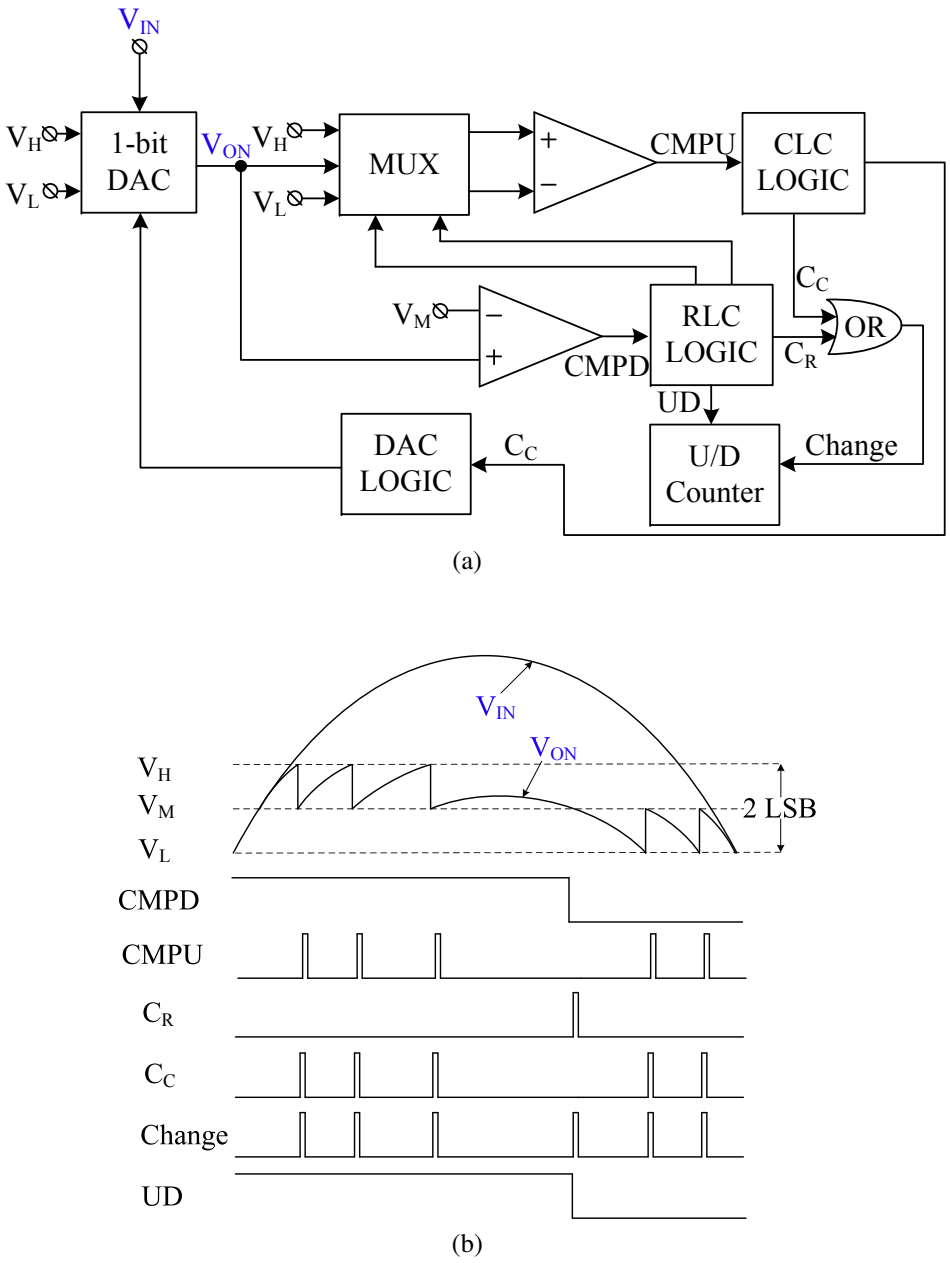


Figure 3.2: (a) Block diagram of the proposed structure. (b) Example waveforms.

For signals like ECG that have short periods of bursts and long periods of inactivity, there are different probabilities for consecutive level crossings and repeated level crossings to happen. Therefore, different power consumption levels of the two comparators can be set for different signals in order to save power. The details of the comparators will be discussed in

the following sub-section. Furthermore, RLC logic controls the MUX, outputs the up/down signal ("UD" in Fig. 3.2(b)) to the up/down counter and the related level-crossing pulse ("C_R" in Fig. 3.2(b)) due to repeated level crossings. CLC logic controls the DAC logic and outputs a pulse ("C_C" in Fig. 3.2(b), triggered by consecutive level crossings). "C_R" and "C_C" are then fed to the input of the logic OR gate to compose "Change" in Fig. 3.2(b). Note that repeated level crossings only refresh the up/down counter while consecutive level crossings update the whole system.

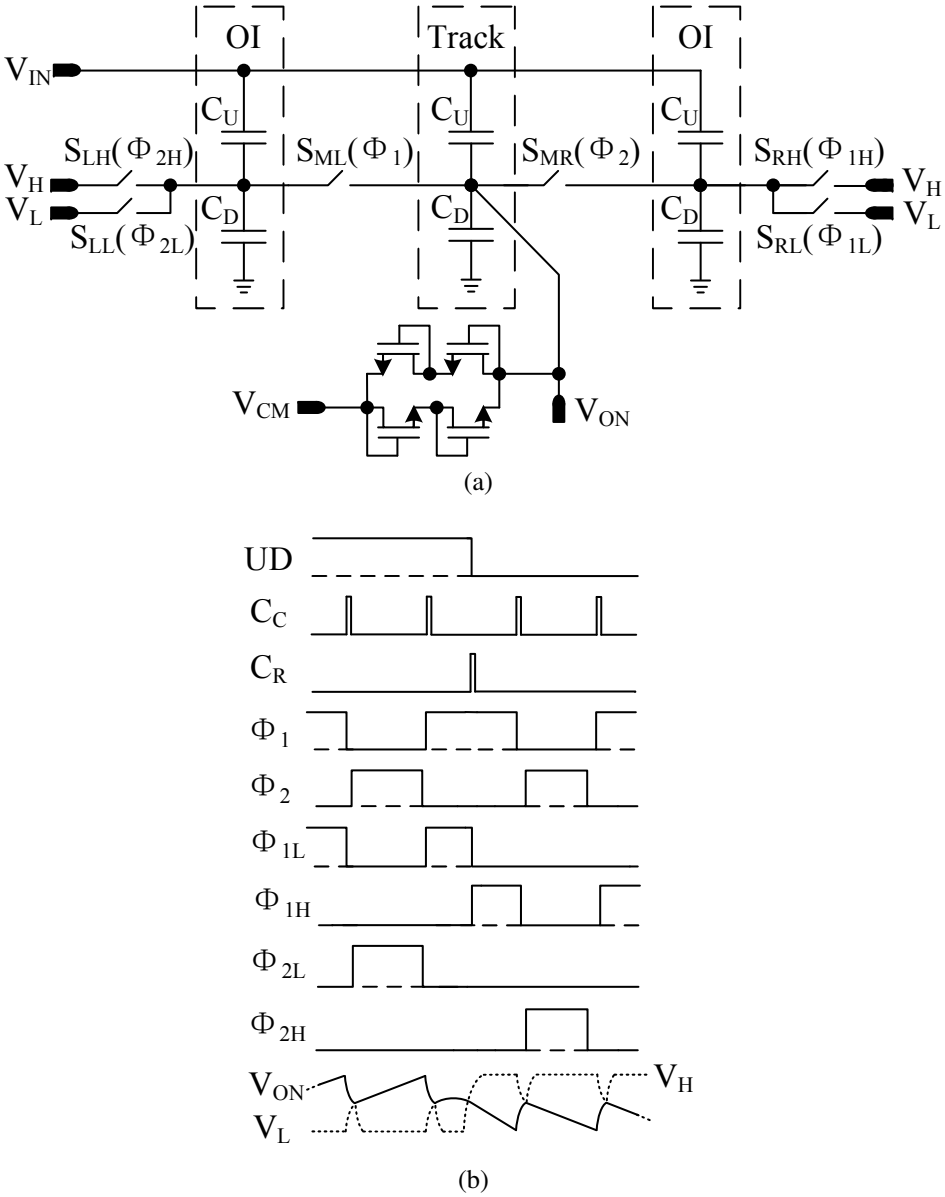


Figure 3.3: (a) Proposed 1 bit DAC (b) Example waveforms

3.3 Circuit Implementation

3.3.1 1 bit DAC

The main requirement of the DAC for the proposed system is injecting an offset voltage while tracking the continuous-time input. The proposed 1-bit DAC for doing so is shown in Fig. 3.3 (a). The waveforms in Fig. 3.3 (b) depict how the switches operate. Different from the previously published two-branch structure [18, 25], there are three identical branches in the capacitor array. The middle one is for tracking the input while the other two are for positive and negative offset injection (OI). Two capacitors in each branch are connected in series in order to achieve a continuous-time AC-coupled input. nMOS transistors are utilized as switches. Due to the nature of the offset-injection mechanism, any mismatch between the capacitors results in offset accumulation, namely, more "C_C" in "up" (UD equals "1") than in "down" (UD equals "0") or vice versa. Therefore, a pseudo resistor [27] comprising 4 transistors is introduced to cancel any unwanted accumulation during offset injection, and also to fix the DC common mode voltage at the output node when the input signal does not vary. In this case, the voltage swing at the output of the DAC is in the order of several mVs or tens of mVs at most, so the ultra-high resistance and ultra-low current of the pseudo resistor is suitable to finely tune and compensate for any possible accumulation when there is mismatch in the capacitor array.

The middle branch is connected to the left (or right) branch for normal operation when V_{ON} stays within the comparison window; the right (or left) branch is connected to V_H or V_L (depending on the signal ranging in between V_L and V_M or V_M and V_H). Therefore, one of the two OI branches is always charged with the needed predefined voltage. Supposing that V_{ON} crosses V_H, the CLC logic thus outputs a "C_C" pulse, which is then converted by the DAC logic to control signals Φ_1, Φ_2 and Φ_{1L} (or Φ_{2L}), injecting negative offset into the capacitor array by charge sharing. Note that Φ_{1H} and Φ_{2H} stay low during this phase. As is shown in Fig. 3.3 (b) for the first "C_C" pulse, S_{ML} and S_{RL} are switched off first to disconnect the left OI branch from the tracking branch and make the right OI branch ready for charge sharing. After that S_{MR} and S_{LL} are closed

to connect the predefined charged right OI branch to the tracking branch and discharge the left OI branch. V_{ON} is thus reset by sharing charge between the tracking branch and the newly connected branch. Due to this, V_{ON} is decreased by 1 LSB. The charging process is similar to the discharging process, but with one of the two OI branches connecting to V_H. In the previously reported two-branch structure [25], it takes some time for the voltage of the OI branch to settle with enough accuracy before it can be reconnected. Improved from the previous two-branch structure, the settling time requirement of the three-branch is relaxed considerably.

$\Phi_1$and Φ_2 are non-overlapping to avoid directly connecting the tracking branch to the voltage reference V_H or V_L. C_D is the unit capacitor while C_U is 14 times larger, so that 14/15 of the input variation falls on the upper plate of C_D. Since the settling time of the capacitor array is not related to the resetting time anymore, we have gotten rid of the trade-off between the settling time and the capacitance. Moreover, power consumption of the capacitor array is not a major concern here as the offset voltage injected at each crossing corresponds to 1 LSB only and is thus small. Considering charge injection of the switches, we should make the switches as small as possible, while the capacitors are preferably made as large as possible. However, due to the trade-off between accuracy and area, we finally set the lower capacitor to 200fF (for a single branch), which is good enough for our targeted overall resolution of 8 bits.

The advantages of the proposed 1-bit DAC include [4]: 1) the input voltage range is not limited, as the tracked input voltage is shifted up or down within the comparison window as soon as it reaches the fixed comparator level. In other words, the input signal swing can be higher than in conventional structures and can even exceed the supply voltage rails; 2) there is no information loss during offset injection, unlike the scheme proposed in [5, 26]; 3) the power consumption of the capacitor array is much lower than that of the conventional structure, as a delta voltage step of only 1 LSB per conversion is required.

3.3.2 Window Comparator

The continuous-time comparator used is shown in Fig. 3.4. The input stage comprises a pMOS input pair loaded by an nMOS current mirror.

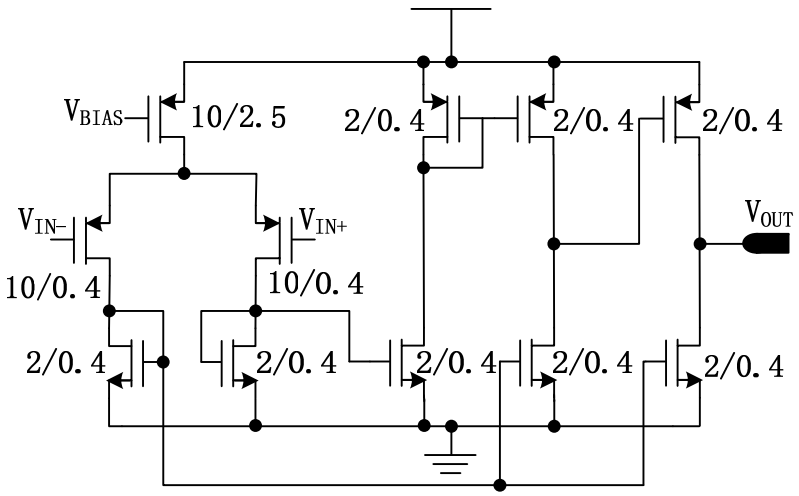


Figure 3.4: Three-stage comparator.

The current from the input stage is amplified by a second and a third stage. All the transistors are operating in subthreshold. The MUX is realized by four switches. Small size transistors were chosen to lower the charge injection.

Considering the two inputs of the upper comparator for the proposed LC-ADC, $V_{IN+}$is always lower than V_{IN-} when the signal stays in between the comparison window. As a consequence, the third stage does not consume static power as the pMOS is shut down by the output of the second stage when there is no level crossing. Only when the V_{IN+} is approaching V_{IN-} the third stage starts to draw current from the power supply.

Although the upper and lower comparators share the same structure, their power consumption is not necessarily equal. Generally, consecutive level crossings happen more often than repeated level crossings. For example, there are only two RLCs in one cycle of any sinusoid signal but a lot more CLCs. Similar results can be found for ExG signals. Therefore, we control the tail current of the comparator by adjusting V_{BIAS}, setting a lower current for the lower comparator while a higher current for the upper comparator. We name this different power consumption allocation "asymmetrical window detection". In this design, the current consumptions are roughly 135 nA and 270 nA for the lower and the upper comparator, respectively.

Offset may cause inaccuracy in the comparison levels. As the compara-

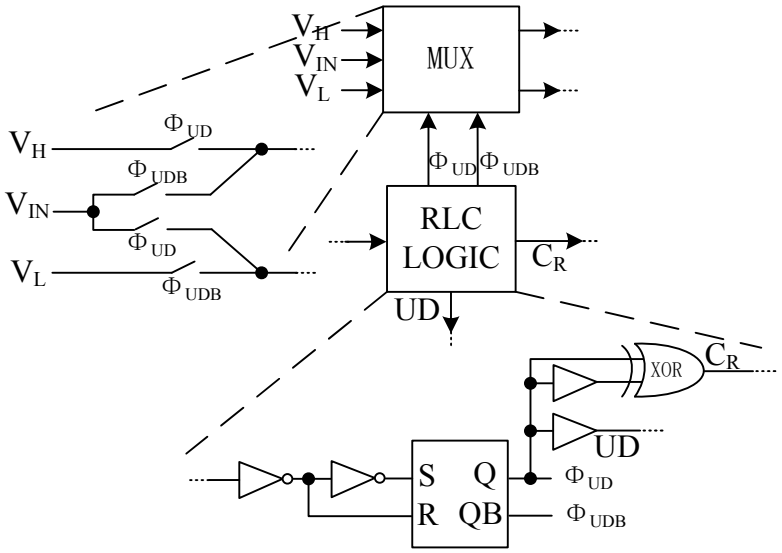


Figure 3.5: Detailed circuits of RLC logic and MUX

tors in LC-ADCs work continuously, it is impossible to introduce auto-zeroing. In previous works, offset was compensated by either applying a compensating DC level at the input [1], or DACs to tune the offset [2, 16, 20]. In this work, off-chip voltage references with potentiometers were adopted as reference levels, so the comparator offset could be compensated by tuning the reference levels.

3.3.3 Digital Blocks

LC-ADCs do not require a clock to trigger the operation of all the blocks, and are instead driven by the input voltage variations. The CLC logic block is modified from the one in [1]. Fig. 3.5 shows the RLC logic block and MUX. Inverters and an RS latch have been added at the output of the comparator to enhance the speed and output swing of its binary output signals. All the switches in the MUX are nMOS transistors, which are controlled by the outputs of the RS latch. Depending on the comparison result from the lower comparator, either V_{IN} and V_L or V_{IN} and V_H pass through the switches. Whenever the input signal crosses the middle level V_M, UD changes and the XOR outputs a C_R pulse.

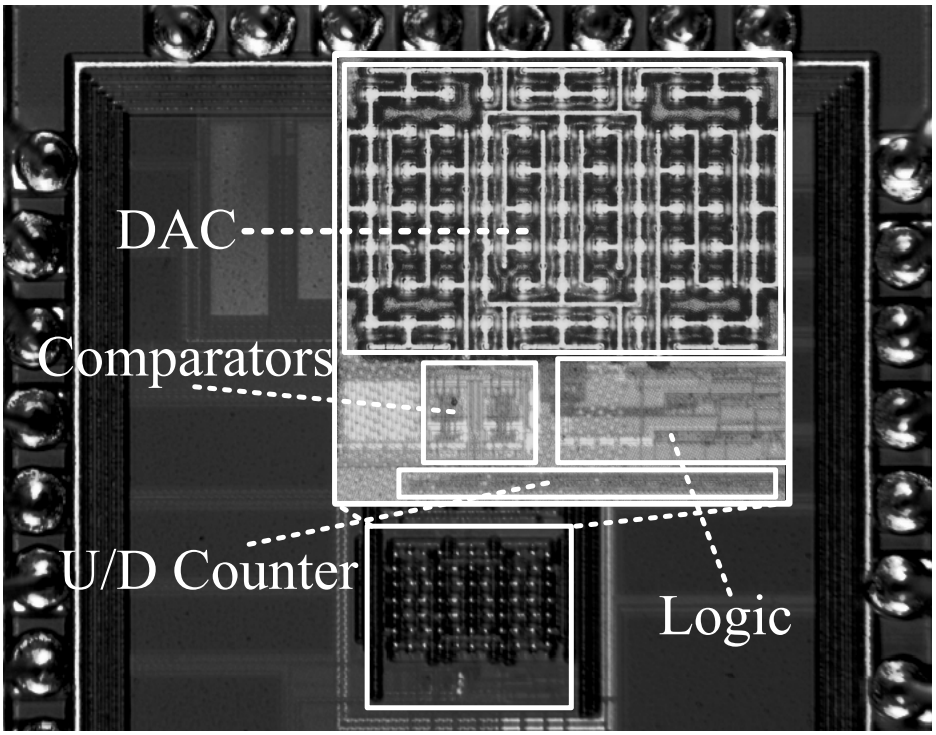


Figure 3.6: Chip micrograph. The active area is approximately 220×203 μm^2.

3.4 Measurements

The proposed LC-ADC has been implemented in AMS 0.18 µm CMOS technology. The active area is approximately 220×203 μm^2. The micrograph of the chip is depicted in Fig. 3.6. The capacitor array dominates the area. The digital supply and analog supply are both 0.8 V. The whole LC-ADC includes all the blocks shown in Fig.3.2 (a). The UD counter has also been integrated on chip. A logic analyser was used in the measurements for counting the time. Since level-crossing sampling is non-uniform sampling, in order to use the standard FFT for signal spectrum analysis, signal reconstruction and interpolation were performed in MATLAB utilizing polynomial interpolation. The order of the polynomial interpolation in the reconstruction has only a slight effect on the SNDR, so we varied the reconstruction order from 3 to 6 for each measurement to find the best SNDR. Different algorithms result in reconstruction accuracy variation. Their effects on accuracy have been investigated and reported in [3, 28, 29] . The measurement results of the prototype and

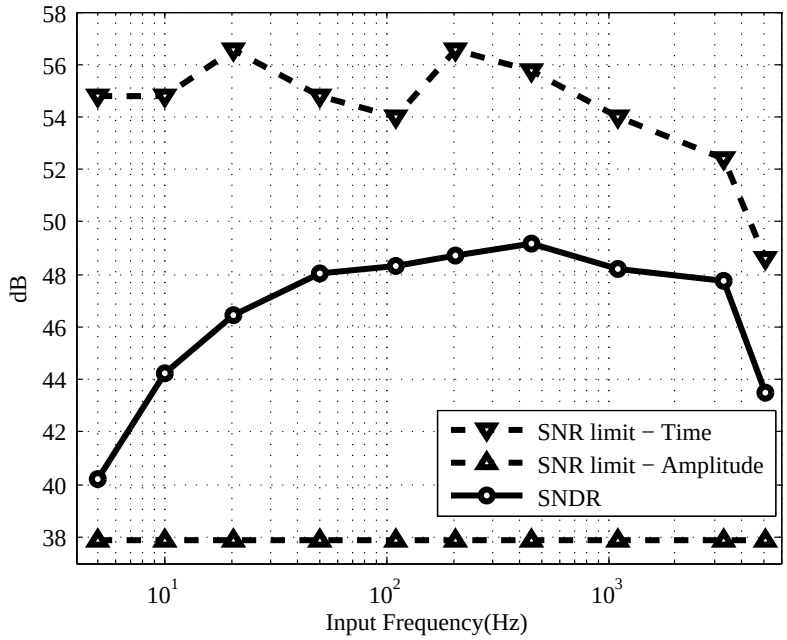


Figure 3.7: SNDR as a function of the input frequency ranging from 5 Hz to 5.1 kHz for a 0.8 V_{PP} input signal. 3rd to 6th order polynomial interpolations were used to reconstruct synchronous signals to calculate the SNDR by means of a standard FFT.

related discussion are presented below.

The dynamic performance of the ADC for an 800 mV_{PP} input signal, its input frequency swept from 5 Hz to 5.1 kHz is shown in Fig. 3.7. Since the input voltage range is not limited by the voltage reference or even the supply voltage, we can achieve a larger LSB from a higher input swing for a given accuracy. But there is a trade-off between power consumption and performance. In the measurements, 16 mV was chosen for 1 LSB. The same value applies for all measurements conducted unless mentioned otherwise. As higher oversampling ratios of the timer result in much larger data sizes and do not improve the performance that much, the logic analyser was adjusted to work from 10 kS/s to 5 MS/s for the entire input frequency range from 5 Hz to 5.1 kHz (i.e., the oversampling ratios are between 980 and 2440).

Note that the varying tendency of the SNDR in this work is different from that of an alias-free LC-ADC [1, 16, 30], in which SNDR rises with input frequency, because there is smaller in-band harmonic distortion as the input frequency increases. As can be seen from Fig. 3.7, the SNDR

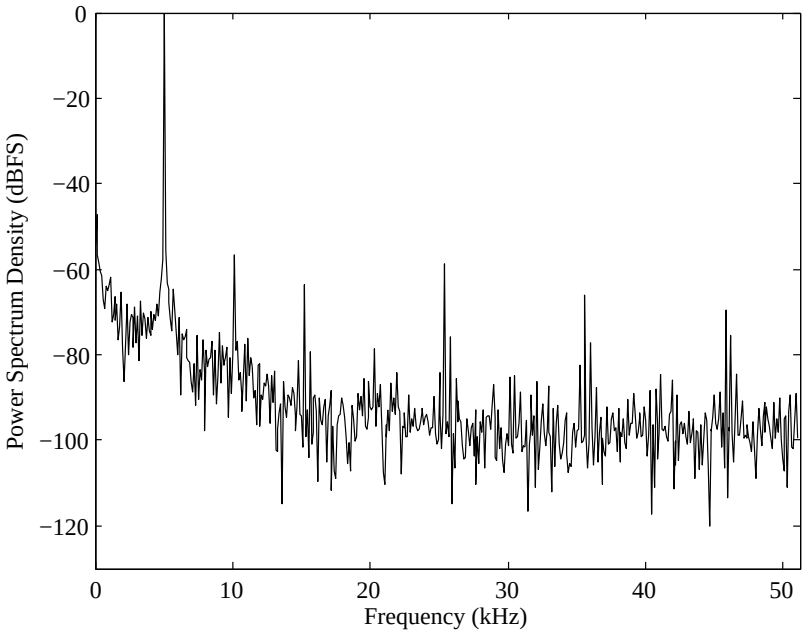


Figure 3.8: FFT of the measured ADC output for a 5.1 kHz sinusoidal input signal, using 1024 points reconstructed at 102.4 kS/s. A 3rd order polynomial interpolator was used to reconstruct the signal. The logic analyser was set at 5 MS/s. The SNDR is 43.5 dB.

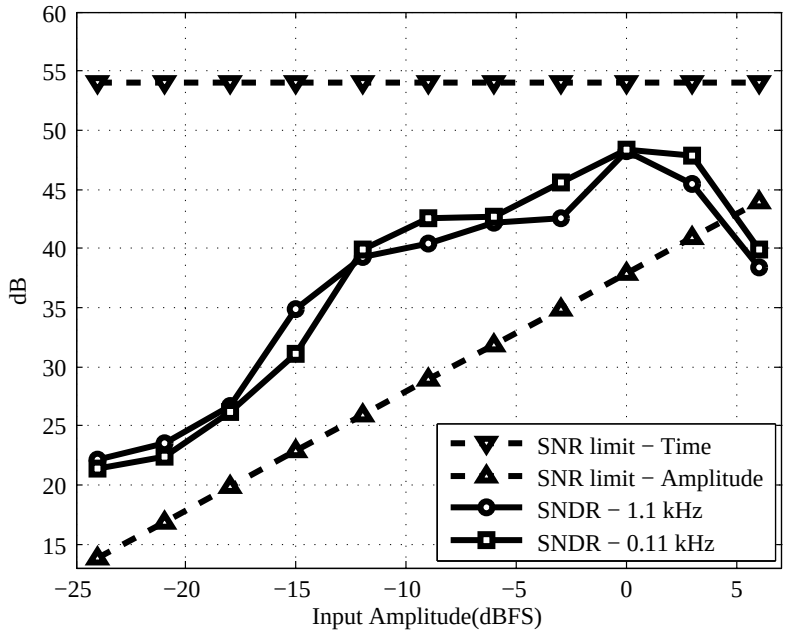


Figure 3.9: SNDR for input amplitude ranging from 50 mV to 1.6 V for input frequencies of 1.1 kHz and 0.11 kHz, respectively. The timer was set to 2 MHz and 200 kHz for 1.1 kHz and 0.11 kHz, respectively.

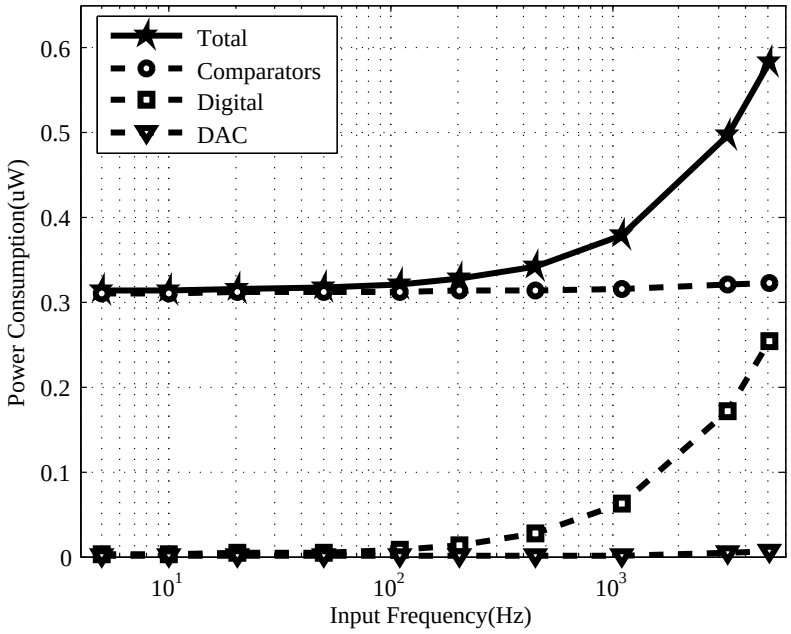


Figure 3.10: Power consumption as a function of input frequency ranging from 5 Hz to 5.1 kHz, for a 0.8V_{PP} input signal.

decreases due to the charge leakage when the input frequency goes down to 5 Hz while it degrades at higher input frequencies because of higher harmonic distortion and slope overload. The theoretical SNR limits due to the finite OSR of the timer and finite amplitude accuracy have also been plotted in Fig. 3.7 as references.

Fig. 3.8 shows the measured spectrum of the ADC output when the input frequency reaches 5.1 kHz. The logic analyser was set at 5 MS/s and a reconstruction sampling frequency of 102.4 kS/s and 1024 points were used to derive the spectrum. The SNDR degradation is mainly due to offset accumulation and slope overload. The offset accumulation could, in principle, be canceled in the digital domain by high-pass filtering, or be compensated by monitoring the mean value of the output bit stream and adding more "1" or "0" to the digital output, or be solved in a closed loop in the analog domain [31].

Since the input operating range of the offset injection based structure is not limited by the power supply, it is interesting to explore the performance of the LC-ADC for input signals that exceed the power supply voltage. A plot of the measured SNDR as a function of the input signal dynamic range is shown in Fig. 3.9 for a 1.1 kHz and a 0.11 kHz si-

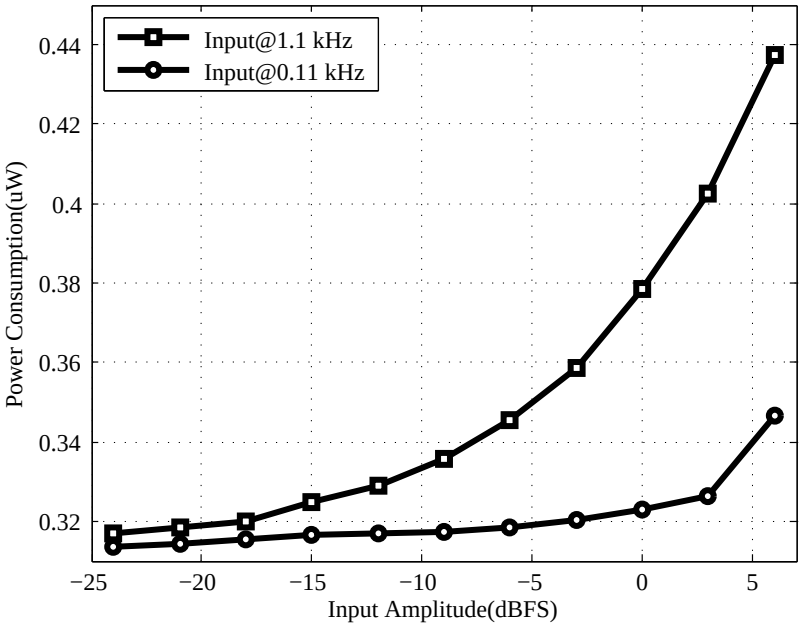


Figure 3.11: Power consumption as a function of the input amplitude ranging from 50 mV to 1.6 V for input frequencies of 1.1 kHz and 0.11 kHz, respectively.

nusoidal signal. The logic analyser was set at 2 MS/s and 200 kS/s for the 1.1 kHz and the 0.11 kHz input signals, respectively. 0 dBFS indicates that the input voltage swing equals the power supply voltage (800 mV). As this design was optimized for an input voltage of 800 mV_{PP}, the peak SNDR of the LC-ADC is achieved at 0 dBFS for both cases. When the input amplitude increases up to 1.6 V, slope overload affects the performance and the SNDR drops. Furthermore, as expected, the SNDR decreases with the input amplitude because fewer levels are crossed for an input signal with lower amplitude. Apparently, the capacitor array suffered more from the slower varying signals, which explains the reason why the SNDR of the LC-ADC for 0.11 kHz is slightly lower than for 1.1 kHz. Also, the SNR limits due to the time accuracy and the amplitude accuracy are included as references. In summary, the overall SNDR is higher than the SNR limit in amplitude because of the timer OSR, and the ADC still functions properly when the input exceeds the power supply.

Fig. 3.10 and Fig. 3.11 show the power consumption that has been measured as a function of the input frequency and amplitude, respectively. The measurements were taken under the same condition as held for Fig.

Table 3.1: Performance Comparison

	[1]	[2]	[5]	[13]	This work
Technology (nm)	90	180	500	130	180
Supply Voltage (V)	1	0.7	3.3	0.8	0.8
Adaptive Resolution	No	Yes	No	Yes	No
Automatic Calibration	No	No	No	Yes	No
SNDR (dB)	47-62	Peak 43.2	Peak 31	47-54	Peak 49
Input Bandwidth (kHz)	0.2 – 4	0.001 - 1.1	0.2-5	0.02 – 20	0.005– 3.3
Full-Scale Input (V_{PP})	0.5	1.4	2.68	0.72	1.6
Power Consumption (µW)	40 @DC	25 @1kHz	106 @1kHz	2.6 - 7.4	0.31 - 0.58
FoM (pJ/Conv.)	4.9-27.3	106	365.7	0.21- 0.88	0.219- 0.565
Active Area (mm^2)	0.06	0.96	0.06	0.36	0.045

3.7 and Fig. 3.9, respectively. The ADC consumes 313 nW and 582 nW for 5 Hz and 5.1 kHz input signals with 800 mV_{PP}, respectively. The total power consumption of the ADC increases with the input frequency. The comparators' power consumption dominates the static power consumption while the digital circuits and the DAC contribute to most of the dynamic power (see Fig. 3.10). Similar varying trends can be found in Fig. 3.11 when the input amplitude changes from 50 mV to 1.6 V. In order to compare with other previously reported LC-ADCs, the well-known equation for the figure of merit (FOM)

$$FOM = \frac{Power}{2 * BW_{eff} * 2^{ENOB}} \tag{3.1}$$

is used [32]. The performance of the LC-ADC is summarized and compared in Table 4.1.

3.5 Conclusions

A level-crossing ADC for biomedical applications has been presented in this chapter. Innovations at both system level and circuit level pave the way to low-power operation for the LC-ADC. Distinguishing RLC from CLC allows for independent operation of both comparators, avoids unnecessary updates of all the blocks in the LC-ADC and offers more design flexibility for the comparators. The use of a 1-bit DAC with three branches relaxes the settling time requirement. The circuit has been designed and fabricated in AMS 0.18 μm CMOS IC technology. Lower power consumption and less design complexity have been achieved due to the proposed topology. The event-driven nature makes the proposed ADC very suitable for biomedical applications.

Chapter 4

Low-Power LC-ADC with Programmable Comparison Window

A single-bit DAC was proposed and discussed in Chapter 3. The presence of the single-bit DAC lowers the power consumption of the single-ended LC-ADC to a new level of sub-micro watt. However, most biomedical readout front-ends adopt fully differential structures to achieve better performance. To fit LC-ADCs in these fully differential systems, differential LC-ADCs should be designed. This chapter describes the design and implementation of a differential low-power single-bit LC-ADC in AMS 0.18μm CMOS technology. A performance comparison with previous works will be listed at the end of the chapter.

4.1 Introduction

Application in wireless body area networks pushes the power consumption of wearable and implantable wireless biomedical readout sensors further to their limits. So far, there is little research on circuit and system design techniques that take advantage of the signal characteristics. Generally, the highest expected frequency of the input signal determines the

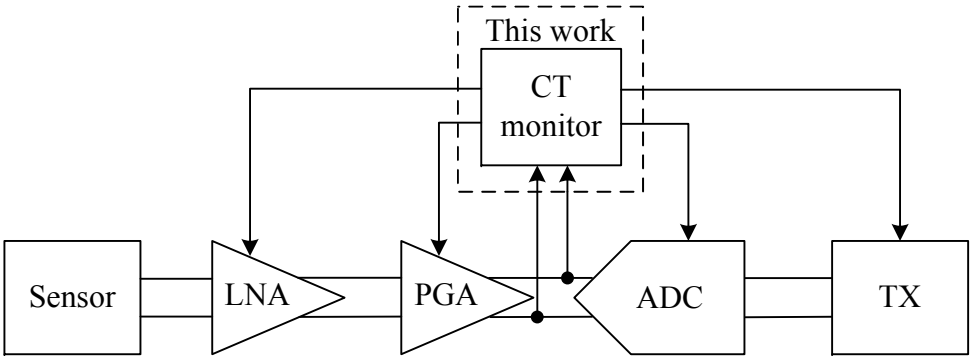


Figure 4.1: A biomedical readout system with continuous-time monitoring of system activity.

system operation bandwidth and speed, and thereby the power consumption. Operating the whole system at its maximum rate regardless of the possible sparsity of the input signal results in a waste of energy. Running the system at an adaptive rate according to the input signal activity may lead to considerable power savings.

To make the readout system adaptive, the frequency and amplitude information of the normal and abnormal excursions of the input signals need to be extracted and be continuously available to adjust the whole system. Such information, available from an activity monitoring block, can be used to control the data transmission rate, the ADC sampling rate, the biasing current of the analog blocks, the gain of the programmable-gain amplifier (PGA) and so on. In some previous works, window comparator based activity monitors can be found in adaptive sampling for data compression [33] and adaptive DC level control for motion artifact compensation [34]. But the operation of these monitors are triggered by clocks, which are usually much slower than the highest possible ADC sampling rates. Therefore, they are not able to truly continuously monitor the whole range of input signals over the complete input bandwidth.

This chapter describes a differential low-power single-bit LC-ADC for this application. A comparator with programmable offset and a low-power single-bit digital-to-analog converter (DAC) are proposed to separate the comparison windows and fix the common-mode voltage of the comparator. Implemented in a 0.18 μm CMOS technology, the proposed LC-ADC uses a chip area of 220×230 μm^2. Operating from a supply voltage of 0.8 V, the ADC input range can exceed the power supply voltage.

It consumes 0.32 - 0.84 μW from 5 Hz to 5.1 kHz with an ENOB of 7.8.

4.2 System Architecture

Normally, a window with an upper and a lower level is necessary for level-crossing detection. However, the structure with two identical comparators as found in previous LC-ADCs or in any window comparator application does not consume its power efficiently, because the input signal only approaches one level at a time, so only one comparator is active for detection while the other one is always idle. To further save power from the idle comparator, the conventional symmetrical comparison window has to be modified.

In the previously reported differential approach [2], two DACs subtract the differential input signals to ±1 LSB, respectively. So there are actually two symmetrical comparison windows in which the negative input is 1 LSB above the positive input and the positive input is 1 LSB above the negative input, respectively. Whenever the differential signals cross each other there is a level crossing. As we discussed in Chapter 3, consecutive level crossings (CLC) and repeated level crossings (RLC) do not necessarily require a symmetrical comparison window. A similar principle can be applied here, in which one comparator is in charge of the consecutive level crossings while the other one is responsible for the repeated level crossings. In the single-ended approach in Chapter 3, the input signal is compared with the reference levels. Similarly, we adopt the use of two single-bit DACs as proposed in Chapter 3 to inject an offset of ±1 LSB to the input differential positive and negative signal, respectively. Now the differential signals are compared with each other to detect the level-crossing event.

The proposed LC-ADC and example waveforms are shown in Fig. 4.2. Instead of tracking the input within the dynamic range by two n-bit DACs, two single-bit DACs with charge sharing are adopted to track and perform the addition or subtraction to the differential input signal whenever there is a level crossing. Two comparators with additional logic and a multiplexer (MUX) are combined. The lower comparator detects the polarity

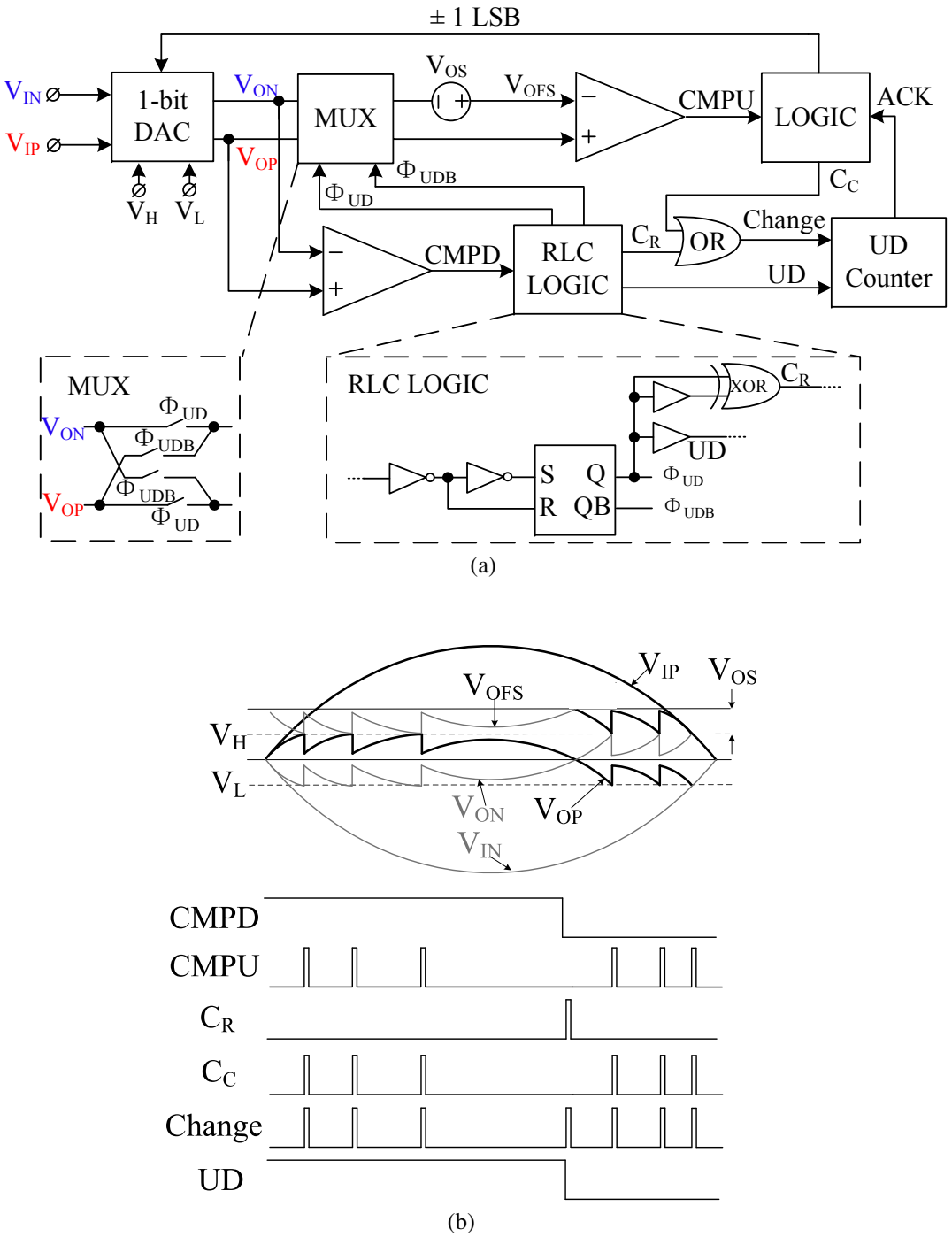


Figure 4.2: (a) Proposed LC-ADC. (b) Example waveforms.

of the input signal ($V_{ON} > V_{OP}$ or $V_{ON} < V_{OP}$), and controls the MUX to switch between (V_{OP}, V_{ON}) and (V_{ON}, V_{OP}) in such a way that the lower one of (V_{OP}, V_{ON}) is always connected to the negative input of the upper comparator. With the introduced built-in offset (V_{OS}) at the negative terminal of the upper comparator, the input at the negative node becomes level shifted up by V_{OS}. Consequently, there are three signals: V_{OP}, V_{ON} and V_{OFS} (V_{OP} or V_{ON} plus V_{OS}). The lower comparator compares the original differential input (V_{OP}, V_{ON}), while the upper one compares V_{OFS} with V_{OP} (or V_{ON}).

In this way we create two comparison windows: the one with solid lines for the upper comparator and the one with dotted lines for the lower comparator (Fig. 4.2(b)). The size of 1 LSB is thus equal to the upper window. Whenever V_{ON} and V_{OP} cross each other, the lower comparator senses this and swaps the two inputs for the upper comparator. So the level-crossing detection is split with the upper comparator detecting level crossings and the lower comparator detecting direction changes. Depending on the frequency of occurrence of the two different crossings, different supply power can be allocated to the comparators. Consequently, with two separate comparison windows, greater flexibility in the design of the comparator is introduced and power consumption can be lowered.

4.3 Circuit Implementation

4.3.1 Comparator with Built-In Offset

As an LC-ADC operates continuously, there is no clock for offset cancellation. In previous works, offset was compensated by either applying a compensating DC level at the input [1], or DACs to tune the offset [2, 16, 20]. However, we make explicit use of the offset in this work and further introduce an imbalance in the comparator input pair. The comparator with built-in offset is shown in Fig. 4.3. The input stage comprises a pMOS input pair loaded by nMOS diodes. The transistors in the dotted box are from the additional input pair to introduce the imbalance in the main input pair. Three bits (D_1-D_1 in Fig. 4.3) are used to digitally

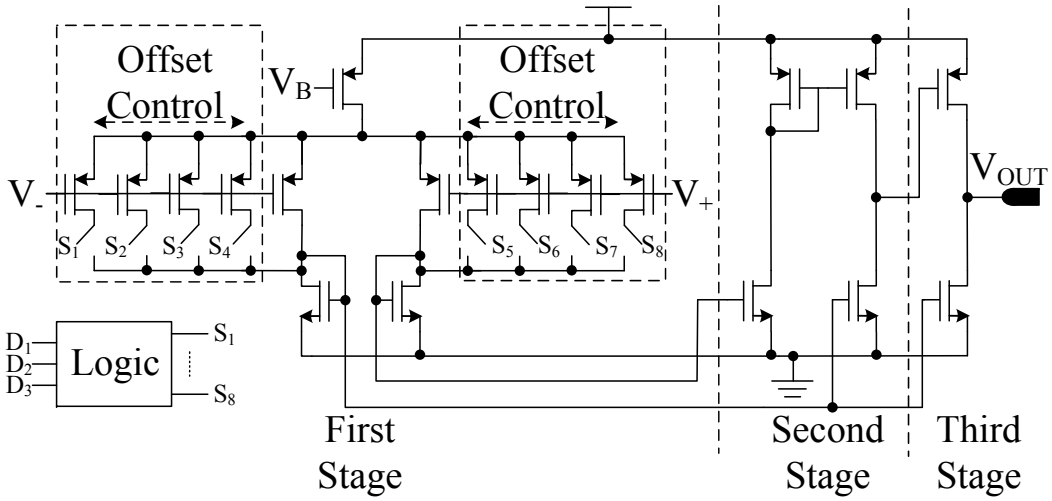


Figure 4.3: Continuous comparator with build-in offset.

control the value of the offset (V_{OS}). The width of the each pMOS transistor of the additional pair is eight times smaller than the one in the main pair. nMOS switches are used at the drain of the pMOS input pair. A programmable offset ranging from -20 mV to 23 mV was obtained from the measurements.

There are two signal paths from V_- to V_{OUT}: the one via the second stage is for gain enhancement while the one via only the third stage is for speed enhancement. Considering the two inputs of the upper comparator, V_+ is always lower than V_- when the signal stays within the comparison window. Therefore, the third stage does not consume static power as the pMOS is shut down by the output of the second stage when $V_- > V_+$. Only when V_+ is approaching V_- the third stage starts to draw current from the power supply. The lower comparator uses a similar structure but with hysteresis to improve the noise robustness.

4.3.2 1-bit DAC

The differential 1-bit DAC is shown in Fig. 4.4. The half-circuit is the same as the 1-bit DAC in Chapter 3. As can be seen from Fig. 4.4, nMOS transistors are utilized as switches. The DAC here is a combination of a charge pump and a tracking circuit, injecting an offset voltage while tracking the continuous-time input. Offset injection in a two-

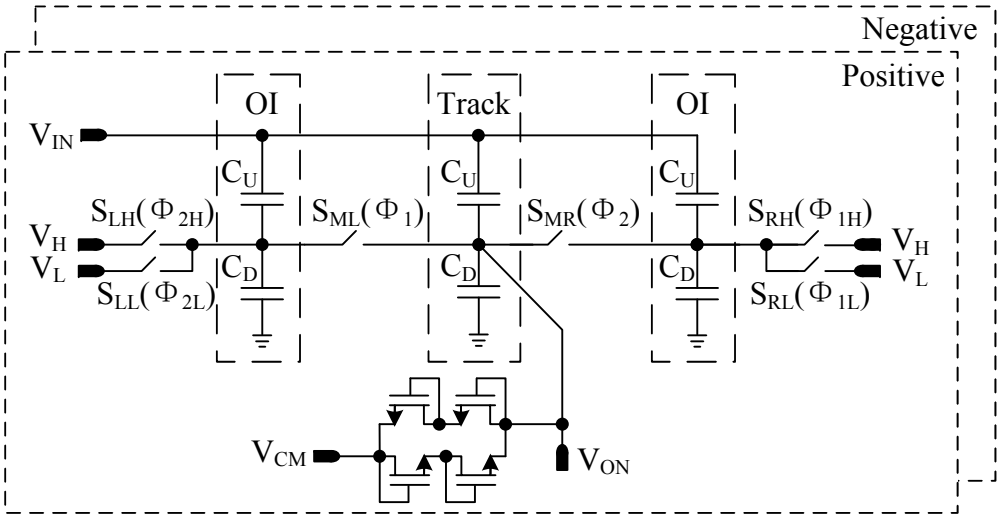


Figure 4.4: Proposed 1-bit DAC.

branch structure as used in [25] requires a certain settling time for re-setting. In this work, three identical branches in the capacitor array are designed. As a consequence, the settling time requirement of the three-branch structure is relaxed considerably. The detailed operation principle can be found in Chapter 3.

The differential structure here does not require much additional design effort. It is actually a matter of reusing the single-bit DAC introduced in Chapter 3. The differential single-bit DACs now operate complementarily, with one single-bit DAC injecting positive offset while the other one injects negative offset, and vice versa. Needless to say, area and power consumption of the differential DAC increase. Since the power consumption from the comparators dominates the total power consumption, the additional power consumption brought by the differential DAC is not critical.

4.3.3 Asynchronous Logic

The asynchronous logic control circuit is shown in Fig. 4.5. CMPU is the output signal from the upper comparator. ACK is the acknowledgement signal from the U/D counter. Reset is for resetting the asynchronous logic at the conversion start up. C_C is the output pulse to the next stage that processes the level-crossing conversion.

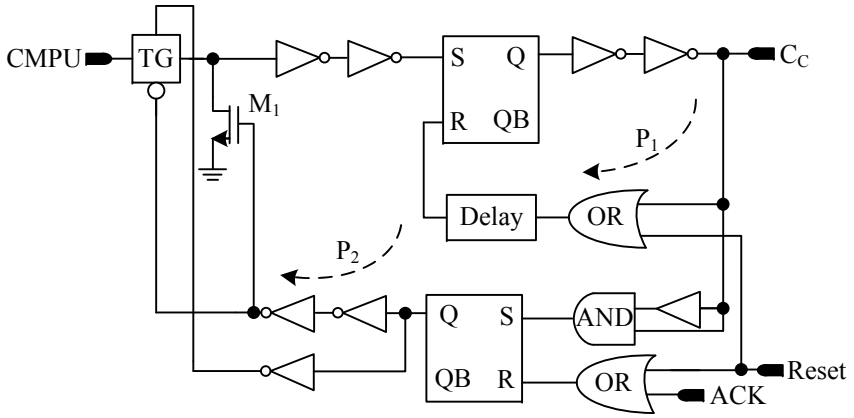


Figure 4.5: Asynchronous logic.

When there is no level crossing, the transmission gate (TG) is on and NMOS M1 is off. Whenever there is a signal crossing about to happen, the output of the comparator will start to rise. As soon as the comparator output (CMPU) crosses the threshold of the following two inverters, the upper SR trigger is set and its output is changing from "low" to "high". There are two following paths controlling the subsequent operation. For the lower path (P_2), the rising edge of the C_C pulse is detected by the detector (AND and the delay chain). The logic AND outputs a pulse that sets the lower SR trigger. Consequently, the TG is switched off and M1 is switched on to pull the drain node to ground. The comparator output is then disconnected from the asynchronous logic. For the upper path (P_1), the delayed rising edge comes later and resets the SR trigger. The delay time is determined from the system requirements. The entire asynchronous logic is disabled until the acknowledgement (ACK) signal from the next stage arrives. When ACK goes high, all the blocks are reset to the normal operation mode ready for the next level crossing.

4.4 Measurement Results

The proposed LC-ADC has been implemented in AMS 0.18 μm CMOS technology. Fig. 4.6 shows the chip micrograph. The active area is approximately 220×230 μm^2. All the blocks shown in Fig. 4.2 (a) were included on the chip. We set 1 LSB equal to 15 mV for all measurements. Since level-crossing sampling is non-uniform sampling, signal

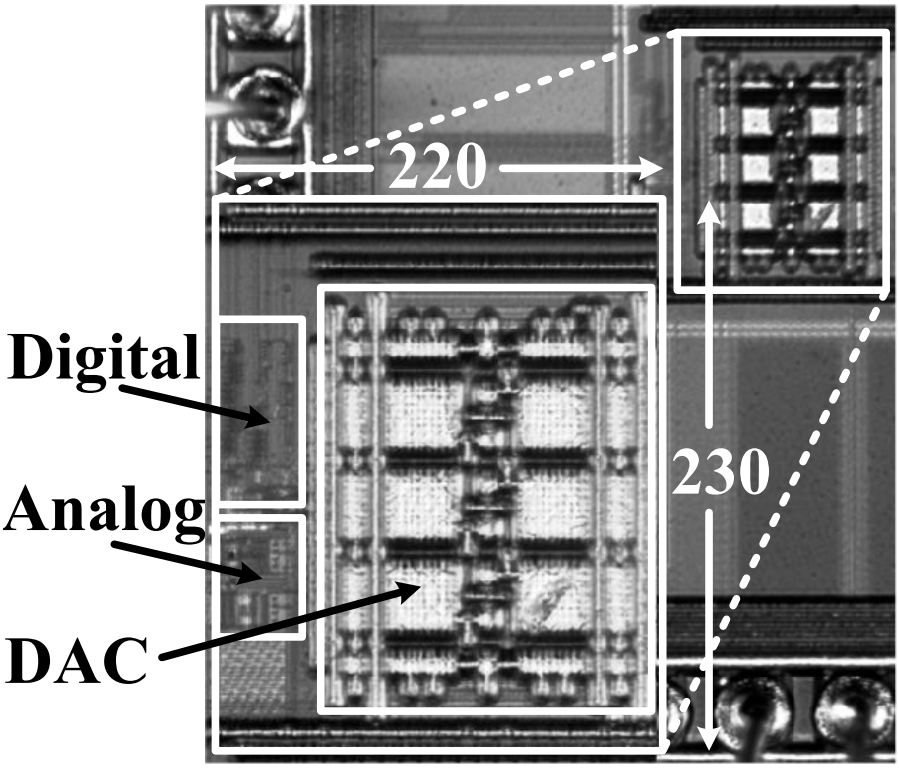


Figure 4.6: Chip micrograph. The active area is approximately 220×230 μm^2.

reconstruction and interpolation were performed in MATLAB utilizing polynomial interpolation. A logic analyzer was used in the measurements for counting the time in between two samples.

As the LC-ADC is an event-driven converter, it is worthwhile to measure to what extent the power consumption of the LC-ADC varies for different input signals. Fig. 4.7 and Fig. 4.8 depicts the power consumption as a function of the input frequency and amplitude, respectively. In Fig. 4.8, an 800 mV_{PP} sinusoidal signal, its frequency swept from 5 Hz to 5.1 kHz, is used. Due to the structure of the DAC, the input range of the LC-ADC can exceed the power supply. For the reliability of the device, a maximum input up to 2.25 V was used. The power consumption for a 0.45 kHz sinusoidal input signal ranging from 50 mV to 2.25 V is shown in Fig. 4.8. The total power consumption of the ADC increases with input frequency and with input amplitude. The analog power consumption dominates at low frequencies and amplitudes while the digital power consumption increases with frequency and amplitude. Fig. 4.9 shows the measured spectrum of the ADC output for a 5.1 kHz input signal. The

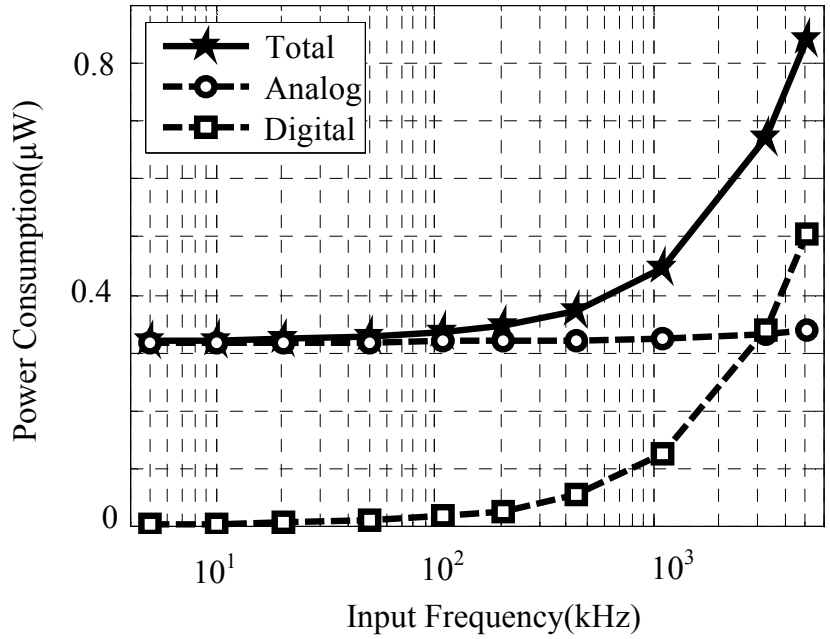


Figure 4.7: Power consumption as a function of input frequency ranging from 5 Hz to 5.1 kHz, for a 0.8 (V_{PP}) input signal.

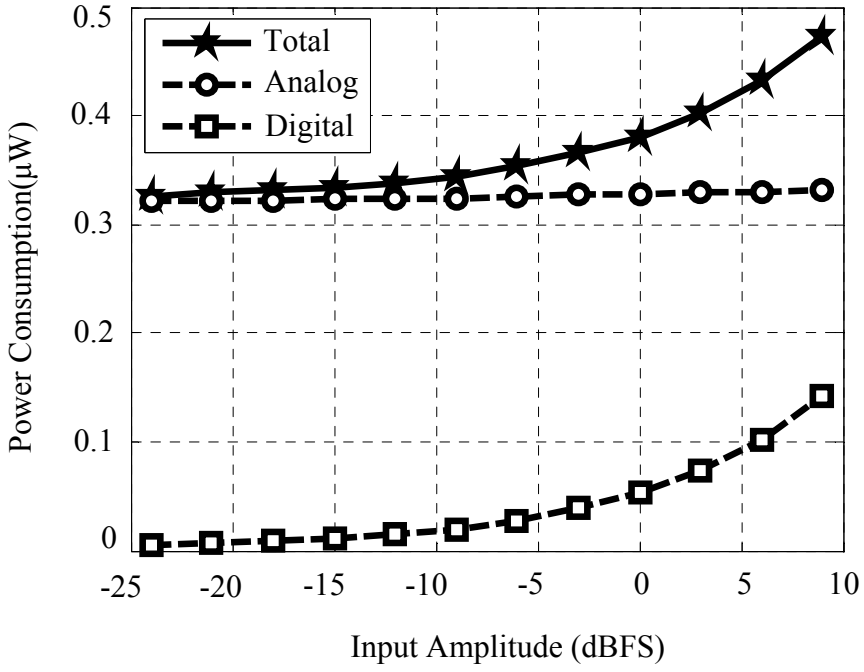


Figure 4.8: Power consumption as a function of input amplitude ranging from 50 mV to 2.25 V, for an input frequency of 0.45 kHz.

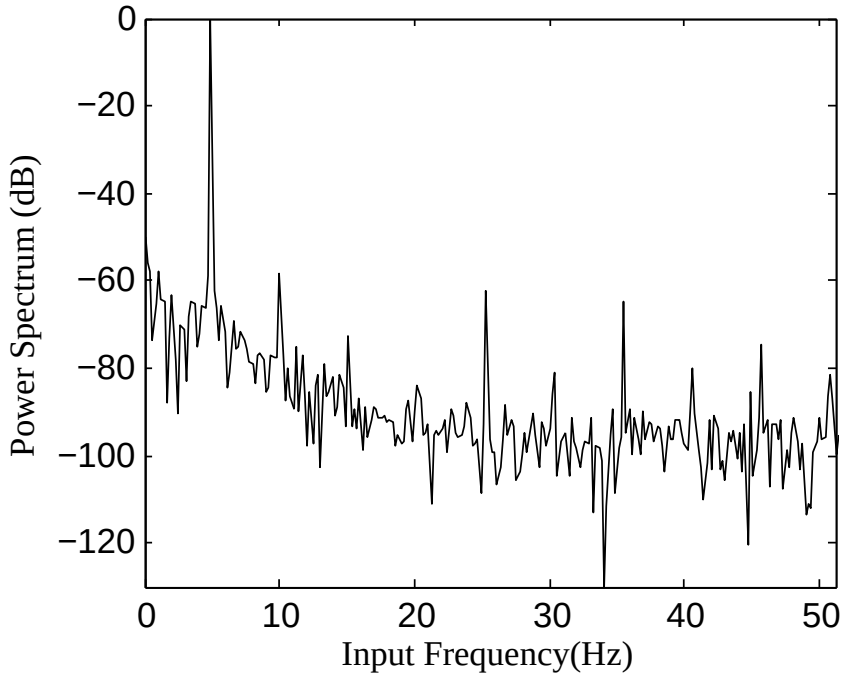


Figure 4.9: FFT of the measured ADC output for a 5.1 kHz sinusoidal input, using 1024 points reconstructed at 102.4 kS/s. A 6th order polynomial interpolator was used to reconstruct the signal.

logic analyzer sampling frequency equals 10 MS/s and a reconstruction sampling frequency of 102.4 kS/s and 1024 points were used to derive the spectrum. The SNDR degradation is mainly due to offset accumulation and slope overload. The low frequency distortion can be corrected by digital filtering or by introducing a mixed-signal loop [19].

The performance of the LC-ADC is summarized and compared in Table 4.1. The proposed LC-ADC achieves sub-microwatt power consumption while maintaining small area and moderate accuracy. Compared to other LC-ADCs [1, 2, 5, 16], the two LC-ADCs proposed in Chapter 3 and Chapter 4 achieve comparable performance in FOM to the one reported in [16, 20] while occupying less area. Since on-chip automatic calibration [16, 20] makes the circuit much more autonomous albeit at the expense of consuming additional power and area, for a future implementation, the introduction of a self-calibration loop and reduction of its associated power and area should be included. This will be discussed in the next chapter.

Table 4.1: Performance Comparison

	[1]	[2]	[5]	[13]	Chapter 3	Chapter 4
Technology (nm)	90	180	500	130	180	180
Supply Voltage (V)	1	0.7	3.3	0.8	0.8	0.8
Adaptive Resolution	No	Yes	No	Yes	No	No
Automatic Calibration	No	No	No	Yes	No	No
SNDR (dB)	47-62	Peak 43.2	Peak 31	47-54	Peak 49	Peak 49.4
Input Bandwidth (kHz)	0.2 – 4	0.001 - 1.1	0.2-5	0.02 – 20	0.005– 3.3	0.005– 5.1
Full-Scale Input (V_{PP})	0.5	1.4	2.68	0.72	1.6	2.25
Power Consumption (μW)	40 @DC	25 @1kHz	106 @1kHz	2.6 - 7.4	0.31 - 0.58	0.32 - 0.84
FoM (pJ/Conv.)	4.9-27.3	106	365.7	0.21- 0.88	0.219- 0.565	0.477
Active Area (mm^2)	0.06	0.96	0.06	0.36	0.045	0.05

4.5 Conclusions

A differential LC-ADC employing a novel level-crossing detection mechanism has been presented. The innovations at both system and circuit level lead to low-power operation for the LC-ADC. The low power and low area, together with the event-driven operation, pave the way for integrating low-power asynchronous LC-ADC in biomedical applications for system monitoring.

Chapter 5

An ECG Recording Front-End with Level-Crossing Sampling

This chapter deals with the design and implementation of an ECG recording front-end with continuous-time level-crossing sampling. The issues of realizing LC-ADCs for biomedical applications are discussed and a fully integrated system solution is described. The recording front-end includes a low-noise amplifier (LNA), a programmable voltage-to-current converter (PVCC), a 7-bit level-crossing ADC with 4-bit calibrating DACs and an RC oscillator to generate the calibration clock. More details of the proposed LC-ADC are discussed in the following sections. The leakage and power consumption issues of realizing LC-ADCs for biomedical applications are discussed in Section 5.1. The system working principle is presented in Section 5.2. Section 5.3 describes the analog front-end, while Section 5.4 presents the LC-ADC implementation. Measurements are reported in Section 5.5, followed by the conclusions in Section 5.6.

5.1 Introduction

Most of the previously reported works on level-crossing sampling, are either theoretical analyses or standalone LC-ADC designs. As there are

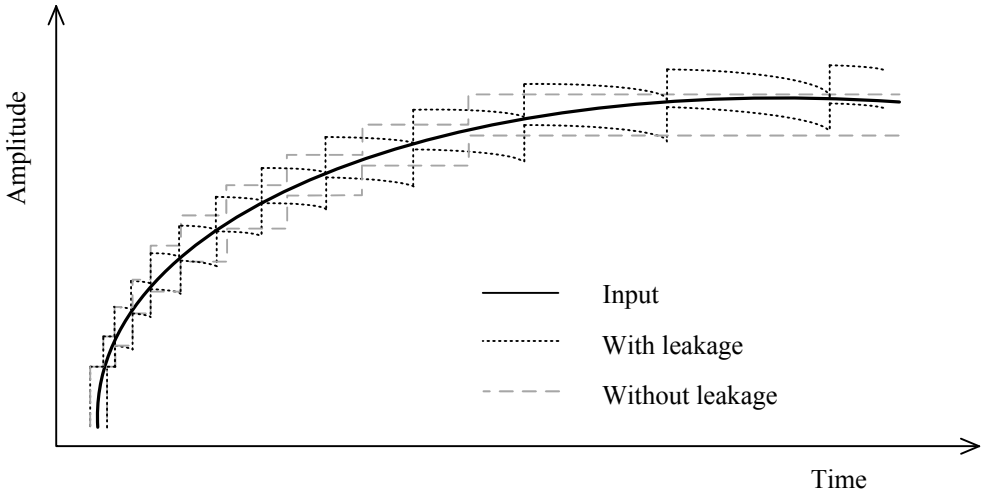


Figure 5.1: Comparison window is distorted due to the leakage in the capacitive DAC.

only few fully integrated systems with level-crossing sampling for biomedical applications, this inspired us to design the whole readout front-end and apply it to biomedical signal recording. This chapter is a follow-up of the previous two chapters, but with the entire readout system integrated on a single chip. As we discussed in previous chapters, the recently published LC-ADCs [1-5, 12, 13, 16, 17, 19, 24-26] can be divided into different categories. First, based on how the level crossing is detected, there are floating-window and fixed-window structures. The floating-window structure suffers from variations of the comparator offset and the need for a large common-mode swing while the fixed-window does not. Second, considering the feedback loops, a distinction can be made between the use of capacitive and resistive DACs. The capacitive DAC does not consume static power but the leakage current becomes a fundamental issue since the LC-ADC does not periodically refresh its capacitor array. As shown in Fig. 5.1, the comparison window is distorted due to the leakage. So it is not practical to use the capacitive DAC in a LC-ADC for applications in which the input frequency can be as low as mHz. The LC-ADC in previous works [4, 35] was implemented with a single-bit capacitive-feedback DAC and fixed-window detection, leading to considerable power savings. However, when the input signal frequency lowers to Hz or sub-Hz, the capacitive DACs are not able to hold the input signal for a sufficiently long time, resulting in dramatic SNDR degradation. In summary, the requirements for integrating an LC-ADC in a readout

system for biomedical applications are the following:

1) the feedback DACs should not suffer from leakage and the performance should not degrade at very low frequencies (down to sub-Hz); 2) fixed-window detection for the comparators is necessary to save power while maintaining the same performance; 3) on-chip automatic calibration should be integrated to reduce offset to improve the robustness.

From the requirements mentioned above, we conclude that a resistive DAC or a current-mode DAC should be chosen because of its better performance at low frequencies, since they are not susceptible to leakage. Both options have their own advantages and disadvantages. We eventually chose the current-mode approach as offset injection and cancellation can be done at the same current summation node, as will be explained in the following sections.

5.2 System Design

To achieve a good tradeoff between power efficiency and conversion accuracy, a typical signal processing chain usually starts with an LNA, followed by a programmable-gain amplifier (PGA) and a successive approximation register (SAR) ADC [33, 36]. The LNA is optimized for noise efficiency [37] and distortion while the PGA is optimized for driving the capacitive SAR-ADC, adjusting the gain based on the input signal level. A simple way to utilize level-crossing sampling is replacing the capacitive SAR-ADC with a capacitive LC-ADC like the ones in [2, 4, 5, 12, 13, 16, 19, 20, 25, 26]. However, as mentioned in Section 3.1, there are leakage related issues associated with capacitive structures at low frequency applications. Also, fixed-window detection should be used as the common-mode voltage of the comparator is fixed and thus the requirements on the comparator design can be achieved. Consequently, a resistive DAC structure [1] is not applicable in this design as the common-mode voltage of the comparator is not fixed. Furthermore, the power supply limits the dynamic range in a voltage domain system, which becomes even more serious for low-voltage designs.

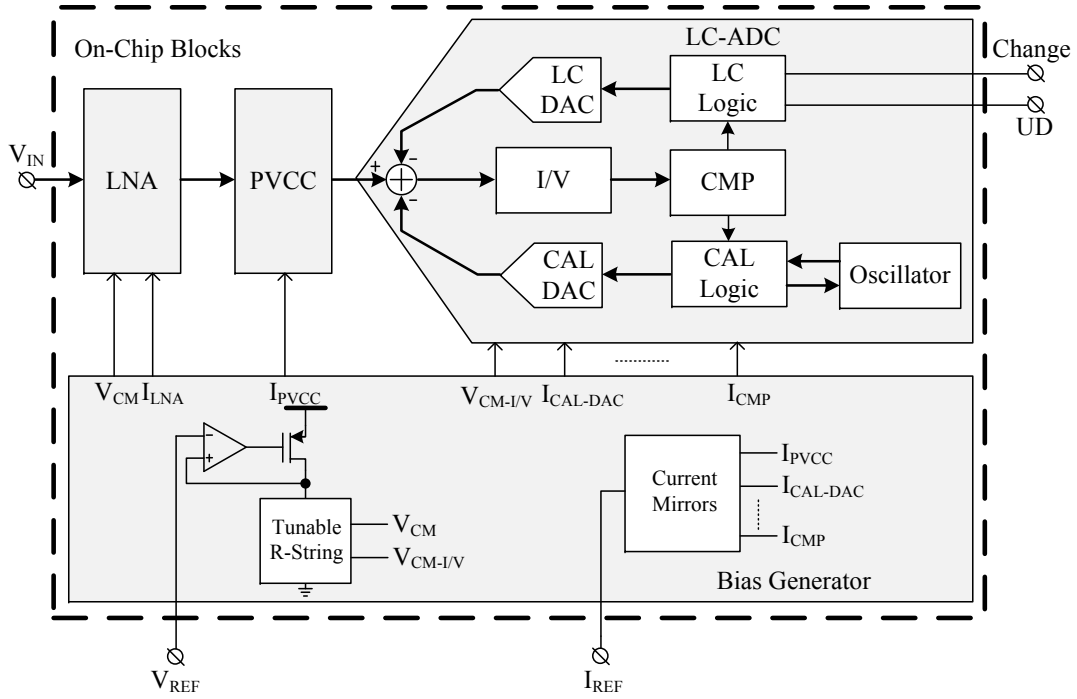


Figure 5.2: Block diagram of the propsed ECG recording front-end.

To overcome the issues mentioned above, we propose the voltage and current mixed system shown in Fig. 5.2. The system is a fully differential system to obtain good linearity. The differential input signal is amplified by the LNA in the voltage domain and then converted into a current by the programmable voltage-to-current converter (PVCC). The PVCC adjusts the gain of the system and outputs current for the LC-ADC. The output currents of the PVCC, the level-crossing DAC (LC DAC) and the calibration DAC (CAL-DAC) are summed at the same node. Then a current-to-voltage (I/V) converter converts the residue current into a voltage. The details of the I/V converter will be discussed in Section 5.3. After the I/V conversion, the comparator (CMP) takes the logic decision from the output of the I/V converter. The control logic (LC Logic and CAL Logic) keeps the whole system operating asynchronously.

As the whole system works continuously, it is impossible to suppress offset inaccuracies by using circuit techniques such as auto-zeroing. To solve this problem, an offset calibration DAC (CAL-DAC) and asynchronous calibration logic (CAL Logic) have been introduced to calibrate the offset of the whole system during the reset. The details of the calibration will be discussed in Section 5.4. Furthermore, bias circuits with

a regulator and current mirrors were also included in the system. The regulator at the left lower corner outputs the tunable common-mode voltage for the LNA and the I/V converter. The current mirror is also made tunable to adjust the system.

The proposed system benefits from four aspects. Firstly, the current-mode DAC does not have the leakage issue mentioned before. Secondly, a higher dynamic range is achievable as the signal amplification in the current domain is not limited by the supply voltage. In other words, higher current consumption brings higher dynamic range, which is not possible in the voltage domain. Thirdly, all the currents can be summed at one node and the feedback DAC (LC DAC) and the offset calibration DAC (CAL-DAC) can be easily integrated, resulting in a reduced design complexity. Fourthly, a differential current-to-voltage (I/V) conversion block keeps the comparison window fixed. The common-mode voltage of the current-to-voltage (I/V) converter determines the common-mode voltage of the comparator and can be easily optimized.

Since the programmable voltage-to-current converter (PVCC) works in class A, a higher biasing current in the PVCC possibly indeed offers larger dynamic range (DR), more phase margin and higher settling accuracy. But the DAC dynamic range and resolution also need to be modified accordingly in order to match the PVCC. So a larger DR can only be achieved at the expense of more power consumption from both the PVCC and the DAC. In this design, given the tradeoff among power consumption, device matching, output voltage swing and distortion, we decided to set the voltage gain of the LNA to 50, and further adjust the gain in the programmable voltage-to-current converter. Considering the power budget and full scale input range of the subsequent LC-ADC, we limited the current swing of the PVCC to 800 nAp-p. Supposing the ECG amplitude to be 1 mV and the PVCC set at its largest gain, the signal amplitude reaches at most 50 mV and 800 nA after the LNA and the PVCC, respectively. Consequently, we set the transconductance of the PVCC from 2 nA/mV to 16 nA/mV (in four steps), which in turn limits the maximum input voltage range of the PVCC to 400 mVp-p and of the LNA to 8 mV at the lowest gain, respectively.

As a higher amplitude resolution for the LC-ADC results in more samples while details are missing if the amplitude resolution is too low [4],

an adaptive-resolution algorithm [2, 16] could be beneficial for this work. However, additional bits are needed in the reconstruction to label the resolution for each sample. The adaptive-resolution algorithm can be included in future work if the issue above can be resolved. The amplitude resolution of the LC-ADC in this work is fixed to 7 bits.

5.3 Analog Front-End

5.3.1 Low-Noise Amplifier

To reject the DC offset from the skin-electrode contact, the LNA has been configured as an AC-coupled band-pass filter, as shown in Fig. 5.3. The high-pass cutoff frequency is set by the pseudo-resistor $R_{PSEUDO1(2)}$ and the negative feedback capacitor $C_{NF1(2)}$. The mid-band gain is set by the ratio between the input capacitor $C_{IN1(2)}$ and the negative feedback capacitor $C_{NF1(2)}$ as $C_{IN1(2)}/C_{NF1(2)}$. The low-pass cutoff frequency is dominated by the LNA gain (A_V), the transconductance (G_m) of the input pair and the compensation capacitor $C_{C1(2)}$ and equals $G_m/2\pi AvC_{C1(2)}$. To increase the input impedance, a positive feedback loop [38] was introduced in this work. The positive feedback capacitor $C_{PF1(2)}$ has been given the same value as $C_{NF1(2)}$. In addition, reset switches $S_{W1(2)}$ have been added to quickly set the input common-mode voltage during system initialization.

Considering the trade-off among noise, device matching, area, power and input impedance, we set the input capacitor and the negative feedback capacitor to about 20 pF and 400 fF, respectively. To increase the input impedance, a positive feedback loop [38] was introduced in this work. The positive feedback capacitor $C_{PF1(2)}$ has been given the same value as $C_{NF1(2)}$. The input impedance, after applying the positive feedback loop, can be expressed by

$$Z_{in}=\frac{V_{in}}{I_{in}-I_{pf}}=\frac{A_V}{sC_{IN1(2)}} \tag{5.1}$$

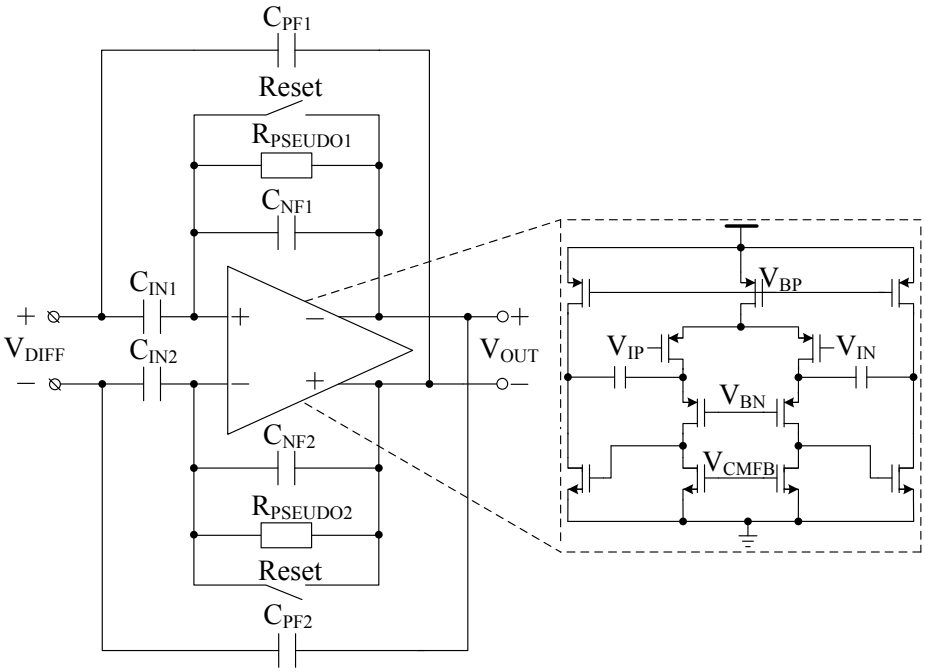


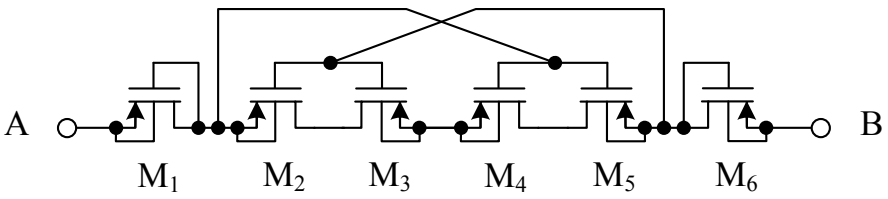
Figure 5.3: Circuit diagram of the LNA.

where V_{in} is the input voltage, I_{in} is the input current and I_{pf} is the current from the positive feedback loop. So the input impedance is boosted by a factor of A_V. In reality, any parasitic capacitance from the source degrades the boost factor [38].

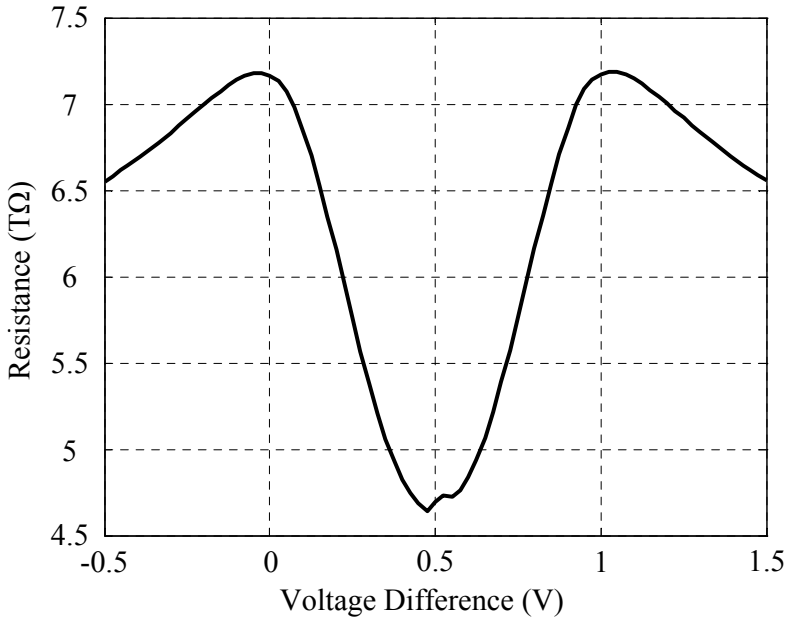
There are three major noise contributors in the LNA: the OTA, the pseudo-resistors and the positive feedback loop. The latter two noise sources can be neglected since: 1) the noise generated by the pseudo-resistor has a limited bandwidth from DC to the high-pass cutoff frequency of the LNA [39-41]; 2) the resistance (electrode contact resistance) seen from the LNA input is several orders of magnitude smaller than the positive feedback capacitor. The input referred noise of the LNA can be expressed by

$$\overline{V^2_{\text{in,LNA}}} = \overline{V^2_{\text{in,LNA}}}\left(1+\frac{C_{NF1(2)}}{C_{IN1(2)}}\right)^2 \tag{5.2}$$

where $V^2_{\text{in,LNA}}$ is the input referred noise of the OTA. A similar analysis can also be found in [39]. So the noise of the LNA is dominated by the noise of the OTA, as expected.



(a)



(b)

Figure 5.4: (a) Circuit diagram of the pseudo-resistor. (b) Simulation results for the DC behavior of the proposed pseudo-resistor.

A fully differential two-stage low-noise operational amplifier with cascode compensation [40] was used to implement the opamp (Fig. 5.3). To minimize the noise, pMOS transistors with large areas were employed for the input pair. Each input branch is biased with a current of 225 nA. The low-pass cutoff frequency is dominated by the LNA gain, the transconductance of the input pair and the compensation capacitor. We set the low-pass cutoff frequency to around 1 kHz, which is enough for the band of interest in the ECG recording application at hand.

Pseudo-resistors bias the input pair at a proper voltage level and determine the high-pass cutoff frequency. Such resistors are usually a bottleneck to improve the linearity performance in the biomedical amplifiers. To set the high-pass cutoff frequency to tens of mHz, a resistance in the

order of 10^{12} to 10^{13} ohm is necessary. Conventional pseudo-resistors [41] do not show a symmetrical characteristic when the voltage on both terminals is varied. Also the resistance varies at least one order of magnitude. All these effects result in distortion in the LNA.

In this work, we propose a balanced pseudo-resistor structure as shown in Fig. 5.4 (a). To guarantee that the high-pass cutoff frequency is low enough, medium-voltage pMOS transistors were adopted. The simulated resistance behavior of the pseudo-resistor is presented in Fig. 5.4 (b). M_1 (M_6) is connected as a diode to generate a voltage drop from both terminals. The inner source-bulk connected pairs M_2 and M_3 (M_4 and M_5) are in series and their gates are controlled by the drain voltage of opposite outer transistor M_6 (M_1). From A to B, or equally from B to A, there are always three drain-coupled pMOS transistors (M_3, M_5 and M_6) and three source-coupled pMOS transistors (M_1, M_2 and M_4). Consequently, a fully balanced structure from both sides of the pseudo-resistor is obtained. For the simulation, we fixed one terminal (A) to 0.5 V and swept the voltage of the other terminal (B) from -0.5 V to 1.5 V. Fig. 5.4 (b) shows a desirable symmetry and tolerable variation in resistance (from 4.7 TΩ to 7.2 TΩ).

5.3.2 Programmable Voltage-to-Current Converter

In conventional voltage-mode systems, a PGA follows the LNA to adjust the gain and drive the subsequent ADC. Since the LC-ADC in this work operates in the current domain, we propose a voltage-to-current (V/I) converter with a tunable resistor string to perform the PGA function. The voltage-to-current conversion requires the following characteristics : 1) the converter should work from a low-voltage supply (1V); 2) the V/I conversion ratio should be digitally controllable; 3) the current after conversion should be readily copied.

The circuit diagram of the V/I converter is shown in Fig. 5.5 (a). The differential input voltage (V_{IP},V_{IN}) is connected to the negative inputs of the operational transconductance amplifiers (OTA). These OTAs are used to further boost the gain of the two loops, respectively. The feedback loop

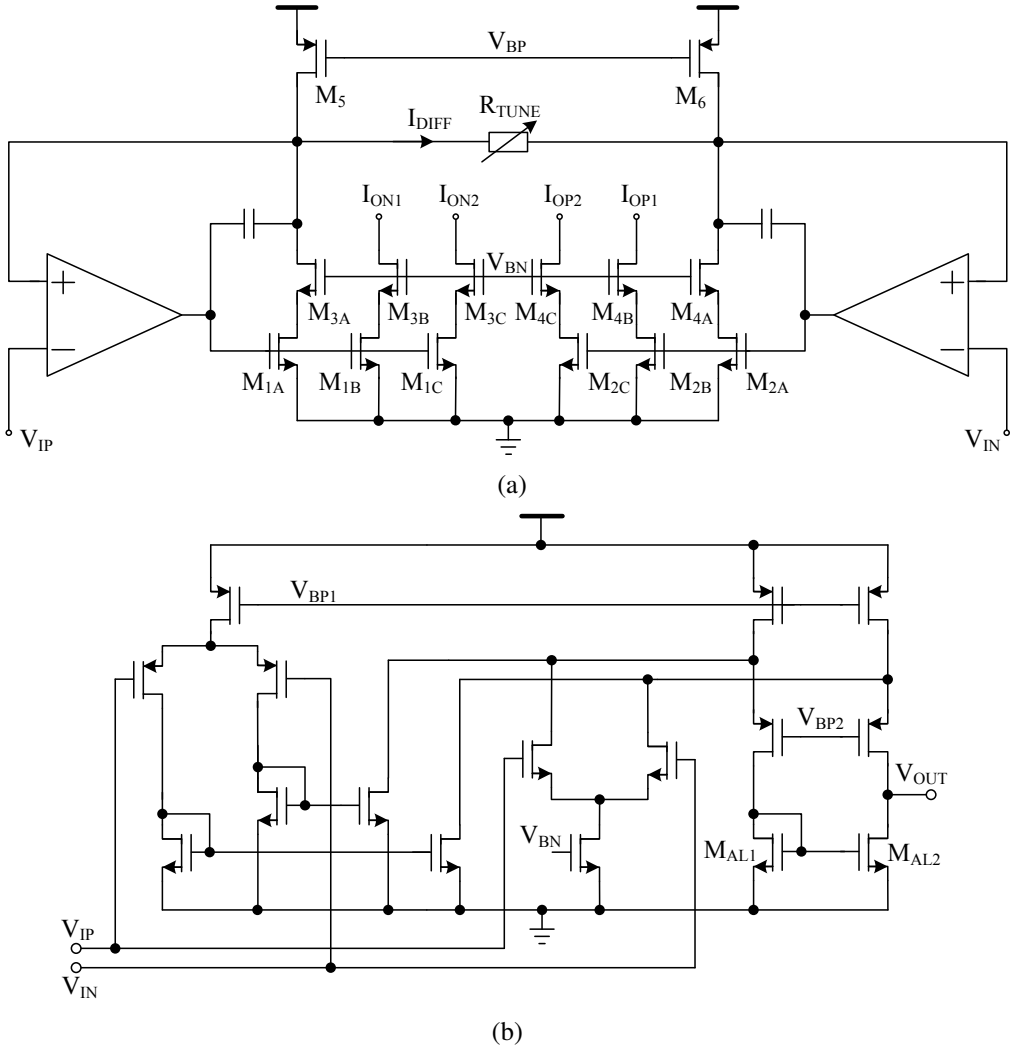


Figure 5.5: (a) Circuit diagram of the V-I converter. (b) OTA used in the V-I converters.

formed by the OTA, $M_{1A}(M_{2A})$ and $M_{3A}(M_{4A})$ forces the positive terminal to follow the differential input (V_{IP}, V_{IN}). The differential voltage drops across the tunable resistor R_{TUNE} and generates the current I_{DIFF}. R_{TUNE} is a resistor string with switches controlled by digital logic. The resistance of R_{TUNE} defines the transconductance of the V/I converter. The output current after conversion is obtained by copying the current from the loop.

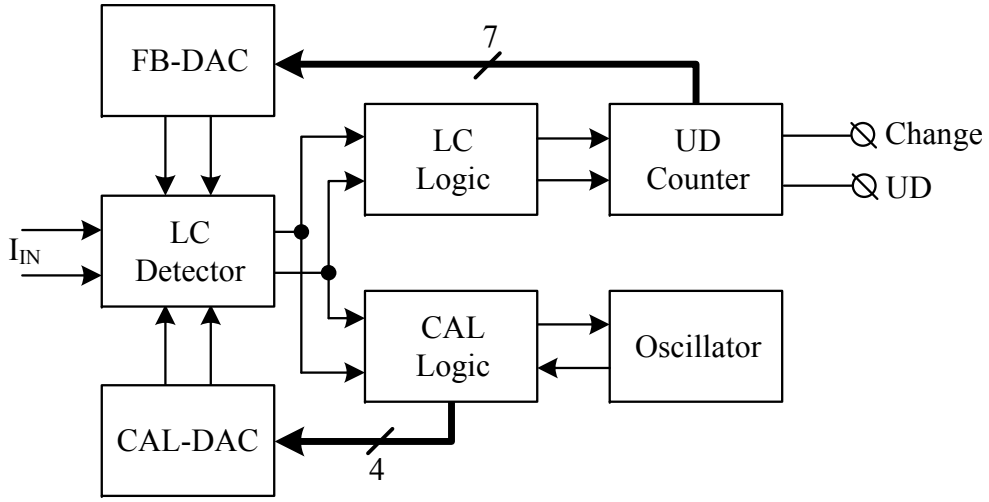
As shown in Fig. 5.5 (a), M_5 and M_6 provide the biasing current for the converter. $M_{1A(B,C)}$ and $M_{2A(B,C)}$ are acting as common-source stages and cascoded by $M_{3A(B,C)}$ and $M_{4A(B,C)}$ to increase the output impedance.

The tunable resistor R_{TUNE} is tuned by two digital bits. The resistance can be set to 175 kΩ, 350 kΩ, 700 kΩ and 1400 kΩ. So the largest transconductance is 8 times larger than the smallest one. Finally, $M_{1B(C)}$ and $M_{2B(C)}$ copy the converted current for the subsequent level-crossing ADC. In this work, the feedback resistor is connected at the drain of the transistors. Therefore, the consumed voltage headroom is minimized while voltage and current swing are maximized. Also, the converted current is readily copied and combined with the following stage, resulting in a flexible design.

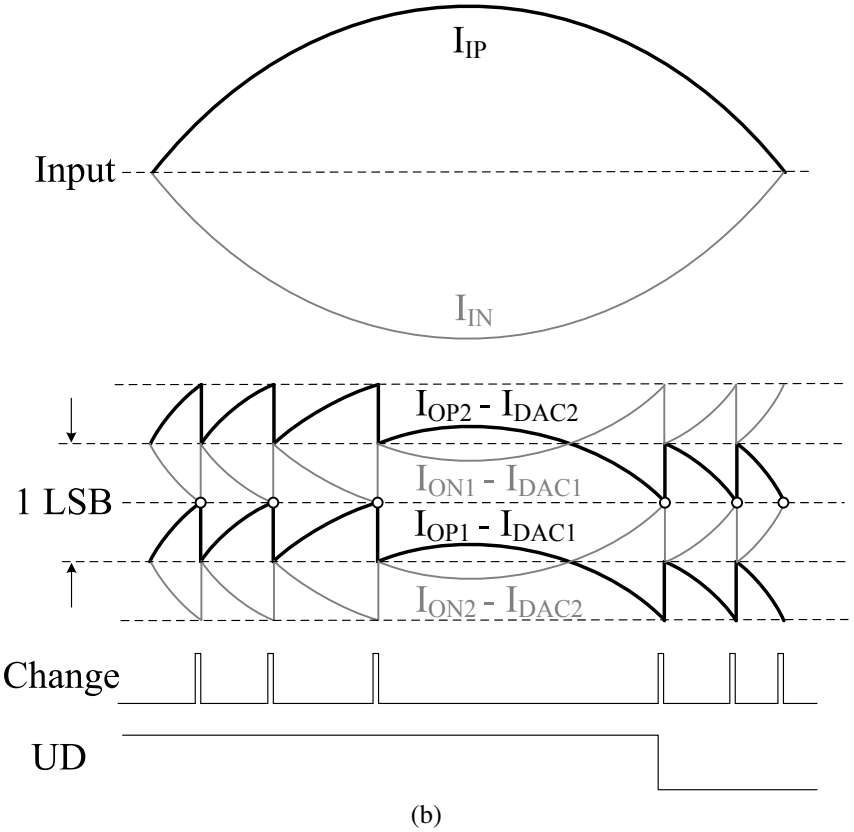
The circuit diagram of the OTA used in the PVCC is shown in Fig. 5.5 (b). Although the gain of the LNA in the previous stage is relatively low (34dB), a rail-to-rail input stage of the OTA is still necessary to guarantee the linearity of the conversion under the low-voltage supply. So a folded cascode amplifier with both pMOS and nMOS input pairs has been designed. To match and bias properly the common-source amplifier ($M_{1A(B,C)}$ and $M_{2A(B,C)}$) at the output of the OTA, the active load (M_{AL1} and M_{AL2} in Fig. 5.5 (b)) is not cascoded. The OTA is only driving the gate of the nMOS transistors, and the current consumption of the OTA is also preferably low to maintain the feedback loop stable, so each OTA here consumes a current of about 120nA.

5.4 Level-Crossing ADC

The block diagram of the proposed LC-ADC is shown in Fig. 5.6(a). The details of all the sub-blocks will be introduced in this section. After the voltage-to-current conversion, I_{IN} is fed to the LC-ADC. There are two DACs in the proposed system. The one that is in the feedback loop is called FB-DAC; the other one that is in the calibration loop is called CAL-DAC. FB-DAC performs the addition or the subtraction whenever there is a level-crossing while CAL-DAC calibrates the offset during the system reset. All the currents are summed at the input node of the level-crossing (LC) detector. The residue current is then converted into a voltage by the current-to-voltage (I/V) converter and compared by the comparator. During system reset, the LC logic, the up/down (UD) counter and the FB-DAC are being reset and the CAL-DAC is triggered by the



(a)



(b)

Figure 5.6: (a) Block diagram of the proposed LC-ADC. (b) Example waveform.

CAL logic and the oscillator to minimize the offset current. The calibration bits are stored in the registers once the reset has been done, and then the FB-DAC starts to work. The working principle of multi-bit LC-ADCs can be found in [1, 2, 13]. Example waveforms illustrating the working principle of the proposed LC-ADC with the FB-DAC are shown in Fig. 5.6 (b). The UD counter functions as a digital integrator. The feedback loop forces the output of the FB-DAC to track the input signal (I_{IN} or I_{IP}) and to inject the offset current to the input, resulting in residue currents ($I_{ON1(2)}$ - $I_{DACN1(2)}$ and $I_{OP1(2)}$ - $I_{DACP1(2)}$). Whenever the two differential residue currents cross each other, the output of the LC detector toggles and the LC logic at the next stage starts to update the UD counter. The FB-DAC injects the offset current and the LC-ADC continues to track the input signal, being ready for the next crossing.

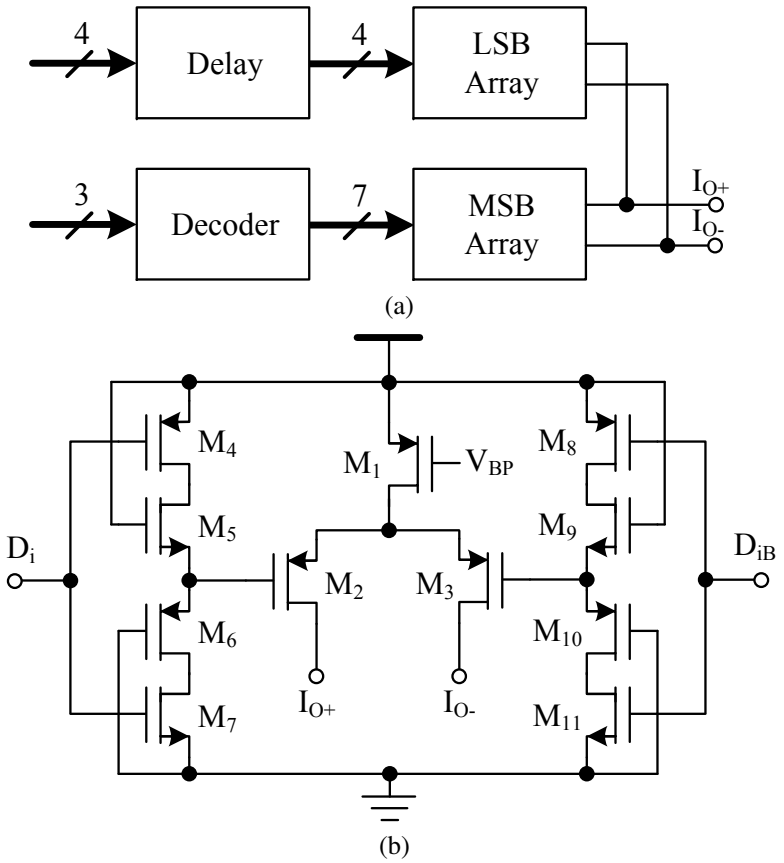


Figure 5.7: (a) Block diagram of the current DAC. (b) Circuit diagram of the current cell.

5.4.1 Segmented Current DAC

For the tradeoff between accuracy and design complexity, the 7-bit DAC is segmented into a 3-bit thermometer-decoded MSB array and a 4-bit binary-weighted LSB array. The system diagram of the segmented current DAC is shown in Fig. 5.7(a). A delay is inserted in front of the LSB array to minimize glitches at the output.

Due to the low voltage supply, the current cell used in both arrays of the DAC was designed with a single-transistor current source (M_1) and a switching transistor pair (M_2, M_3) as is shown in Fig. 5.7 (b). Since the interested signal band for ECG signals is below 500Hz, the speed and settling time are not an issue in this design. The driving circuit is composed of M_4-M_7 (M_8-M_{11}). M_5 and M_6 (M_9 and M_{10}) limit the output swing and reduce the clock feedthrough from the previous stage. Consequently, transistors M_2 and M_3 operate in the saturation region and a cascode configuration is formed. Therefore, the output impedance of the current cell is enhanced.

5.4.2 Level-Crossing Detector

The residue current from both the PVCC and the DACs are summed at the input node (I+, I-) of the level-crossing detector. The current is converted into a voltage and subsequently the comparator outputs a logic high or low. The level-crossing detector is shown in Fig. 5.8 (a). It consists of a differential current-to-voltage (I/V) converter and a voltage comparator. The I/V converter is similar to the one in [42], but designed with a single-stage fully differential amplifier. The voltage comparator is depicted in Fig. 5.8 (b).

As the outputs of the PVCC and the DAC are both current mirrors, the PVCC and the DAC output CM voltage is preferably fixed at a favorable biasing point. This is critical for the continuous-time operation and tracking accuracy. A simple current comparator with open-loop operation does not suffice to quickly stabilize the CM voltage of the current summation node when the input current (I+, I-) varies. More complicated current comparators always have internal feedback (negative or positive)

to either sense the small current difference or speed up the comparison. Furthermre, these current comparators always have a non-linear (e.g. log-domain) I-V conversion and output their high and low values in terms of voltage.

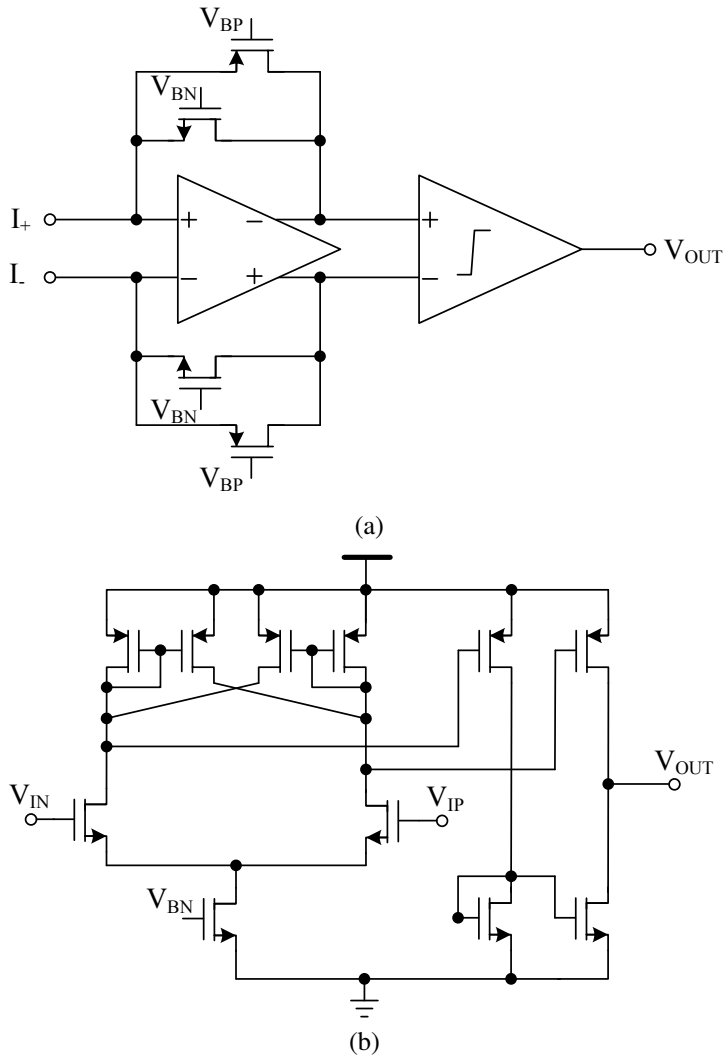


Figure 5.8: (a) Level-crossing detector with an I/V converter as the first stage and a comparator as the second stage. (b) Circuit diagram of the comparator.

The I/V converter utilizes both pMOS transistors and nMOS transistors in the feedback loop to achieve symmetrical performance for current sourcing and sinking. The pMOS transistors and nMOS transistors are biased in the subthreshold region. They exhibit the largest resistance when the

input is at the optimum common-mode voltage level. A desirable high transresistance is thus obtained. Hence, a small input current difference is converted into a large voltage difference. In the level-crossing ADCs, this is a favorable situation as the input current difference is always within 1 LSB.

Consequently, the use of the non-linear resistances of the MOSFETs (the ones biased by V_{BN} and V_{BP} in Fig. 8 (a)) in the I-V converter offers two advantages: 1) a high-resistance path to sense and convert a small input current into a large voltage; 2) a low-resistance path (via either the nMOS or pMOS) to stabilize the CM voltage of the current summation node when the voltage there deviates from its favorable biasing condition for the PVCC and the DAC. So the I-V converter stabilizes the CM voltage and buffers the current summation node for the following voltage comparator.

The voltage comparator is depicted in Fig. 5.8 (b). To improve the noise robustness, hysteresis has been added to the comparator by means of the cross-coupled pMOS current mirrors.

5.4.3 Delay Cell in The Asynchronous Logic

In the level-crossing ADC, the whole system is based on an asynchronous hand-shake protocol highly relying on delay, so a delay cell for the hand-shake operation is vital for the correct system operation. The asynchronous logic used is modified from the one in [1]. We only discuss the delay here.

The block diagram of the delay is shown in Fig. 5.9 (a). The circuit diagram of a single delay cell is presented in Fig. 5.9 (b). All the current sources in the delay cell share the same biasing voltages V_{BN} and V_{BP}. IN is the signal from the asynchronous logic control, and it can be considered to be an enable signal. IN equals "0" means there is no level crossing. Otherwise, the delay cell is enabled to transmit a "1" from the previous cell to the REQ of the next cell. Once the "1" is acquired from the next cell, ACK together with the rising edge detector (RED) generate a "1" to RST_NS to reset the previous cell.

The delay cell in [43] is based on a structure called thyristor [44]. The advantages of such a delay cell include low-voltage operation, no static

current consumption and that pulse width is not related to the delay time. The delay cell in [43] has only an nMOS transistor based thyristor. In this design, we added a pMOS transistor based thyristor in cascade to further improve the robustness. The detailed working principle of each thyristor based delay element can be found in [1]. The delay time is defined by the delay capacitor C and the current source in the dashed box.

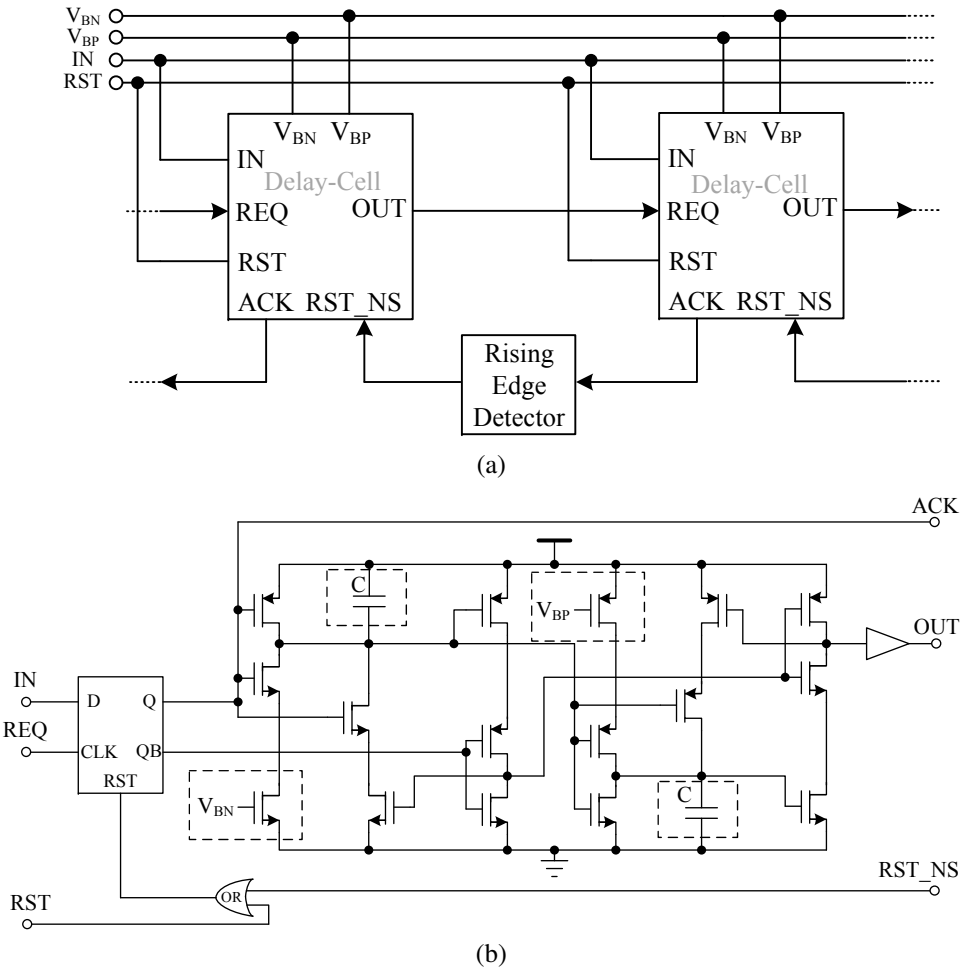


Figure 5.9: (a) Delay chain used in the asynchronous logic control. (b) Circuit diagram of a delay cell.

5.4.4 Offset Calibration

A simplified block diagram of the offset calibration is shown in Fig. 5.10 (a). Different from the asynchronous logic control based on a delay chain

in the feedback loop, the offset calibration control here utilizes an oscillator. The calibration DAC circuit itself here is the same as the 4-bit binary-weighted DAC in the feedback loop.

An example waveform of the digital control logic for offset calibration is shown in Fig. 5.10 (b). At system reset, the rising edge detector (RED) generates a pulse to reset all the blocks. The logic control block then outputs an enable signal to activate the oscillator, which starts to generate pulses. The comparator output controls the up/down counter to count up (or down) to decrease the voltage difference at the input of the comparator.

There are two possible conditions during calibration: 1) the offset is within the calibration range; or 2) the offset exceeds the calibration range. The first case results in comparator toggling while the latter one causes data overflow of the up/down counter. In both cases, the logic control can detect either the toggling pulses from the comparator or the data overflow (OVF) pulses from the up/down counter. Example waveforms of the signal at the input of the comparator (V_{IP},V_{IN}) and the finishing pulse for calibration are shown in Fig. 5.10 (c) and (d). Dotted lines are used to denote the repeated cycles. The comparator toggling (or data overflow) generates a finishing pulse to trigger the shift registers in the control logic to count. The length of the shift registers determines the number of repeated cycles. To make the calibration more robust, the number of repeated cycles was set to 16. The control logic disables the oscillator output after the repeated number of cycles reaches 16.

The LSB current in the CAL-DAC determines the minimum distinguishable offset. A larger CAL-DAC dynamic range gives a larger calibration dynamic range. So for a fixed resolution (4-bit in our case), there is a trade-off between the calibration range and the minimum distinguishable offset. For more calibration bits (> 4 bits), the calibration range and the minimum offset can be both improved but more area and parasitic capacitance will be added.

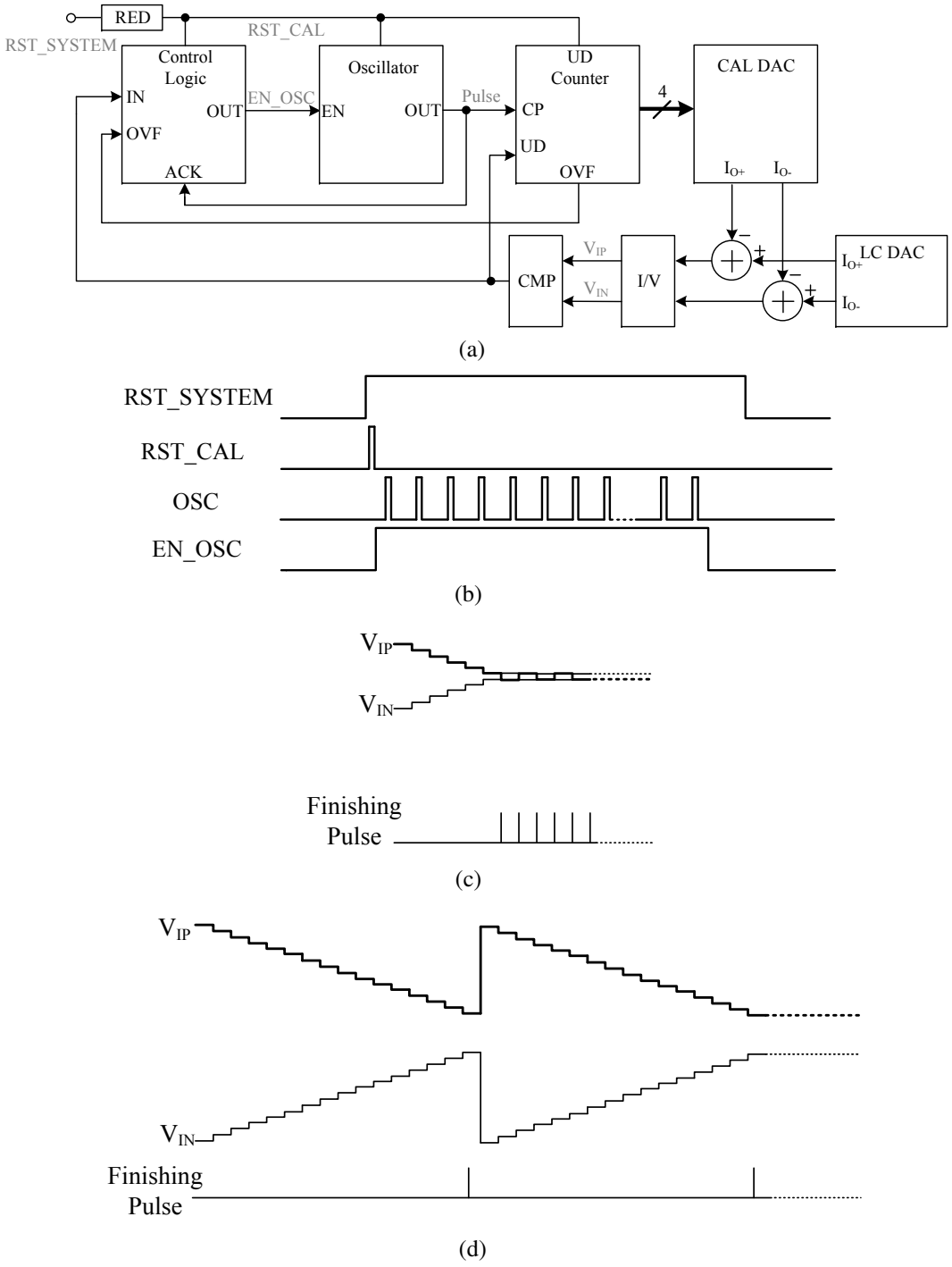


Figure 5.10: (a) Simplified block diagram of the offset calibration. RED denotes the rising edge detector. (b) Example waveforms of the digtal logic control. (c) Example waveforms of the offset calibration. The offset is within the calibration range. $V_{IP}$and V_{IN} denote the comparator input while the finishing pulse is taken from calibration control logic. (d) The offset exceeds the calibration range. Repeated cycles are ignored and depicted by the dotted line to clarify the waveform.

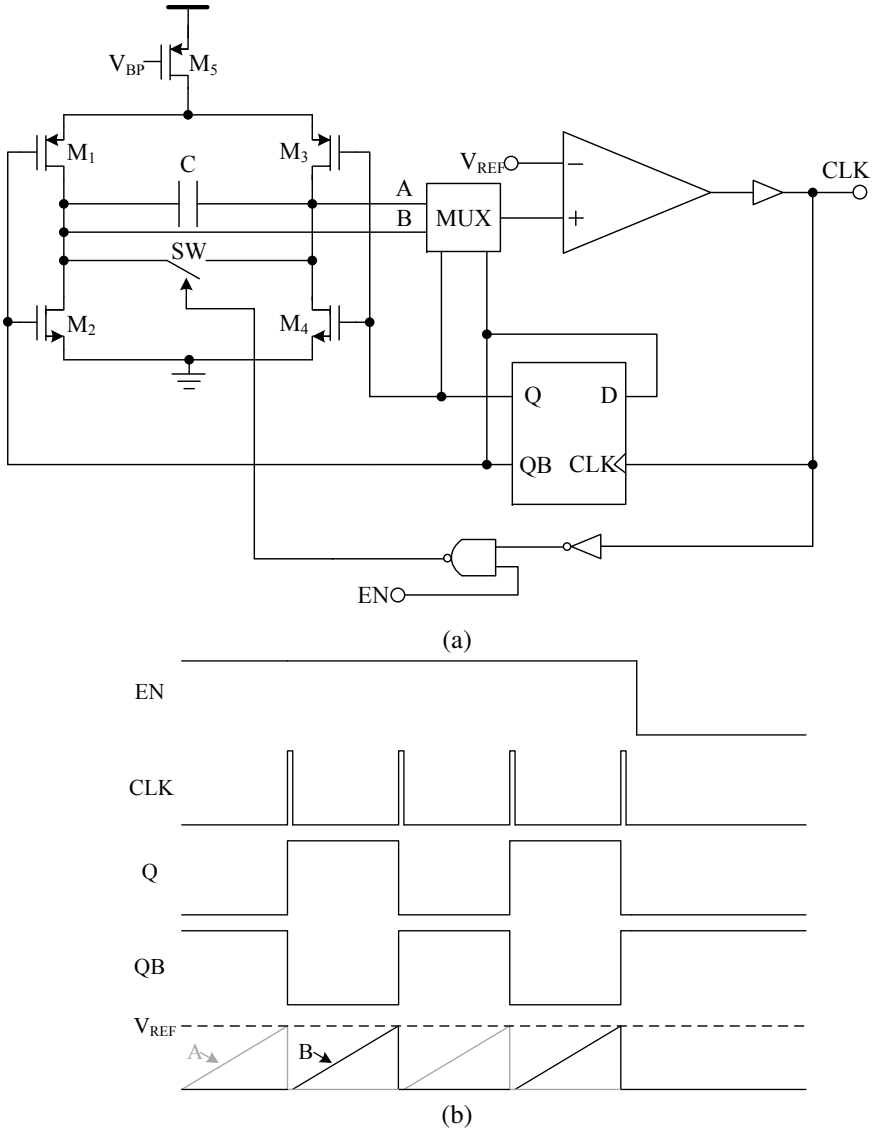


Figure 5.11: (a) Block diagram of the oscillator. (b) Example waveforms of the oscillator.

5.4.5 Oscillator

Since the offset calibration at the system reset requires a clock, an oscillator has been integrated in this recording front-end. As the output voltage of the calibration DAC needs to be settled well after each calibration step (1 LSB), the time interval for each step is preferably long. Furthermore, as an oscillator with a lower oscillation frequency can be designed with lower current consumption, we set the oscillation frequency around 30

Hz, which in turn gives 33mS for the calibration DAC to settle for each calibration step. Note that nonideal factors such as comparator offset, jitter, temperature variation, power supply variation, etc, are not important for this application as the calibration only needs a functional clock.

A simple oscillator with one comparator and one capacitor is proposed in this work. The block diagram of the oscillator is shown in Fig. 5.11 (a). Example waveforms are shown in Fig. 5.11 (b). M_5 is a current mirror output stage providing the charging current for capacitor C. M_1- M_4 work as switches to charge or discharge the capacitor. The feedback loop is formed in such a way that the plate of the capacitor that is being charged is connected by the MUX to the positive terminal of the comparator. Once the MUX output voltage crosses reference voltage V_{REF}, the comparator generates a pulse to make the DFF toggle to reset the loop. The oscillator consumes less than 50 nW and can be enabled by the signal EN.

5.5 Measurements

The proposed ECG recording front-end has been implemented in AMS 0.18 µm HV CMOS technology. The active area is approximately 690×710 μm^2. A microphotograph of the chip is shown in Fig. 5.12. The supply voltage was set to 1 V for all the measurements.

The measured frequency response of the LNA is shown in Fig. 5.13. The high-pass cutoff frequency is around 60 mHz while the low-pass cutoff frequency is approximately 950 Hz. If needed, the low-pass cutoff frequency can be further lowered by external capacitors to reject more noise, as the band of interest for ECG application is up to 500 Hz.

Fig. 5.14 shows the measured input-referred noise power spectrum density (PSD) of the LNA. The input-referred noise integrated from 60 mHz to 950 Hz results in 3.77 µVrms. The noise efficiency factor (NEF) introduced in [37] quantifies the tradeoff among power, noise and bandwidth and is defined by:

$$\text{NEF}=V_{rms,in}\sqrt{\frac{2*I_{TOT}}{\pi*V_T*4kT*BW}} \tag{5.3}$$

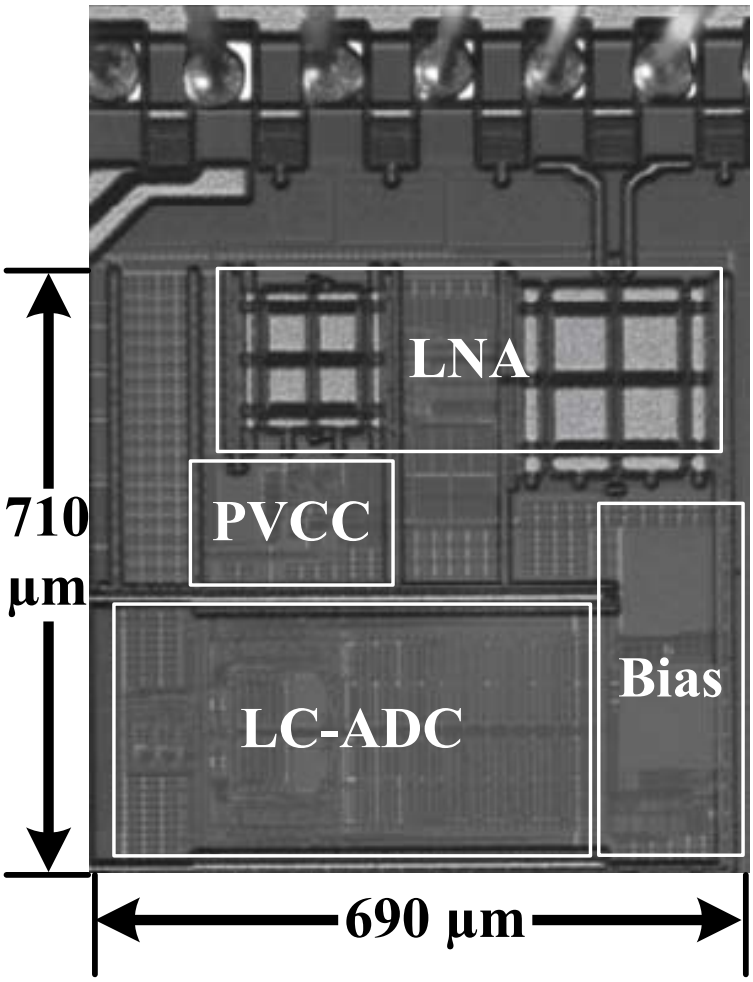


Figure 5.12: Die microphotograph of the ECG readout front-end implemented in a 0.18 µm CMOS process. The core area is 690×710 µm^2.

where $V_{rms,in}$ is the input-referred rms noise voltage, I_{tot} is the total current consumption of the amplifier, and BW is the amplifier bandwidth. The LNA in this work achieves an NEF of 4. In biomedical applications where signal fidelity is important, the THD performance is also critical. Although the maximum input-referred range of the system is 8 mV_{PP}, we applied input sinusoidal signal amplitudes up to 10 mV_{PP} to check the performance of the LNA. The THD at 10mV_{PP} input is 0.15%, which is good enough for the targeted system resolution of 8 bits. The measured THD in turn verifies the performance of the proposed fully balanced pseudo-resistor.

Due to the limited number of pads, we did not leave test pads for measuring the LC-ADC alone in this work. Furthermore, designing an off-chip

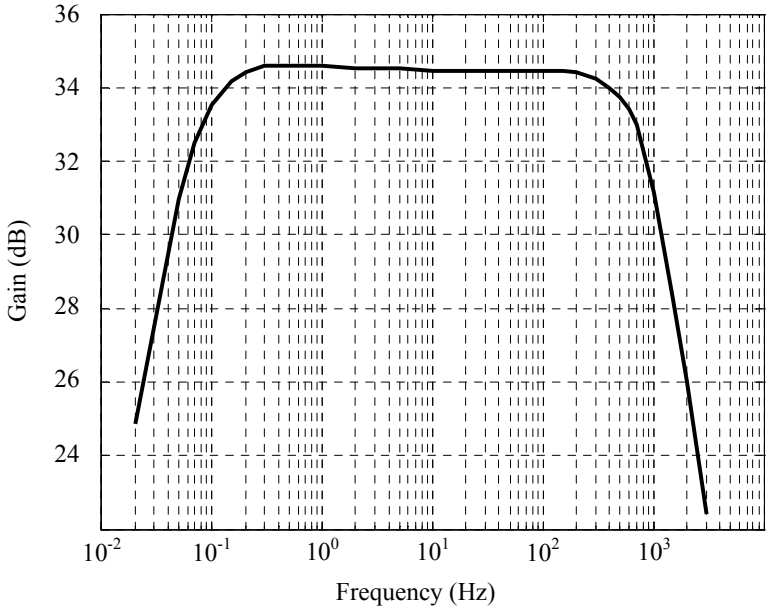


Figure 5.13: Gain-bandwidth measurement of the LNA. The high-pass cutoff frequency is around 60 mHz while the low-pass frequency is approximately 950Hz.

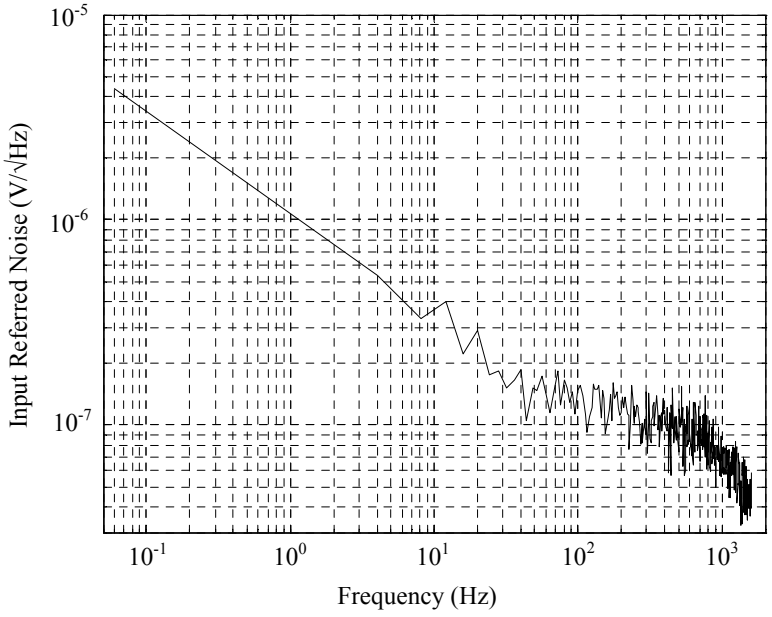


Figure 5.14: Measured input-referred noise voltage PSD of the LNA. Four-time averaging was used during the measurement.

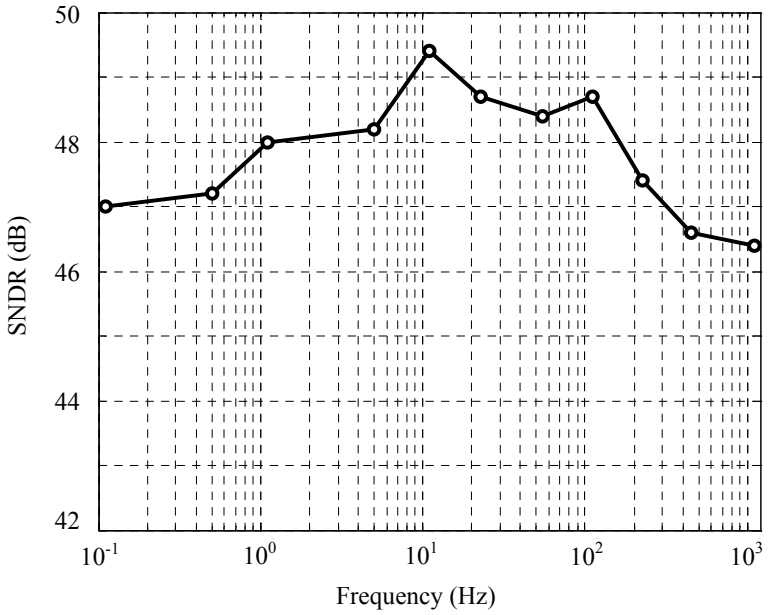


Figure 5.15: SNDR as a function of the input frequency ranging from 0.11 Hz to 1.1 kHz for a 6 mV_{PP} input signal.

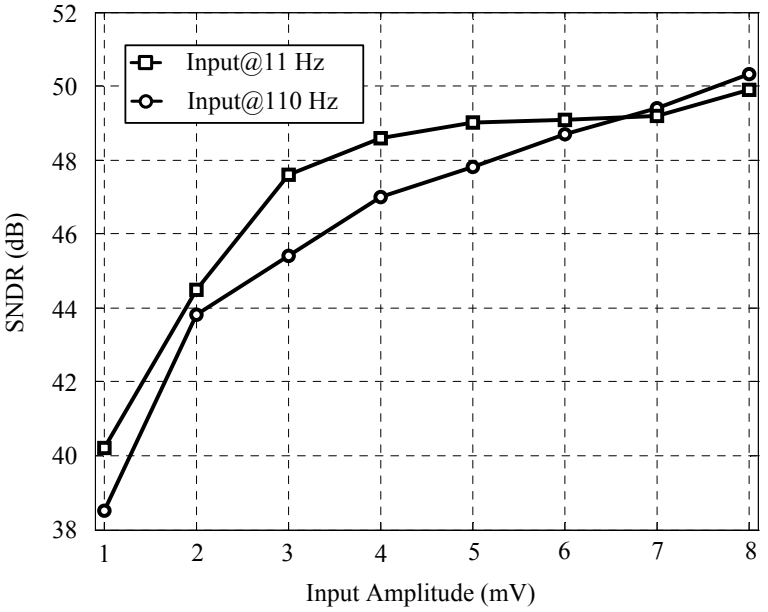


Figure 5.16: SNDR for input amplitudes ranging from 1 mV to 8 mV for input frequencies of 11 Hz and 110 Hz, respectively.

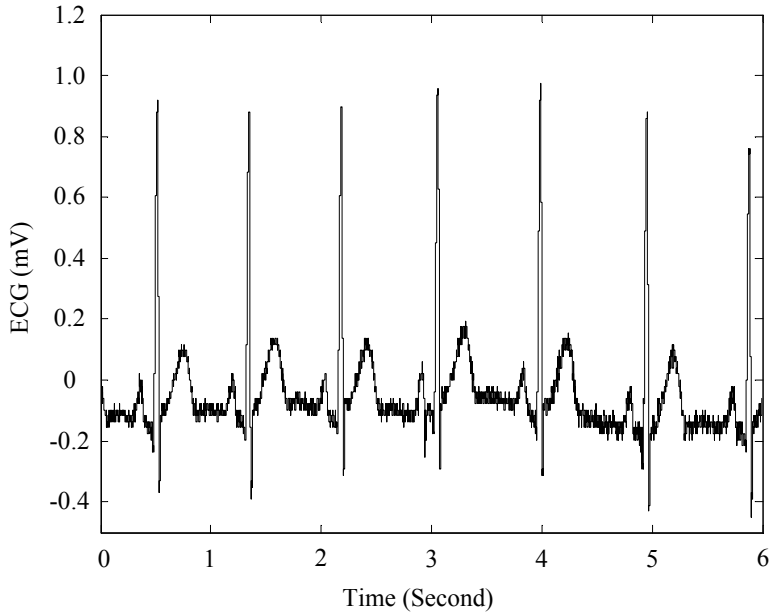


Figure 5.17: Example of a recorded ECG after reconstruction from the acquired digital signal. ECG is acquired by connecting two electrodes to the backsides of the subject's hands and setting the transconductance of the PVCC to 8 nA/mV (R_{TUNE} = 350 kΩ).

current driver complicates the measurements. So the test signals going into the LC-ADC are always from the output of the LNA and the PVCC. In other words, the SNDR we obtained from the LC-ADC output is the SNDR of the whole system. In line with previous works [35, 4], a logic analyzer was used in the measurements to count the time in between the asynchronous samples. Signal reconstruction and interpolation were performed in MATLAB utilizing polynomial interpolation. A fifth order polynomial interpolator was used throughout all the measurements. The SNDR as a function of the input frequency ranging from 0.11 Hz to 1.1 kHz for a 6 mV_{PP} input sinusoid signal has been tested and is shown in Fig. 5.15. The timer was adjusted to work from 5 kS/s to 5 MS/s (i.e. the oversampling ratios are between 980 and 4545) for the entire input frequency range from 0.11 Hz to 1.1 kHz.

The measured SNDR as a function of the input signal dynamic range is shown in Fig. 5.16 for a 11 Hz and a 110 Hz sinusoidal signal. The logic analyzer was set at 50 kS/s and 500 kS/s for the 11 Hz and the 110 Hz input signals, respectively. The input signal range at the input of the LNA

Table 5.1: Performance Summary

Parameter	Value
Technology	0.18 µm
Supply Voltage	1 V
LNA Voltage Gain	34 dB
LNA Input-Referred Noise	3.77 μV_{RMS} (60 mHz-950 Hz)
LNA NEF	4
LNA THD	0.15 % @ 10 mV_{PP} input
LNA CMRR	67dB (@ 50 Hz)
PVCC Transconductance	2/4/8/16 nA/mV
ADC SNDR	46.4 - 50.2 dB
Total Power	8.49 µW@1kHz, 8 mV_{PP} input
Chip Area (active)	690 ×710 μm^2

was from 1 mV to 8 mV.

The fabricated chip was also used to record the ECG signal from a human volunteer to verify proper functioning. A typical three-electrode measurement was performed. The reference electrode was at the right leg of the subject, the other two electrodes were at the back sides of the subject's hands and connected to the differential input of the LNA. The transconductance of the PVCC was set to its second largest one (8 nA/mV). The acquired digital data after reconstruction is shown in Fig. 5.17.

The performance of the proposed system is summarized in Table 5.1. The system achieves better performance than another LC sampling based readout system [5]. The LC sampling system is not yet comparable to standard approaches ([33, 36]) in terms of power. However, the system has some other advantages that conventional systems are not able to offer. The LC sampling system generates fewer samples and thus holds the potential to consume less power in wireless transmission, data storage and computation. Furthermore, the current swing of the current-mode system is not limited by the supply voltage, thus offering larger dynamic range than the voltage-mode system in a low-voltage supply environment. Future work may focus on integration into a wireless system. Processing the data locally for feature extraction (QRS detection [11, 12]) can also

be promising.

5.6 Conclusion

An ECG recording system with level-crossing sampling has been presented in this chapter. A voltage and current mixed-mode system was proposed. The LNA with fully balanced pseudo-resistors provides good linearity. Resolving the input signal further in the current domain allows for a large dynamic range while operating from a low-voltage supply, avoids leakage and offers more design flexibility. The use of a current feedback DAC eases the integration of calibration blocks in the continuous-time domain. The circuit has been designed and fabricated in a 0.18 µm CMOS IC technology. The proposed system is also very suitable for other biomedical applications where the signals are sparse.

Chapter 6

Conclusions and Recommendations for Future Work

In this thesis, the design of standalone level-crossing ADCs and their system integration in a biomedical readout application has been presented. In Chapter 2, various LC-ADCs and related system integrations were classified and discussed. Equipped with the asymmetrical window detection method and the single-bit DAC, a single-ended LC-ADC (Chapter 3) and a differential LC-ADC (Chapter 4) have been implemented. Chapter 5 addressed the issues that are related to the system integration of LC-ADCs and proposed a fully integrated ECG readout front-end with level-crossing sampling. This final chapter will first list the conclusions of the thesis, then list its contributions and finally give suggestions for future work.

6.1 Conclusions

This thesis focuses on the implementation and system integration of level-crossing ADCs. Previously reported standalone LC-ADCs and LC-ADCs based systems have been analyzed and classified from various aspects

(Chapter 2). Based on different application requirements, different design topologies have been proposed in this thesis (Chapter 3 - Chapter 5). An asymmetrical window detection method and a charge-accumulation single-bit DAC have been proposed and implemented in LC-ADCs (Chapter 3 and Chapter 4). The asymmetrical window detection enables the two comparators used in LC-ADCs to consume power more efficiently while keeping the same window detection function without sacrificing performance. The charge-accumulation single-bit DAC is more suitable for LC-ADCs in low-power designs as each conversion only requires to perform charge subtraction and addition by 1 LSB. The single-bit DAC with three branches also relaxes the settling time requirement. The measurement results show that the combination of asymmetrical window detection and a single-bit DAC can reduce the power consumption of LC-ADCs down to a much lower level compared to conventional LC-ADCs. A single-ended single-bit LC-ADC (Chapter 3) and a differential single-bit LC-ADC (Chapter 4), both of them based on asymmetrical window detection, have been implemented successfully, lowering the power consumption from several micro watts (conventional) to sub-micro watt (Chapter 3 and Chapter 4). Compared to other multi-bit LC-ADCs, the proposed single-bit LC-ADCs consume less power and less area while maintaining moderate resolution.

Issues of integrating LC-ADCs into a biomedical readout front-end have been addressed in Chapter 5. A voltage and current mixed-mode system has been proposed. The LNA with fully balanced pseudo-resistors provides good linearity. Resolving the input signal further in the current domain allows for a large dynamic range while operating from a low-voltage supply, avoids leakage and offers more design flexibility for the following LC-ADC. The use of a current-steering DAC eases the integration of the calibration blocks in the feedback loop. The oscillator enables the foreground calibration of the offset at system start-up, resulting in a more robust design. The challenges in the performance of the standalone LC-ADCs and related system integration identified in previous chapters have been addressed by these circuits.

Briefly summarized, the contributions presented in this thesis are:

1. Classification of previously reported LC-ADCs. Summary of the offset calibration and system applications of LC-ADCs. (Chapter 2)

2. The realization of two asymmetrical window detection methods and a charge-accumulation single-bit DAC to improve the power efficiency of LC-ADCs. (Chapter 3 and 4)

3. Integration of a current-mode LC-ADC in a biomedical readout front-end. Realization of a fully balanced pseudo-resistor and handshake based foreground calibration for offset calibration in the continuous-time domain. (Chapter 5)

6.2 Recommendations for Future Work

This thesis has described the implementation and the system integration of LC-ADCs. In this emerging field, several related areas of research can be explored further in the future based on this work.

Due to the charge accumulation, the proposed single-bit LC-ADCs are sensitive to device mismatch. In other words, the injected offset for subtraction can never be exactly equal to the one for addition, resulting in a very small DC drift in the reconstructed signal over time (possibly leading to up/down counter overflow). Future work on single-bit LC-ADCs may focus on introducing a calibrating loop that checks the output digital bits constantly and feeds back the needed offset charge to calibrate the drift. Furthermore, on-chip capacitor calibration for the single-bit DAC can also effectively reduce the drift to an negligible level.

Since biomedical signals are sparse, LC-ADCs that resolve these signals in the charge domain always suffer from charge leakage. The charge leakage can be studied and compensated. A related work for compensating charge leakge can be found in [45]. Although a voltage and current mixed-mode system has been integrated in the biomedical readout front-end (Chapter 5), a pure voltage-mode or current-mode readout system might also be options for such an application in future works. But system-level studies need to be carried out on power consumption, linearity, noise, resolution, etc.

Due to the limited number of pads, the function of the offset calibrating loop can only be measured by counting the pulses from the oscillator.

However, it is worth exploring further as the proposed offset calibration loop is a foreground calibration for continuous-time operation of the basic analog circuit (comparators and amplifiers). For future works, a more comprehensive study of the calibrating accuracy and dynamic range has to be done. Furthermore, the proposed calibration principle can also be applied to other circuits and systems, for instance, a replacement of the (ADPM) in an instrumentation amplifier [46]. The proposed calibrating principle can also be combined with chopping to possibly lower offsets of any system.

Since the proposed ECG readout front-end is a sub-system in a wireless powered ECG sensor node that also embodies an energy harvester, power-management unit and transmitter, more system-level study and simulations need to be carried out to optimize the entire system. Although the data can be transmitted asynchronously, reconstructing the signal at the receiver side while keeping the same accuracy can be difficult. Apart from addressing these technical challenges, the support of industrial standards also plays a key role in the development of wireless event-driven applications.

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Summary

This thesis describes the theory, design and implementation of level-crossing ADCs and their system integration. The goal of this work is to explore methods at both the circuit level and the system level to improve the energy efficiency of LC-ADCs and integrate LC-ADCs in biomedical readout systems. Two single-bit capacitive LC-ADCs and an ECG recording front-end with a multi-bit current-mode LC-ADC are presented to demonstrate the effectiveness of these techniques.

Chapter 1 introduces the background of the thesis topic. The basic knowledge of level-crossing sampling is described. In a wireless sensor node, the system power consumption is usually dominated by the wireless power transmission. Reducing the data size is crucial to save system power consumption under such circumstances. Therefore, a comparison between conventional uniform sampling and level-crossing sampling is made in terms of sampling data size. For low resolution (< 7 bits) in amplitude, LC-ADCs generate fewer samples than uniform-sampling ADCs for various biomedical signals (ECG, EEG, EMG, ECoG). Furthermore, the design challenges and motivation of realizing a level-crossing sampling based readout system are described.

Chapter 2 reviews and analyzes previously reported LC-ADCs from different aspects. Based on various window detection methods and feedback DACs, LC-ADCs are classified into various groups. Advantages and disadvantages of each structure are discussed. Since LC-ADCs work in the continuous-time domain without a clock, conventional offset cancellation topologies are not applicable. Therefore, LC-ADCs with automatic on-chip offset calibration are reviewed. Moreover, LC-ADCs with various system applications are discussed.

Two standalone level-crossing ADCs for biomedical applications are presented in Chapter 3 and Chapter 4, respectively. A single-bit charge accumulation DAC is proposed to save power consumption while relaxing the settling time requirement. Asymmetrical window detection allows the two comparators to consume power more efficiently without sacrificing performance. Innovations at both system level and circuit level pave the way to low-power operation for the LC-ADC. The circuits have been designed and fabricated in AMS 0.18 μm CMOS IC technology. Compared to other LC-ADCs, lower power consumption and less design complexity have been achieved due to the proposed topologies. The event-driven nature makes the proposed ADC very suitable for biomedical applications.

Chapter 5 presents the system integration of an LC-ADC. An ECG recording system with level-crossing sampling is proposed. The system is a voltage and current mixed-mode system. The LNA with fully balanced pseudo-resistors provides good linearity. Resolving the input signal further in the current domain allows for a large dynamic range while operating from a low-voltage supply, avoids leakage and offers more design flexibility. The use of a current feedback DAC eases the integration of calibration blocks in the continuous-time domain. The circuit has been designed and fabricated in a 0.18 μm CMOS IC technology. The proposed system is also very suitable for other biomedical applications where the signals are sparse.

In the final chapter, the thesis is summarized and concluded. The measurement results confirm the effectiveness of the techniques presented in this thesis. Last but not least, possible improvements and research fields that are related to this work are discussed. Suggestions for future work are made.

Samenvatting

Dit proefschrift beschrijft de theorie, het ontwerp en de implementatie van niveau-door kruisende (Eng. 'level-crossing') ADC's en hun systeem-integratie. Het doel van dit werk is methoden op zowel circuit-niveau als systeem-niveau te onderzoeken om de energie-efficiëntie van LC-ADC's te verbeteren en het integreren van LC-ADC's in biomedische uitlees systemen. Twee enkel-bit capacitieve LC-ADC's en een ECG-opname front-end met een multi-bit stroom-dmen LC-ADC zijn gepresenteerd om de effectiviteit van deze technieken te demonstreren.

Hoofdstuk 1 introduceert de achtergrond van het onderwerp van dit proefschrift. De basis-kennis van niveau-kruisend bemonsteren is hier beschreven. In een draadloos sensor-knooppunt wordt het vermogensverbruik van het systeem meestal gedomineerd door de draadloze vermogens-overdracht. Het verminderen van de gegevens-omvang is cruciaal voor het besparen van het vermogensverbruik van het systeem onder dergelijke omstandigheden. Daarom is een vergelijking gemaakt tussen conventioneel uniforme bemonstering en niveau-kruisend bemonsteren in termen van bemonsterings-gegevens-grootte. Voor lage resolutie (< 7 bits) in amplitude genereren, LC-ADC's minder monsters dan uniforme-bemonstering ADC's voor verschillende biomedische signalen (ECG, EEG, EMG, ECoG). Bovendien zijn de ontwerp-uitdagingen en motivatie beschreven.

Hoofdstuk 2 herziet en analyseert de eerder gerapporteerde LC-ADC's vanuit verschillende aspecten. Op basis van verschillende niveau-detectie-methoden en teruggekoppelde DAC's zijn LC-ADC's geclassificeerd in verschillende groepen. De voor- en nadelen van elke structuur zijn besproken. Omdat LC-ADC's werken in het continue-tijdsdomein zonder een klok, zijn conventionele offset-annulerings-topologieën niet toepasbaar. LC-ADC's met automatische on-chip offset-calibratie zijn herzien.

Bovendien zijn LC-ADC's met verschillende systeem-toepassingen besproken. Deze systeem-applicaties tonen een zeer veelbelovende mogelijkheid voor LC-ADC's.

Twee op zichzelf staande niveau-kruisende ADC's voor biomedische toepassingen zijn gepresenteerd in Hoofdstuk 3 en 4, respectievelijk. Een enkel-bit lading-vermeerderings-DAC is voorgesteld om het vermogensverbruik te verminderen en verbetert tegelijkertijd de vereiste inregeltijd (Eng. 'settling time'). Asymmetrische niveau-detectie staat de twee comparators toe om de vermogens-efficiëntie te verbeteren zonder prestatieverlies. Innovaties zowel op systeem-als op circuit-niveau maakt en laag vermogen sverbruik mogelijk voor de LC-ADC. De circuits zijn ontworpen en gefabriceerd in AMS 0.18 μm CMOS IC-technologie. Vergeleken met andere LC-ADC's is er een lager vermogensverbruik en minder ontwerpcomplexiteit bereikt door de voorgestelde topologieën. De voorvalgestuurde (Eng. 'event-driven') eigenschap maakt de voorgestelde ADC zeer geschikt voor biomedische toepassingen.

Hoofdstruk 5 presenteert de systeem-integratie van een LC-ADC. Een ECG uitlees-systeem met niveau-kruisend bemonsteren is voorgesteld. Het systeem is een spanning-en stroom-gecombineerd systeem. De LNA met volledig gebalanceerde pseudo-weerstanden zorgt voor een goede lineariteit. Door het ingangssignaal verder in het stroom-domein te verwerken kan een groot dynamisch bereik gerealiseerd worden met een lage voedingsspanning, kan lekkage voorkomen worden en biedt het meer ontwerp-flexibiliteit. Het gebruik van een stroom-teruggekoppelde DAC vergemakkelijkt de integratie van calibratie blokken in het continue-tijdsdomein. De circuits zijn ontworpen en gefabriceerd in een 0.18 μm CMOS IC-technologie. Het voorgestelde systeem is ook zeer geschikt voor andere biomedische toepassingen waar de signalen schaars zijn.

In het laatste hoofdstuk is het proefschrift samengevat en geconcludeerd. De meetresultaten bevestigen de effectiviteit van de technieken gepresenteerd in dit proefschrift. Ten slotte maar niet ten minste, zijn mogelijke verbeteringen en onderzoeksvelden gerelateerd aan dit werk besproken. Suggesties voor toekomstig werk zijn gemaakt.

List of Abbreviations

ADC **Analog-to-digital converter**

ADPM **Automatic differential-pair matching**

AICs **Analog-to-information converters**

CLC **Consecutive level crossing**

CMOS **Complementary metal–oxide–semiconductor**

CMRR **Common-mode rejection ratio**

CT **Continuous time**

CW **Clocked window**

DAC **Digital-to-analog converter**

DEC **Decrement**

DNL **Differential nonlinearity**

DSP **Digital signal processing**

ECG **Electrocardiogram**

ECoG **Electrocorticography**

EEG **Electroencephalography**

EMG **Electromyography**

ENOB **Effective number of bits**

FoM **Figure of merit**

INC **Increment**

LC **Level crossing**

LNA **Low-noise amplifier**

LSB **Least-significant bit**

MSB **Most-significant bit**

NEF **Noise efficiency factor**

OSR **Oversampling ratio**

OTA **Operational transconductance amplifier**

PGA **Programmable-gain ampifier**

PLL **Phase-lock loop**

PVCC **Programmable voltage-to-current converter**

RED **Rising edge detector**

REQ **Requirement**

RLC **Repeated level crossing**

SAR **Successive approximation register**

SNDR **Signal-to-noise and distortion ratio**

SNR **Signal-to-noise ratio**

THD **Total harmonic distortion**

UD **Up down**

US **Uniform sampling**

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About the Author

Yongjia Li (S'11) was born in Yibin, Sichuan Province, China. He received the B.E. degree from Hebei University of Technology, Tianjin, China, in 2007 and the M.Sc. degree from Southeast University, Nanjing, China, in 2010, both in electrical engineering.

He is currently working towards the Ph.D. degree in the Section Bioelectronics of Delft University of Technology, Delft, The Netherlands. His research interests include low-power sensors for wearable and implantable biomedical applications and power management.

In his spare time, he enjoys running, cycling, playing football, table tennis and guitar. He also likes brewing beer (blond, abbey dubbel, abbey tripel, Wit, imperial stout, IPA).