Level Crossing Analog to Digital Converters

Janamani C. Ayyangalam
08407604

Under the Guidance of

Prof. A. N. Chandorkar

April 28, 2015

Outline

- Motivation
- Theory of level cross sampling scheme
- Reported level crossing ADC architectures
  - Level crossing asynchronous ADC
  - Signal dependent variable resolution ADC
  - Adaptive asynchronous ADC
- Proposed level crossing ADC architectures
  - Architecture for high activity signals
  - Architecture for low activity signals
- Conclusion & Future work
- References

Motivation

" If a function $X(t)$ contains no frequencies higher than B Hz, it is determined by giving its ordinates at a series of points spaced $1/2B$ seconds apart "

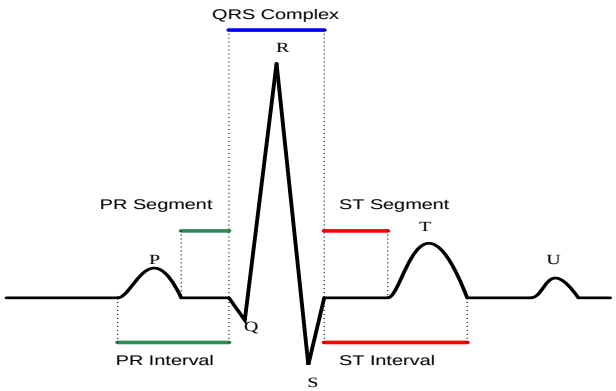
– Nyquist sampling theorem

- Signals have interesting statistical properties.
  - Always constant and may vary during brief moments.
  - Maximum frequency is very high compared to the normal frequency.
- Nyquist signal processing architectures do not take advantage of them.
- Results in a large number of samples without any relevant information.
- Nyquist signal processing architecture should be active all the time.

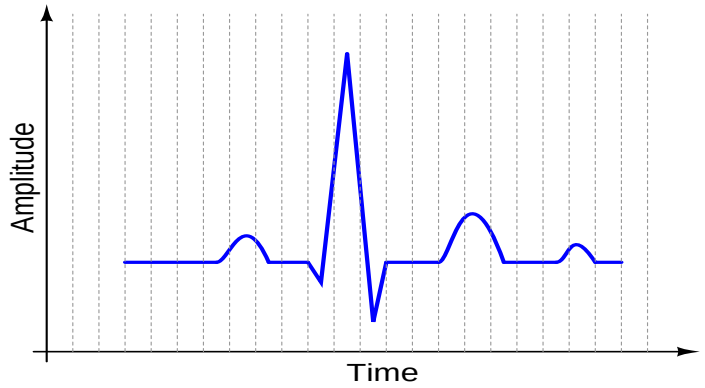
Motivation

Some signals are constant most of the time. For example

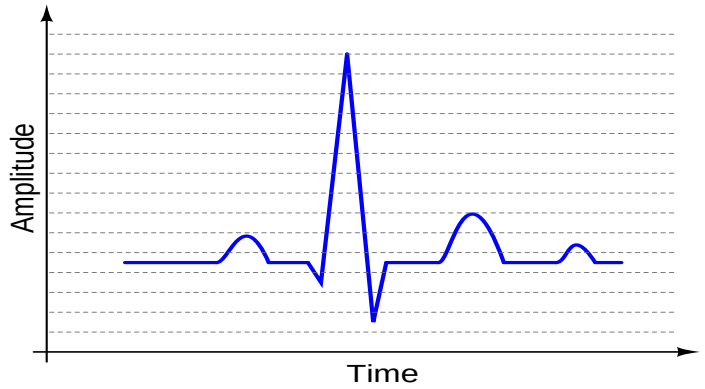
- Signals generated from heart (ECG)
- Signals from temperature sensors
- Signals from pressure sensors etc.,



Electrocardiogram(ECG) signal



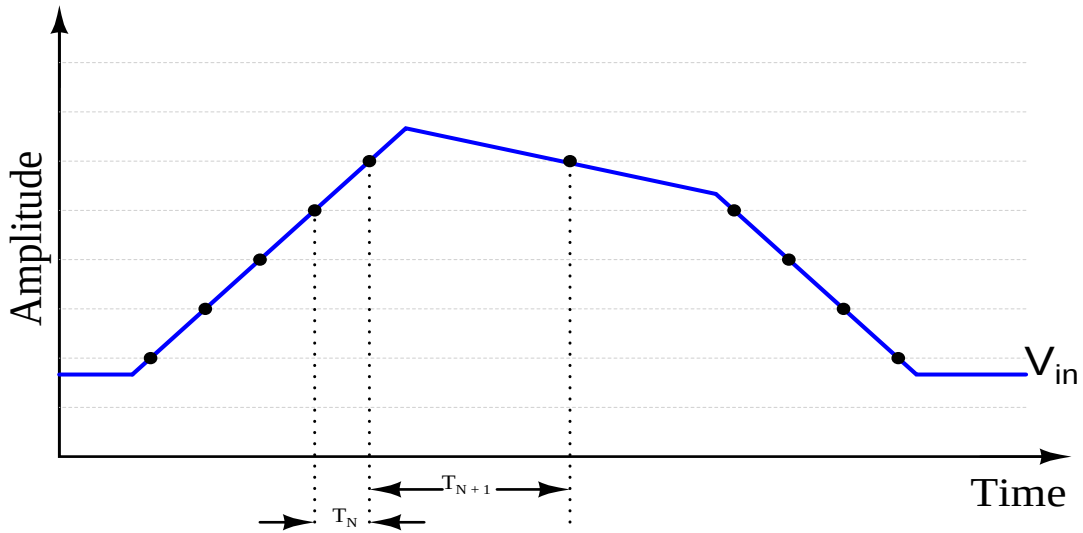
Nyquist sampling for ECG signal



Level cross sampling for ECG signal

Level crossing sampling scheme

- The principle of level crossing sampling is the dual of Nyquist sampling.
- A sample is taken only when V_{in} crosses one of quantization levels.
- It leads to reduction in no of digital samples and activity of the circuit.
- Level cross sampling scheme simplifies design of Asynchronous ADCs.



Level Cross Sampling Scheme

Level cross sampling vs Nyquist sampling

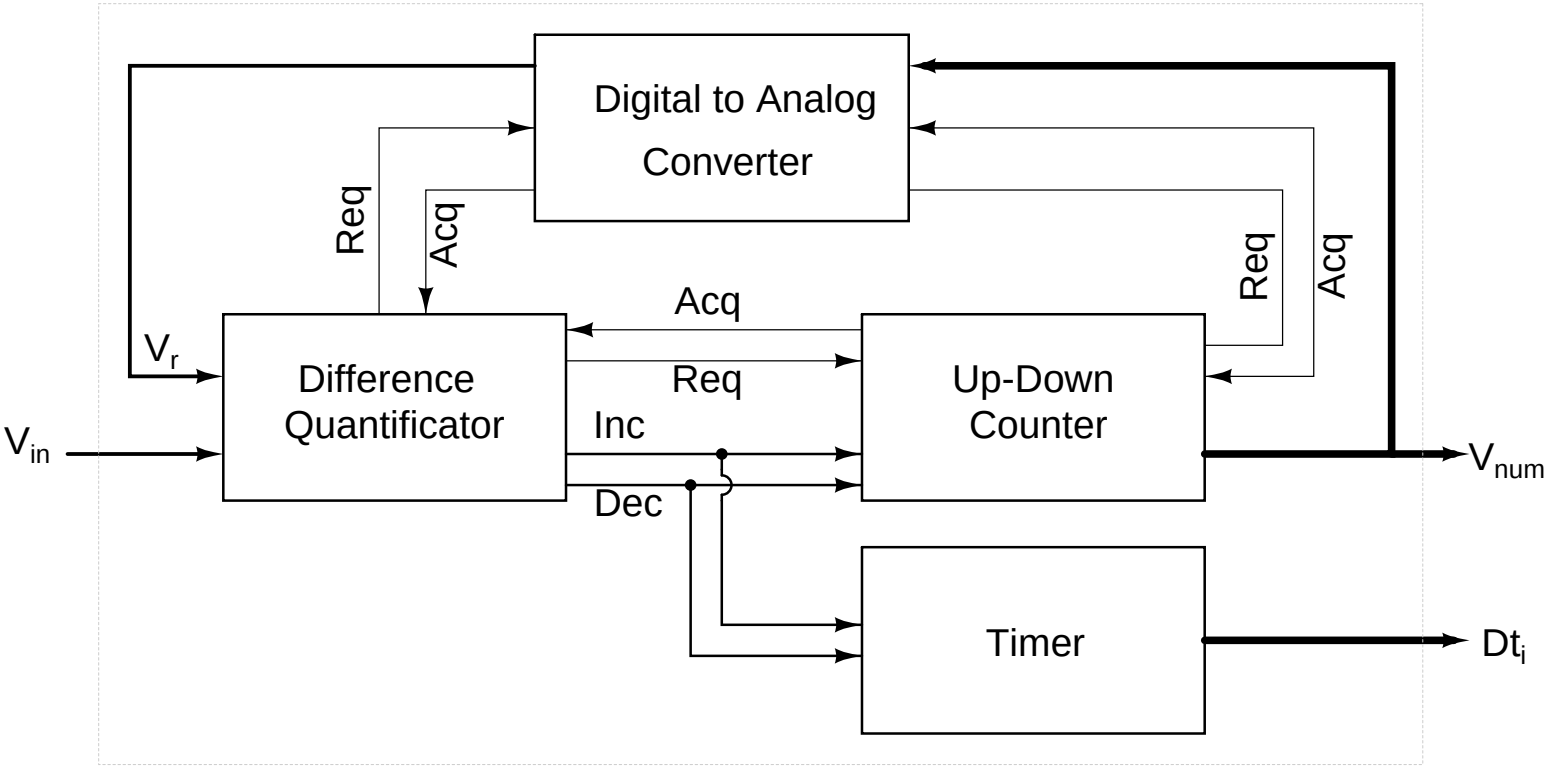
Difference between Nyquist sampling & Level cross sampling schemes

	Nyquist sampling	Level cross sampling
Conversion trigger	Clock	Level crossing
Amplitude	Quantized	Exact value
Time	Exact value	Quantized
SNR dependency	Number of bits	Timer period
Converter output	Amplitude	Amplitude & Time

Advantages of level cross sampling over Nyquist sampling

- Reduction in number of samples from ADC
- Reduction in activity of the ADC circuit

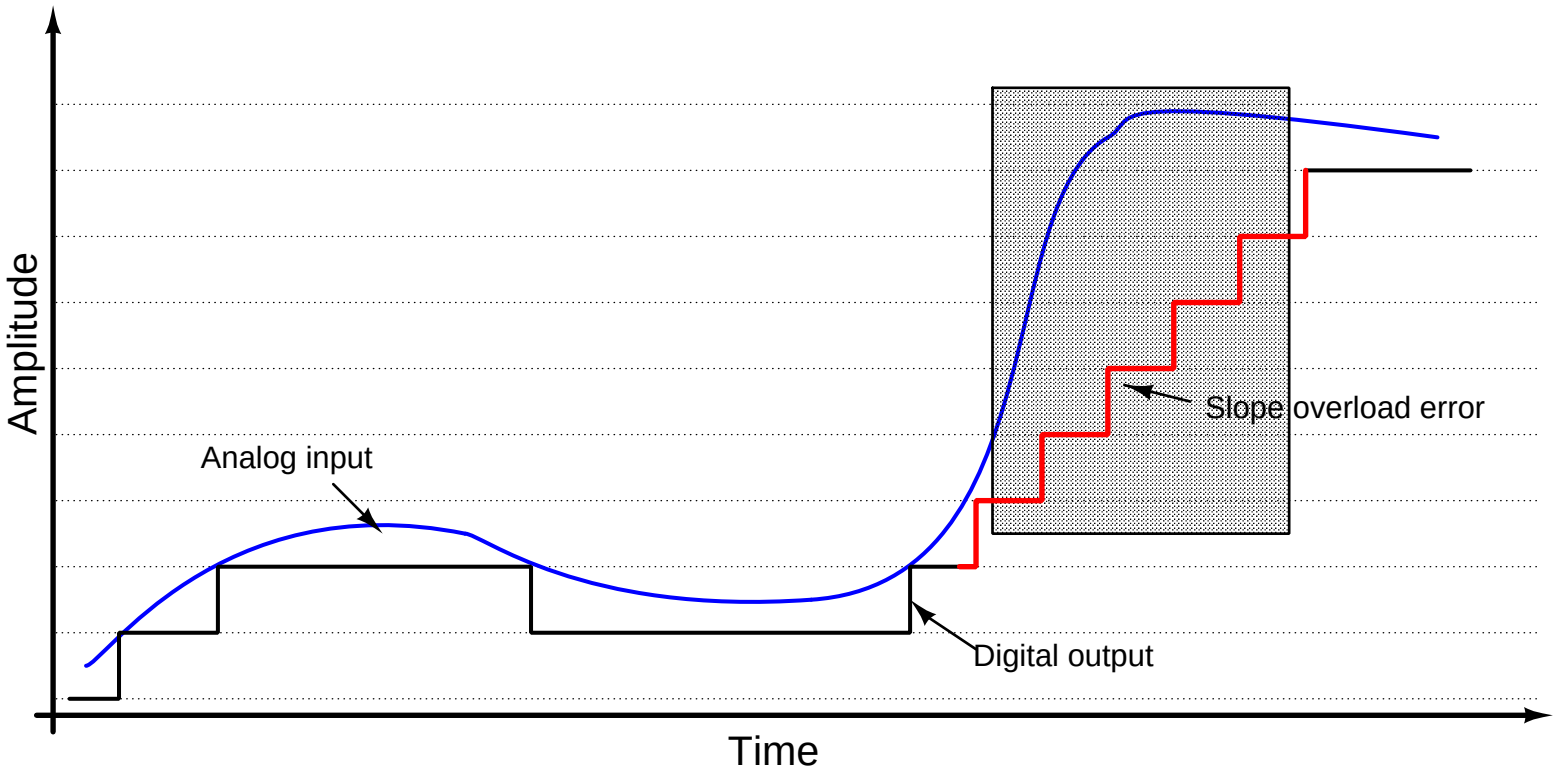
Level crossing asynchronous ADC



Block diagram of the level crossing asynchronous ADC

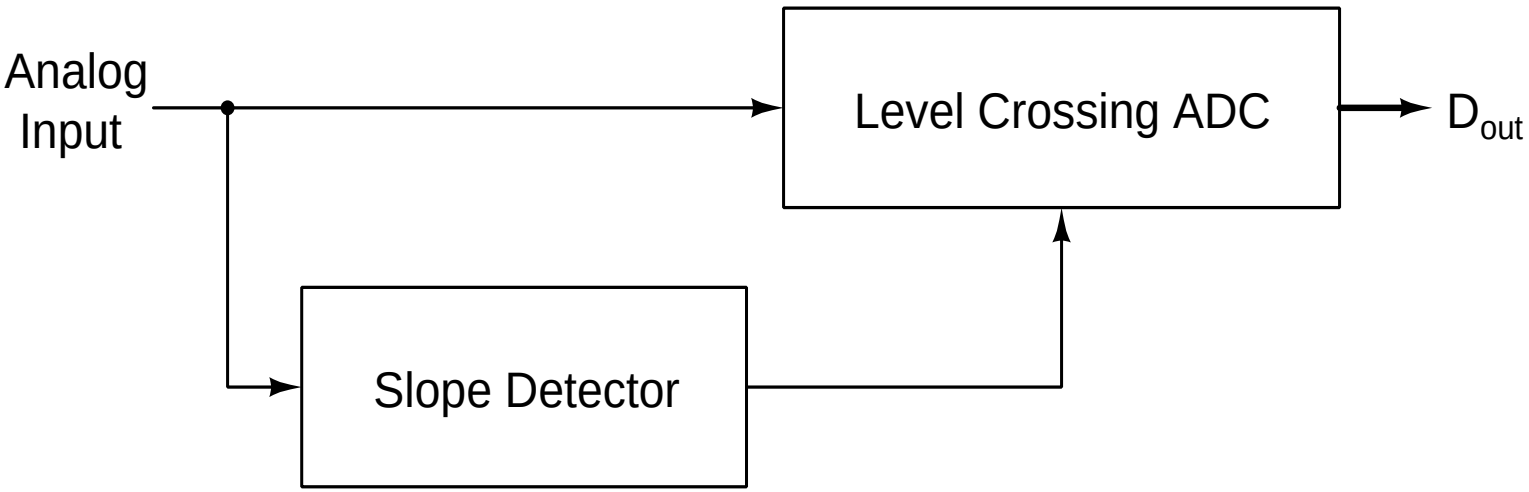
E. Allier et. al "A 120nm low power asynchronous ADC" 2005.

Drawbacks of level crossing asynchronous ADC



Waveform showing slope overload error in level crossing ADC

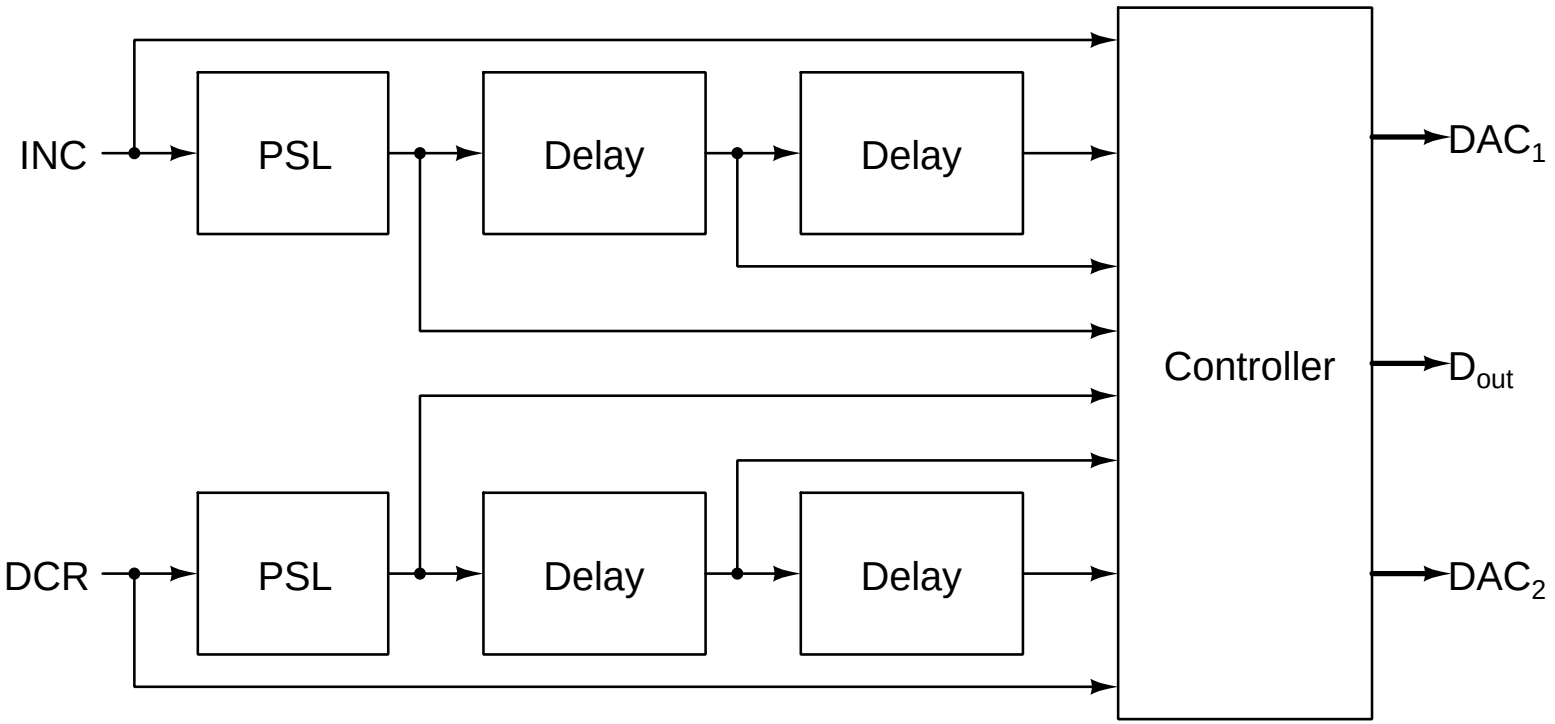
Signal dependent variable resolution ADC



Block diagram of the signal dependent variable resolution ADC

M. Kurchuk et. al "Signal-dependent variable-resolution quantization for continuous-time DSP" 2009.

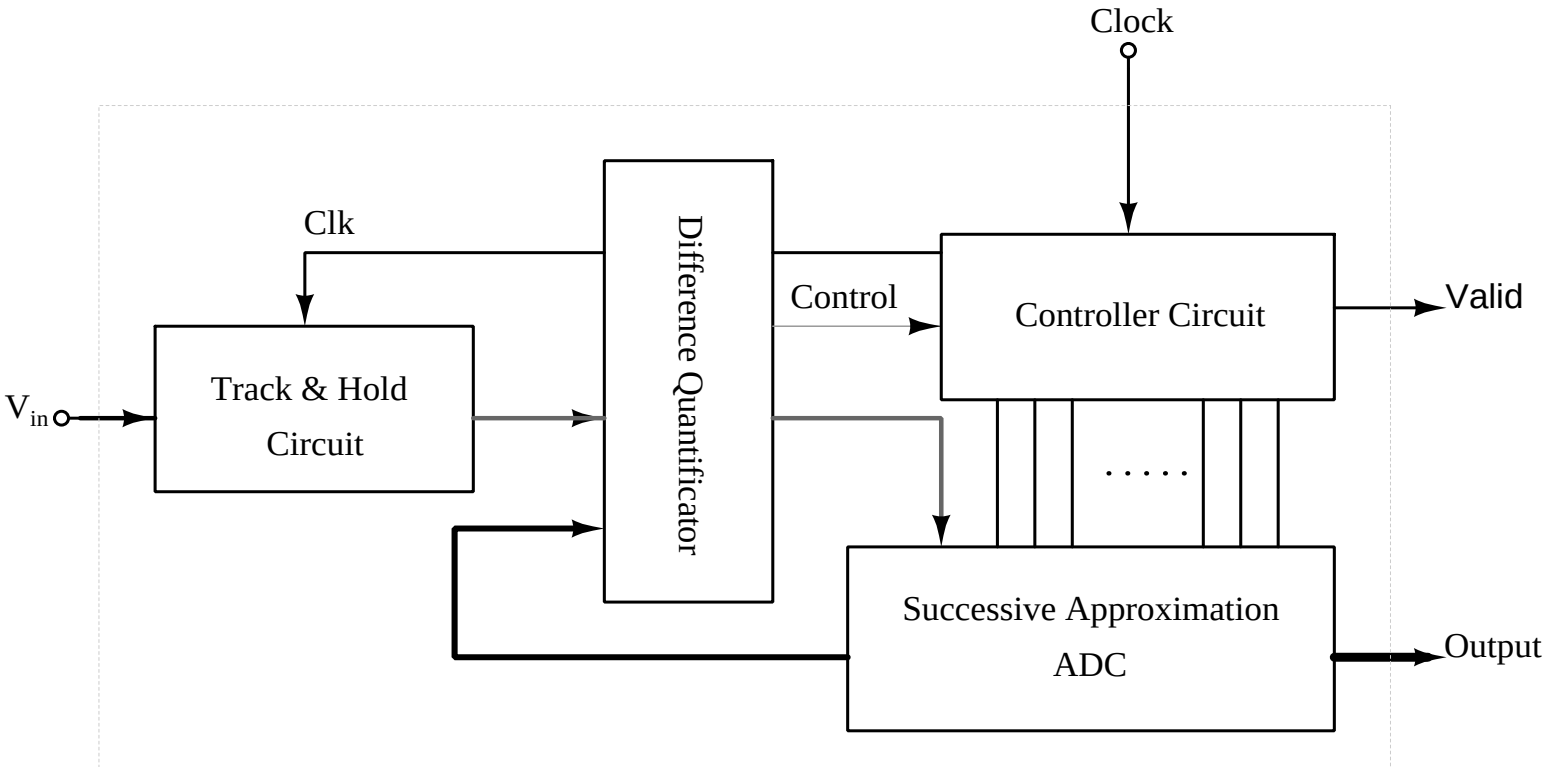
Adaptive asynchronous ADC



Block diagram of the adaptive asynchronous ADC

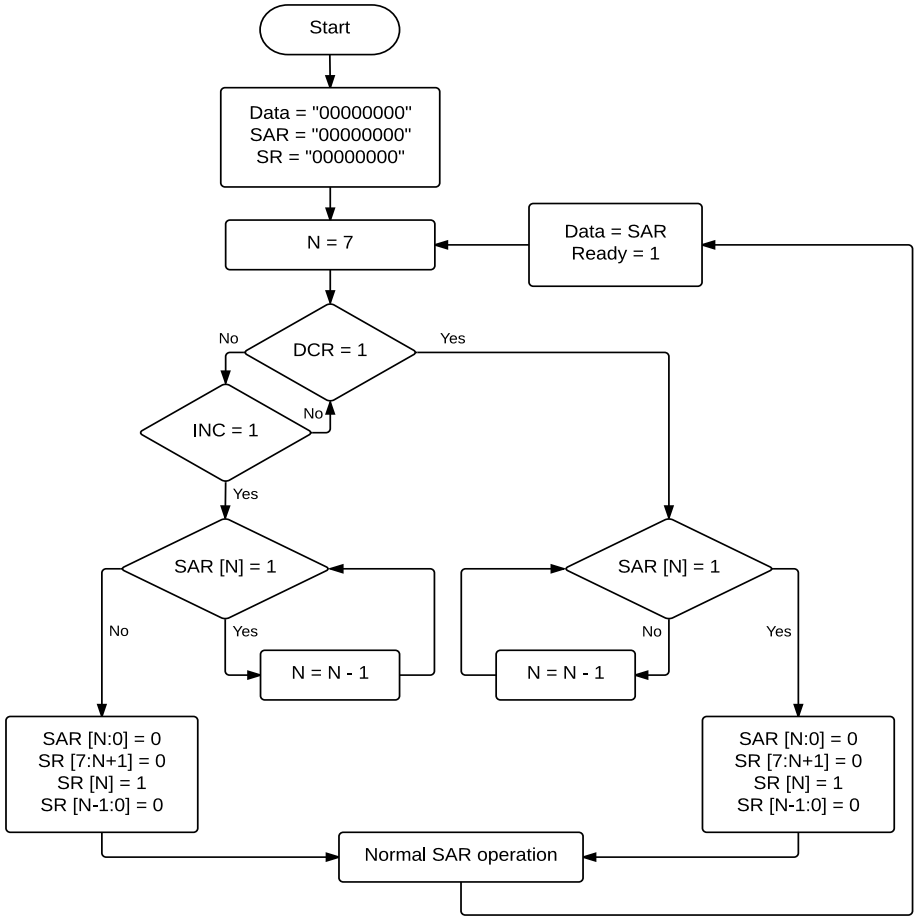
R. Agarwal et. al "Adaptive asynchronous A to D conversion for compressed biomedical sensing" 2009.

Proposed level crossing ADC architecture

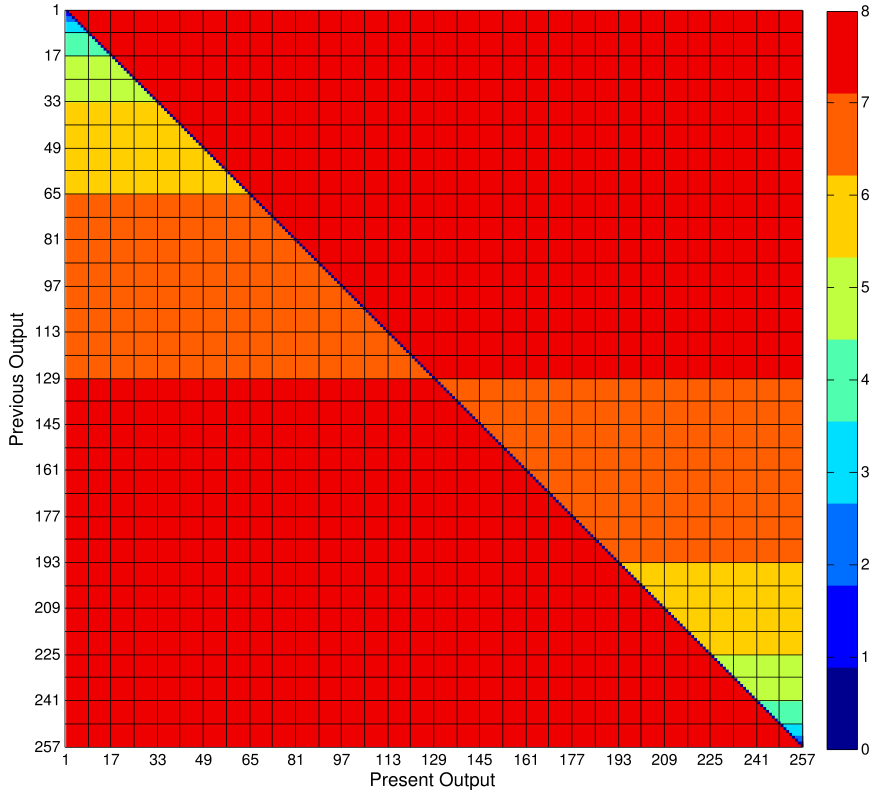


Block diagram of the proposed level crossing ADC architecture

Controller operation for high activity ratio signals

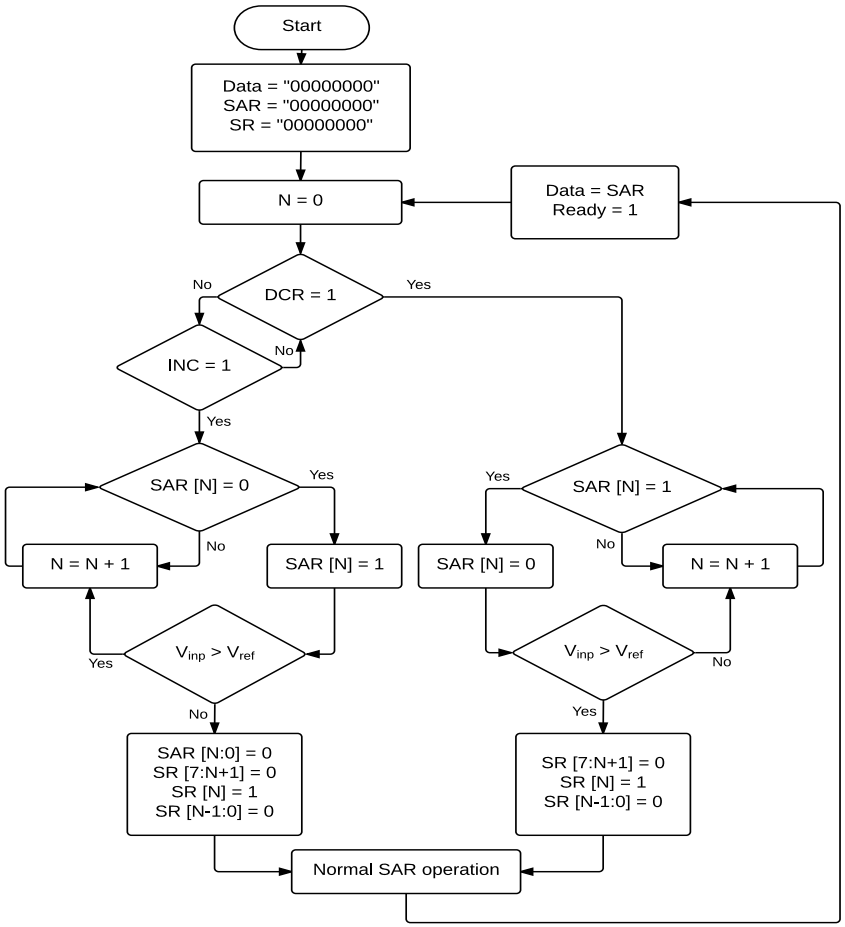


Controller for high activity ratio signals

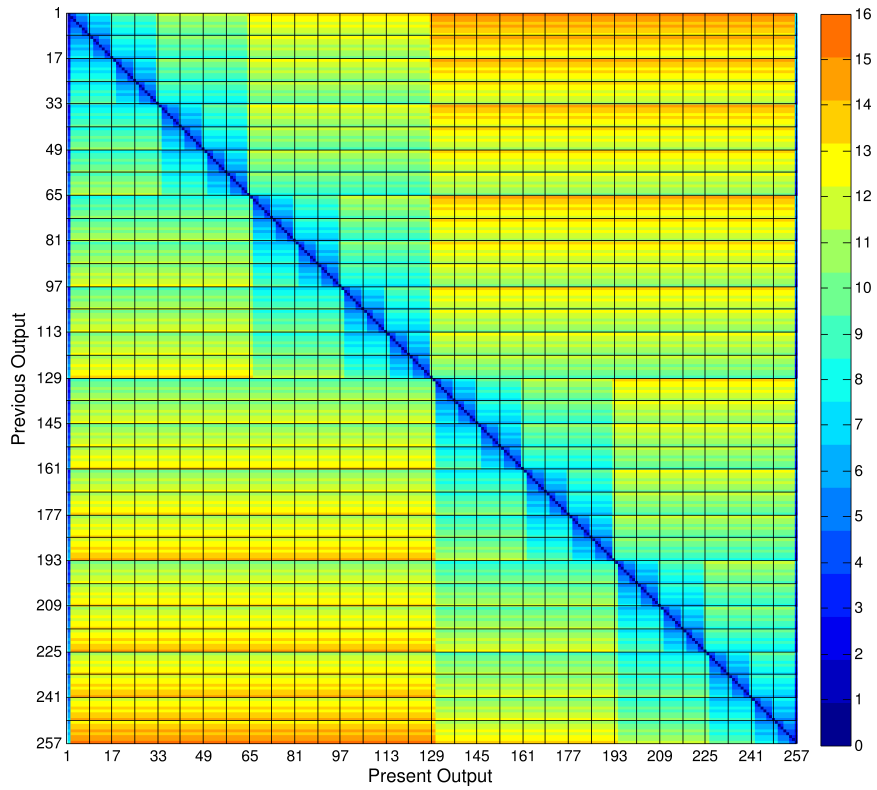


Number of clock cycles needed for conversion

Controller operation for low activity ratio signals

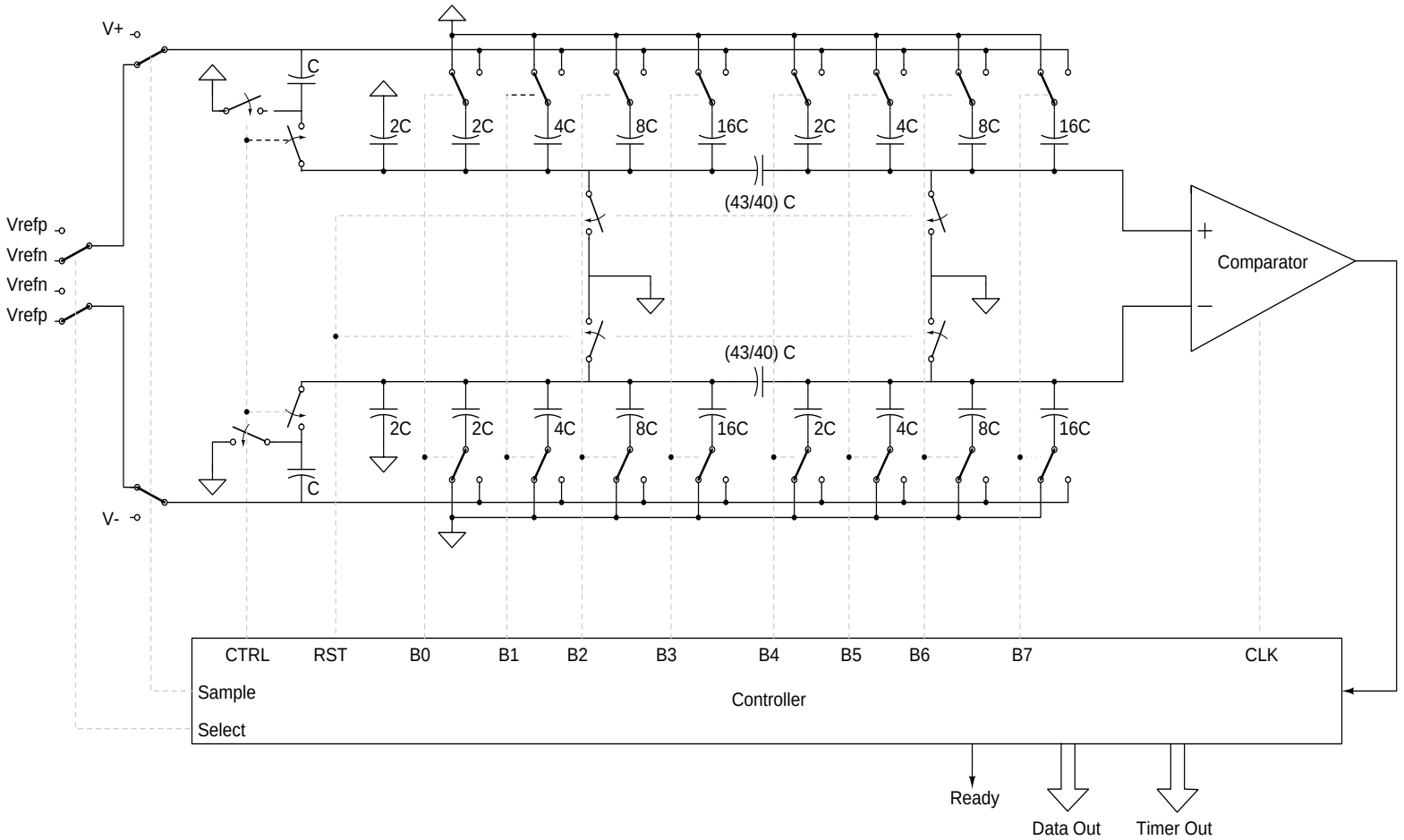


Controller for low activity ratio signals



Number of clock cycles needed for conversion

Circuit diagram of proposed ADC architecture



Proposed level crossing ADC circuit diagram

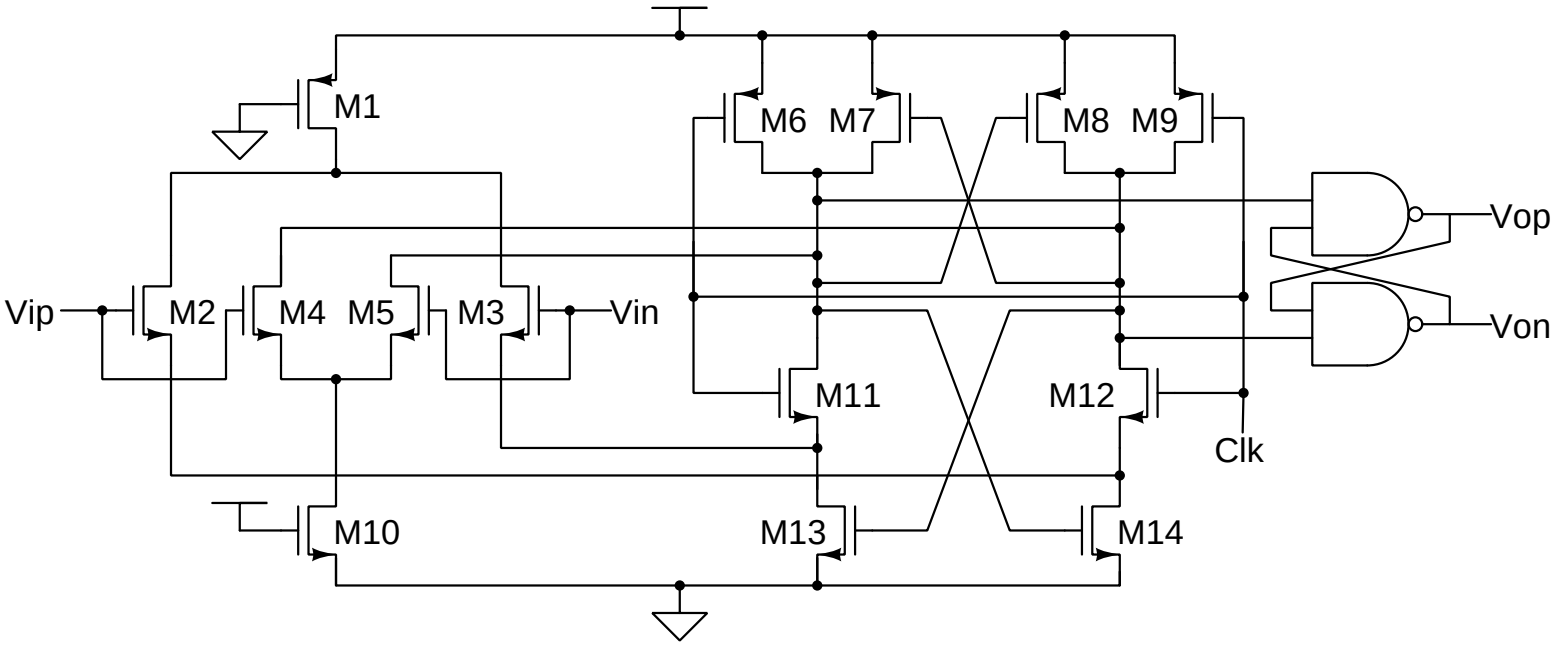
Building blocks for proposed level crossing ADC

- ADC specifications
  - Technology - UMC 180nm
  - Power supply - 1.8 V
  - Resolution - 8-bit
  - Peak to peak analog input voltage - 1 V
  - Maximum analog input frequency - 20K Hz
- Analog Blocks
  - Clocked Comparator
  - Track & Hold
  - Non overlapping clock generator
  - Switching network for capacitor array
  - Capacitor array
- Digital Blocks
  - Controller for high activity signals
  - Controller for low activity signals

Building blocks for proposed level crossing ADC

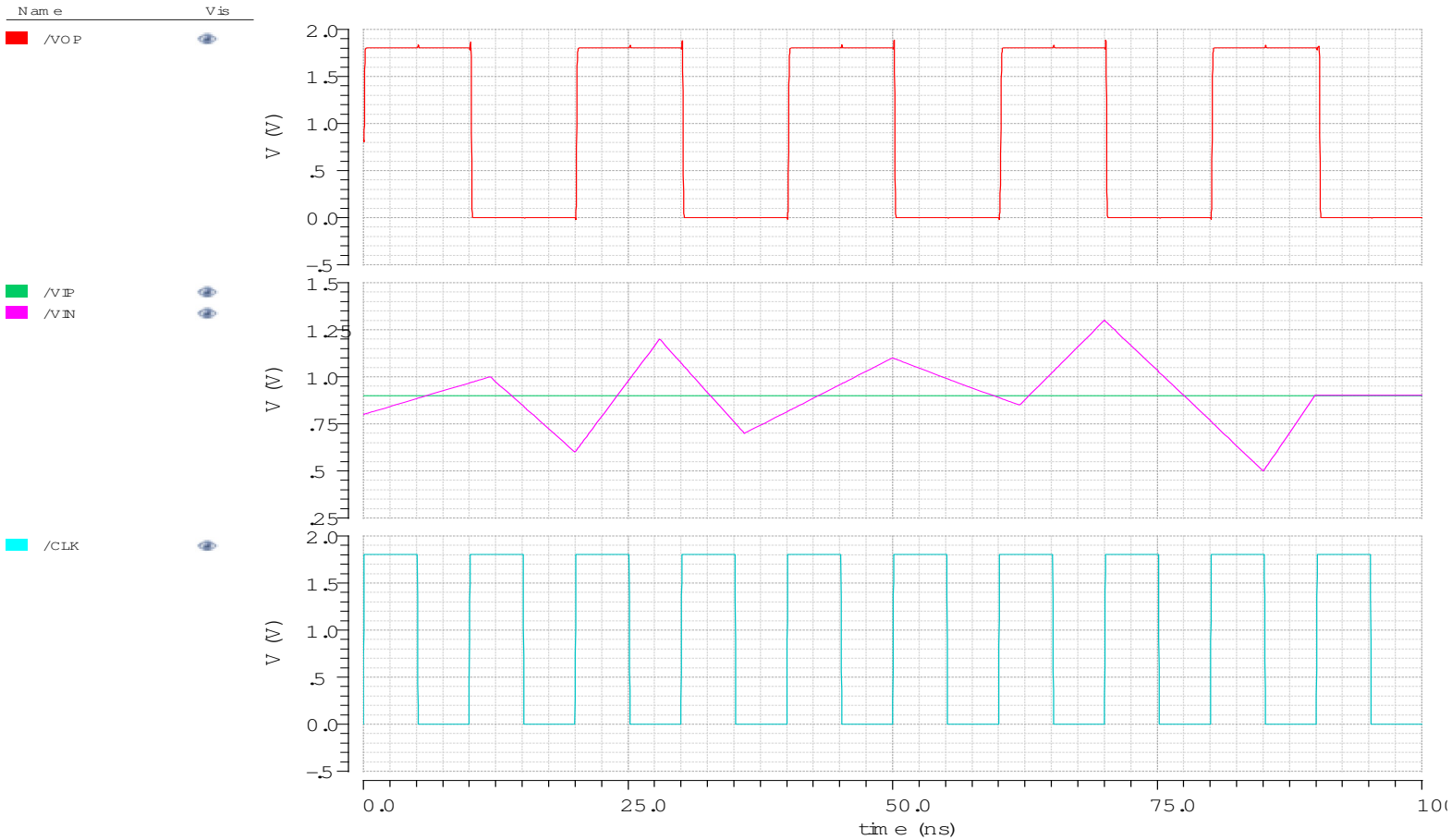
- Capacitor array is implemented using MIM capacitors.
- Switches for Capacitor array are implemented using analog MUX.
- Split capacitor array method is used in Capacitor array for DAC.
- Digital blocks are implemented using Faraday design kit.

Building blocks for proposed level crossing ADC



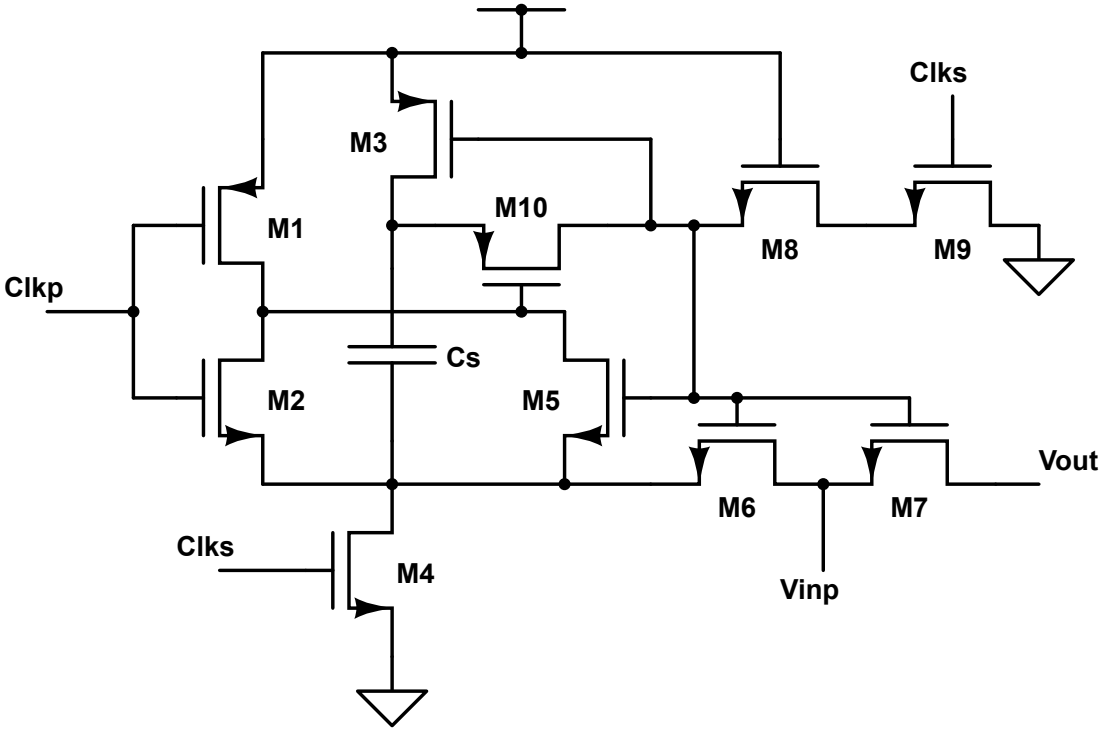
Clocked Comparator used in proposed ADC architecture

Building blocks for proposed level crossing ADC



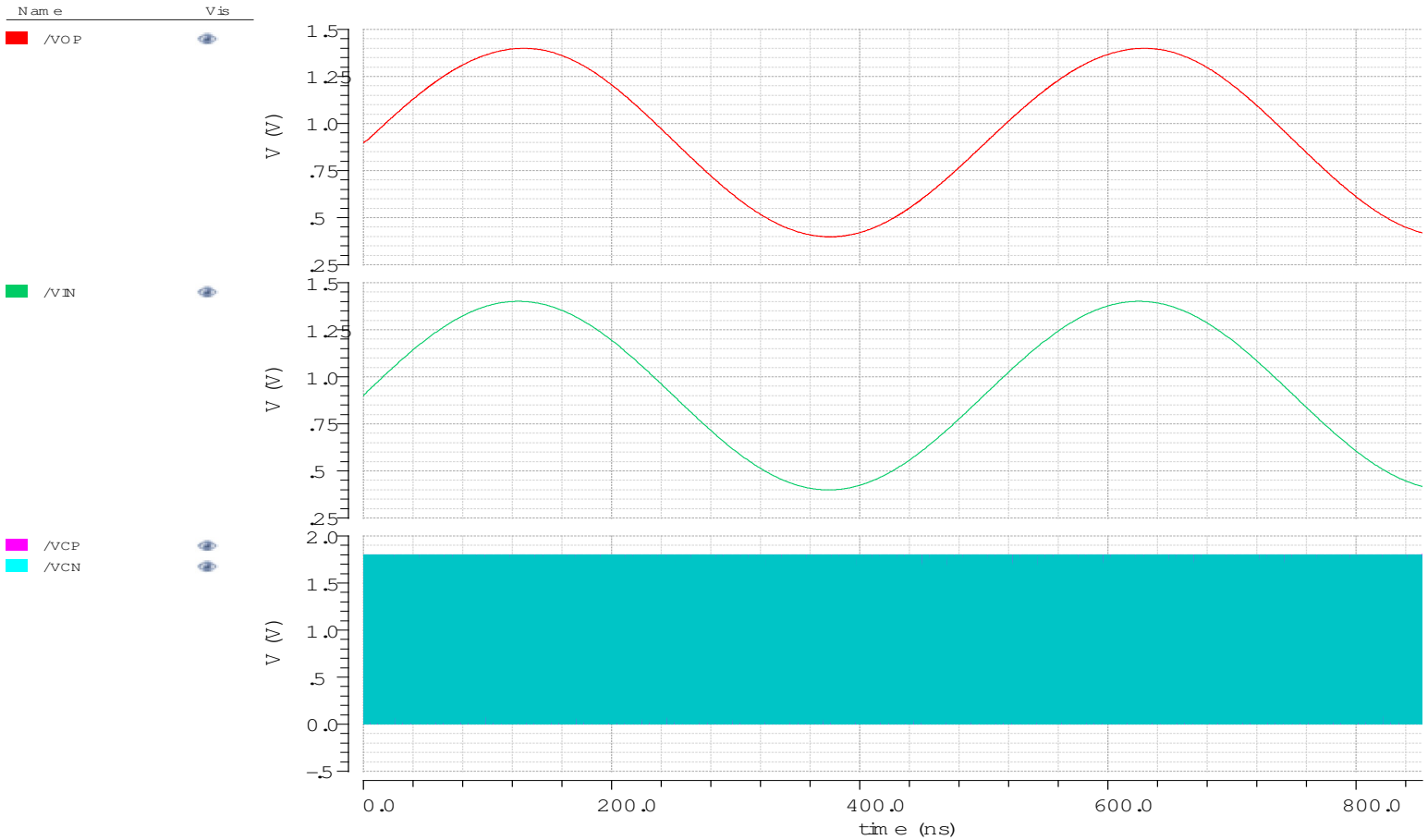
Simulation results of Clocked Comparator used in proposed ADC architecture

Building blocks for proposed level crossing ADC



Track and Hold used in proposed ADC architecture

Building blocks for proposed level crossing ADC



Simulation results of Track and Hold used in proposed ADC architecture

Future work

- Future Work
  - Complete the connections between individual modules.
  - Complete the layout of capacitor array & Switching network.
  - Complete the place & route of controller blocks.
  - Send both designs for tapeouts in August.
  - Modify the proposed architecture for repetitive signals.
- Problems encountered when implementing design
  - Applying Timing constraints for multiple clock domains.
  - Problem with the capacitor layout because of multiplier.
  - Problem with the capacitor layout because of parasitics.

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