A Study of Successive Approximation Registers and Implementation of an Ultra-Low Power 10-bit SAR ADC in 65nm CMOS Technology

Master's thesis performed in
Electronic Devices
by

Raheleh Hedayati

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This thesis work initially investigates and compares different structures of SAR control logics including the conventional structures and the delay line based controller. Additionally, it focuses on selection of suitable dynamic comparator architecture. Based on this analysis, dynamic two-stage comparator is selected due to its energy efficiency and capability of working in low supply voltages. Eventually, based on these studies an ultra-low power 10-bit SAR ADC in 65 nm technology is designed. Simulation results predict that the ADC consumes 12.4nW and achieves an energy efficiency of 14.7fJ/conversion at supply voltage of 1V and sampling frequency of 1kS/s. It has a signal-to-noise-and-distortion (SINAD) ratio of 60.29dB and effective-number-of-bits (ENOB) of 9.72 bits. The ADC is functional down to supply voltage of 0.5V with proper performance and minimal power consumption of 6.28nW.

Keywords
SAR ADC, SAR Logic, Dynamic Comparator, Low Power

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This thesis work initially investigates and compares different structures of SAR control logics including the conventional structures and the delay line based controller. Additionally, it focuses on selection of suitable dynamic comparator architecture. Based on this analysis, dynamic two-stage comparator is selected due to its energy efficiency and capability of working in low supply voltages. Eventually, based on these studies an ultra-low power 10-bit SAR ADC in 65 nm technology is designed. Simulation results predict that the ADC consumes 12.4nW and achieves an energy efficiency of 14.7fJ/conversion at supply voltage of 1V and sampling frequency of 1kS/s. It has a signal-to-noise-and-distortion (SINAD) ratio of 60.29dB and effective-number-of-bits (ENOB) of 9.72 bits. The ADC is functional down to supply voltage of 0.5V with proper performance and minimal power consumption of 6.28nW.

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Abbreviation

ADC	Analog to Digital Converter
BWC	Binary-Weighted Capacitor
DAC	Digital to Analog Converter
DNL	Differential Non Linearity
DFF	Delay type Flip Flop
DL	Delay Line
DR	Dynamic Range
ENOB	Effective Number of Bits
FOM	Figure of Merit
FFT	Fast Fourier Transform
HD	Harmonic Distortion
INL	Integral Non Linearity
LSB	Least Significant Bit
MSB	Most Significant Bit
SAR	Successive Approximation Register
SINAD	Signal to Noise and Distortion Ratio
SFDR	Spurious-Free Dynamic Range
SNR	Signal to Noise Ratio
SHC	Sample and Hold Circuit
TWC	Two-Stage Weighted Capacitor

Contents

Chapter 1
Introduction

Pacemaker is an example of implantable devices for medical application. In this chapter, a concise background about pacemaker and its building blocks are provided. Then, the motivation and organization of this thesis work are presented.

1.1 Background

Pacemakers directly control the pattern and speed of the heartbeat. When the heart stops beating or it beats too slowly, pacemaker provides weak electrical signals with approximately 70 beats per minute to correct the timing of the heart beat [1].

This medical device contains a battery, a generator and pacing leads. The leads connect the pacemaker to the heart and stimulate the heart with the pulses generated in pacemaker. Battery and generator are inside a titanium container which is placed inside the body.

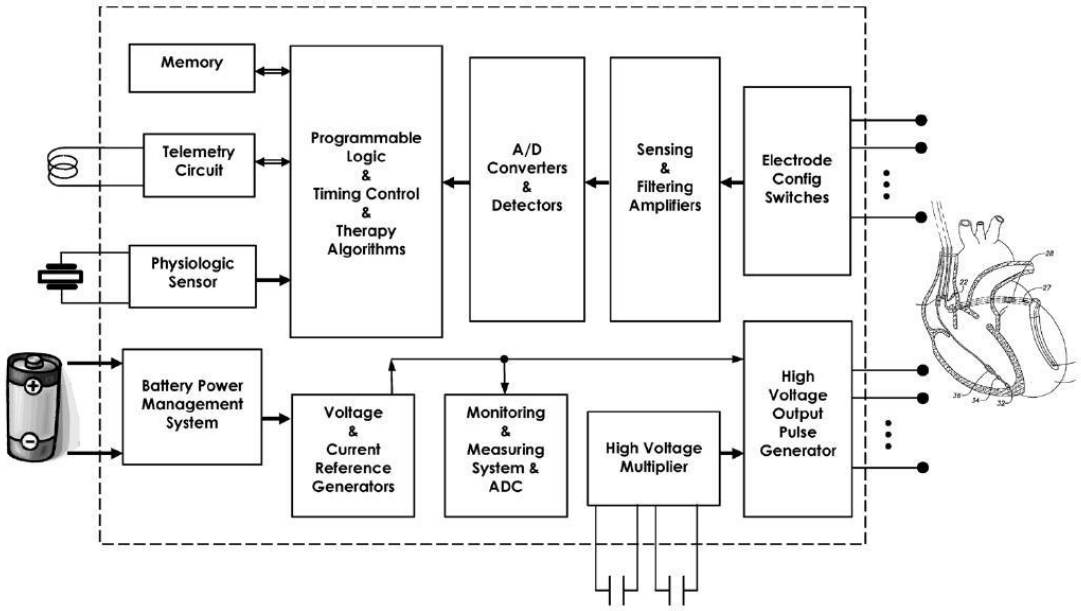


Figure 1.1. Pacemaker functional blocks borrowed from [2]

Figure 1.1 shows the block diagram of a pacemaker. The main blocks fall into four parts [2]:

1) At the input, there are sensing system, amplifier, filter, and analog to digital converter.
2) The digital output of the ADC is fed to the logic block which consists of a programmable logic, timing control system and therapy algorithms.
3) Current and voltage reference generator and battery power management
4) At the output of the pacemaker, high voltage pulse generator and multiplier exist.

1.2 Motivation

The life time of the artificial pacemakers should last up to 10 years which mandate low power consumption per operation [2]. The analog to digital converter is the crucial part of an implantable pacemaker since it consumes a large amount of power as the interface between sensed analog signal and digital signal processor block. Therefore, decreasing the power consumption of the ADC is a major concern.

Low power ADCs with moderate resolution and low sampling frequency is suited for biomedical application. These specifications make SAR ADC the suitable choice. It consumes low power due to its simple structure. Moreover, SAR ADC is scalable with the technology scaling since most parts of the architecture apart from the comparator are digital.

In this thesis, different structures of SAR control logics and dynamic latched comparators are studied; then, a 10-bit SAR ADC is designed and implemented in 65nm CMOS technology. The main target is to design an ultra-low power 10-bit SAR ADC operating at f_s= 1kS/s.

1.3 Thesis outline

In this thesis, Chapter 2 reviews the fundamentals of A/D conversion and performance metrics of A/D converter.
Chapter 3 presents the different architectures of SAR ADC and introduces sub-modules of the SAR ADC.

In chapter 4, various structures of SAR control logic are designed. In the following delay line based SAR controllers are investigated and a comparison in terms of power efficiency is presented.
Chapter 5 reviews the performance metric and types of comparator.
In chapter 6, three different dynamic latch comparators are implemented and a comparison is presented.
Chapter 7 deals with the design of the DAC and implementation of the SAR ADC. Additionally presents the performance evaluation of the designed ADC.
In chapter 8, a concise summary of the thesis work is presented.

Chapter 2

ADC Principles and Performance Metrics

Analog to digital converters are the interface between the analog input signal and digital signal processing block. In this chapter, analog to digital conversion principles are briefly reviewed. In the following, the static and dynamic performance metrics are presented.

2.1 Analog to Digital Conversion fundamentals

2.1.1 Resolution

The number of bits at the output of ADC is called resolution. V_{LSB} is the smallest step that can be detected which is equal to $\frac{V_{REF}}{2^N}$ for an N bit ADC. However in reality the effective resolution is lower than N bits due to different error sources [3].

2.1.2 Quantization Error

In an A/D converter, when the analog input data is quantized to a finite number of steps, quantization error occurs. The maximum quantization error is $\frac{V_{LSB}}{2}$. This phenomenon even takes place in an ideal ADC. Assuming that the quantization error is uncorrelated, it can be modeled as white noise.

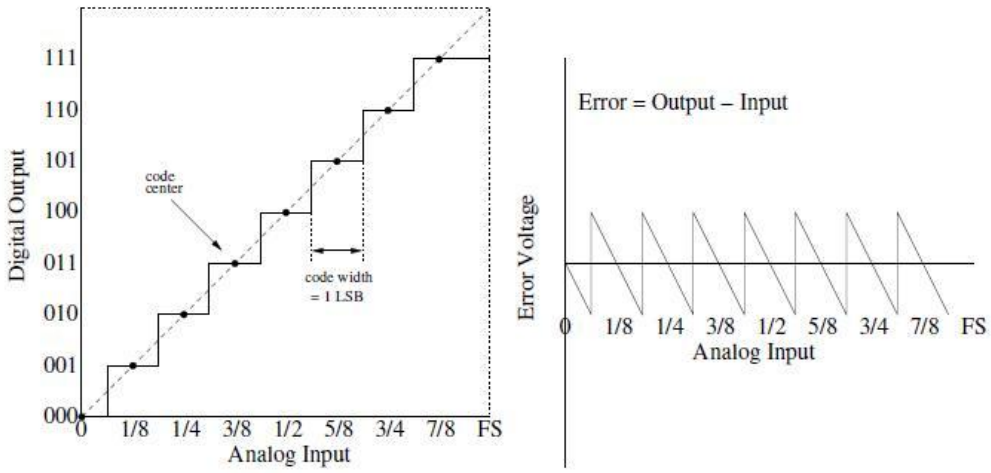


Figure 2.1. Quantization error of an ideal ADC, borrowed from [4]

2.2 Static Performance

2.2.1 Offset and Full Scale Error

Offset error is the deviation of code transition voltage at first step from the ideal one which is $\frac{LSB}{2}$. Full scale error is the deviation of the last code transition voltage from the ideal one. These errors are shown in Figure 2.2.

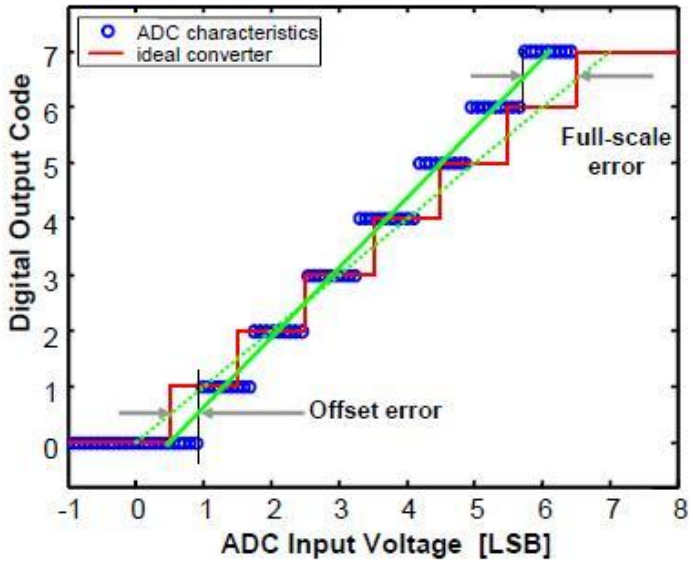


Figure 2.2. Offset and full scale error, borrowed from [5]

2.2.2 Differential Nonlinearity

Deviation of the code transition width from the ideal one (1 LSB) is called differential nonlinearity (DNL). For narrow code width, DNL is negative while for the wide one DNL is positive. In an ideal ADC the code width is always one, thus, DNL is zero.

2.2.3 Integral Nonlinearity

Integral nonlinearity (INL) is the difference between the code centers from the ideal line. INL can also be specified as the sum of DNLs [5]. Additionally, INL can be defined as the distance of the code centers with the best fit line. Figure 2.4 depicts the maximum INL which is measured with the ideal one.

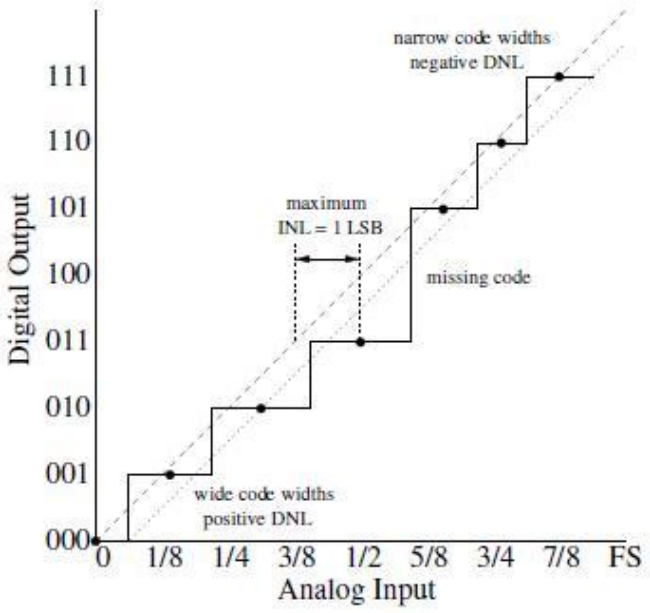


Figure 2.4. DNL and maximum INL, borrowed from [4]

2.2.4 Missing Code

When a digital code at the ADC output is not produced for the corresponding input voltage, there is a missing code. An example of missing code is illustrated in Figure 2.4. Whenever there is a missing code DNL is -1.

2.3 Dynamic Performance

2.3.1 Signal-to-Noise Ratio

Signal to Noise ratio (SNR) is the ratio of the input signal power over the total noise power.

$$SNR = 10.\log_{10}\frac{P_S}{P_N} \tag{2.2}$$

In an ideal ADC the only noise source is the quantization error.

$$P_S = V_{in\_max}^2 = (\frac{2^N.V_{LSB}}{2\sqrt{2}})^2 \tag{2.3}$$

$$P_N = V_{error}^2 = (\frac{V_{LSB}}{\sqrt{12}})^2 \tag{2.4}$$

By inserting P_S and P_N into Equation 2.2 SNR of an ideal ADC is expressed as below:

$$SNR = 20.\log_{10}\frac{\frac{2^N.V_{LSB}}{2\sqrt{2}}}{\frac{V_{LSB}}{\sqrt{12}}} = 6.02N + 1.76 \tag{2.5}$$

2.3.2 Spurious-Free Dynamic Range

Spurious-Free Dynamic Range (SFDR) is defined as the ratio of the input signal to the largest peak of spur or harmonic distortion tone. SFDR is presented mathematically in Equation 2.6.

$$SFDR = 20.\log_{10}\frac{V_{Signal}}{V_{Spurious}} \tag{2.6}$$

2.3.3 Signal-to-Noise-and-Distortion Ratio

Signal-to-Noise-and-Distortion Ratio (SINAD) is the value of the input signal over the sum of the total noise and harmonic components. Equation 2.7 indicates the SINAD mathematically.

$$SINAD = 20.\log_{10}\frac{V_{Signal}}{V_{Noise}+V_{HD}} \tag{2.7}$$

2.3.4 Effective Number of Bits

Effective Number of Bits (ENOB) is obtained from SINAD. ENOB is commonly used instead of SINAD, since it presents SINAD in the number of bits. ENOB is achieved using Equation 2.5.

$$ENOB = \frac{(SINAD - 1.76)\ dB}{6.02\ dB} \tag{2.8}$$

Chapter 3
Successive Approximation Register ADC

This chapter presents a literature review of SAR ADC. First, successive approximation algorithm is explained and different architectures of SAR ADC are investigated. In the following, the operations of the sub-modules of the SAR ADC are described.

3.1 Successive Approximation Algorithm

Successive Approximation Register ADC is a proper choice for low power applications. SAR ADC employs a successive approximation algorithm to convert analog input to a digital code successively. In other words, one bit is determined in each clock cycle using binary search algorithm.

In order to investigate the operation of the SAR ADC, consider a 4 bit ADC. As shown in Figure 3.1, in the first clock cycle DAC voltage is set to half of V_{ref} by setting the code to 1000, then the input voltage is compared to $\frac{V_{ref}}{2}$ and based on the comparison result, MSB is defined. If $V_{in} > \frac{V_{ref}}{2}$ the MSB will not be changed and will remain at one, otherwise the MSB is reset to zero. So here MSB (D3) remains at one. In the next clock cycle the DAC input is set to 1100 and again V_{in} is compared to $\frac{3V_{ref}}{4}$. D2 retains its value since $V_{in} > \frac{3V_{ref}}{4}$. For the next bit the DAC input is set to 1110. Based on comparison, D1 is reset to zero since $V_{in} < \frac{7V_{ref}}{8}$ and finally for defining LSB, the DAC input is set to 1101. D0 is one because $V_{in} > \frac{13V_{ref}}{16}$. Therefore, the analog input is converted to the digital code 1101 in four clock cycles.

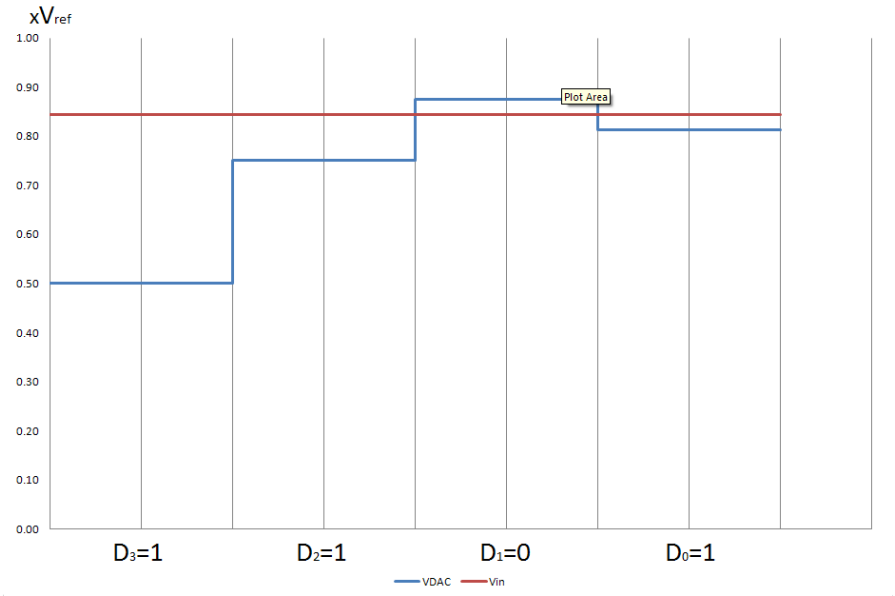


Figure 3.1. 4-bit SAR ADC operation

3.2 Two Different Architectures of SAR ADC

3.2.1 Separate DAC and Sample and Hold Circuit

Figure 3.2 illustrates the block diagram of a SAR ADC including a sample and hold circuit which is a common architecture for SAR ADC. In this configuration, the comparator offset voltage can be modeled as a voltage source in series combination with the output of the sample-and-hold circuit which implies the addition of the offset to the analog input. As a result, an offset appears in the overall characteristic. Therefore, the linearity of the A/D converter is not affected by the comparator offset voltage [6]. The drawback of this approach is that it consumes high power due to separate S/H circuit.

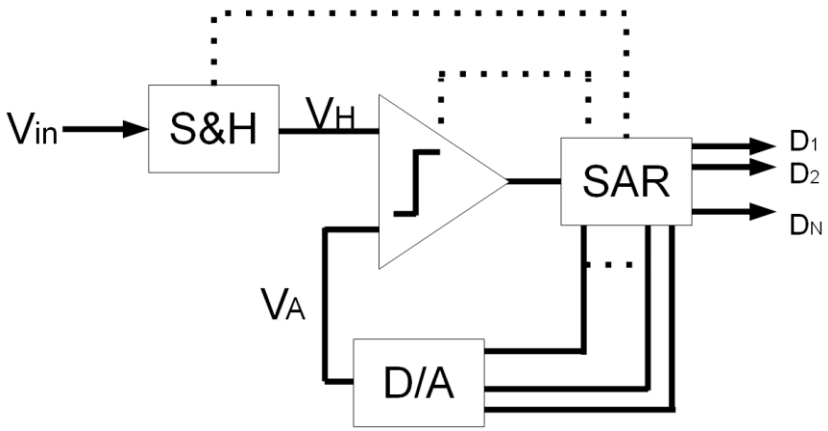


Figure 3.2. SAR ADC architecture

3.2.2 Charge Redistribution Architecture

This architecture encompasses a capacitive DAC which also operates as a sample and hold. The block diagram of the charge redistribution SAR ADC is illustrated in Figure 3.3. The D/A converter usually contains a binary-weighted capacitor array. In each conversion, first the analog input is sampled and stored in the capacitor array and then the output of the DAC is compared to V_{CM} for N clock cycle. The output of the DAC successively follows the V_{CM} voltage at the comparator's input and reaches V_{CM} at the end of each conversion.

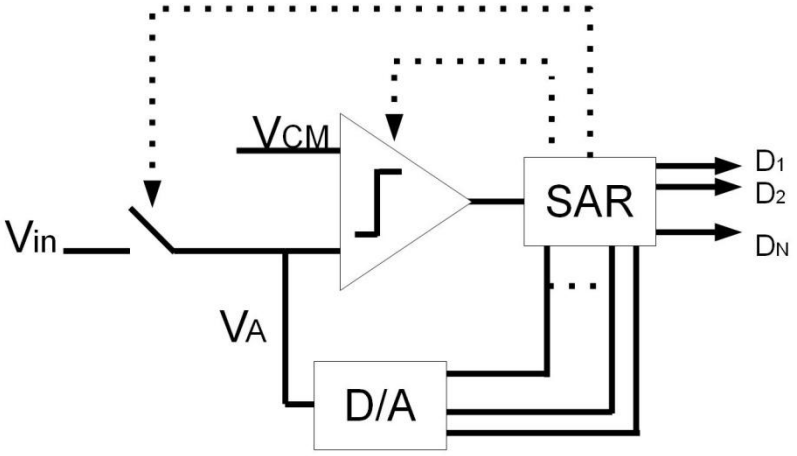


Figure 3.3. SAR ADC with capacitive DAC

The main advantage of this configuration is its low power consumption due to inherent sample-and-hold operation inside the capacitive DAC.

3.3 Sub-blocks of SAR ADC

3.3.1 Sample and Hold

In general, Sample and hold circuit (SHC) contains a switch and a capacitor. In the tracking mode, when the sampling signal is high and the switch is connected, it tracks the analog input signal. Then, it holds the value when the sampling signal turns to low in the hold mode. In this case, sample and hold provides a constant voltage at the input of the ADC during conversion. Regardless of the type of S/H (inherent or separate S/H), sampling operation has a great impact on the dynamic performance of the ADC such as SNDR.

3.3.2 Successive Approximation Register

Successive Approximation Register (SAR) control logic determines each bit successively. The SA register contains N bit for an N-bit ADC. There are 3 possibilities for each bit, it can be set to '1', reset to '0' or keeps its value.
In the first step, MSB is set to '1' and other bits are reset to '0', the digital word is converted to the analog value through DAC. The analog signal at the output of the DAC is inserted to the input of the comparator and is compared to the sampled input. Based on the comparator result, the SAR controller defines the MSB value. If the input is higher than the output of the DAC, the MSB remains at '1', otherwise it is reset to '0'. The rest of bits are determined in the same manner. In the last cycle, the converted digital word is stored. Therefore, an N-bit SAR ADC takes N+1 clock cycles to perform a conversion. Different architectures of SAR logics are implemented and compared in Chapter4.

3.3.3 Comparator

Comparator is the only analog block of a SAR ADC and performs the actual conversion. It compares the analog sampled input to the analog output of the DAC and generates digital output of '0' or '1' which will be used in the SAR logic. Accuracy and speed of the comparator are two important factors. The comparator need to resolve voltages with small differences. The offset voltage

of the comparator employed in SAR ADC is translated to the transfer characteristic of the ADC thus will not affect the linearity of ADC. The comparators are discussed in detail in Chapter5 and implementation of different comparators and comparison between them are presented in Chapter6.

3.3.4 Digital to Analog Converter

The digital to analog converter (DAC) converts the digital word at the output of the SAR logic to an analog value. Then in the comparator, this value is compared to the input signal.
In the capacitive DAC with inherent Sample and Hold, the sampling operation is performed by DAC and is called charge redistribution DAC. Nowadays, charge redistribution DACs are commonly used. They consume less power and induce less mismatch errors compared to the resistive based DAC. Charge redistribution DAC has fast conversion time. Moreover, they are fabricated easily [6], [7]. In the following three different architectures of capacitive DAC are presented.

Binary-Weighted Capacitor Array

An N-bit binary-weighted capacitor array is shown in Figure 3.5. It consists of scaled binary capacitors, i.e., $2^{N-1}C$, $2^{N-2}C$… 2C, C, C. The last capacitor is a dummy that has equal value as the LSB capacitor. Thus, the total value of the capacitors is $2^{N}C$.

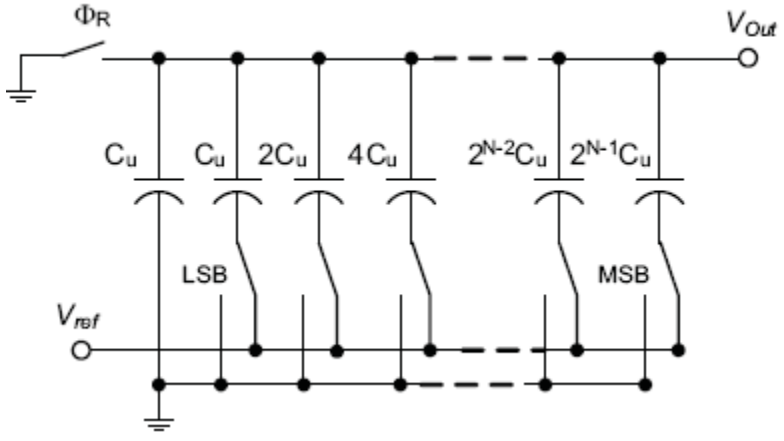


Figure 3.5. Binary-weighted capacitor array DAC [8]

First, in the reset phase all the bottom plates are grounded. During the redistribution mode in which the actual conversion is performed, based on the provided digital code, the switches are connected to either V_{ref} or ground.
The occupied area and power consumption of the BWC is increased with the increase of the resolution [8].

Two-Stage Weighted Capacitor Array

Two-stage capacitor array was first proposed in [9] to mitigate the large capacitance size in BWC array. Figure 3.6 illustrates a TWC array. In this approach the BWC array is divided into two smaller BWC and a coupling capacitor is added between two parts. The value of the coupling capacitor is determined in Equation 3.1 [8].

$$C_{split} = \frac{2^{\frac{N}{2}}}{2^{\frac{N}{2}-1}} \tag{3.1}$$

This architecture reduces occupied area and power consumption.

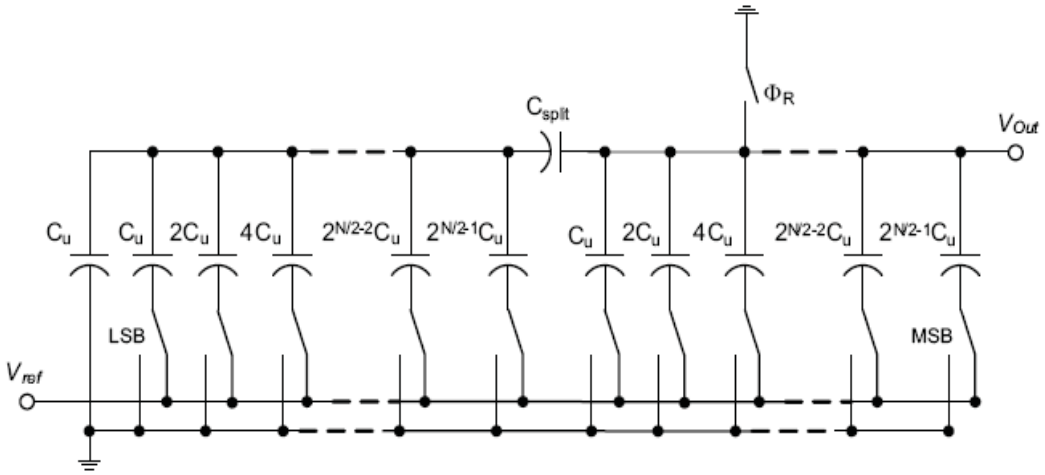


Figure 3.6. Two-stage capacitor array DAC [8]

C-2C Capacitor Array

C-2C ladder is an extension of TWC array. Figure 3.7 shows a C-2C ladder example. In this configuration, the values of the capacitors are drastically reduced. As a result, this type of DAC can achieve higher speed while consuming less power. The power consumption increases linearly, in contrast to BWC in which the power rises exponentially. The main drawback of this

configuration is the degradation of the linearity due to parasitic capacitances [10].

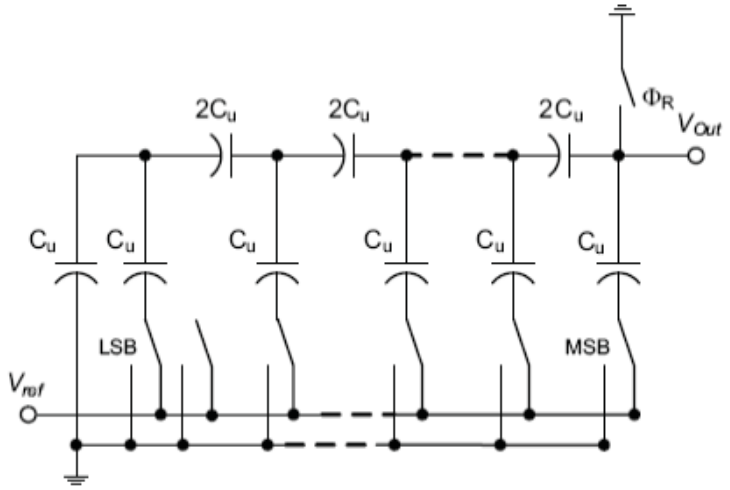


Figure3.7. C-2C ladder [8]

Chapter 4
Successive Approximation Register (SAR) Control Logic

In this chapter, SAR control logic operation is described and then two conventional structures of SAR are reviewed and implemented in 65nm CMOS technology. In the following, delay line based controller is investigated. Finally, a comparison between them in terms of power, speed, and voltage scalability is presented.

4.1 SAR Logic Operation

Successive approximation register ADC implements the binary search algorithm using SAR control logic. In general, there are mainly two fundamentally different approaches to designing the SAR logic. The first one which is proposed by Anderson consists of a ring counter and a shift register. At least 2N flip flops are employed in this kind of SAR [14]. The other, which is proposed by Rossi, contains N flip flops and some combinational logic [15].

SAR control logic determines the value of bits sequentially based on the result of the comparator. SAR operation can be represented using a sequential Finite State Machine which is illustrated in Table 4.1. Each conversion takes 12 clock cycles. In the first clock cycle, SAR is in the reset mode and all the outputs are zero. In the next ten clock cycles, data is converted and each bit is determined sequentially. The last cycle is for storing the results of the complete conversion.

Table 4.1: Finite State Machine algorithm

Cycle	Sample	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	comp
0	1	0	0	0	0	0	0	0	0	0	0	-
1	0	1	0	0	0	0	0	0	0	0	0	a_9
2	0	a_9	1	0	0	0	0	0	0	0	0	a_8
3	0	a_9	a_8	1	0	0	0	0	0	0	0	a_7
4	0	a_9	a_8	a_7	1	0	0	0	0	0	0	a_6
5	0	a_9	a_8	a_7	a_6	1	0	0	0	0	0	a_5
6	0	a_9	a_8	a_7	a_6	a_5	1	0	0	0	0	a_4
7	0	a_9	a_8	a_7	a_6	a_5	a_4	1	0	0	0	a_3
8	0	a_9	a_8	a_7	a_6	a_5	a_4	a_3	1	0	0	a_2
9	0	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	1	0	a_1
10	0	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	0	a_0
11	0	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	-

4.2 SAR Logic Type1

SAR architecture shown in Figure 4.1 is presented in [14] and is commonly used in SAR ADCs due to its straightforward design technique. This control logic encompasses a ring counter and a code register. The ring counter is in fact a shift register.

For each conversion, in clock cycle 0, the EOC signal is high and all Flip Flops outputs are reset to zero, and for the rest of cycles EOC is low. In the next clock cycle, the most significant Flip Flop is set to one which corresponds to MSB of the digital word to the DAC. Then the counter shifts '1' through the Flip Flops from MSB to LSB.

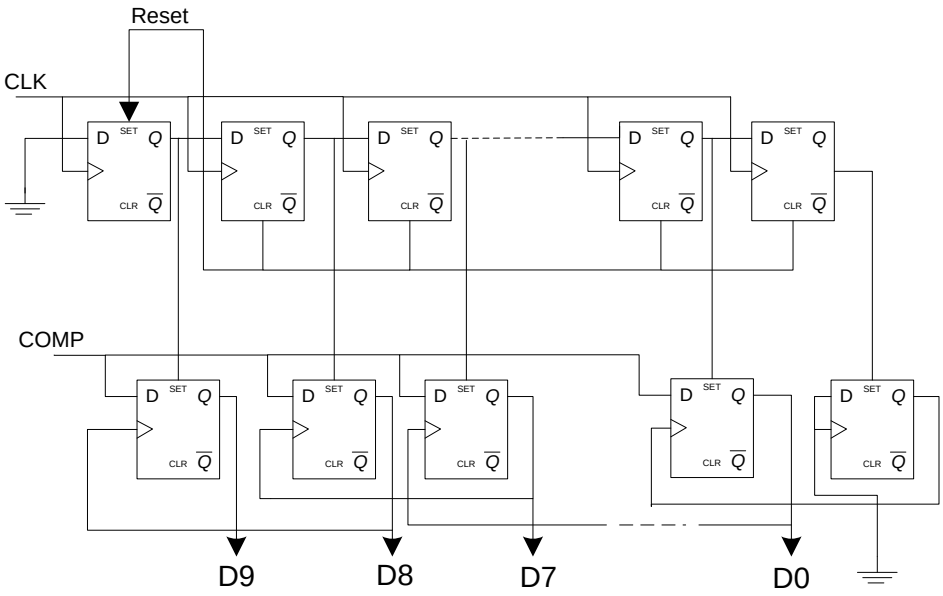


Figure 4.1. SAR block diagram

In each clock cycle, one of the outputs in the ring counter sets a Flip Flop in the code register. The output of this Flip Flop which is set by the ring counter is used as the clock signal for the previous Flip Flop. At rising edge of the clock, this Flip Flop loads the result from the comparator. Figure 4.2 shows the transient response. At the end of each conversion, EOC signal turns to high. This type of SAR logic, converts each sample in 12 clock cycles.

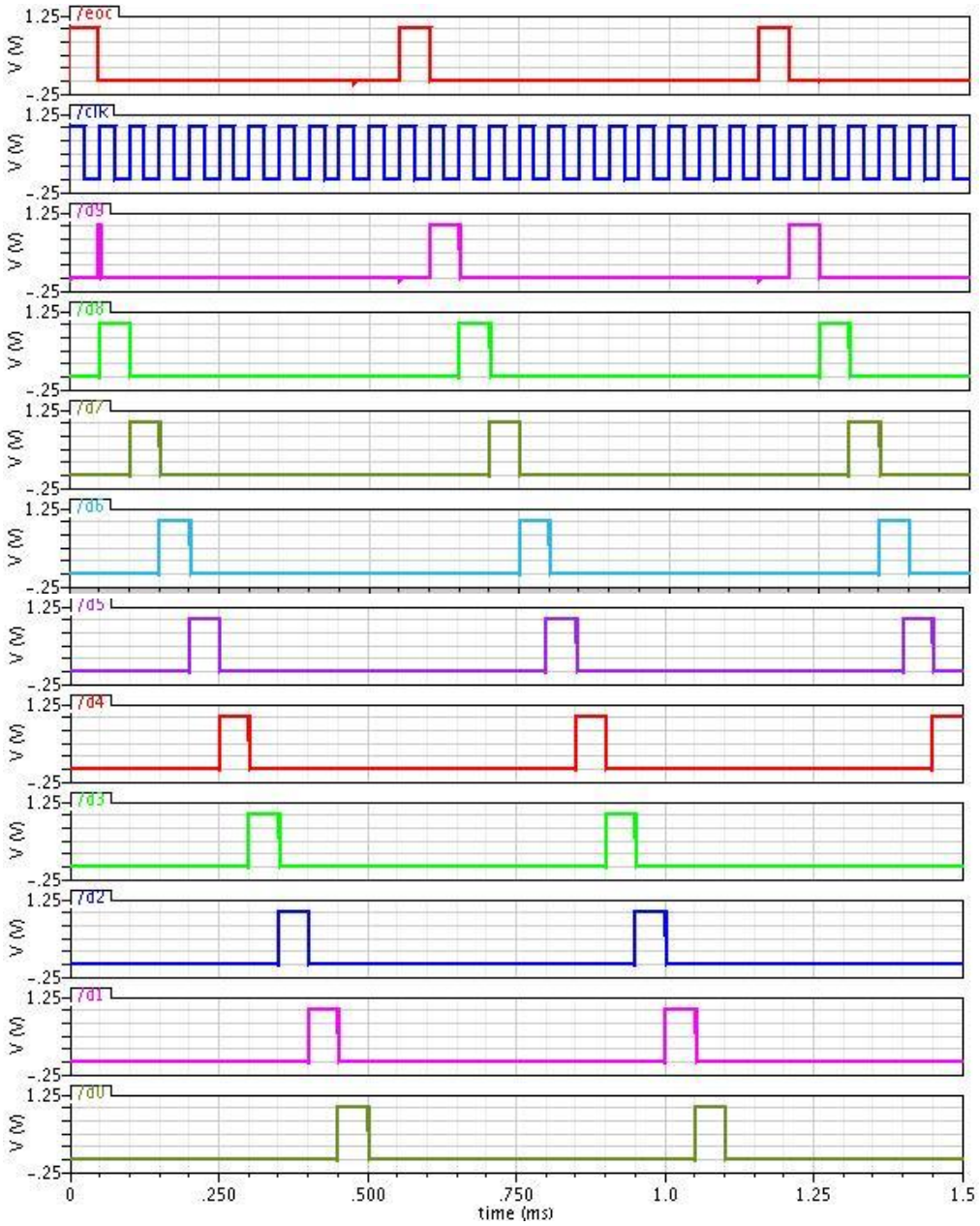


Figure 4.2. Transient response of the SAR logic type 1

The Flip Flops which are employed in this structure are set-reset D-FFs. For low power purpose, transmission gate based Flip Flops are used [17]. Minimum size transistors with double length are chosen for improving the power performance. The schematic of the DFF is illustrated in Figure 4.3. In order to decrease the leakage power even more while simultaneously maintaining the speed, high threshold voltage transistors are used in the non-

critical paths and low-V_T transistors in the critical path. Thus, this dual threshold approach provides high performance Flip-Flops [18].

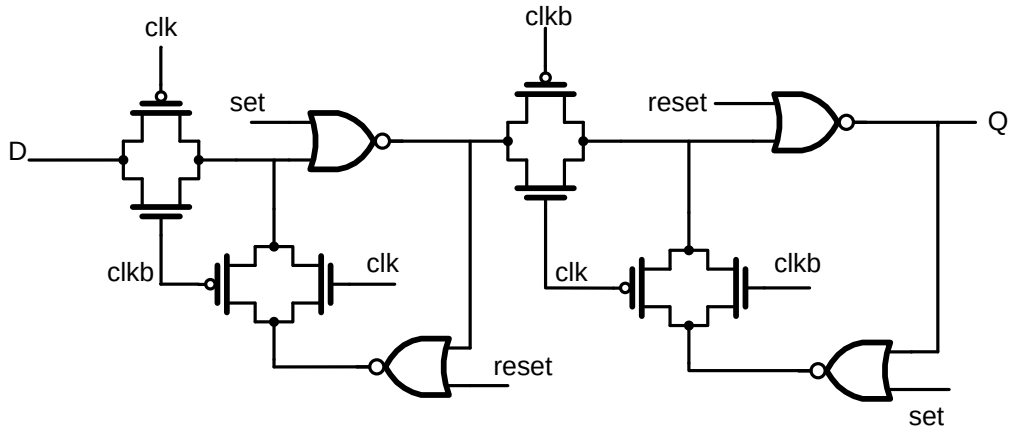


Figure 4.3. Transmission gate based Flip-Flop

Figure 4.4 illustrates total power consumption of the SAR logic versus frequency.

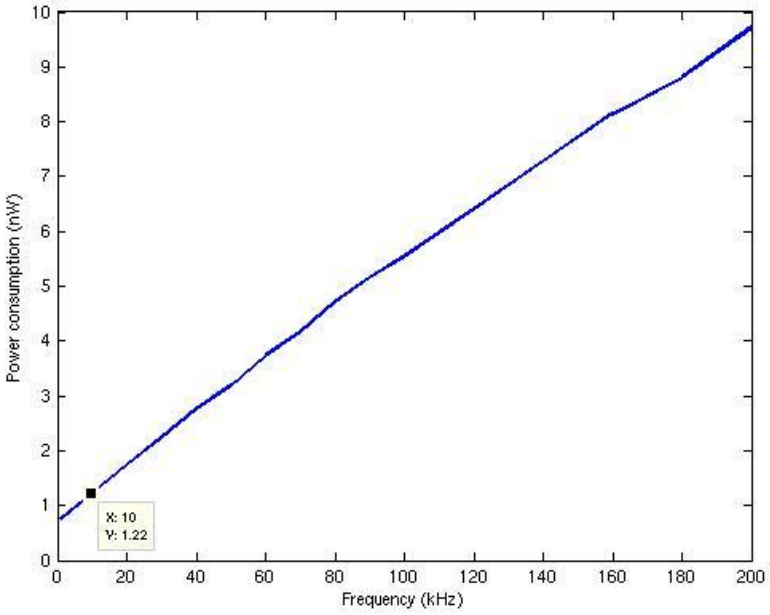


Figure 4.4. Average power vs. frequency

The measured leakage power is 707pW which is %58 of the total power at sampling frequency of 1kS/s.

The architecture shown in Figure 4.1 has some advantages. First, it is low power due to low signal transition. Furthermore, since this logic is iterative, it can be extended to higher resolutions by just extending the shift registers.

In order to decrease the power even more, supply voltage can be reduced. Figures 4.5 and 4.6 illustrate the power consumption and propagation delay under different supply voltages, respectively.

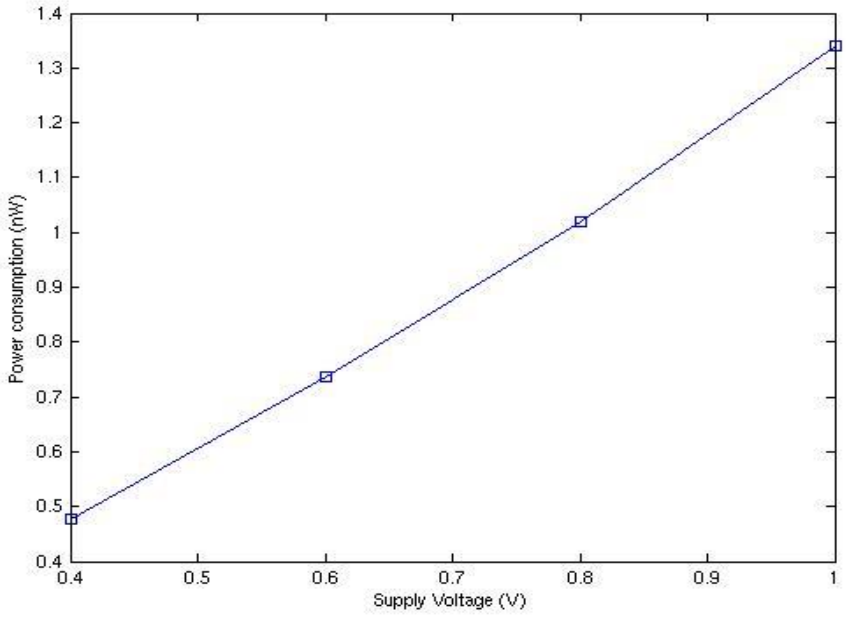


Figure 4.5. Power consumption vs. scaled V_{DD}

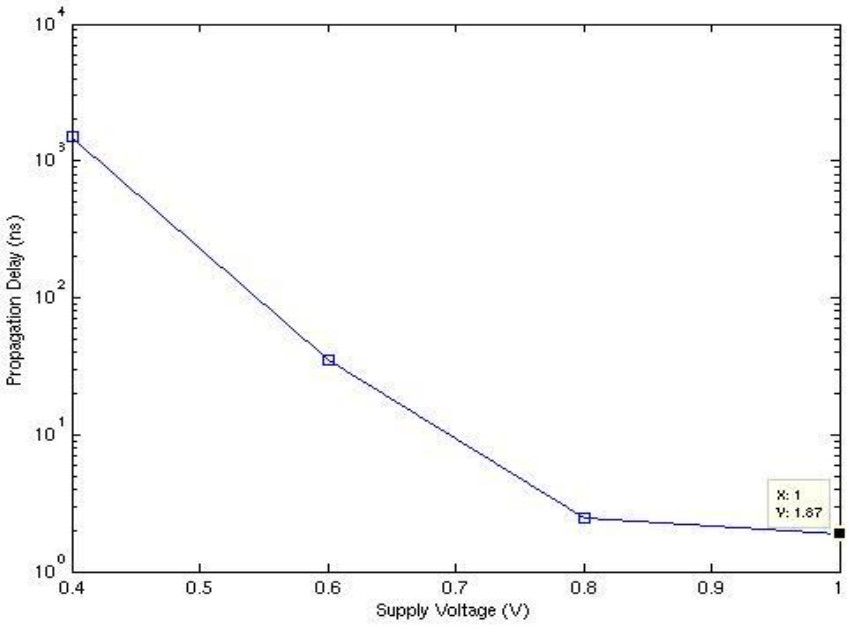


Figure 4.6 Propagation delay vs. scaled V_{DD}

4.3 SAR Logic Type2

For an N bit SAR ADC, digital control logic needs at least N flip-flops to perform conversion. Therefore, a non-redundant SAR employs minimum number of flip-flops. These FFs both guess and store the converted result.
For its operation, at the initialization step (step 0), SAR assigns MSB to 1 and the other bits to 0. This word is equivalent to $\frac{V_{ref}}{2}$ after being applied to D/A converter. At step1, the SAR control logic makes its decision based on the output of the comparator. If it is high, MSB remains 1 otherwise SAR changes MSB to 0. Thus the value of MSB is defined now. Simultaneously SAR sets next MSB to 1. Applying this word to DAC again, input voltage is compared to the DAC output and SAR defines the value of this next MSB based on the result of the comparator. Therefore, successive approximation logic determines all the bits sequentially. Figure 4.7 shows 10-bit SAR logic. The design is based on the logic proposed by Rossi [15].

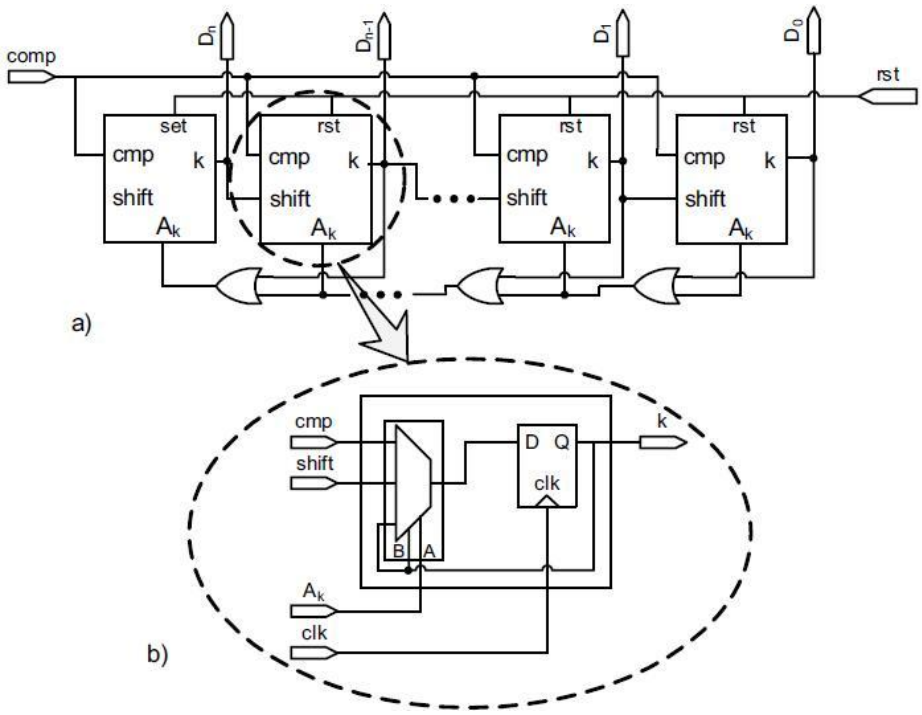


Figure 4.7. Successive approximation logic [15]

As it can be seen from the Table 4.1, there are three possibilities for each bit.

1. Shifting right
2. Taking the comparator results
3. Memorization mode

As illustrated in Figure 4.7, non-redundant successive approximation control logic contains an N-bit shift register and OR chain. Each Flip Flop can take the result of the comparator, the output of the previous Flip Flop, or the value of the OR gate in each step.
For its operation, at initialization state the first Flip Flop on the left is set to 1 and the rest of Flip Flops are reset to 0. This condition is provided by an external control signal called start signal. In the next steps, one of three possible inputs is taken for each Flip Flop. Since there are three possible inputs, a multiplexer is required. Inside of the Flip Flop is shown in Figure 4.6 (b). Although a three input 3:1 mux is required, a 4:1 mux is employed for implementation of the SAR for simplicity. A and B are the control signals of the multiplexer. The appropriate input is selected according to the table 4.2.

Table 4.2

A	B	
1	-	Memorization
0	1	Data load
0	0	Shift right

The conversion is terminated by applying high voltage to the OR chain. Consequently, SAR enters the storing mode. In general, at the end of each conversion, converted result is stored in the SAR. This is performed by connecting the output of the last Flip Flop to the OR chain. Therefore, end of conversion is defined by the least significant Flip Flop on the right.

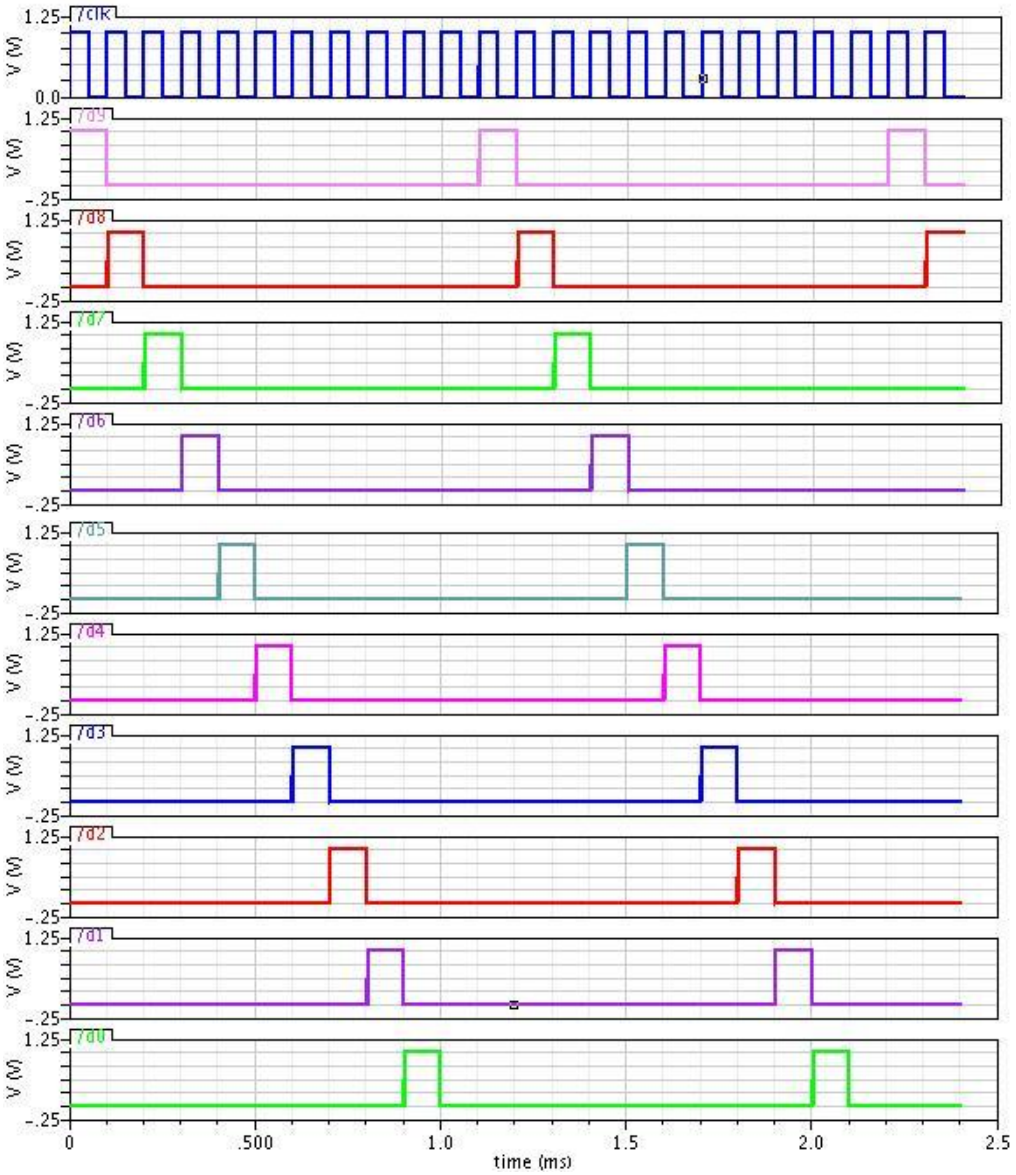


Figure 4.8. Transient response of SAR logic type 2

Figure 4.8 shows the transient response of the SAR control logic. Each conversion takes 11 clock cycles in this type of SAR controller.
Figure 4.9 presents the total power consumption of SAR versus frequency. In order to consider clock power in the total power, some drivers are used for clock distribution.

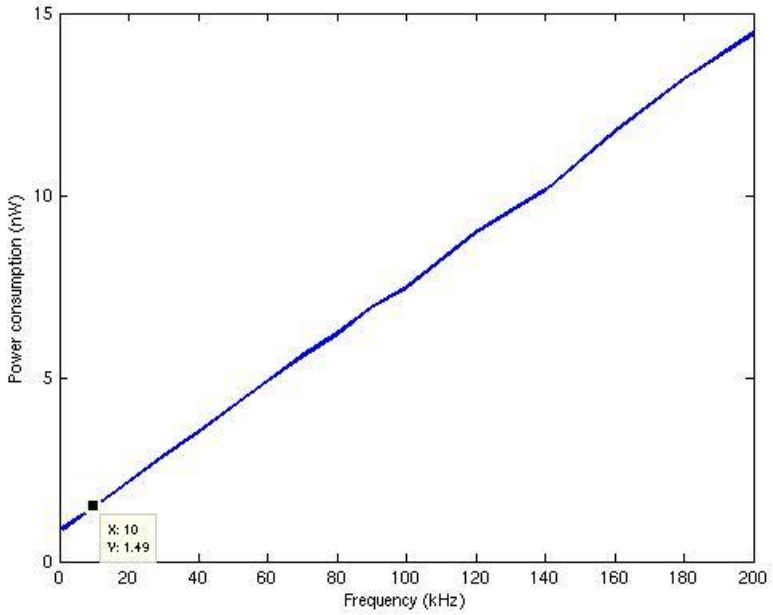


Figure 4.9. Average power vs. frequency

The leakage power for this type of SAR is 824pW which is %55 of the total power at 1kS/s.
This architecture is iterative; therefore by extending the sequence of FFs higher resolutions can be achieved. Start signal should be adjusted manually for different clock frequencies. However, this problem is mitigated by adding a counter to the structure. The behavior of the circuit by applying different supply voltages at the sampling frequency of 1kS/s is illustrated in Figures 4.10 and 4.11.

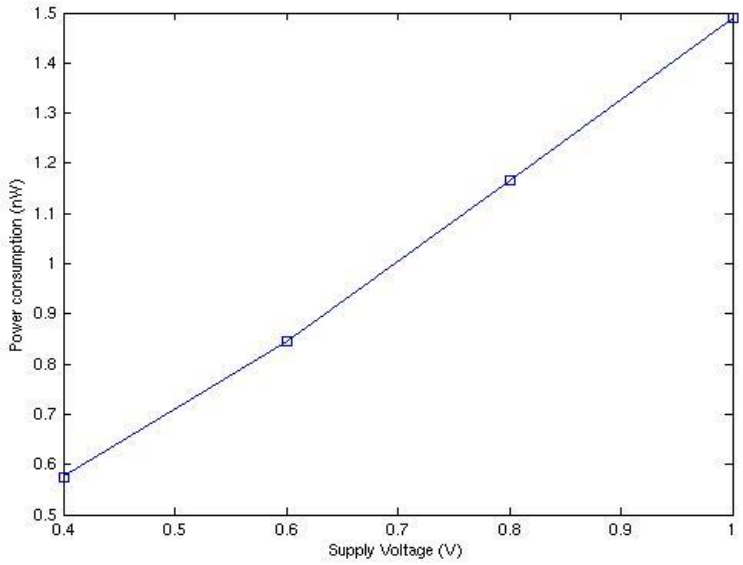


Figure 4.10. Power consumption vs. scaled V_{DD}

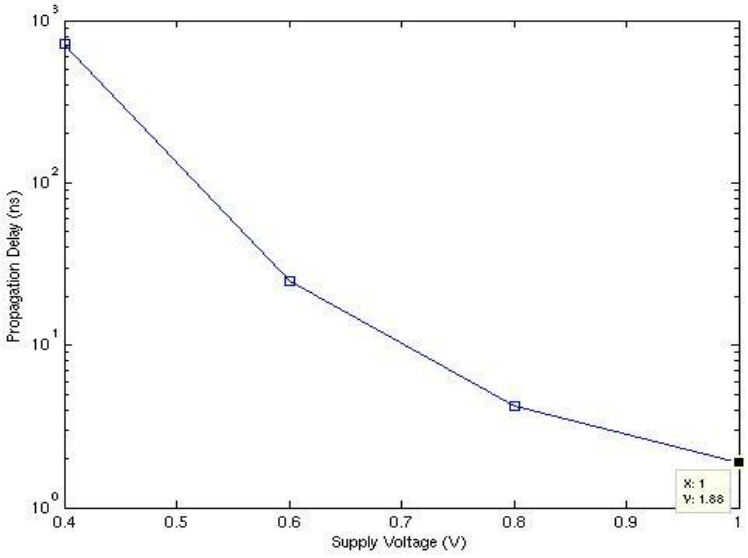


Figure 4.11. Propagation delay vs. scaled V_{DD}

4.3.1 Non-redundant SAR with counter

A counter is added to the non-redundant SAR in order to generate the start signal automatically. Non-redundant SAR architecture contains a sequence of three-input Flip-Flops, a 4 bit counter and a decoder. The schematic view is shown in Figure 4.12.

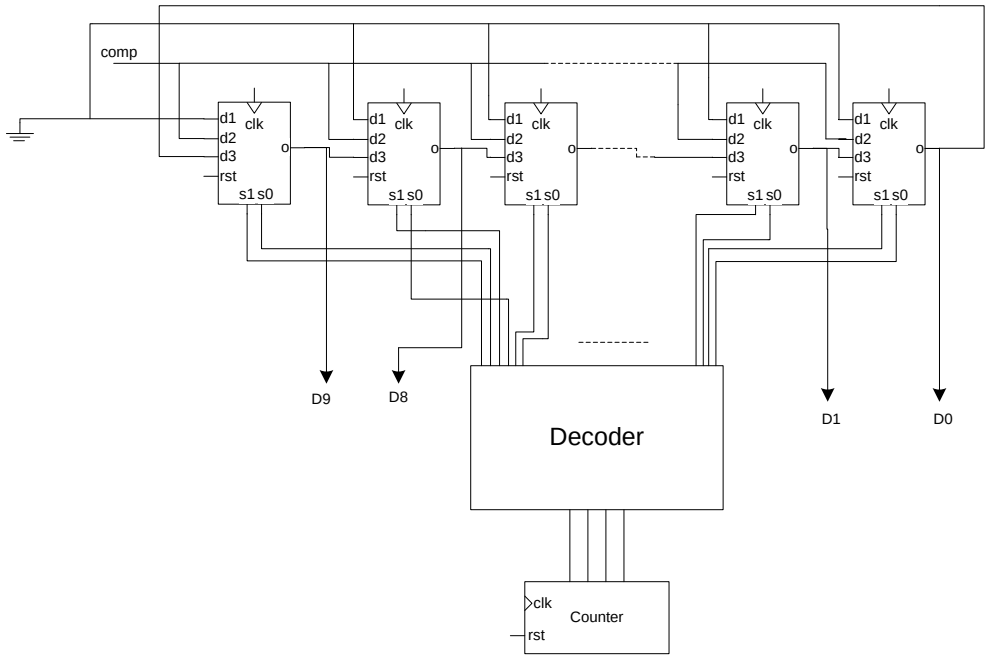


Figure 4.12. Schematic view of the control logic

There is a 4:1 mux inside of each FF block which is shown in Figure 4.7(b). This digital logic is similar to non-redundant SAR in [15]. The differences are the 4-bit counter and a decoder which are added to the schematic. There are some minor changes in the finite state machine which is implementing the SAR operation.
Each bit has 4 possibilities in the new structure:

1. Storing the previous state (memorization)
2. Value of the previous Flip Flop (right shift)
3. Result of the comparator
4. Assigning 0 or 1

For a complete conversion 12 clock cycles are required. At initialization state all the outputs are reset to zero. The start of the conversion is identified by the end of conversion (EOC) signal. As mentioned above, SAR has a 10-bit shift register. Each D-FF has four external inputs and hence a 4:1 mux. The multiplexer has two control bits and functions according to the truth table below.

Table 4.3

A	B	
0	0	Memorization
0	1	Assigning 1 or 0
1	0	Comparator value
1	1	Shift right

The 4-bit counter generates control bits A and B, then the decoder defines the counter value. D0 to D9 are the digital output data of the A/D converter. The transient response of the SAR logic is illustrated in Figure 4.13. As it can be seen from the figure this types of SAR, converts a sampled data in 12 clock cycles.

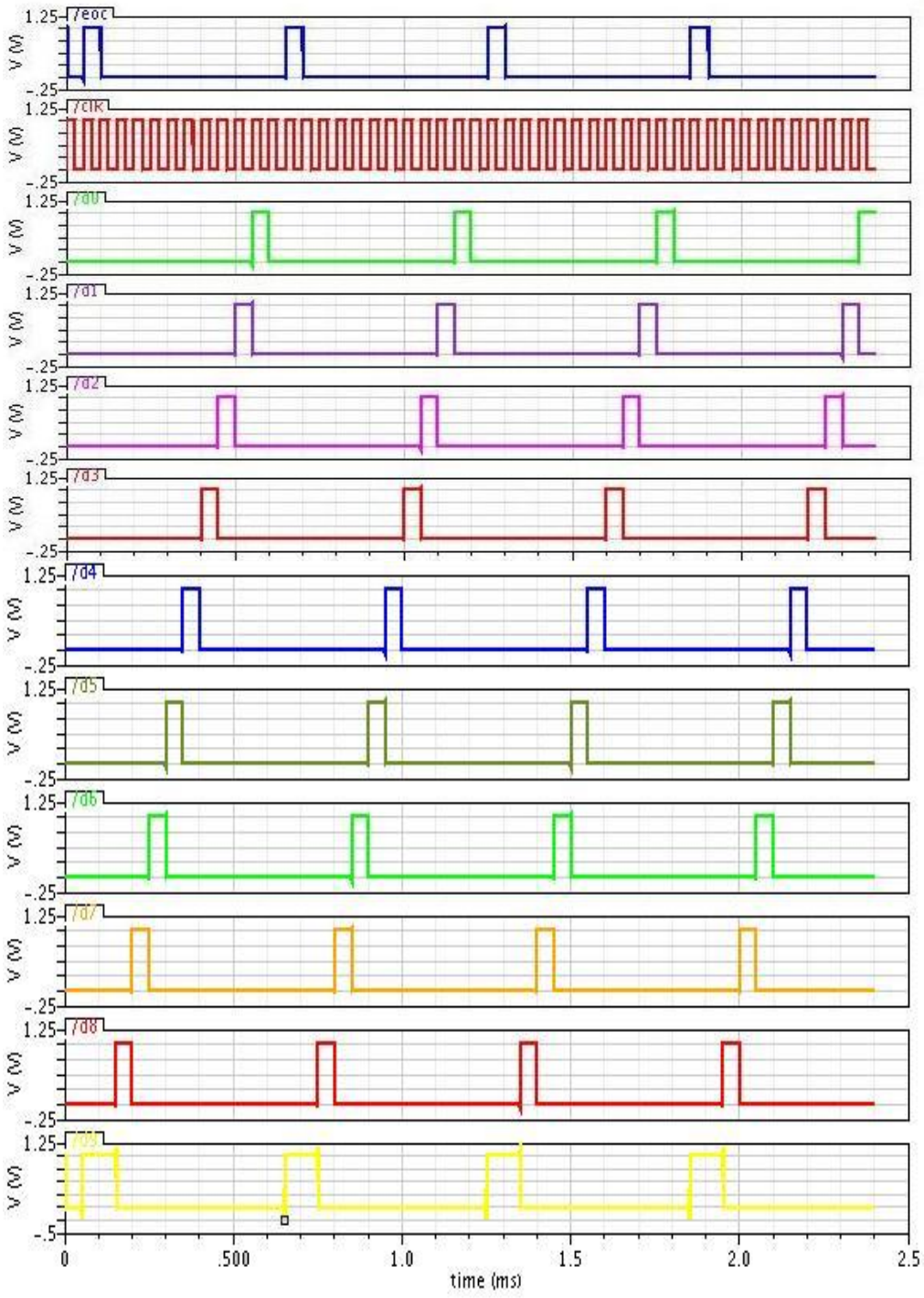


Figure 4.13. Transient response of non-redundant SAR with counter

Figure 4.14 represents the total power consumption of the SAR versus frequency. The drawback of this configuration is that the logic is not iterative, thus by changing the resolution the entire decoder needs to be changed.

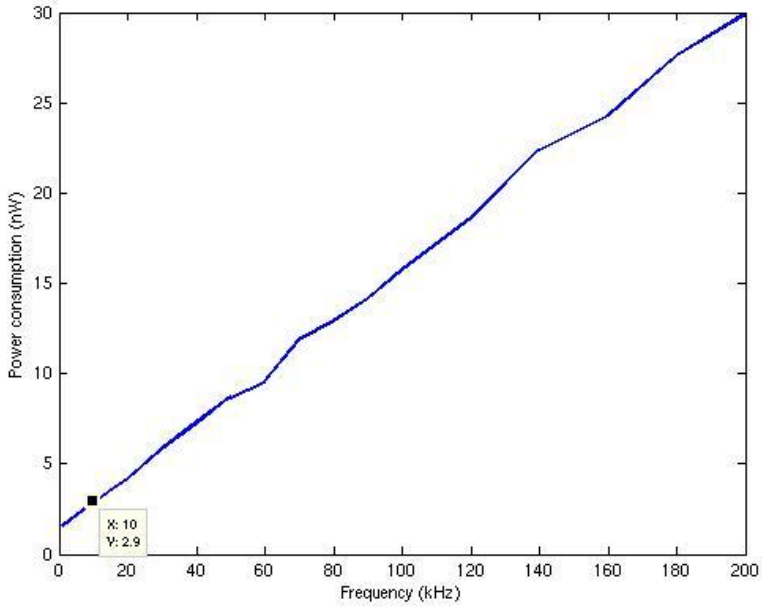


Figure 4.14. Average power vs. frequency

The leakage power of this structure is 1.4nW which is %48 of the total power at 1kS/s.

The circuit was simulated under different supply voltages and the results of the power consumption and propagation delay are shown in Figures 4.15 and 4.16, respectively.

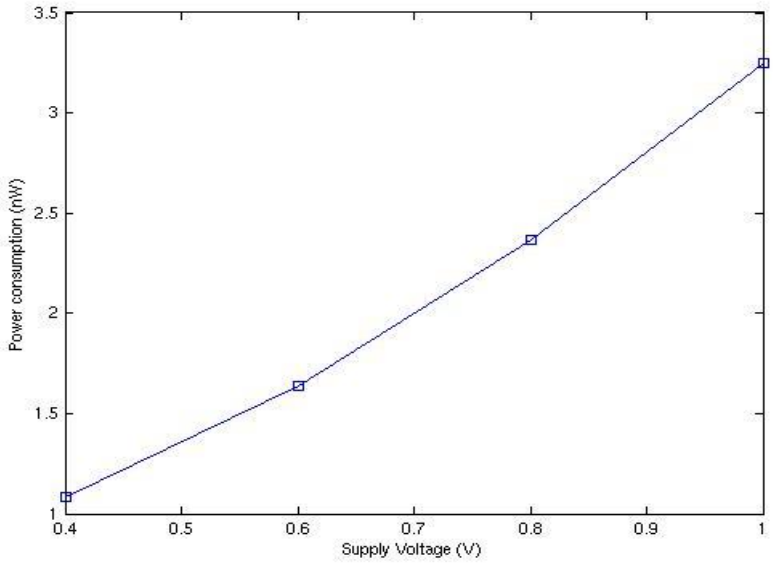


Figure 4.15. Power consumption vs. scaled V_{DD}

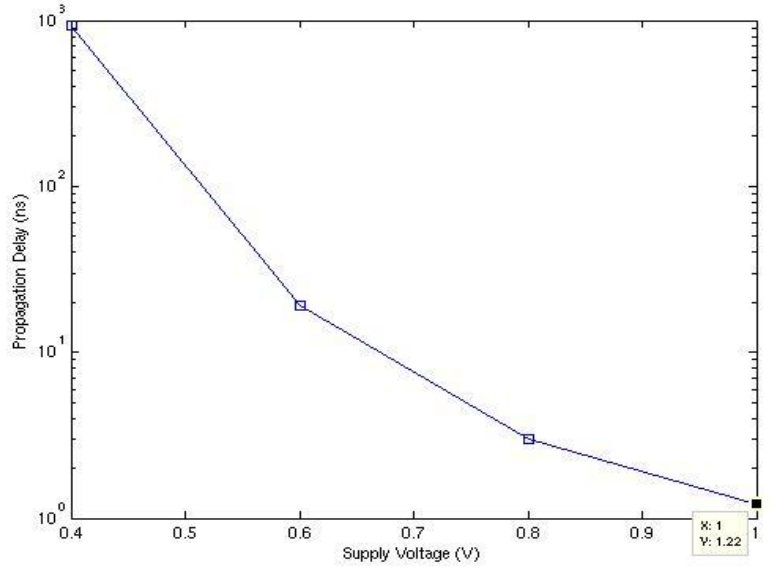


Figure 4.16. Propagation delay vs. scaled V_{DD}

4.4 Delay Line Based SAR Control Logic

Delay line circuits are used for clock generation purposes. Typically, a wide range of adjustment is desired to achieve different clock frequencies from high to low. An adjustable delay line encompasses a string of variable delay elements. Variable delay components are voltage or current controlled elements. In fact, RC time constant of each delay element determines its delay. Hence, varying the total resistance or capacitance leads to different delays [19].

Delay elements are vulnerable to the noise of power supplies which causes jitter in the generated clock. Therefore, designing delay elements with wide adjusting range and low jitter which are also equipped with power supply noise rejection circuits is desired. There are several kinds of delay elements. In this thesis work some of them which consume less power are explored.

4.4.1 Inverter Based Delay Line

Inverter delay line is constructed from a chain of inverters in a row. Figure 4.17 (a) shows an inverter delay element. The required control signals for SAR algorithm are generated by employing some gates and alternately delaying rising and falling times. This is accomplished by increasing the channel length of NMOS or PMOS transistors in turns. These sequential pulses control some parts of SAR [16].
Inverter delay line has some difficulties in its implementation. For example, large delays cannot be realized by inverter delay line since many stages are required, which is not feasible and also increases jitter at the output proportional to the square root of the number of stages.

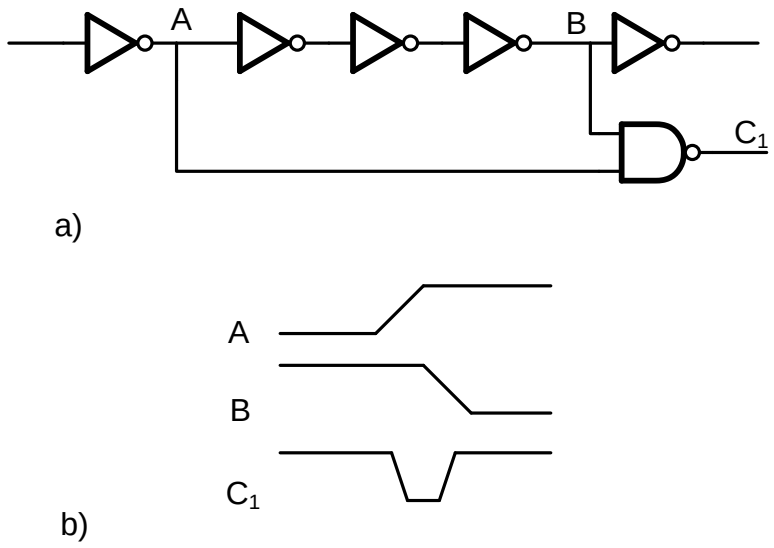


Figure 4.17. Delay lined based SAR controller a) inverter delay element b) waveforms at A, B, and C1 nodes

After sampling phase, ADC starts to convert the sampled input data. Sample signal is an external signal which is inverted, see voltage A, as shown in Figure 4.17 (b). When A is low, B is high and then voltage A with a certain delay turns to 1. Therefore, a pulse C_1 at the output of the NAND gate is generated which is active low and is a control signal for SAR algorithm. For increasing the width of these control pulses, the rising and falling times should be increased alternately. In this configuration when A becomes high, the NMOS transistor in the inverter is on and PMOS transistor is not conducting. The large length of NMOS causes the capacitance at the output of the inverter discharge slowly and B turns to low voltage slowly and C1 becomes high again. In order to delay the rising edge, a PMOS transistor with large channel length should be used and for delaying a falling edge an NMOS transistor with large channel length can be employed. One of the drawbacks of this configuration is that the delay value of each delay element is not precise because of the process and temperature variation as well as power supply noise. However, the width of these control signals should be large enough for DAC and comparator to settle. Therefore, this inaccuracy of delay does not affect the ADC performance.

The generated control signals are shown in Figure 4.18.

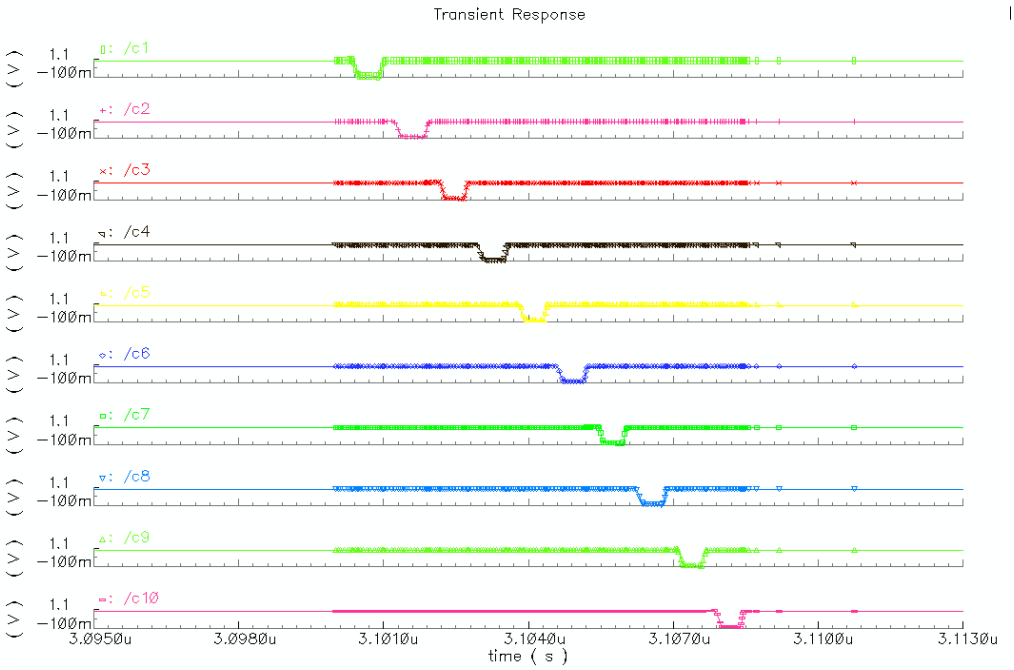


Figure 4.18. Produced control signal from delay line

Since the PMOS and NMOS transistors in a simple inverter will not conduct simultaneously, there is no static power consumption, which is the main advantage of the inverter based delay line. However, there are some periods of time in which both transistors are in the saturation region and conduct, causing short circuit current flows between power rails. Short circuit may also occur when one of the transistors is in the saturation region while the other is in the triode region. This delay line can provide an adjustable delay by using a multiplexer. As a result, it is a digitally controlled system which is not power efficient and precise compared to the analog control systems. Thus analog control delay elements are desirable [20].

4.4.2 Current-Starved Inverter Delay Line

For having a voltage controlled delay element, current controlled transistors can be added in series to the inverter. This structure is called current-starved inverter which is shown in Figure 4.19.

Delay can be adjusted by changing the current through the inverter. For instance, larger delay is achieved as a result of decreasing the current. Changing the control gate voltage in fact varies the resistance of the transistor. Therefore, Current Starved Inverter is a resistive controlled delay element.

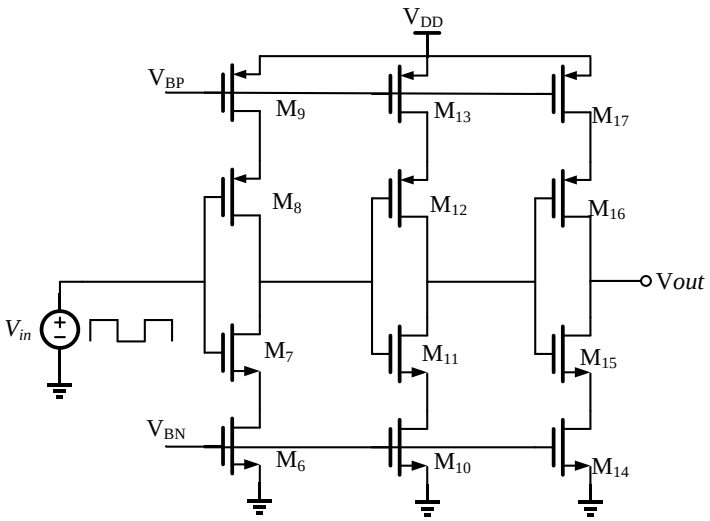


Figure 4.19. Current-starved delay element

4.4.3 Capacitive-Controlled Delay Element

An example of a capacitive-controlled delay element is shown in Figure 4.20. M_1 is in the triode region and acts as an adjustable resistance. This transistor decouples an explicit output capacitance [19].

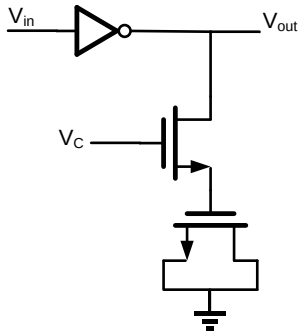


Figure 4.20. Capacitive controlled delay element

The maximum delay that can be obtained with capacitive-controlled delay elements is limited to $R \cdot (C_{in} + C_{exp})$. Thus, achieving a large delay mandates a large number of delay elements.

4.5 Comparison

Widths of transistors are minimum size since the operating frequency is quite low for biomedical applications and lowering power consumption is the primary target. However, for decreasing the leakage, length is chosen to be 1.5 times the minimum length. It should be mentioned that in all the schematics presented in this work, transistors are high V_T which leads to lower leakage power. The logics are compared more or less in the same situation.

All the outputs are loaded with NMOS transistors as switches in the capacitor array DAC. The rising time of the clock is 1ns. However, it can be increased up to 2ns to achieve lower dynamic power with preserving the performance. External asynchronous signals to the logic, including reset and start signals, are synchronized through two D-FFs. All clock signals are buffered. According to the simulation for a fan-out of 12 Flip Flops, a simple two inverter in a row can be used as a driver with proper aspect ratio. Figure 4.21 illustrates the power consumption of the three successive approximation logics versus frequency. From the simulation results, SAR logic with a sequencer and a code register is more power efficient.

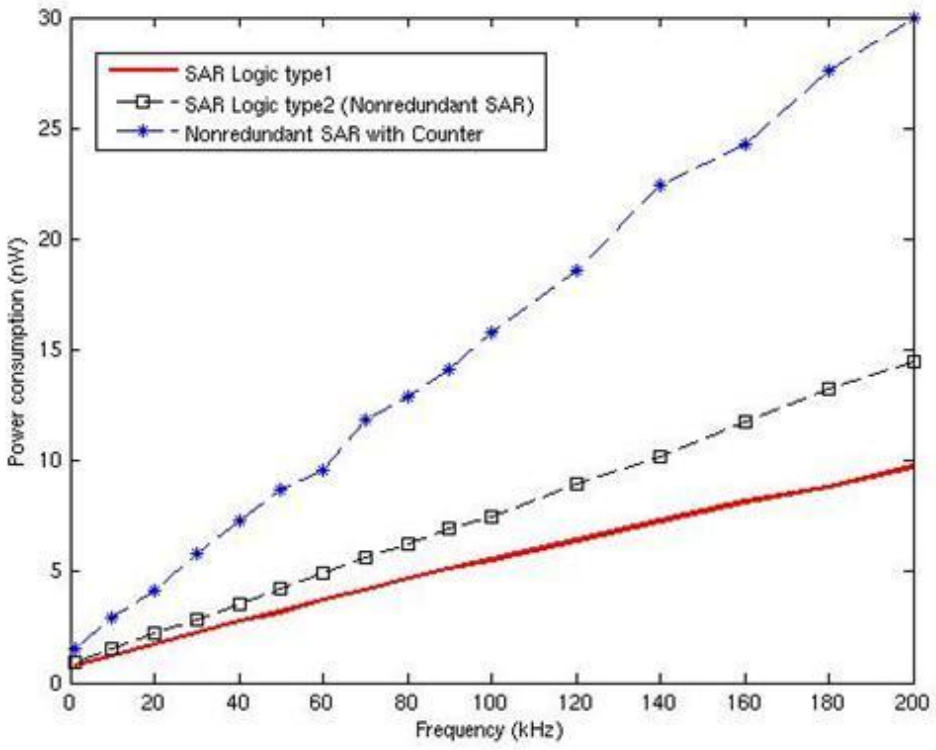


Figure 4.21. Average power vs. frequency

Figure 4.22 shows a comparison between the power consumption of the three logics versus scaled supply voltage at 1KS/s.

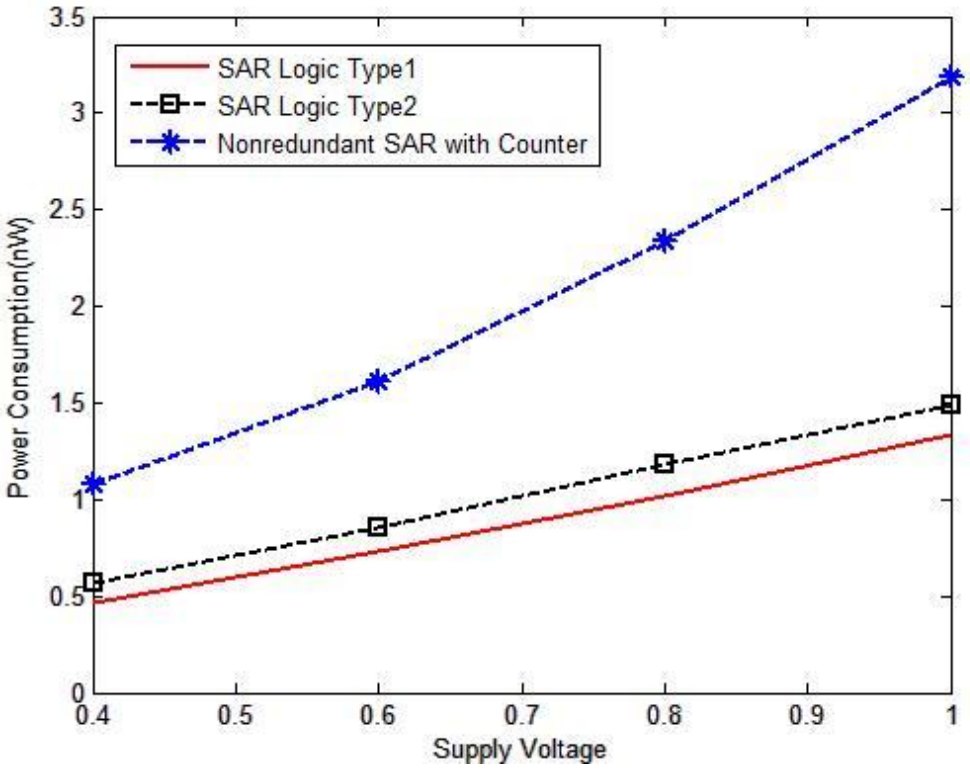


Figure 4.22. Average power vs. scaled supply voltage

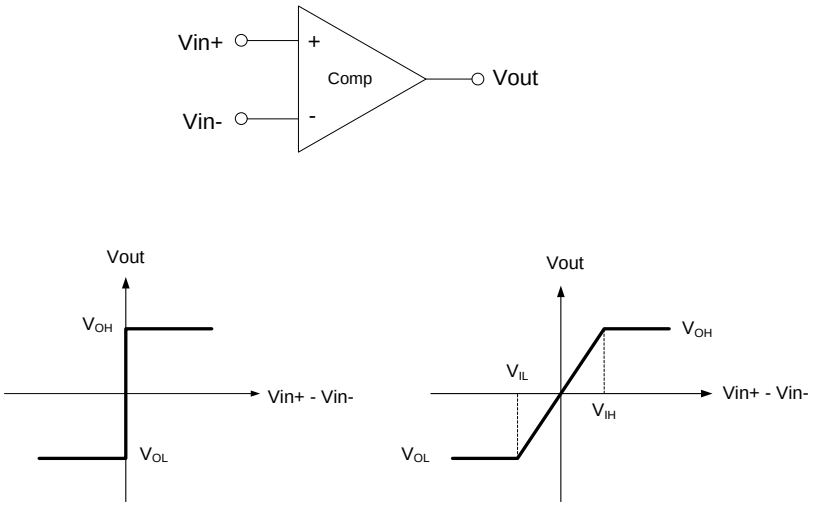
Delay line can be used to control the SAR. In general, delay lines consume more power compared to the conventional SAR control logics. Therefore, conventional SAR logic type1 is employed in the designed ADC.

Chapter 5
Comparator Design

A brief description of a comparator is described and then the performance metrics of a comparator are discussed. Finally, basic comparator types are presented and a comparator suitable for low power applications is chosen.

5.1 Comparator

Comparator is one of the building blocks of A/D converters. In some sorts of ADCs such as flash ADC, the comparator has a great impact on the performance of the whole ADC. However, in some cases the error produced by the comparator can be compensated in the followed digital processing block. Figure 5.1 illustrates the comparator and the voltage transfer function of an ideal as well as a real comparator [6]. A comparator generates a logic output high or low based on the comparison of the analog input with a reference voltage. In an ideal comparator, with infinite gain, for input voltages higher than the reference voltage, the comparator outputs logical one and for the input voltages lower than the reference voltage it produces zero at the output.



a) ideal comparator b) real comparator

Figure 5.1. Input-output characteristic of an ideal and real comparator

However, in reality due to finite gain, comparator results in one when $V_{in} > V_{ref} + V_{IH}$, and is set to zero when $V_{in} < V_{ref} + V_{IL}$.

A typical comparator architecture containing a pre-amplifier and a regenerative latch is illustrated in Figure 5.2 [6].

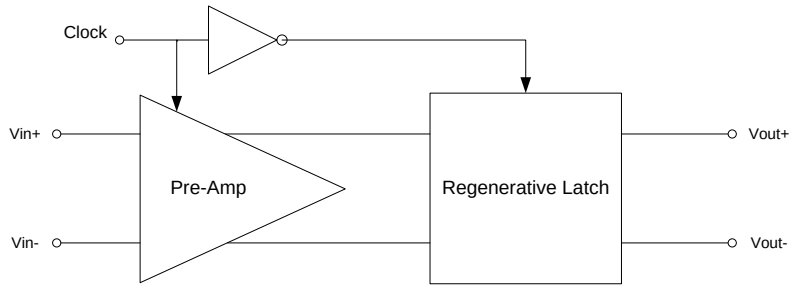


Figure 5.2. Typical block diagram of a comparator

5.2 Performance Metrics of Comparators

Speed, accuracy, low power consumption and wide input common mode range are some design considerations for comparators, which define performance metrics of a comparator.

5.2.1 Resolution

The minimum input voltage difference which is detectable by a comparator is called resolution. Noise and input referred offset are considered as limiting factors of the resolution.

In an A/D converter the minimum required resolution is denoted as V_{LSB}. For instance, in an N-bit ADC, the comparator should be able to detect one LSB which is $V_{LSB} = \frac{1}{2^N}$.

5.2.2 Propagation Delay

Propagation delay defines speed of the comparator, i.e. how fast the comparator decides. It also affects the ADC speed. As shown in Figure 5.3, rising propagation delay is measured between the transition points of the input and output signal when they reach 50% of the signal levels. According to the definition, propagation delay time is the average time of the rising and falling propagation delay times.

$$t_p = \frac{t_{pr}+t_{pf}}{2} \tag{5.1}$$

The propagation delay is shown in Figure 5.3.

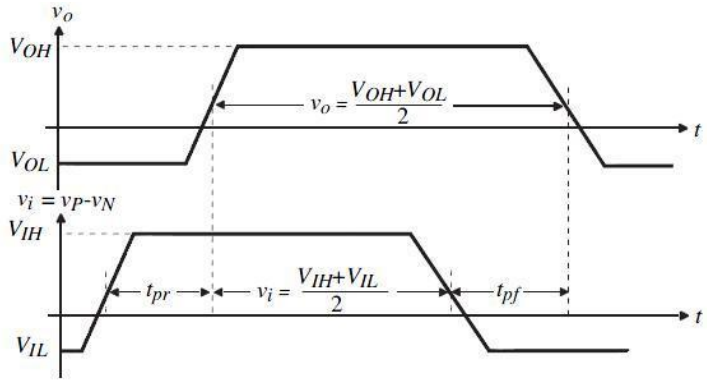


Figure 5.3. Rising and falling propagation delays [28]

Propagation delay of a clocked comparator is measured between the 50% transition points of the clock signal and the differential output signal ($V_{OH} - V_{OL}$).

5.2.3 Comparison Rate

Comparison rate is the highest frequency in which a comparator results in a correct value and is defined by the overdrive recovery test. Assume the input difference of the comparator toggles from a large value to a small one, if the comparator responds correctly to this large voltage variation at its input, the comparator has recovered from an overdrive at this frequency. Comparison rate depends on the speed or basically on the recovery time of the regenerative latch and the preamplifier. [6]

5.2.4 Input-Referred Offset

The static offset at the input of the comparator originates from mismatches in identical devices such as input pair transistors. Therefore, the behavior of the comparator might arbitrarily change. In other words, the comparator may result in high voltage at its output when the input voltage is less than the reference voltage and also it may result in low voltage when the input voltage is higher than the reference. In the presence of offset voltage, the input-referred offset can be modeled as is shown in Figure 5.4. According to this model the comparator decides based on the following equations:

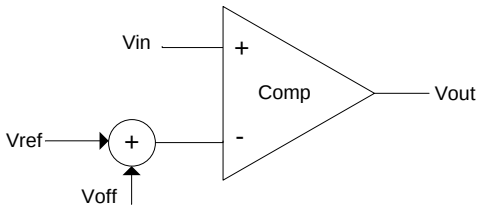


Figure 5.4. Comparator with offset modeling

If $Vin > V_{ref} + V_{off}$ then $V_{out} = V_H$

If $V_{in} < V_{ref} + V_{off}$ then $V_{out} = V_L$

This non-ideality of the comparator can adversely affect the accuracy of the comparator, and consequently decrease the resolution of the ADC.

Input-referred offset can be reduced by the aid of some techniques and/or by using a pre-amplifier in the comparator architecture at the expense of complexity and more power consumption.

5.2.5 Kickback Noise

Kickback noise is in fact the voltage disturbance at the input nodes of the comparator due to large variation of the voltage at internal nodes. These switching effect of the latch are coupled to the input nodes via parasitic capacitances and vary the input voltage. This disturbance is known as kickback noise.

There are some ways to reduce the impact of the kickback noise. The effect can be alleviated by employing a pre-amplifier before latch and also isolating the input nodes by using cascode transistors as switches.

5.2.6 Metastability

Metastability is an error which occurs in a comparator containing a latch. Considering a comparator with two operation phases, reset or pre-amp phase and regeneration phase, the latch is assigned a certain time referred to as regeneration time which is half of the clock period. This means that a latch

generates a logic level in this time. When the input voltage is close to the reference voltage, the latch takes more time to produce a logical level which results in a metastable state. In other words, a metastable situation occurs when the latch is not able to switch to a valid logical level, zero or one, in the regeneration time constant and reaches an intermediate value. Therefore, an important issue in latch design is to compute the probability of this occurrence. Metastability causes errors in comparators and can adversely affect the accuracy of the comparator and the ADC.

5.3 Comparator Architectures

There are various comparator types. In this thesis three basic types of comparators are described. The comparator topology is chosen based on the specific application. In the following, appropriate comparator architecture for low power application is selected.

5.3.1 Open-Loop Comparator

Open-loop comparator is in fact a high gain amplifier with differential input and single ended output with large swing. A two stage op-amp without compensation is an excellent realization of open-loop comparator which is illustrated in Figure 5.5. Since precise gain in not required in comparator, no compensation technique is needed.

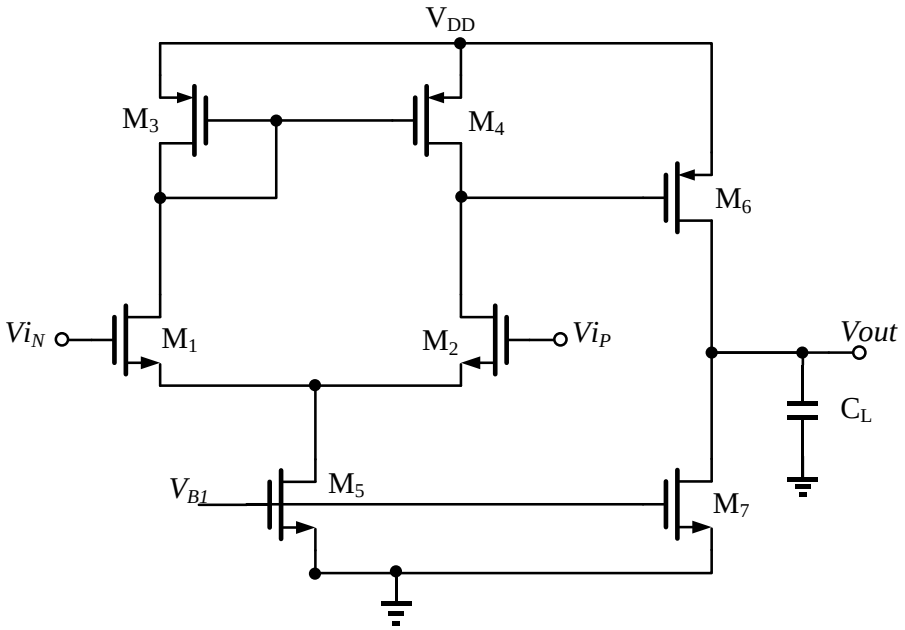


Figure 5.5. Open-loop comparator

This comparator has two poles which compared to the one-pole implementation of the open loop comparator achieves higher speed. In one stage amplifier which has one pole, increasing the gain and simultaneously maintaining the large bandwidth, f_u, poses limitation on the gain bandwidth, f_c, which results in speed reduction of the comparator. In order to mitigate this problem two stage comparator has been proposed. Cascading two stages with lower gain in each stage leads to higher speed however it introduces more input-referred offset voltage. Furthermore, this configuration consumes more power; therefore this type of comparator is not suited for high speed A/D converters as well as low power ADCs.

5.3.2 Latched Comparator Following Pre-amplifier

In this configuration the pre-amplifier attenuates the latch offset by its gain.

$$V_{off\_T}^2 = V_{off\_amp}^2 + \frac{V_{off\_latch}^2}{A_{preamp}} \tag{5.2}$$

This configuration of comparator benefits from low input-referred offset and thus is capable of detecting small voltage differences at its inputs.

According to the Equation 5.2 for input referred offset, increasing pre-amplifier gain results in much lower offset voltage at the input. However, increasing the gain reduces the speed of the comparator. Thus, this comparator exhibits a speed-gain tradeoff. In this architecture, pre-amplifier is a single pole, one stage amplifier.

The relation between unity gain frequency, gain, and 3-dB cutoff frequency is defined as below:

$$f_{cutoff} = \frac{f_u}{A_{preamp}} \tag{5.3}$$

Frequency response for a single pole amplifier is shown in Figure 5.6 [28].

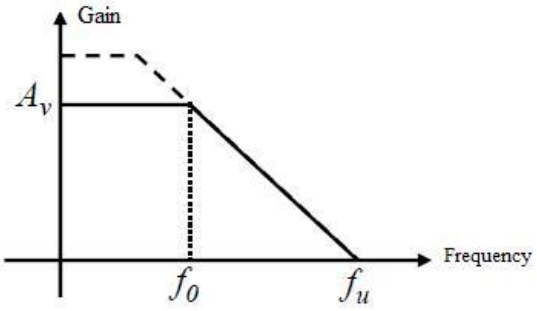


Figure 5.6. Frequency response of a single pole amplifier

If maintaining f_u is desired when the gain is increased, f_c or the pole value will decrease and consequently reduce the comparator speed.

An example of a comparator including latch and preamplifier is illustrated in Figure 5.7.

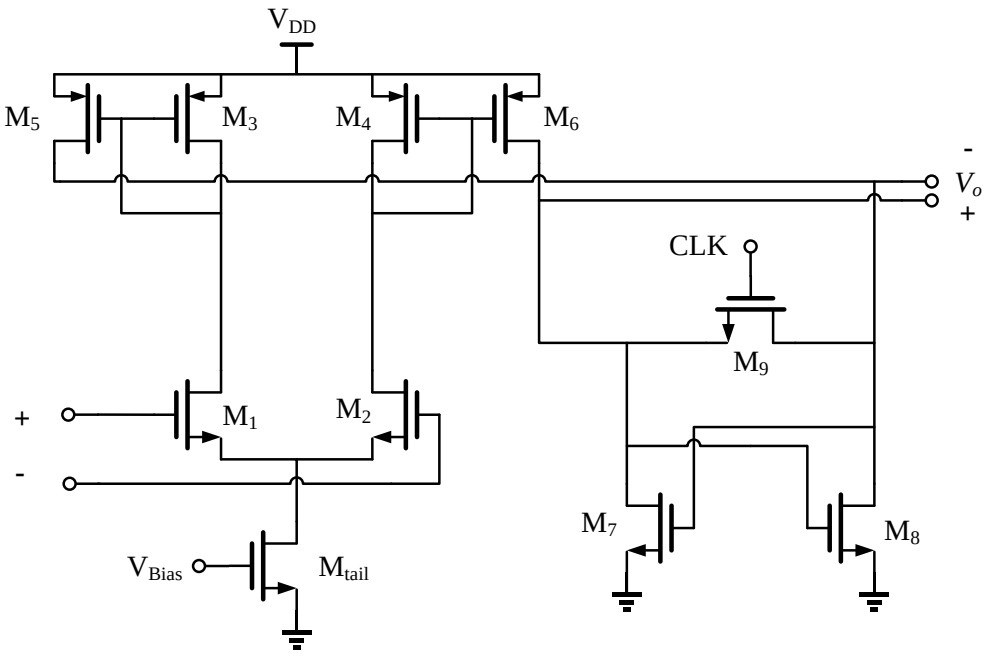


Figure 5.7. Comparator schematic including latch and pre-amplifier

Static latch consumes static power which is not attractive for low power applications. Comparator delay is demonstrated in Equation 5.4. It is in fact the delay time of a latched comparator, which is described in the next section. The only difference is that the pre-amplifier gain added to the equation.

$$T_d = \frac{C}{g_m} \ln\left(A_{preamp} \frac{V_{out}}{V_{in}}\right) \quad (5.4)$$

5.3.3 Dynamic Latched Comparator

Latch only comparators are clocked comparators. They operate based on amplification and positive feedback. An example of a latched only comparator is shown in Figure 5.8.

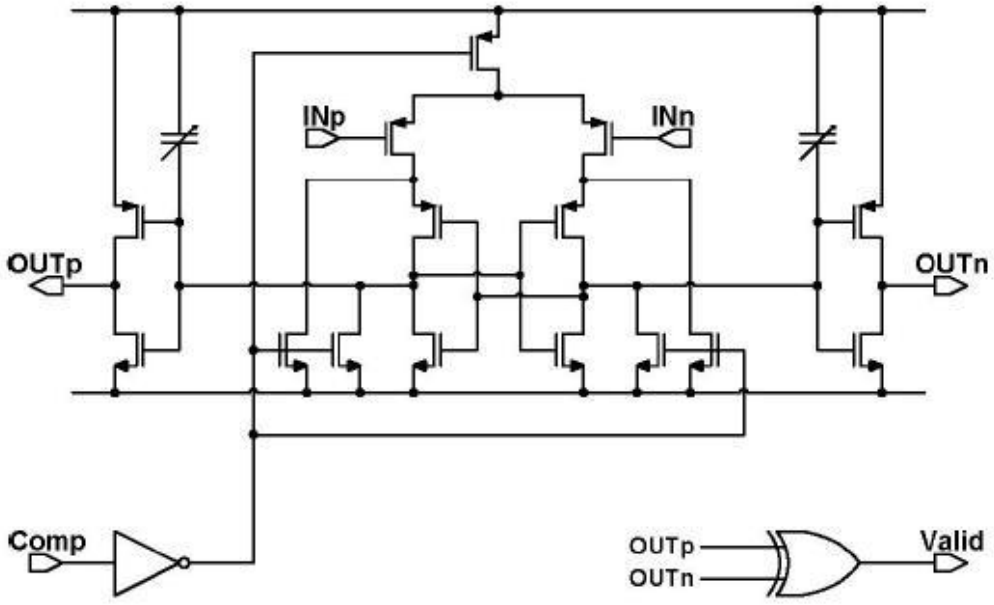


Figure 5.8. Dynamic Latched Comparator circuit [26]

Figure 5.9 shows the operation of the comparator. There are two operation phases, reset phase and regeneration or evaluation phase. In the reset phase, the output nodes are charged to supply voltage or discharged to the ground depending on the architecture of comparator. During the reset phase, the comparator tracks the input, and then in the regeneration phase the positive feedback produces a digital value at the comparator output. One of the advantages of dynamic latched comparators is their power efficiency since they only consume power in regeneration phase and there is no static power consumption in the reset phase.

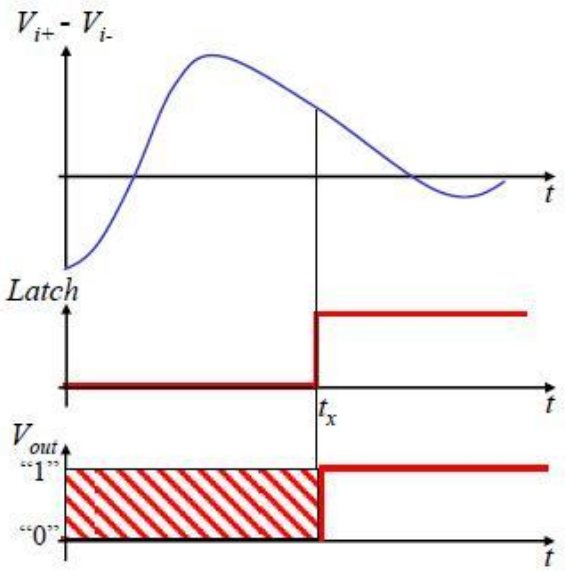


Figure 5.9. Latched Comparator Operation [28]

Dynamic latched architecture is the most power efficient comparator, however, it introduces large input referred offset which makes it unappealing for high resolution ADCs. This effect can be reduced by increasing the width of input transistors in differential pair. Employing offset cancelation techniques in the comparator implementation is also an effective approach to mitigate this problem. Furthermore, the offset voltage can be reduced by using a pre-amplifier which is previously described as a latched comparator with preamplifier. However, in all the mentioned methods, offset reduction is achieved at the cost of more power consumption.

Latched comparators are fast and are suited to be used in high speed ADCs. In order to derive the delay equation, the latched comparator can be modeled as a single pole comparator with positive feedback. The delay time of this comparator is calculated as below [28]:

$$T_d = \frac{C}{g_m} \ln\left(\frac{V_{out}}{V_{in}}\right) \tag{5.5}$$

Chapter 6
Implementation of Dynamic Latched Comparators

In this chapter, different architectures of dynamic latched comparators, aimed for low power application are designed, and then their performances are measured.

6.1 Simple Architecture of Dynamic Latched Comparator

Figure 6.1 illustrates an example of dynamic latch comparator presented in [18]. When clock signal is low, in reset phase, the reset transistors are switched on and charge the output nodes as well as drain nodes of the input transistors to supply voltage. Current source transistor (M_{tail}) is off, thus,no current flows through the circuit during the reset phase. When clock signal turns to high, reset transistors are disabled and the tail transistor is turned on. The inverters of the cross coupled circuitry inside the latch receive different amount of current depending on the input voltage and start to regenerate the comparator's output. In other words, the drain voltage of each input transistors (M_1, M_2) start to discharge from V_{DD} to ground with different rates depending on their input voltage. Once the drain voltage of either of the transistors drops below V_{DD}-V_{th}, NMOS transistor of the inverter is turned on and output node starts to discharge and positive feedback is activated. Once the output node reaches V_{DD}- $|V_{th}|$ the PMOS transistor of the other inverter is turned on. Consequently, the output voltage is regenerated and after regeneration phase one of the outputs is 1 while the other is 0.

In this configuration, the PMOS switch transistors (M_5, M_7, M_8, and M_{10}) which charge drain of input transistors to V_{DD} during the reset phase, increase the time period that input transistors are in saturation region during regeneration phase. As a result, higher gain is attained.

The drain nodes of input transistors have large voltage variations causing a large kickback noise. Furthermore, the variation of the operation region of input transistors causes voltage variation at their gates producing kickback noise. In the reset mode, differential input pair transistors are off. When the comparator enters the evaluation phase, V_{DS} is high and transistors are in

saturation region, then these nodes are discharged to zero in the regeneration phase causing transistors to enter the triode region [18].

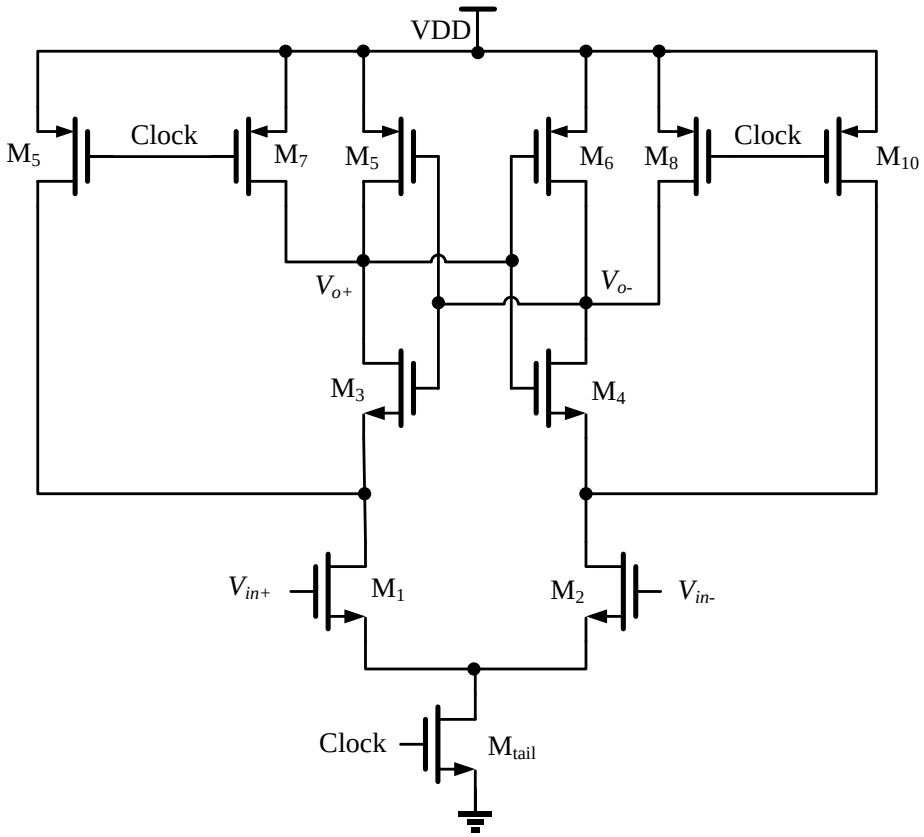


Figure6.1. N-type Latched Comparator Circuit

This implementation is not appropriate for low voltage applications since it is a stack of four transistors demanding excessive headroom voltage which is not feasible in low voltage technologies.

Moreover, for enhancing the comparator speed the current through the latch must be increased via increasing the tail current. Thus, the size of tail transistor should be increased which in turn, increases the current of differential input pair transistors. Consequently, the time period in which the input transistors are in saturation region decreases leading to a lower comparator gain. As a result, the effect of input-referred offset voltage is more significant. In other words, higher gain and thus lower offset voltage can be attained at the cost of speed reduction. Therefore, there is a tradeoff between speed, offset voltage and power consumption [23].

6.1.1 Simulation Results of N-type Latched Comparator

To verify the functionality and evaluate the performance, the comparator was simulated in Cadence and the results are shown in the following figures. Two inverters are inserted at the outputs of the comparator to recover the voltage level at the outputs of the comparator. In order to hold the result of the comparator during the reset phase, a NOR type Set-Reset Latch is used in this test bench. Figure 6.2 shows the SR latch.

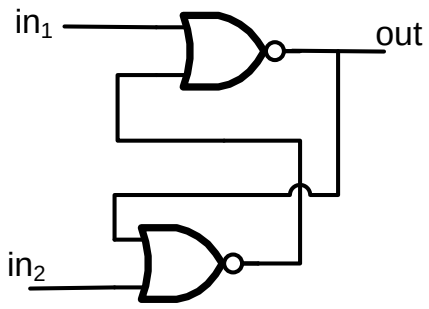


Figure6.2. NOR type SR latch

In 65nm technology the minimum width and length of a CMOS transistor are 135nm and 60 nm, respectively. Sizing of the input transistors has a great impact on offset voltage. As shown in (6.1), increasing the size of the input transistors results in reduction of the input referred offset voltage.

$$V_{offset} \propto \frac{1}{\sqrt{W.L}} \tag{6.1}$$

In this design, the input transistors are three times larger than the minimum width in order to decrease the input-referred offset voltage.

As it is mentioned above, the tail width is set to the minimum width in order to minimize the power consumption and also achieve higher gain which results in lower offset voltage. In order to decrease the leakage power, the length of transistors is chosen two or three times larger than the minimum length.

By employing both high V_T and low V_T transistors, lower leakage power is achieved without any speed reduction. Table 6.1 shows the aspect ratio of the transistors of the comparator.

Table6.1. Optimized Size of Transistors

Component	Width(µm)	Length(µm)	Transistor type
M_{tail}	0.135	0.12	High V_T
$M_{1,2}$	0.405	0.18	Low V_T
$M_{3,4}$	0.270	0.12	Low V_T
$M_{5,6}$	0.540	0.12	High V_T
$M_{7,8,9,10}$	0.135	0.12	High V_T

The comparator was simulated with V_{DD}= 1V, clock frequency= 100 kHz, input frequency = 5 kHz with full swing, and temperature = 27ºC.
The comparator operation is shown in Figure 6.3.

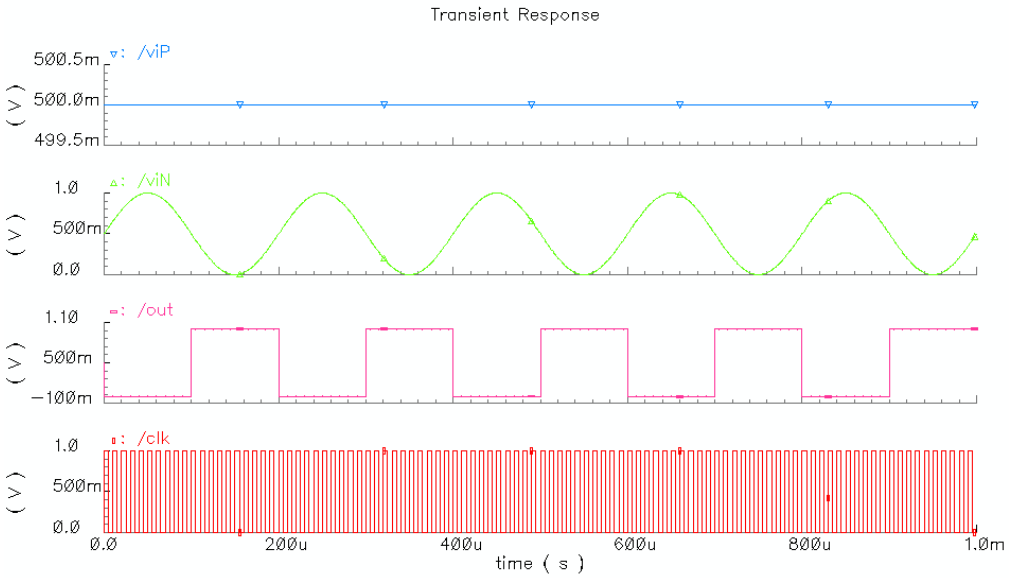


Figure6.3 Transient response of the comparator

In order to measure the input referred offset, the device mismatch is considered and a method which relies on Monte Carlo analysis is used. For this purpose a simple test bench is created. The input voltage is a ramp which is sampled with a sample and hold. The obtained staircase signal is applied to the input of the comparator and a DC threshold voltage is applied to the other input of the comparator [24]. The test bench circuit is shown in Figure6.4.

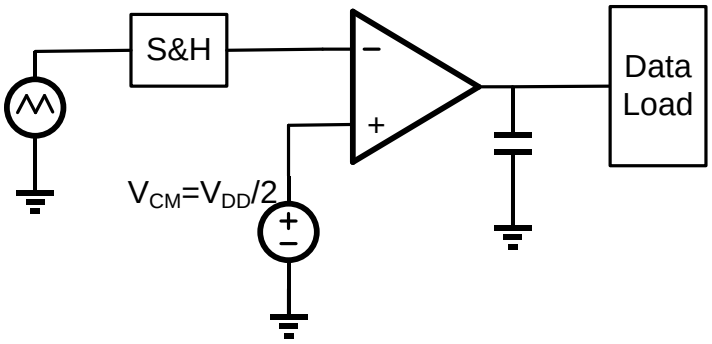


Figure6.4. Test bench circuit for offset simulation

First, Monte-Carlo simulation is run for 500 times and the output results are stored in a file. Then in MATLAB, by performing some post-processing on the stored results, the input referred offset is evaluated. Figure 6.5 shows the probability of the occurrence of "1" at the output versus the input voltage. The statistical properties of the comparator such as threshold voltage and offset can be extracted from this curve. Offset is defined as the deviation from the threshold voltage.

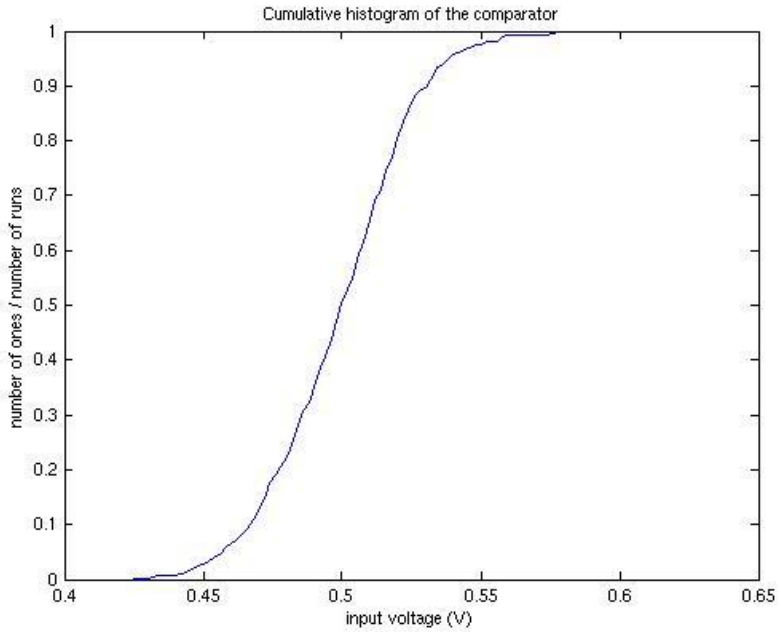


Figure6.5. Monte-Carlo simulation Results

The simulation results are presented in table 6.2.

Table6.2. Simulation results

Performance Metric	Value	Unit
Power Consumption	276	pW
Input-Referred Offset voltage	8.1	mV
Propagation Delay	2.1	ns

Since this comparator aimed for low power and low speed application, delay is in the last priority. The results show that the power consumption is quite low. The offset voltage is higher than one LSB which is reasonable for dynamic latch comparator. Further reduction of offset voltage is achievable by using offset cancelation techniques at expense of higher power consumption and more complexity.

In order to evaluate the scalability of the comparator with supply voltage, the comparator is simulated with different supply voltages. The power consumption and propagation delay of the comparator versus different supply voltages are given in table6.3.

Table6.3. Simulation results for scaled V_{DD}

V_{DD} (V)	Power Consumption (pW)	Propagation Delay (ns)
1	276	2.1
0.8	216	5.3
0.6	159	31.5
0.4	107	1400

According to the results, decreasing V_{DD} reduces the power consumption and increase the delay of the comparator. For V_{DD} = 0.4 V the propagation delay is 1.4 µs which is quite large so this architecture does not perfectly work under 0.4V.
This comparator shows a relatively constant offset voltage over different supply voltages.

6.2 Energy Efficient Dynamic Two-Stage Latched Comparator

To mitigate the problems of the previous structure, dynamic two-stage latched comparator has been proposed. This comparator is energy efficient and fast and has lower input referred offset voltage. An example of two-stage comparator is illustrated in Figure 6.6 [16].

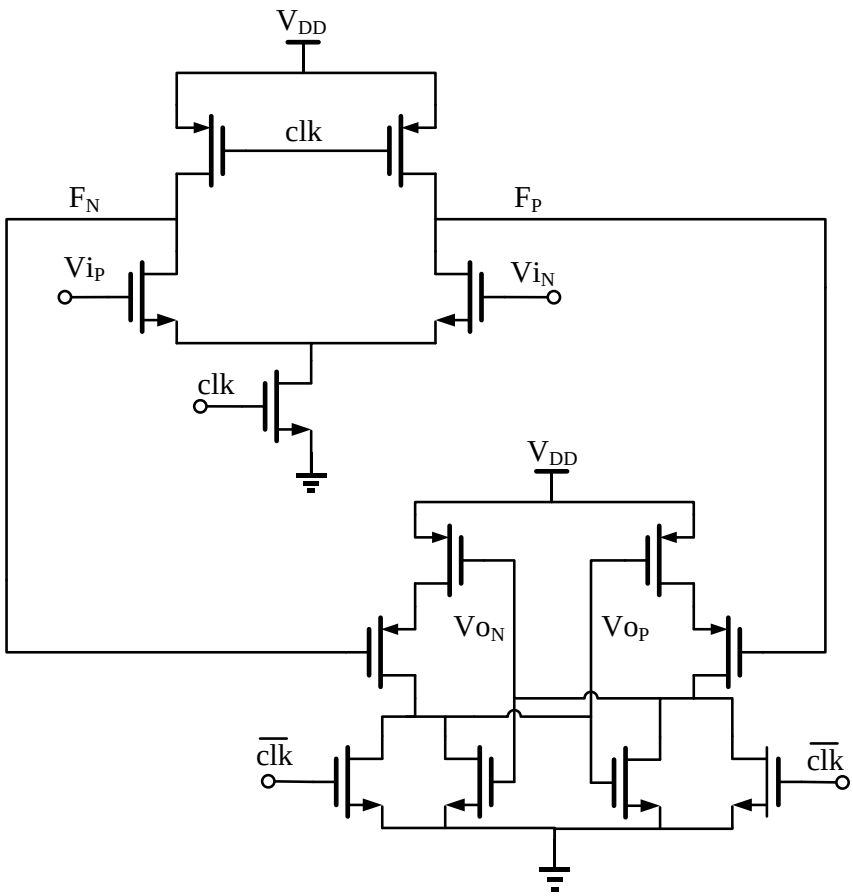


Figure6.6. comparator schematic

The first stage is a voltage amplifier and the second stage is a latch. During the reset phase when clock signal is low, PMOS transistors in the first stage charge F nodes to V_{DD} and turn off the latch stage. In this phase, the output nodes are reset to zero through NMOS switches in the latch stage. This architecture is power efficient and fast due to low capacitance at F nodes which are mainly drain diffusion capacitances of NMOS and PMOS transistors connected to these nodes.

When clock turns to high in regeneration phase, the tail transistor is turned on and amplification in the first stage is initiated. F nodes start to discharge through differential input pair transistors in the first stage. These nodes are discharged with different rates proportional to the input voltage. Once either of the output nodes of the first stage (F nodes) drops to an amount around V_{th} of the input transistors of the latch stage, these transistors are switched on and amplification starts in the second stage. Gradually, the output voltage increases and positive feedback system is activated and generates output level of high and low voltage in the regeneration phase.

The first stage consumes power only when the parasitic capacitances at F nodes are discharged. The Second stage dissipates power until the rail-to-rail output voltage is generated.

6.2.1 Simulation Results of Two-Stage Latched Comparator

The comparator was simulated in Cadence to examine the functionality and performance. The results of the simulation are presented in the following. In this comparator, two inverters are added to recover the voltage level at the output of the comparator. A NAND type SR latch is also used to hold the comparator result during the reset phase. NAND type SR latch is shown in Figure 6.7.

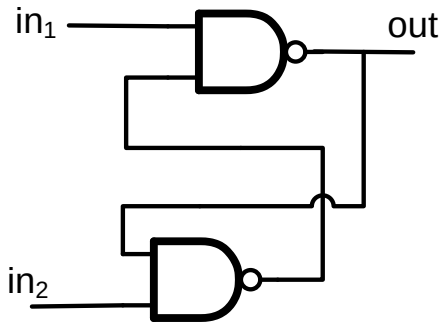


Figure6.7. NAND type SR latch

The transistors are sized to meet the requirements targeting minimum power consumption. First, all the transistors are minimum size with double length to mitigate the leakage problem. Then for improving the performance in terms of offset voltage and delay, input transistors are chosen to be three times larger than the minimum size. The optimized transistor sizes are presented in table 6.4.

In order to further decrease the leakage power while maintaining the speed of the comparator, High V_T transistors are employed occasionally.

Table6.4. Aspect ratio of the transistors

Component	Width(µm)	Length(µm)	Transistor type
M_{tail}	0.135	0.12	High V_T
$M_{1,2}$	0.405	0.18	Low V_T
$M_{3,4}$	0.135	0.12	Low V_T
$M_{5,6}$	0.135	0.12	High V_T
$M_{7,8}$(pmoslatch)	0.540	0.12	High V_T
$M_{9,10}$*(nmoslatch)*	0.270	0.12	Low V_T
$M_{11,12}$	0.135	0.12	Low V_T

The comparator was simulated under V_{DD}= 1V, Clock frequency= 100 kHz, input frequency = 5 kHz with full swing, and temperature = 27ºC.

For measuring input referred offset voltage, Monte-Carlo simulation is run for 500 times and the same test bench as the previous case is used. Figure 6.8 shows the results of the Monte-Carlo simulation after performing post-processing in MATLAB. Offset can be extracted from this curve.

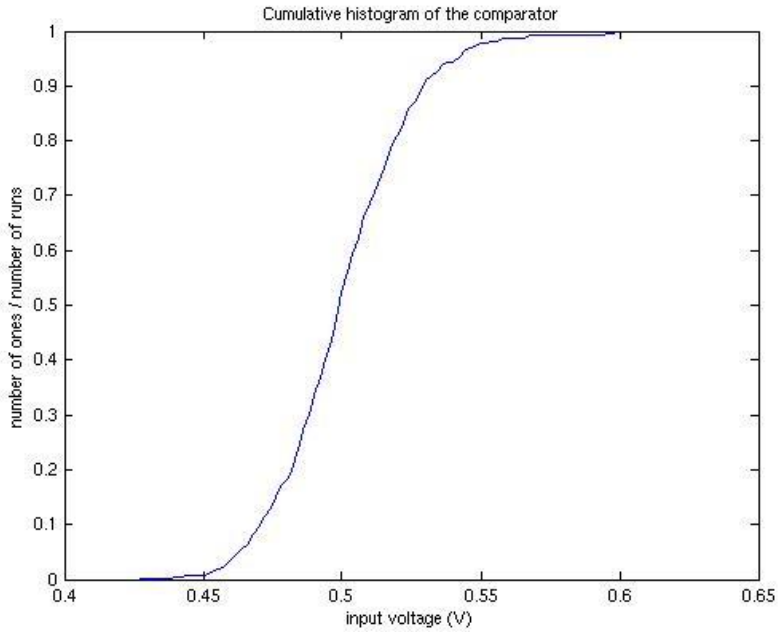


Figure 6.8. Monte-Carlo Simulation Results

The simulation results are presented in table6.5.

Table6.5. Simulation results

Performance Metric	Value	Unit
Power Consumption	257	pW
Input-Referred Offset voltage	7.2	mV
Propagation Delay	1.27	ns

Compared to the latch-only comparator, two-stage latch comparator exhibits lower offset and higher speed while consuming almost the same power. As mentioned before, further reduction of offset voltage is achievable by using offset cancelation techniques at expense of higher power consumption and more complexity.

Scalability with different supply voltages is verified by simulating the circuit with different V_{DD}. Power consumption and delay of the comparator versus different supply voltages are given in table6.6.

Table6.6. Simulation results over the scaled supply voltage

V_{DD} (V)	Power Consumption (pW)	Propagation Delay (ns)
1	257	1.27
0.8	199	2.7
0.6	144	19
0.4	94	657

As VDD decreases, power consumption decreases while propagation delay increases. Compared to the latch-only comparator, this structure is functional at V_{DD} = 0.4 V and the propagation delay is 657 ns which is smaller than the delay of the previous comparator.
This comparator shows a relatively constant offset voltage for different supply voltages.

6.3 Modified Two-Stage Latched Comparator

In this architecture, two inverters are inserted between the two stages of the conventional two-stage dynamic latched comparator in order to strengthen the voltage signal at Di nodes providing higher regeneration speed. In addition to the advantage of the conventional two-stage dynamic latched comparator such as power efficiency, high speed, and low kickback noise, this architecture provides lower input-referred offset. The comparator schematic is shown in Figure 6.9 [23].

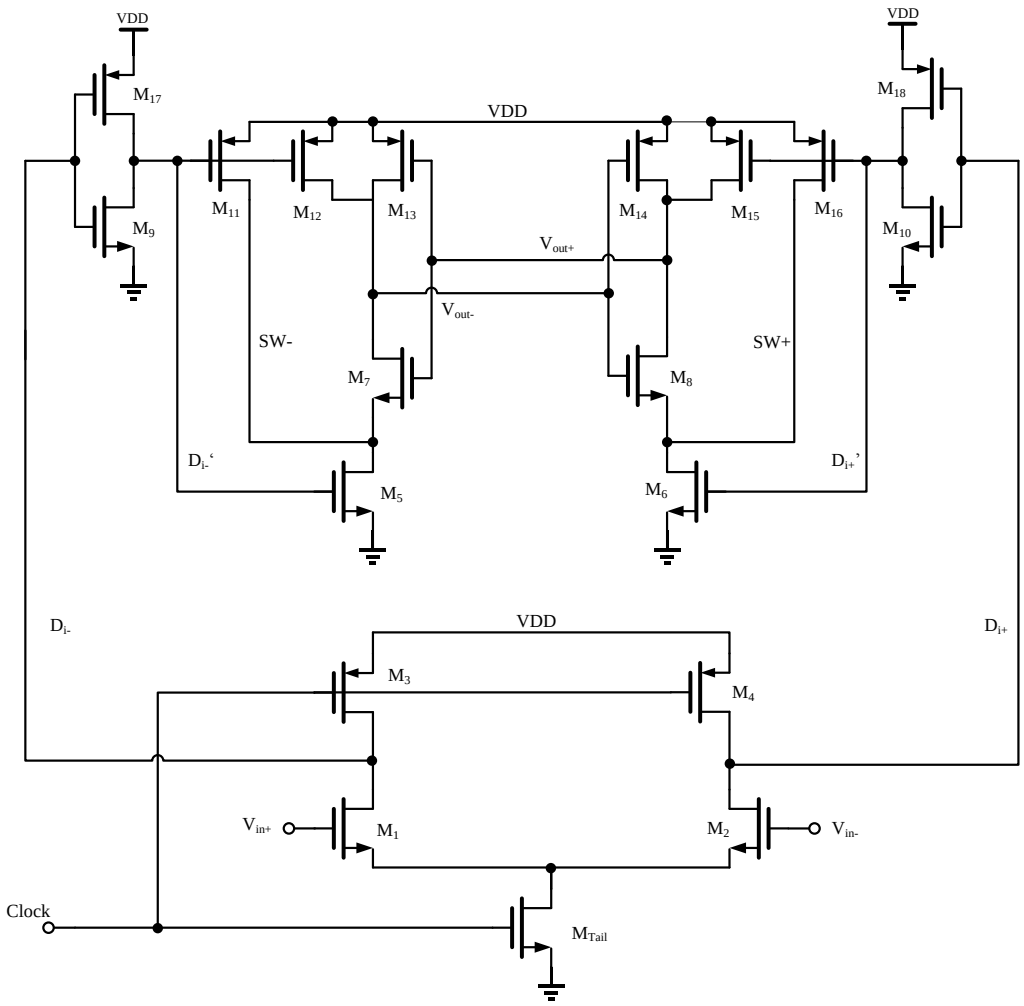


Figure 6.9. Transistor-level schematic of comparator2

In the reset phase when clock signal is low, PMOS transistors in the gain stage are on (M_3, M_4) and charge the capacitances of Di nodes to V_{DD} and subsequently the Di' nodes are discharged to ground, thus, there is no static path and no static power dissipation during reset phase. The Di' nodes are discharged to ground and the PMOS transistors of the regeneration stage turn on and charge the output nodes as well as regenerative nodes i.e. drain of the NMOS transistors (M_5 and M_6) to V_{DD}.

During evaluation phase when clock signal turns to high, the Di nodes discharge through input and tail transistors to the ground with different rate, depending on the input voltage. While Di nodes are discharged, Di' nodes start to charge from 0 to V_{DD} with different rate. Once either of Di' nodes reaches V_{th}, the NMOS transistor (M_5 or M_6) in the second stage is switched on, then the other transistor is also turned on.
As a result, latch is activated and regenerates the digital voltage at the output from the small $\Delta V_{Di'}$.

6.3.1 Simulation Results of Modified Two-Stage Latched Comparator

This comparator was simulated in Cadence. In this structure for recovering the output voltage, two inverters are added at the output and like previous comparator a NAND type SR latch is used to keep the comparator result during reset phase.

Sizes of the transistors are optimized to meet the required specification. The priority is the power consumption. The component sizes are presented in table 6.7.

In order to further decrease the leakage power while maintaining the speed of the comparator, in some places High V_T transistors are employed. Increasing the sizes of the inverters between the stages, results in lower propagation delay.

Table6.7. Aspect ratio of the transistors

Component	Width(µm)	Length(µm)	Transistor type
M_{tail}	0.135	0.12	High V_T
$M_{1,2}$	0.405	0.18	Low V_T
$M_{3,4}$	0.135	0.12	Low V_T
$M_{5,6}$	0.135	0.12	High V_T
$M_{7,8}$	0.27	0.12	High V_T
$M_{9,10}$	0.135	0.12	Low V_T
$M_{11,12,15,16}$	0.135	0.12	Low V_T
$M_{13,14}$	0.54	0.12	High V_T
$M_{17,18}$	0.27	0.12	Low V_T

The comparator was simulated under V_{DD}= 1V, Clock frequency= 100 kHz, input frequency = 5 kHz with full swing, and temperature = 27ºC.

For measuring input referred offset voltage, Monte-Carlo simulation is run for 500 times and same test bench is used as for the previous one. Figure 6.10 shows the results of the Monte-Carlo simulation after performing post-processing in MATLAB. Offset can be extracted from this curve.

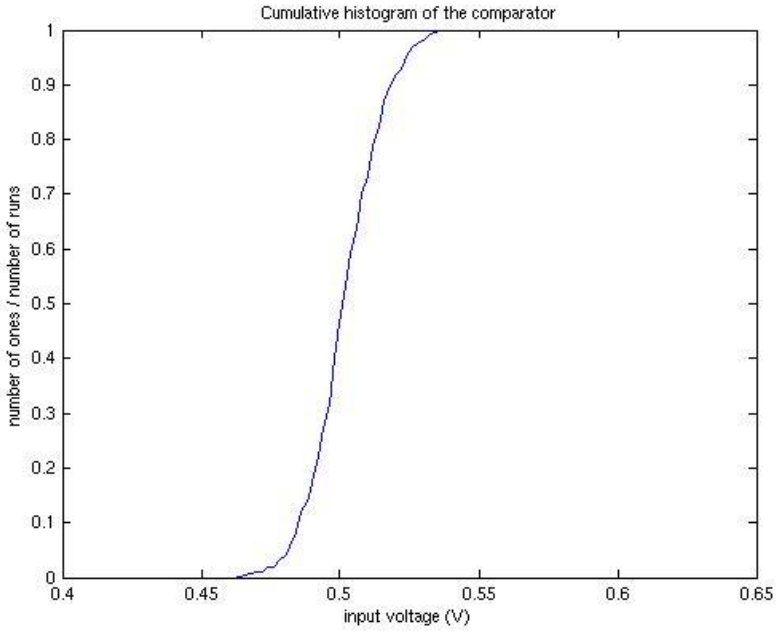


Figure6.10. Monte-Carlo Simulation Results

The simulation results are presented in table below:

Table6.8. Simulation results

Performance Metric	Value	Unit
Power Consumption	1.2	nW
Input-Referred Offset voltage	5.2	mV
Propagation Delay	0.92	ns

In compare to the two-stage latch comparator, this architecture shows lower offset and higher speed while consuming more power.

Scalability with different supply voltages is verified by simulating the circuit with different V_{DD}. Power consumption and delay of the comparator versus different supply voltages are given in table 6.6.

Table6.6. Simulation results over the scaled supply voltage

V_{DD} (V)	Power Consumption (nW)	Propagation Delay (ns)
1	1.2	0.92
0.8	0.529	2.1
0.6	0.274	15
0.4	0.130	382

This comparator also shows a relatively constant offset voltage for different supply voltages. The propagation delay and power consumption of the comparators are illustrated in the figures below:

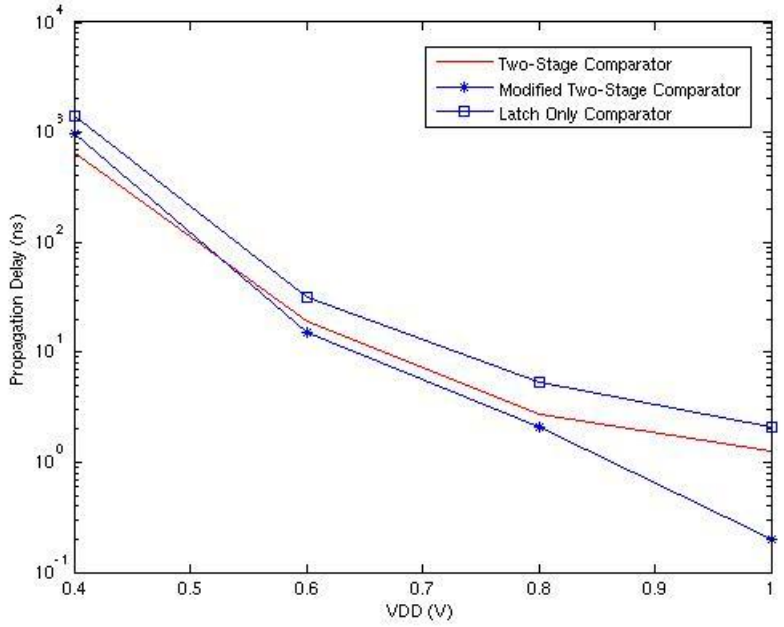


Figure6.11. Propagation delay comparison

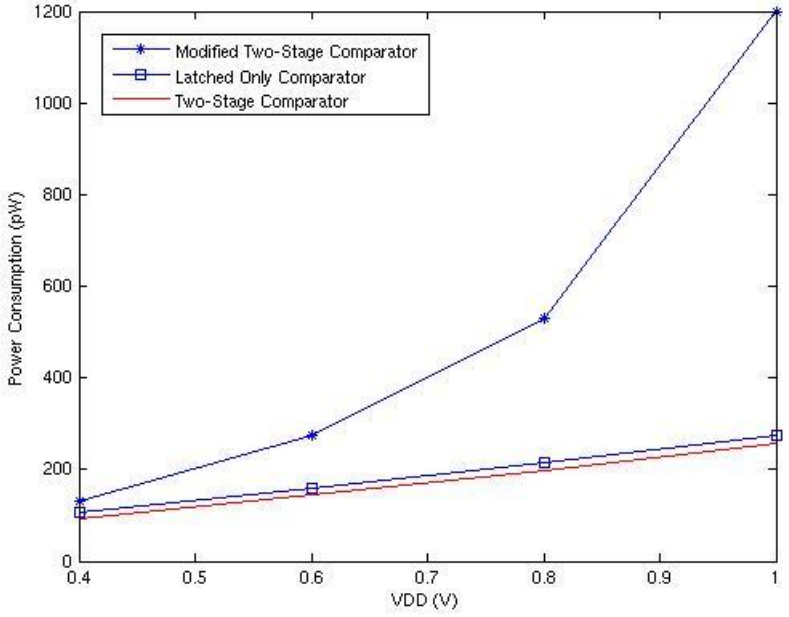


Figure6.12. Power consumption comparison

Since the priority is the power consumption, the last comparator consumes more power while the first two comparator designs are ultra-low power, but the two-stage comparator has lower offset, which makes it a good candidate for the ADC in pacemaker.

Chapter 7
Implementation of SAR ADC and Performance Evaluation

In this chapter, first the implementation of 10-bit SAR ADC in 65nm CMOS process technology at 1kS/s and supply voltage of 1V is investigated followed by the design of 10-bit charge redistribution DAC, then test bench and simulation setup for verification of the performance is discussed and finally, simulation results for low supply voltage as well as high temperature are presented to evaluate their influence on power consumption.

7.1 Implementation of SAR ADC

First, the SAR A/D converter was simulated in high level model. Then, each block was replaced with its transistor level design. Based on the results obtained in the previous chapters the suitable architectures for the blocks were chosen. In this work, a dynamic two-stage comparator (see Chapter 6 for more details), a SAR controller containing a sequencer and a shift register, SAR logic type 1(Chapter 4), and charge redistribution DAC were selected in order to meet the low power requirements. In the following, the design of D/A converter is provided.

7.1.1 Design of 10-bit D/A Converter

In this thesis a 10-bit charge-redistribution DAC with BWC array was implemented in 65nm CMOS process. Figure 7.1 shows the block diagram of the 10-bit DAC.

There are three phases of operation to perform a conversion:

First, in the sampling phase switch S_1 connects the top plats of all capacitors to the V_{CM} and the bottom plates are connected to V_{IN}. Thus, the input voltage is sampled on the capacitor array.

During the hold phase, S_1 is opened and the rest of switches connect the bottom plates to ground therefore a charge of $-V_{IN} + V_{CM}$ is stored in the capacitor array.

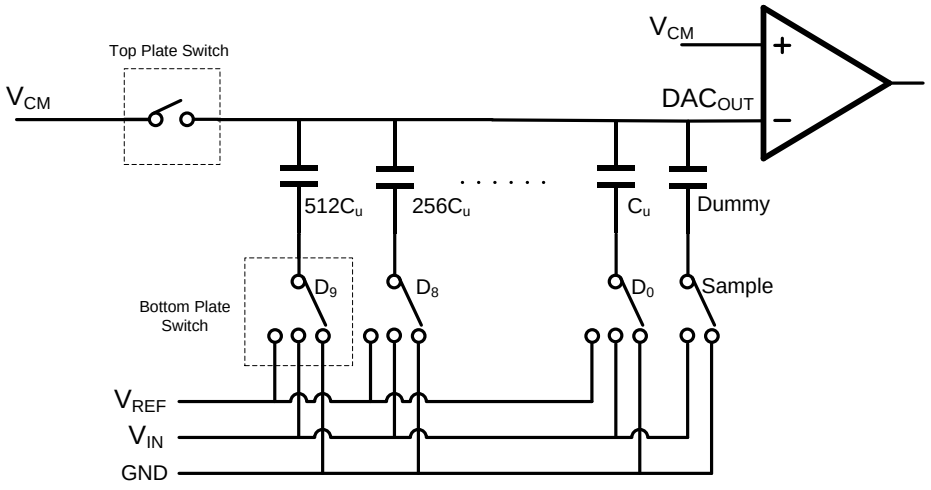


Figure7.1. DAC schematic view

In redistribution phase, the digital code determines the status of the switches and the actual conversion is performed in this phase. In the beginning of the conversion, D_9 is high so the MSB capacitor is connected to V_{REF}. At this step the output voltage of the DAC is equal to $-V_{IN} + V_{CM} + 0.5V_{REF}$ and is compared to V_{CM}. Based on the comparator result, D_9 remains connected to V_{REF} if the comparator output is one, or change the connection to ground when the result of the comparator is zero. Thus, the MSB is defined. Next, D_8 is connected to V_{REF}. Depending on the value of D_9, $V_{out\text{-}DAC}$ is $-V_{IN} + V_{CM} + 0.5D_9 \cdot V_{REF} + 0.25V_{REF}$ and is compared to V_{CM}. All the bits are generated successively and $V_{out\text{-}DAC}$ in the last step is defined as below:

$$V_{out_{DAC}} = -V_{IN} + V_{CM} + D_9\frac{V_{REF}}{2} + D_8\frac{V_{REF}}{4} + \ldots + D_2\frac{V_{REF}}{2^8} + D_1\frac{V_{REF}}{2^9} + D_0\frac{V_{REF}}{2^{10}} \qquad (7.1)$$

Binary-Weighted Capacitor Array

The linearity of ADC is restricted by the linearity of the DAC which is caused by the capacitor mismatch. Therefore, choosing an appropriate value for the unit capacitance is vital. Reducing the unit capacitance value improves the linearity but deteriorates the noise performance at the same time due to $\frac{KT}{C}$ thermal noise. The minimum value of the unit capacitor is limited by several factors including $\frac{KT}{C}$ thermal noise, capacitor matching and the value of the parasitic capacitances [11].

A unit capacitance of 20fF is chosen in this design. The values of the other capacitors in the capacitor array are defined based on the unit capacitance.

Switches Implementation

The operation of the bottom plate switches are presented in table 7.1. The block diagram of the switch can be obtained from the table.

Table7.1. Bottom switch operation

Sample	Digital data	V_{Bottom_plate}
1	x	V_{IN}
0	1	V_{REF}
0	0	GND

NMOS switches can properly pass a zero while PMOS switches can pass a strong one. On the other hand, CMOS transmission gate combined both features of NMOS and PMOS switch and is capable of properly passing both zero and one. It also benefits from low on-resistance [25].

In this design, V_{REF} is set to V_{DD}; therefore PMOS switch is used for V_{REF}. NMOS switch is employed to ground the bottom plate. Since V_{in} varies from 0 to 1, CMOS TG is chosen for V_{in}. Figure 7.2 (a) shows the block diagram of bottom plate switches [12].

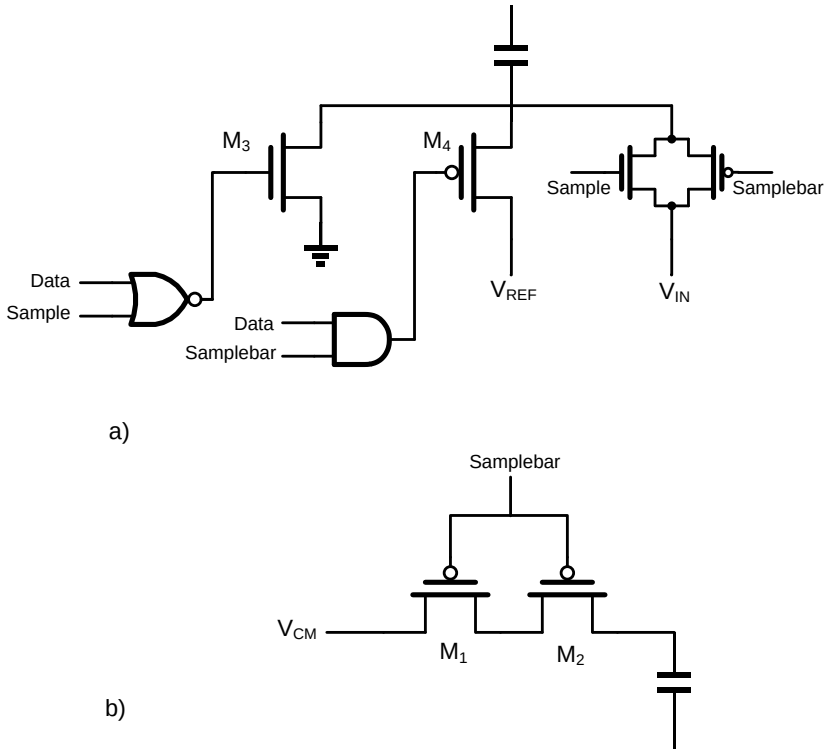


Figure7.2. Schematic views of a) bottom plate switch and b) top plate switch

The leakage current contribution of the top plate switch is significant in this low speed design since most of the time this switch is off and it only turns on during the sampling phase. The leakage current of the top plate switch adversely affect the linearity of the DAC and consequently the linearity of ADC [13]. In order to alleviate this problem, a stack of two PMOS switches are used in series; this switch is depicted in Figure 7.2 (b).The sizes of the switches are presented in table 7.2.

Table 7.2. Sizing of the switches

Transistor	W(µm)	L(µm)
M_3	0.135	0.06
M_4	0.54	0.12
$TG_{\_NMOS}$	0.135	0.06
$TG_{\_PMOS}$	0.54	0.06
$Inv_{\_NMOS}$	0.135	0.12
$Inv_{\_PMOS}$	0.45	0.12
$NOR_{\_NMOS}$	0.135	0.12
$NOR_{\_PMOS}$	0.81	0.12
$NAND_{\_NMOS}$	0.27	0.12
$NAND_{\_PMOS}$	0.45	0.12
$M_{1,2}$	0.135	0.06

7.2 Performance Evaluation

Figure 7.3 represents the test bench for ADC performance measurement. As indicated in the figure, the 10-bit output data is stored in a Verilog-A file. Then, the stored data is read in MATLAB and post-processing operations are performed to measure the dynamic performance of ADC including SFDR, SINAD and ENOB.

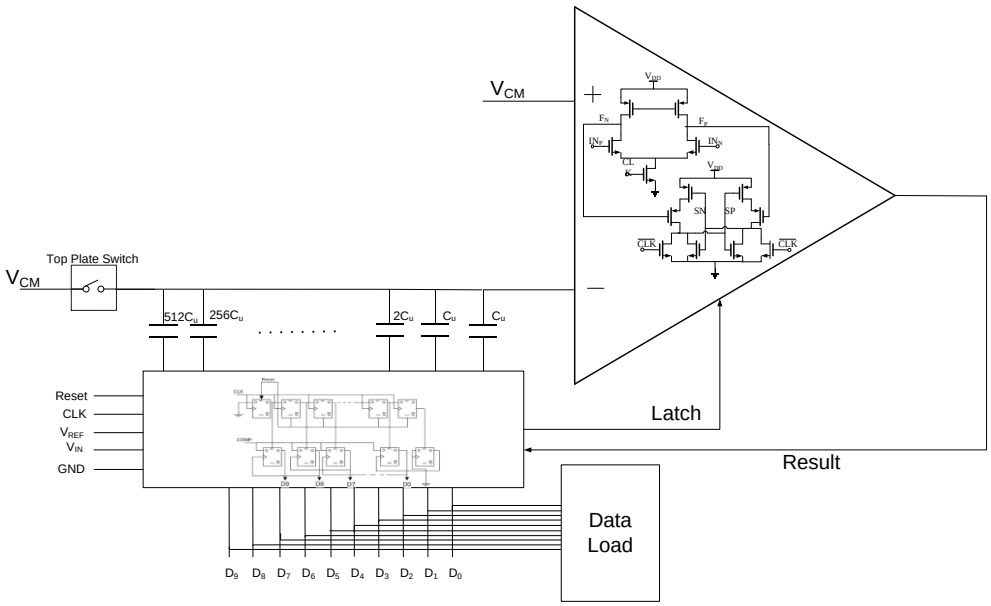


Figure7.3. SAR ADC test bench for measuring dynamic performance

7.2.1 Power Consumption measurement

The ADC is simulated with $V_{DD}= V_{REF} = 2.V_{CM} = 1V$, and sampling frequency of 1kS/s. The input signal is a full swing sinusoidal with $f_{in}= 450Hz$. The simulation results under 27ºC and 80ºC temperatures are presented in table 7.3.

Table7.3. Power consumption of different blocks of ADC

Block	Power Consumption at 27ºC (nW)	Power Consumption at 80ºC (nW)
DAC	10.4	11.1
SAR	1.54	2.028
Comparator	0.26	0.620
Clock Power	0.208	0.224
Total	12.408	13.97

The total power consumption of the implemented SAR ADC including the clock power is almost 12.4nW. The distribution of power consumption between different blocks of ADC is shown in figure 7.4.

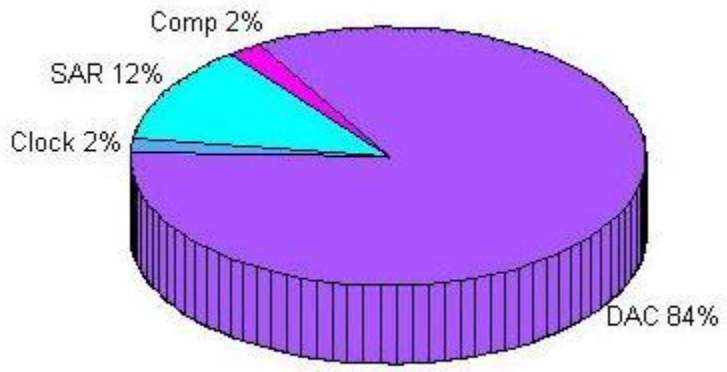


Figure7.4. Power distribution

As shown in the Figure 7.4, DAC consumes the largest amount of power among other blocks which is %84. As discussed above, the unit capacitance in the DAC is chosen to be 20 fF. After DAC, SAR control logic with %12, clock power and comparator both with %2 consumes the largest amount of power respectively.

In order to testify the voltage scalability of the ADC, it is simulated with scaled supply voltage. Table 7.4 presents the power consumption of ADC blocks. The ADC can properly operate with scaled supply voltage down to 0.5V and consumes a minimum power of 6.28nW.

Table 7.4. Power consumption (nW)

Block	V_{DD}=1V	V_{DD}=0.8V	V_{DD}=0.6V	V_{DD}=0.5V
DAC	10.4	7.6	6.12	5.44
SAR	1.54	1.1	0.79	0.64
Comparator	0.26	0.2	0.15	0.11
Clock Power	0.208	0.157	0.109	0.085
Total	12.408	9.057	7.17	6.275

7.2.2 Dynamic Performance Evaluation

As described in Chapter 2 the dynamic performance is evaluated by calculating the SFDR, SINAD, and ENOB of ADC. For this purpose, a full swing sinusoidal wave with f_{in} = 30.273438 Hz which is based on coherent sampling is applied to the input of ADC. The simulation is performed to achieve 1024 samples with sampling frequency of 1kS/s. Then, Fast Fourier Transform of the stored output data is executed in MATLAB and by performing some post processing the SFDR, SINAD, and ENOB are measured.

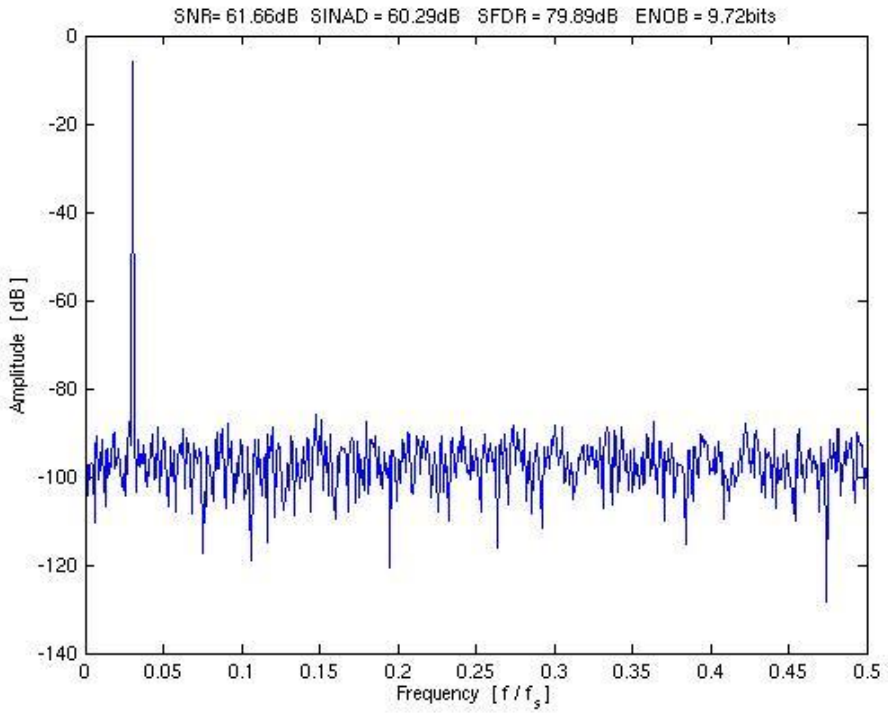


Figure7.5. FFT of the ADC output for F_{in}=30.273438Hz

The FFT of 10-bit ADC output is shown in Figure7.5. The simulation results predict that the ADC have SINAD=60.29, SFDR=79.89, and achieves 9.72 of ENOB which are reasonable for schematic level simulation.

Energy per conversion-step can be calculated using FOM definition of ADC which is given by Equation 7.2 [16].

$$FOM = \frac{P}{2^{ENOB}.F_S} \text{ (fJ/conversion-step)} \qquad (7.2)$$

Table 7.5 summarize the performance parameters of the designed SAR ADC.

Table 7.5. Performance parameters of ADC

Performances	Result	Unit
Process Technology	65nm	-
Supply Voltage	1	V
Resolution	10	bits
Sampling Frequency	1	kS/s
Power Consumption	12.4	nW
SINAD	60.29	dB
SFDR	79.89	dB
ENOB	9.72	bits
FOM	14.7	fJ/conversion-step

Finally, a result comparison with other works is presented in table 7.6.

Table 7.6. Comparison with other published works

Performances	This work	[30]	[26]	[31]	[16]
Technology	65nm	0.18µm	90nm	0.18µm	65nm
Supply Voltage (V)	1	1	1	1	1
Resolution	10	12	9	8	10
Sampling Frequency(S/s)	1k	100k	20M	400k	1M
ENOB	9.72	10.55	7.8	7.31	8.75
Power Consumption(W)	12.4n	25µ	290µ	6.15µ	1.9µ
FOM (fJ/conversion-step)	14.7	167	65	97	4.4

Chapter 8
Summary

This thesis presents implementation of a 10-bit SAR ADC operating at 1kS/s and supply voltage of 1 V in 65nm CMOS technology. The power consumption of 12.4nW is achieved. The ADC employs a charge-redistribution DAC, a dynamic two-stage comparator, and a SAR control logic containing a sequencer and a ring counter. The ADC exhibits good performance and achieves an FOM of 14.7fJ/conversion-step with ENOB of 9.72 bit.

In this work, after a deep study on different possible structures of SAR logic, they are implemented and compared in terms of power consumption and speed. Comparison results obtained in Chapter 4 indicate that the designed conventional SAR logic with a sequencer and a ring counter, consumes the lowest power of 1.2nW at 1kS/s. Thus the power consumption of the SAR control logic is significantly reduced and consumes only %12 of the total power.

Designing the comparator is a crucial part of ADC design. In this work, comparator performance metrics as well as several types of comparators are studied, such as open loop comparator, pre-amplifier preceding a latch comparator, and dynamic comparator. Based on these studies, dynamic comparators consume lower power compared to the other approaches. Therefore, diverse architectures of dynamic comparators are implemented and compared regarding power consumption, speed, and accuracy. Consequently, the dynamic two-stage comparator is selected to be used in the designed ADC.

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