Level Crossing Analog to Digital Converters

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Under the Guidance of

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Outline

- Motivation
- Theory of level cross sampling scheme
- Reported level crossing ADC architectures
  - Level crossing asynchronous ADC
  - Signal dependent variable resolution ADC
  - Adaptive asynchronous ADC
- Proposed level crossing ADC architectures
  - Architecture for high activity signals
  - Architecture for low activity signals
- Conclusion & Future work
- References

Building Blocks for proposed ADC

- ADC specifications
  - Technology - UMC 180nm
  - Power supply - 1.8 V
  - Resolution - 8-bit
  - Peak to peak analog input voltage - 1 V (0.4 to 1.4)
  - Maximum analog input frequency - 20K Hz
- Analog Blocks
  - Clocked Comparator
  - Track & Hold
  - Non Overlapping Clock Generator
  - Driver Network
  - Binary Weighted Capacitor Array

Comparision between architectures

Future work

- Future Work
  - Complete the connections between individual modules.
  - Complete the layout of capacitor array & Switching network.
  - Complete the place & route of controller blocks.
  - Send both designs for tapeouts in August.
  - Modify the proposed architecture for repetitive signals.
- Problems encountered when implementing design
  - Applying Timing constraints for multiple clock domains.
  - Problem with the capacitor layout because of multiplier.
  - Problem with the capacitor layout because of parasitics.
- Prsently working on Connecting digital controller circuit with analog blocks.

References


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