Ph.D.Progress Report

High Speed Signal Generation in CMOS Technologies for Emerging Optical Communications

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Abstract

Analog Front End (AFE) is an important real world interface for all the Digital Processing Systems. Important blocks of the AFE are Analog to Digital converter (ADC) and Digital to Analog converter (DAC) for optical communication, telephony, Satellite communications applications, Medical Instruments etc. High speed and high spectral efficiency (SE) optical modulation/detection techniques are essential for future cost-effective optical transport networks. Coherent detection with digital signal processing (DSP) is very promising to achieve high SE with the powerful equalization of the linear distortion created by chromatic dispersion (CD) and polarization-mode dispersion (PMD).

The constant advance of CMOS digital circuit process has lead to the trend of digitizing an analog signal and performing digital signal processing as early as possible in a signal processing system, which in turn leads to an increasing requirement on Digital-to-analog (DAC) and analog-to-digital converter (ADC). Pseudo Random Bit Sequence (PRBS) generators are widely used for testing the correct functionality of high speed digital and analog circuits when no other sources are available. It is important that the PRBS generator be able to produce sufficient long sequences. They can also be integrated on the same chip as the device under test (DUT) for built-in self test (BIST) purposes. This also helps to reduce noise, interconnect delay parasitic capacitances and cost so on-chip testing is preferred for high frequency applications.

Testing high-speed DACs is even more challenging, as it requires large number of high-speed synchronized input signals with specific test patterns. In this work, $(2^9 - 1)$ PRBS generator is targeted for 20Gb/s data-rate, 10GHz clock frequency with 1V power supply in 90nm UMC cmos process. Pseudo Random Binary Sequence is essentially a random sequence of binary numbers. The implementation of PRBS generator is based on the linear feedback shift register (LFSR). A sequence of consecutive $(N \times (2^n - 1))$ bits comprise one data pattern, here n is number of bits and this pattern will repeat itself over time. Designed PRBS generator has been simulated after parasitic capacitance and resistance extraction. It is working upto 9Gb/s data rate and multiplexing is done after modifying the conventional architecture to ensure the correct operation of multiplexer for 18Gb/s data-rate as a output. The proposed test approach covers all levels and transitions necessary for testing the dynamic behavior of the DAC completely. The resultant eye-diagram from pseudo-random data testing can be used to extract more than intuitive data for its characterization.

Acknowledgements

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Chapter 1

Introduction

Emerging optical links target more than 100Gb/s capacities with bandwidth efficient modulation formats [1]. For this multilevel - signaling is an attractive solution. Higher bit rates can be achieved by polarization multiplexing with Quadrature Amplitude Modulation. This is done by Optical-Electrical-Optical technique in [1]. For this multilevel-signaling is required as described in Fig. 1.1.

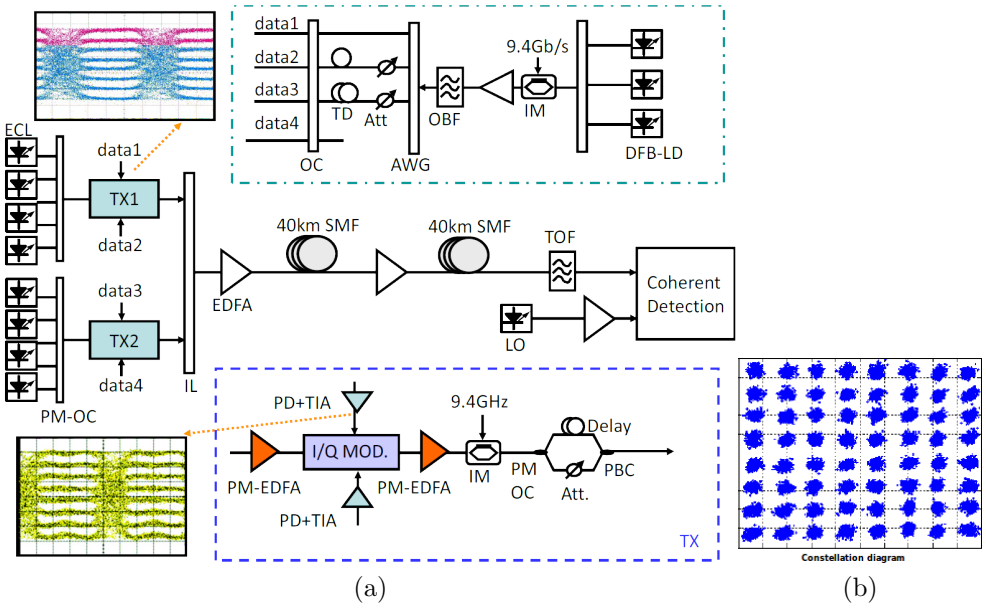


Figure 1.1: (a) Optical Experimental setup for two 112.8-Gbits/s PM-RZ-64QAM transmitters for odd and even channels, each modulating four 25 GHz-spaced wavelengths. TD:time delay, Att:atttenuator, IM: intensity modulator, PM-OC :polarization-maintained optical coupler, OBF, optical bandpass filter, MOD: optical modultator, AWG: arrayed waveguide grating, IL: 12.5/25GHz interleaver, TOF: tunable optical filter. (b) Constellation Diagram.

By the use of this technique, 8 levels(3 bits) are achieved. Then they used QAM (Quadrature Amplitude Modulation) to get additional 3 bits. After that finally 12 bits are achieved by polarization multiplexing. This Electrical-Optical-Electrical circuitry can be replaced by pure electrical circuitry. High speed digital to analog converter (DAC) can be used to replace Electrical-Optical-Electrical circuitry, but in this case knowing the limitation of circuitry is quite challenging. To our best knowledge, the maximum data rate in CMOS technologies for DAC is about 56 GS/s [2]. For getting such a high speed, thick gate current steering DAC is used. This shows design of high speed DAC requires very efficient circuitry. Also this shows that to get high speed digital to analog conversion, it is necessary to find out the limitation of circuits and accordingly necessary modifications are required.

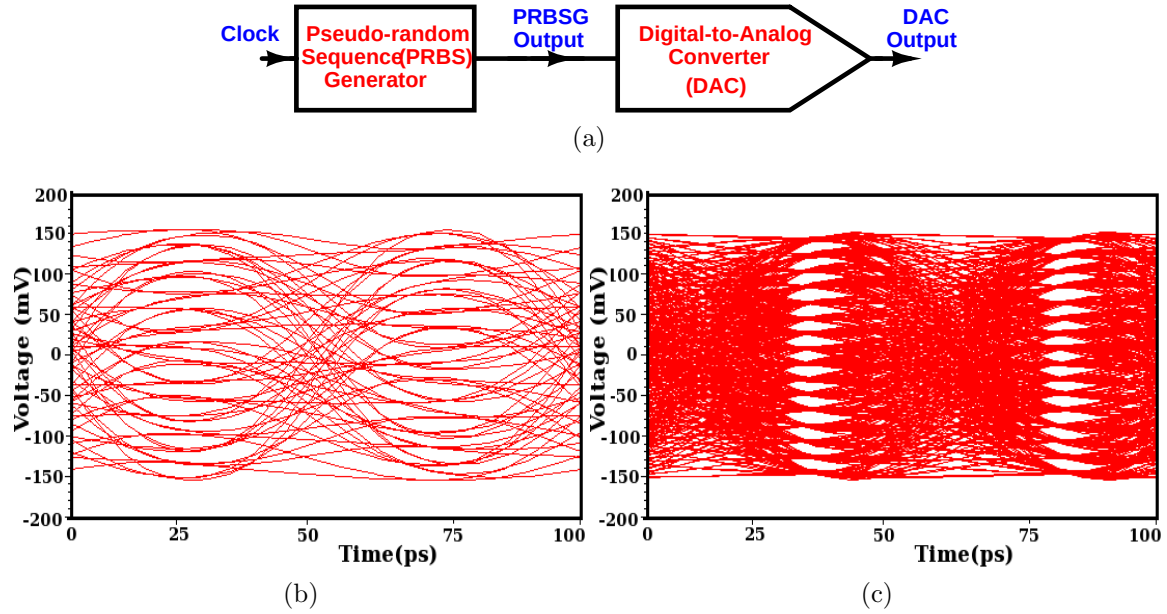


Figure 1.2: (a) Block diagram of testing of DAC with PRBS. (b)Eye diagram of $2^6 - 1$ (25% transition coverage)and (c)Eye diagram of $2^9 - 1$ (200% transition coverage) PRBS generator testing 4 bit DAC.

Testing a high speed DAC itself is challenging because it requires multiple high speed I/Os. In both the designs, current mode is used for high speed [3, 4]. Almost all publications for high speed DACs only show output for a ramp generator which doesn't indicate the true dynamic performance of the DAC. Hence, On-chip high-speed PRBS generator is equally important (as important as the DAC itself) to test the DAC. In Fig. 1.2 by eye diagram it is clearly visible that the DAC output is not performing as desired but this can't be find out by applying normal ramp signal because even if we get 8 levels at output doesn't indicate the correct operation of the DAC. The output should be correct if different level transition is applied to the DAC. To ensure correct operation, requirement of Test pattern generation (PRBS Generator) is important. PRBS generators used in test equipment for optical communications are themselves very expensive. For example, price

for 150 Mb/s -12.5 Gb/s Pattern Generator (N4903A-G13) of Agilent Technologies is approximately $100000 (50 lakhs rupees), typically uses expensive III-V or SiGe technologies.

PRBS generators are desirable to provide high speed test data patterns. In reference [5], $(2^7 - 1)$ PRBS generator is designed by simple linear feedback shift register (LFSR) architecture but its power consumption is quite high. Similarly, in reference [6], they used simple LFSR architecture with inductive peaking technique to get high bandwidth. In reference [5] and reference [6] also, they used inductive peaking technique to get high data rate (3Gb/s and 5Gb/s) and to get 12Gb/s and 15Gb/s they used multiplexing technique. Minimum requirement for covering all transitions is satisfied by using a 2^m-1 PRBS generator to test an m-bit input of DUT [7]. Therefore, 2^8-1 PRBS circuit is essential for 4 channel output. For 4 de-correlated sequence generation, 2^7-1 PRBS generator are used in [8] − [10], which doesn't cover all transitions until power consuming, shifting of initial condition circuit is not incorporated, 2^{11}-1 PRBS generator is used in [11] and 2^{31}-1 bit PRBS generator is used in [6] [12] [13], which takes longer time to cover maximum length sequence (MLS) and has increased circuitry because of number of DFF is proportional to size of PRBS generator. This increases power, area and cost. In [9], comparison of the circuitry required for series and parallel PRBS generators of different sizes with and without multiplexer are dissucssed and have chosen one minimal circuitry PRBS generator topology. In multiplexing technique, inputs are applied with different phase difference and select line selects the input such that it will increase the output frequency. For example, in 2-input Multiplexer, if second input is 180 degree phase shifted to first input with same frequency of select or signal than output frequency will get doubled.

In this report, Selection of correct PRBS generator topology is discussed for multi channel output and a multi-channel multiplexing technique depending on tapping of PRBS generator is proposed which covers all transitions with minimal circuitry. In general, low voltage swing (approximately 200mV) for clock signal is used to reduce power in CML. Incomplete switching of differential pairs causes problem of residual current in circuitry. This problem is more prominent in multiplexer. In this report, solution of this residual current is proposed which results a balanced output voltage, low jitter current mode logic (CML) multiplexer. This report focuses on the design of 20-GHz clock frequency, $2^9 - 1$ CMOS PRBS generator in a 90nm CMOS process. This report covers the PRBS circuit analysis and post layout simulated results. we worked to find out the limiting factors for bandwidth in schematic and layout levels. In CMOS circuits, bandwidth depends on position of first pole and first pole depends on inverse of multiplication of total load resistance and capacitance seen from the load which also includes parasitic capacitances and resistances so estimation of capacitance seen from the output becomes very important. Our research work includes understanding the factors that limit their performance, devising techniques to overcome them and fabricating DAC and high-speed signal generators for optical links using CMOS technologies.

Chapter 2

PRBS Generator

This chapter presents a 4 × 18 Gb/s 2^9-1 pseudo-random binary sequence (PRBS) generator in 90nm CMOS technology to test a 4-bit 18 GS/s digital to analog converter (DAC). For getting the architecture, "Multi-channel multiplexing technique" is proposed to generate four de-correlated sequences that covers all test-vectors and transitions from a single 9-bit LFSR with minimal circuitry in minimum number of cycles. Improved CML (current mode logic) multiplexer design ensures peak-to-peak jitter of 2.35ps, and small amplitude variation as compare to coventional multiplexer. The data latches are clocked at half-rate in order to reduce power dissipation, and are followed by 2:1 multiplexers to achieve the desired data-rate, consuming 60mW per output lane (total 240 mW) of power from a 1 V supply. The PRBS and DAC can together be used for generating pseudo-random multi-level symbol sequences for high-speed communication links.

2.1 Multi-channel Multiplexing Technique

The aim of this multi-channel multiplexing technique is to generate 4 de-correlated sequences that cover all transitions to test high speed DACs using PRBS in efficient manner. Figure 1.2b shows it becomes difficult to get correct information out of eye diagram without exhausting testing. Figure 1.2c shows need of all transition coverage for assessment of true dynamic behavior of DAC. Multi-channel multiplexing technique states that for exhaustive testing of an m-bit DAC, (a) each channel should be more than one clock cycle apart and (b) multiplexing is applied on $\leq$2m-bit linear feedback shift register (LFSR) which has minimum number of XORs ensuring maximum DFF output is used to generate testing sequence for minimal circuitry. [14]

An equivalence class of machine is used which generates maximal length sequences as a non overlapping series of 8-bit words. This is achieved at the expense of a 2-fold increase in combinational logic i.e. XOR but with no increase in the number of storage elements required i.e. DFF. Accordingly, the 8-bit in memory at any point of time does

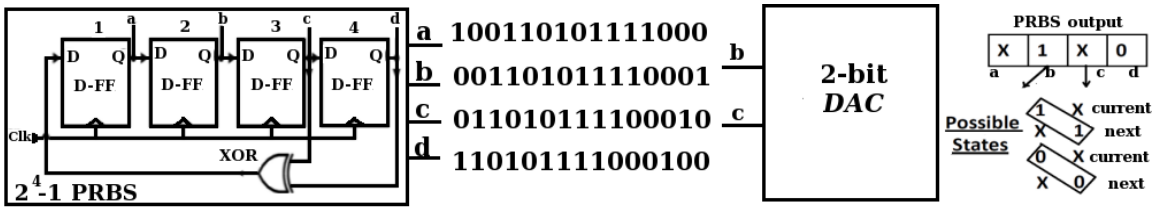


Figure 2.1: Block diagram showing DAC testing with one clock cycle delayed PRBS output covers half of total transitions because of two bits are fixed.

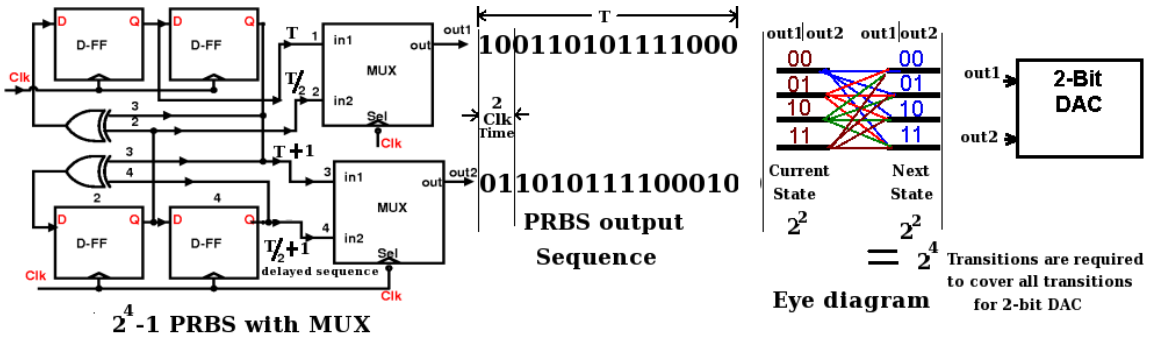


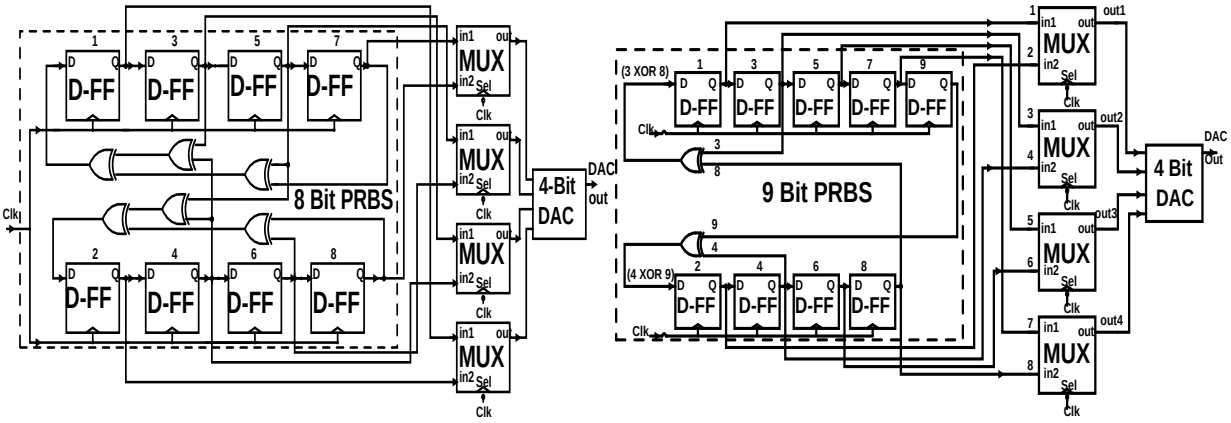
Figure 2.2: Block diagram showing DAC testing with two clock cycle delayed PRBS output covers all transitions.

not correspond to consecutive bits from one m-sequence but were bits from several phase shift. As a result it is not possible to serialise the parallel output. Further, considerable statistical validation of the word sequences was required since the simple relationship to the original m-sequence, which has been preserved here, was broken.

For example, Fig. 2.1 shows 4 bit PRBS generator output is applied to the one clock cycle delayed inputs to DAC then it covers only half of the total transitions because of two bits are fixed. Figure 2.2 shows series-parallel PRBS generator topology ensures 2 PRBS sequences for multiplexing which is T/2 time apart where T is maximum sequence length (MLS) of PRBS. PRBS generated is in double rate after MUX and automatically every multiplexer output is 2 clock period apart to each other and if we want to cover all transitions then after every state all possible state should come so the PRBS generator requirement is $2^n \times 2^n = 2^{2n}$ for n-bit DAC (Fig. 2.2). In this report, testing device is 4-bit DAC. Therefore, 2^8-1 PRBS generator is required to cover all transitions for 4 output channels. Characteristic equation of 2^8-1 LFSR is

$$x^8 + x^6 + x^5 + x^4 + 1 = 0 \tag{2.1}$$

In transition characterisation matrix for decimating an n-stage sequence by a a factor k the characteristic equation is shifted to the k_{th} row in the transition matrix. The rows



(a) (b)

Figure 2.3: Block diagram of (a) 2^8-1 PRBS generator (b)$2^9 - 1$ PRBS generator testing 4 bit DAC.

k-1, k-2, ...1 are obtained by shifting the elements to the left successively. the diagonal array of "1s" is shifted below the k_{th} row. This procedure is demonstrated in the following example for a PN sequence is demonstrated in the following example for a PN sequence with 8 stage and decimation by 2 (k = 2). the transition matrix for this application is shown below [15]:

$$\left[\begin{array}{c||cccccccc||c} Din & Q_1 & Q_2 & Q_3 & Q_4 & Q_5 & Q_6 & Q_7 & Q_8 & \\ \hline D_1 & 0 & 0 & 1 & 1 & 1 & 0 & 1 & 0 & = Q_3 \bigoplus Q_4 \bigoplus Q_5 \bigoplus Q_7 \\ D_2 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 1 & = Q_4 \bigoplus Q_5 \bigoplus Q_6 \bigoplus Q_8 \\ D_3 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & = Q_1 \\ D_4 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & = Q_2 \\ D_5 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & = Q_3 \\ D_6 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & = Q_4 \\ D_7 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & = Q_5 \\ D_8 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & = Q_6 \end{array}\right] \tag{2.2}$$

These 4 tappings make circuit complex as shown in Fig. 2.3a. Critical path in this case includes 2 XOR gates. In multi-channel multiplexing technique, LFSR tapping is considered as an important parameter. Some LFSRs require only two taps to generate the MLS. In these cases, number of required XOR gate reduces. As, number of XOR gates reduce in the critical path of the circuit, propagation delay of gate reduces and maximum clock frequency increases.

This technique ensures exhausting testing using every DFF output node to generate testing sequence. This is further improved by choosing one extra bit, circuit complexity and capacitive loading at most of the nodes are reduced because of less number of required XOR gates. Characteristic equation of 2^9-1 LFSR is

$$x^9 + x^5 + 1 = 0 \tag{2.3}$$

$$\left[\begin{array}{c||cccccccc||c} Din & Q_1 & Q_2 & Q_3 & Q_4 & Q_5 & Q_6 & Q_7 & Q_8 & Q_9 & \\ \hline D_1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & = Q_4 \bigoplus Q_8 \\ D_2 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & = Q_5 \bigoplus Q_9 \\ D_3 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & = Q_1 \\ D_4 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & = Q_2 \\ D_5 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & = Q_3 \\ D_6 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & = Q_4 \\ D_7 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & = Q_5 \\ D_7 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & = Q_6 \\ D_7 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & = Q_7 \end{array}\right] \tag{2.4}$$

Less number of tappings reduce circuit complexity as shown in Fig. 2.3b.

2^9-1 PRBS generator completes exhaustive testing in 511 clock cycles including 0-0 transition which is missing in 2^8-1 PRBS generator. Area required is also approximately 10% less in 2^9-1 PRBS generator as compare to 2^8-1 PRBS generator. This technique removes the logic depth and reduces power consumption by minimum one gate and increase the maximum operating frequency. This is applicable to all more than 2 tappings LFSRs. To the best of our knowledge, this $2^9 - 1$ PRBS generator is most efficient topology for testing 4 channel testing device (4-bit DAC in this report). Topology functionality is verified with MATLAB prior to circuit design.

2.2 Circuit Implementation

Pseudo-random bit sequence (PRBS) generators are required to provide high-speed test data pattern for the components of the serial link systems. A single LFSR core is used to generate 4 de-correlated sequences results in low power per channel. CML latches, D flip-flops, XORs, buffers and MUXes are needed to combine the parallel sequences into the final high speed PRBS. In CML logic circuits bottom bias transistor is removed keeping area reduction in mind. This area reduction helps improving speed of circuits during layout design.

2.2.1 CML D-Flip Flop

A high-speed realization of D-FF is achieved through current-mode logic using two latch consisting a sensitive differential amplifier followed by a positive feedback circuit are connected in Master-Slave fashion as shown in Figure 2.4.

CML Latch

In the Latch circuit, if the clock is high all current passes through M_5 and the transistor pair M_1, M_2 behaves like a differential amplifier. This is called track phase. Total current

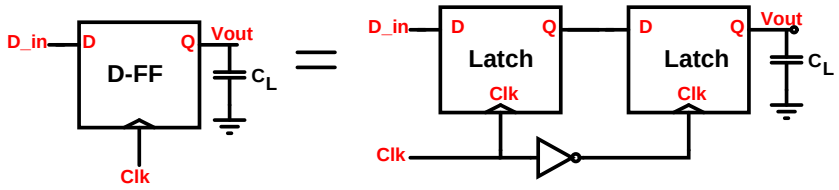


Figure 2.4: Block diagram showing two latches connected in master-slave fashion to form a D Flip-Flop (MS-DFF).

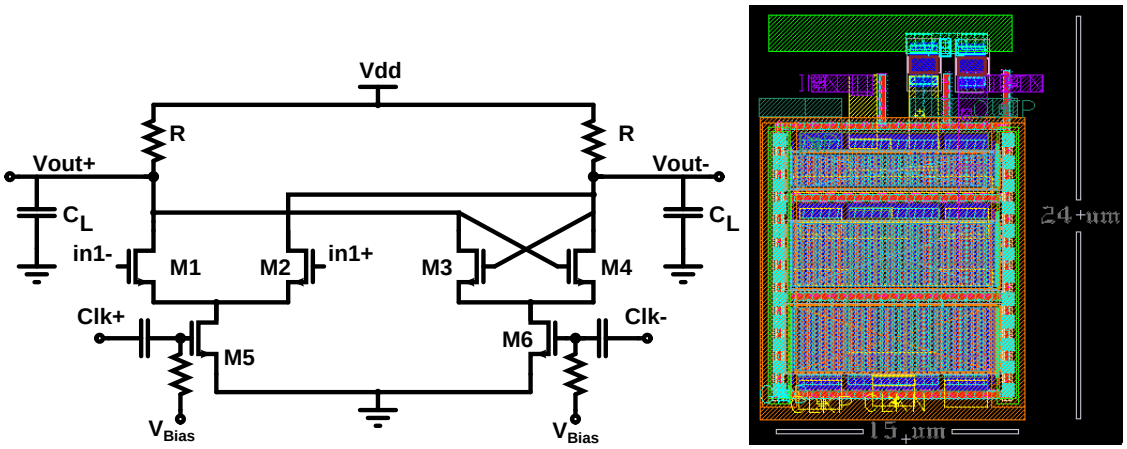


Figure 2.5: (a)Circuit diagram of Latch and (b) layout of Latch.

flowing through latch is 7mA. A load resistance of 60 ohm produces voltage swing of

$$\Delta V = I_d \times R_{load} = 7m \times 60\Omega = 420mV$$

To switch a next MOSFET, 300mV is required and this voltage swing is enough [16]. The clock is 200mV single ended biased at 0.45V. output biased voltage is 0.8V. In the negative phase of clock it behaves like a latch. The output of the differential amplifier tracks the input signal with a propagation delay that depends on the load impedance R and the amount of output capacitance C_L that has to be charged and discharged according to signal. In negative phase of clock, by means of positive feedback the initial voltage difference (V_{out+})-(V_{out-}) is regenerated to a full logic value. The maximum clock rate would be limited by the frequency response of the preamplifier i.e. track during the track phase, rather than by the speed of the latch during latch phase. The Latch (Fig. 2.5) is working with 11 Gb/s data-rate with 11 GHz clock frequency. Triangular wave is chosen as clock frequency to test latch and DFF in wrost case. Single sided output voltage swing is 300mV. The $max\{f_{clk}\}$ is given by the following equation:

$$max\{f_{clk}\} = \frac{1}{2 \times \ln 2 \times R_L \times C_L} \tag{2.5}$$

where,

f_{clk} = Clock frequency of Latch.

R_L = Load resistance.

C_L = Load capacitance.

$max\{f_{clk}\}$ for D flip flop is 11GHz.

Post Layout Simulation

Simulation (Fig. 2.6) is performed in typical-typical process in 100°C temperature after parasitic resistance and capacitnace extraction.

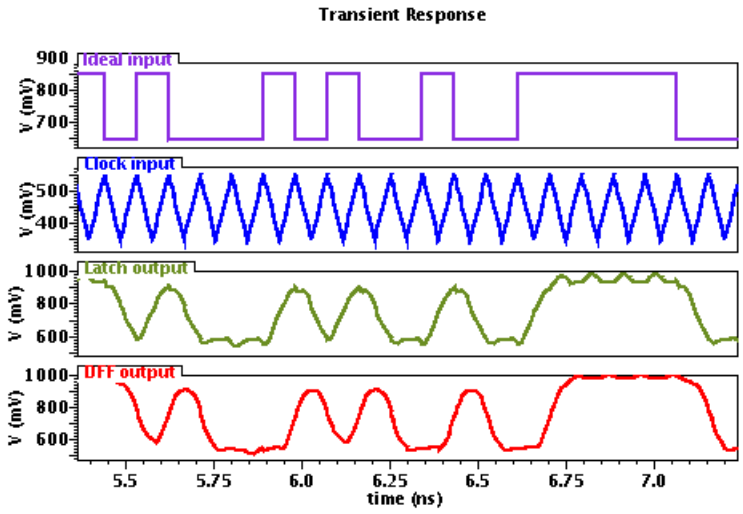


Figure 2.6: Post layout simulation showing, latch and DFF work with 11GHz trinagular clock upto 11Gb/s data rate.

2.2.2 CML XOR Gate

The XOR is implemented in CML logic and uses a gilbert cell to perform the logical function. Logically, gilbert cell is a multiplexer. Due to the inputs are on the same voltage level, the input B' dc level is shifted by RC configuration. The design and operation of this XOR is easily understood by Figure 2.18 and Table 2.1.

Table 2.1: XOR Truth table

XOR Truth table				Connection for MUX to XOR	
in1	**in2**	**output**		**MUX**	**XOR**
0	0	0		in1	in1bar
0	1	1		in2	in1
1	0	1		Sel	in2
1	1	0			

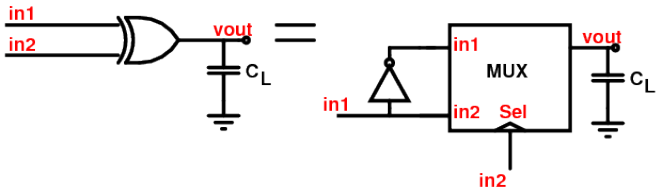


Figure 2.7: Based on the Truth table, CML MUX Connection for MUX to XOR conversion is shown.

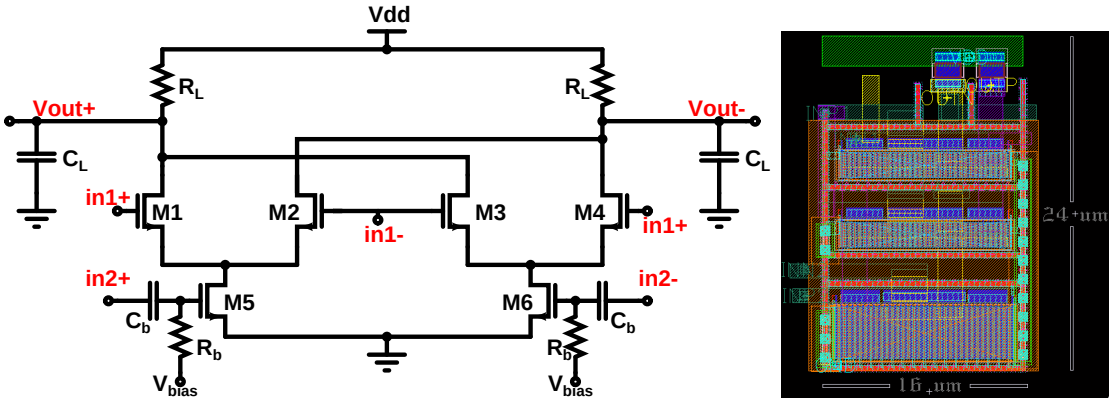


Figure 2.8: (a)Circuit diagram of XOR and (b) layout of XOR.

Post Layout Simulation

Simulation (Fig. 2.10)is performed in typical-typical process at 100°C temperature after parasitic capacitance and resistance extraction.

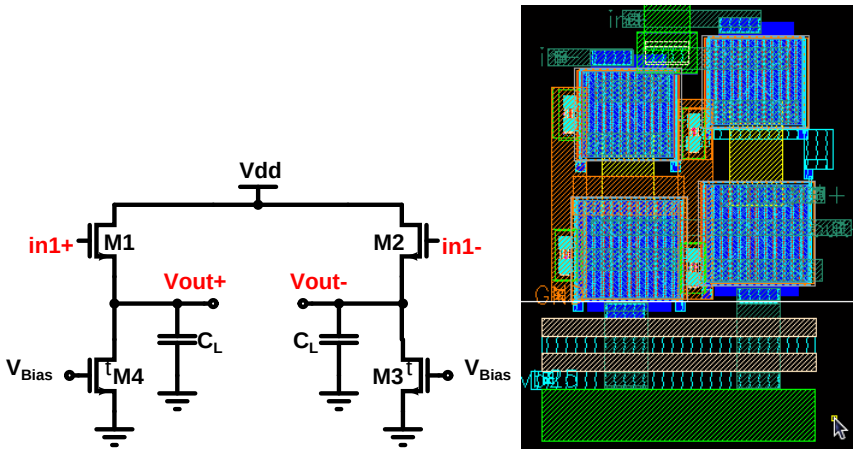


Figure 2.9: (a)Circuit diagram of Levelshifter and (b) layout of Levelshifter.

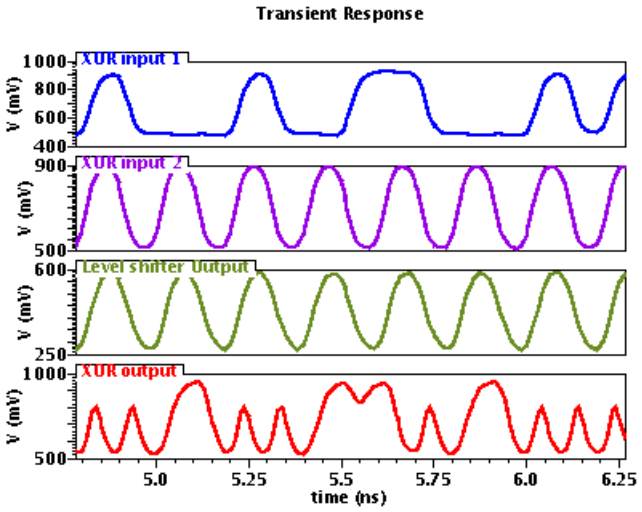


Figure 2.10: Post layout simulation of XOR response when applied one input of 10Gb/s and another in 20Gb/s that is level shifted to 0.45V.

2.2.3 Serializer

The serializer architecture consists of two master-slave DFF, a latch, two 10-Gb/s and a 20-Gb/s buffers and a selector circuit(a 2:1 MUX) as shown in Fig 2.11. The glitches might occur due to simultaneous arrival of both the inputs to the 2:1 MUX. To avoid this situation, one of the input is delayed by half the clock cycle by introducing one latch in one of the input path. Moreover, if another input arrives at an arbitrary time then, trench and spike may occur, which may be large enough to be considered as wrong logic. Therefore,

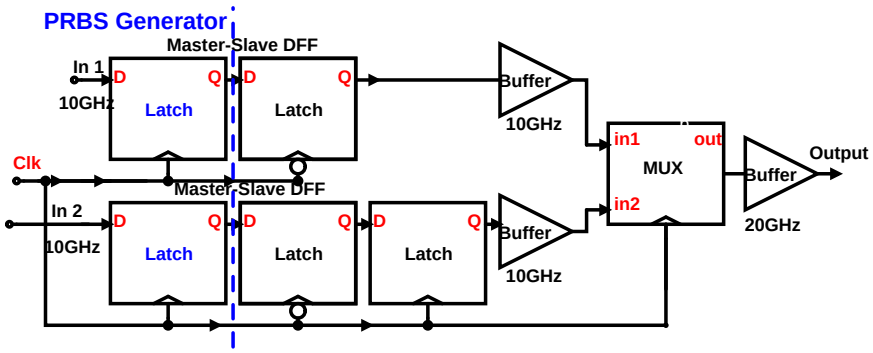


Figure 2.11: Serializer architecture.

master-slave flip flops are used before 2:1 MUX to ensure correct data. Input of serializer is coming from PRBS so one latch is chosen as common in serializer as shown in Fig. 2.11.

CML MUX

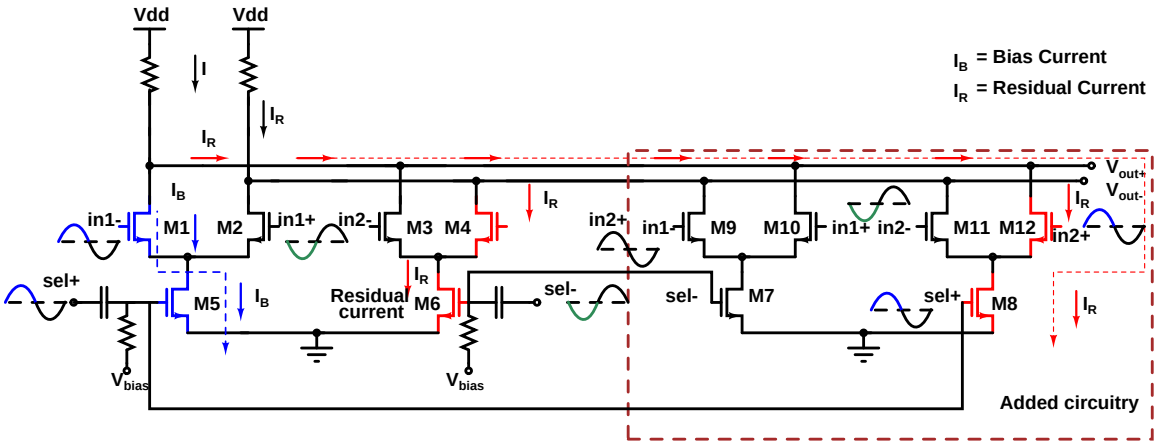
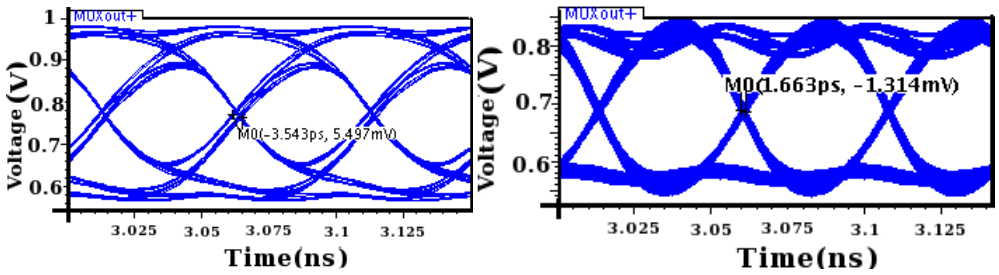


Figure 2.12: Circuit diagram of the proposed 2:1 MUX showing added circuitry for solving residual current problem (I_R = residual current I_B = bias current).

The main problem in the conventional 2:1 MUX is imperfect switching of Differential pair. Current flows due to this, causes two output voltage levels for 'high' and two output levels for 'low' and variation in rise and fall time at the output. This current varies depending on circuit configurations, specifications and technology. As technology is scaling down, this residual current is increasing. In 90nm technology, it can be one fourth of total bias current. To avoid consequence, In proposed MUX, extra current is added through extra differential amplifiers with current capacity of this residual current as shown in Fig. 2.12. Other cases work in similar fashion. It draws 5mA current including amount of

Table 2.2: Modified MUX operation

Sel_+	Sel_-	in_{1-}	in_{2-}	Conventional	Proposed
				$V_{out+} = V_{dd} - I_B \times R$ $V_{out-} = V_{dd} - I_R \times R$	$V_{out+} = V_{dd} - I_B \times R - I_R \times R$ $V_{out-} = V_{dd} - I_R \times R$
				$V_{out+} = V_{dd} - I_B \times R - I_R \times R$ $V_{out-} = V_{dd}$	$V_{out+} = V_{dd} - I_B \times R - I_R \times R$ $V_{out-} = V_{dd} - I_R \times R$
				$V_{out+} = V_{dd} - I_R \times R$ $V_{out-} = V_{dd} - I_B \times R$	$V_{out+} = V_{dd} - I_B \times R - I_R \times R$ $V_{out-} = V_{dd} - I_R \times R$
				$V_{out+} = V_{dd}$ $V_{out-} = V_{dd} - I_B \times R - I_R \times R$	$V_{out+} = V_{dd} - I_B \times R - I_R \times R$ $V_{out-} = V_{dd} - I_R \times R$



(a) (b)

Figure 2.13: Eye diagram of 2:1 MUX (a) conventional 2:1 MUX (b)proposed 2:1 MUX.

extra current i.e. 1mA which is flowing from extra circuitry. It draws extra 1mA current but it improves MUX output response significantly so this extra power loss in manageable. Figure 2.13 shows difference between conventional and modified circuit simulation results.

Post Layout Simulation

Simulation (Fig. 2.15) is performed in typical-typical process at 100°C temperature.

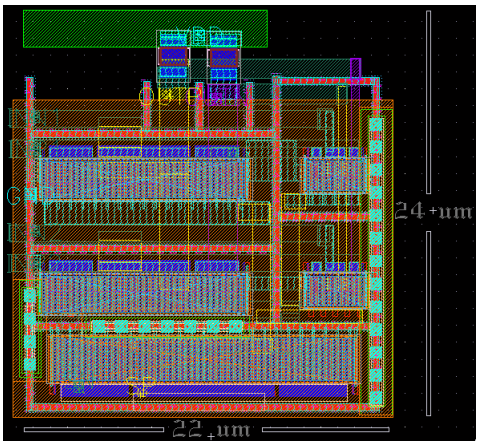


Figure 2.14: Layout of MUX.

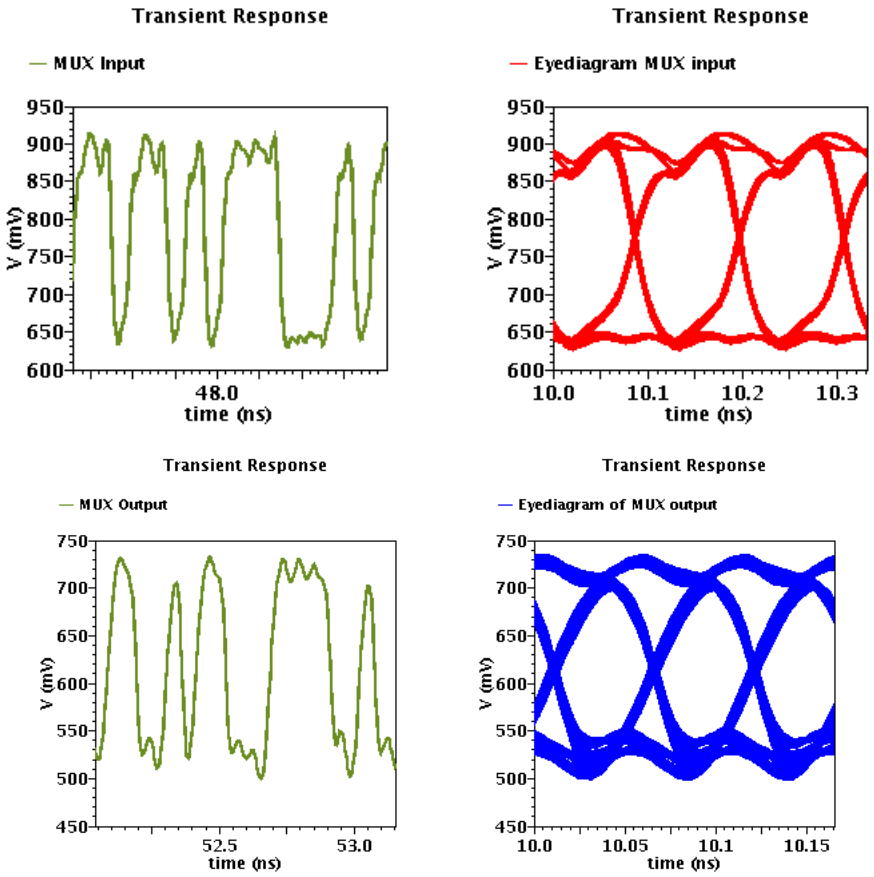
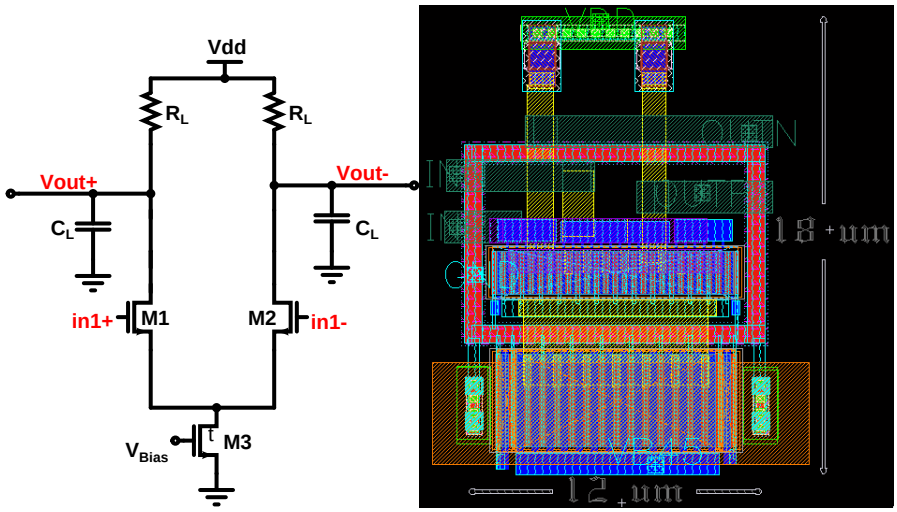


Figure 2.15: (a)Input of MUX at 9Gb/s data rate and (b) MUX output at 18Gb/s data rate.

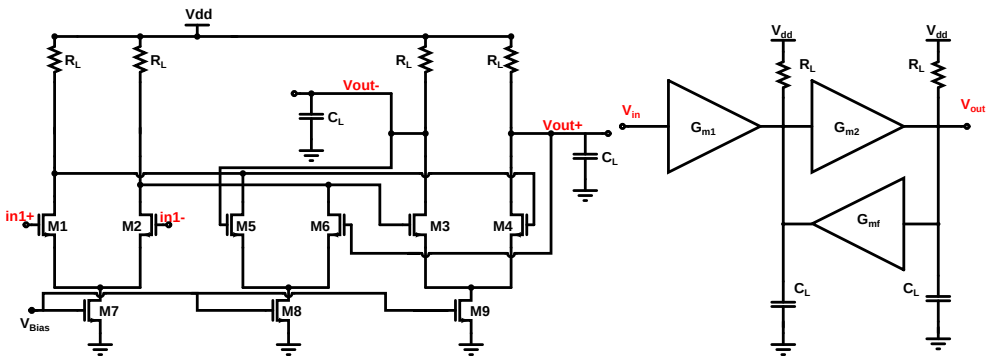
2.2.4 10-Gb/s Buffer and 20-Gb/s Buffer



(a) (b)

Figure 2.16: (a)Circuit diagram and (b) Layout of 10-Gb/s Buffer.

Current mode logic buffer is differential amplifier type structure with gain one [4]. It draws 5mA current. as shown in Fig. 2.17b Such an arrangement employs a transconduc-



(a) (b)

Figure 2.17: (a) 20Gb/s buffer architecture and (b) It's block diagram show the active feedback technique to enhance rise time of input signal.

tance stage G_{mf} to return a fraction of the output to the input of G_{m2} [17], The transfer function of the overall amplifier is given by

$$\frac{V_{out}}{V_{in}} = \frac{A_{vo}{\omega_n}^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.6}$$

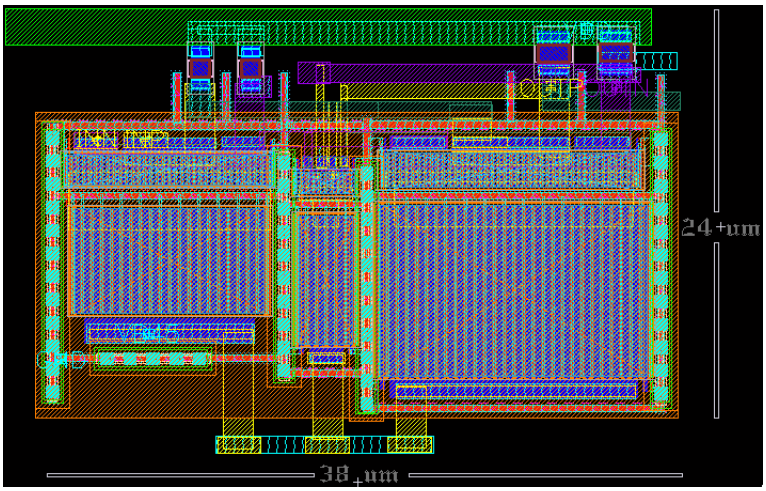


Figure 2.18: Layout of 20Gb/s data rate Buffer.

where,

$$A_{vo} = \frac{G_{m1}G_{m2}R_{L1}R_{L2}}{1 + G_{m1}G_{m2}R_{L1}R_{L2}} \tag{2.7}$$

$$\zeta = \frac{1}{2}\frac{R_{L1}C_1 + R_{L2}C_2}{\sqrt{R_{L1}R_{L2}C_1C_2(1 + G_{mf}G_{m2}R_{L1}R_{L2})}} \tag{2.8}$$

$${\omega_n}^2 = \frac{1 + G_{mf}G_{m2}R_{L1}R_{L2}}{R_{L1}R_{L2}C_1C_2} \tag{2.9}$$

For an maximally-flat Butterworth response, $\zeta = \sqrt{2}/2$ and the -3dB bandwidth, $\omega_{-3dB} = 2\pi f_{-3dB} = \omega_n/2\pi$

$$A_{vo}\omega_{-3dB} = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}} = \frac{G_{m1}G_{m2}}{C_1C_2}\frac{1}{\omega_{-3dB}} = f_T\frac{f_T}{f_{-3dB}} \tag{2.10}$$

The result reveals that active feedback increases the GBW beyond the technology f_T by a factor equal to the ratio of f_T and the cell bandwidth [17]. This buffer is working with 20-Gb/s data rate with single sided output voltage swing of 280V. It draws 8mA current.

2.3 Post Layout Simulation of PRBS Generator

Simulation (Fig. 2.20) is performed in typical-typical process in 100°C temperature after parasitic resistance and capacitnace extraction. PRBS output is 405 mV single ended voltage swing at 9Gb/s data rate with common mode of 0.75 V with 1.56 ps jitter$_{pp}$. This simulation is carried out with traingular wave of 9GHz clock frequency. Eye-diagram

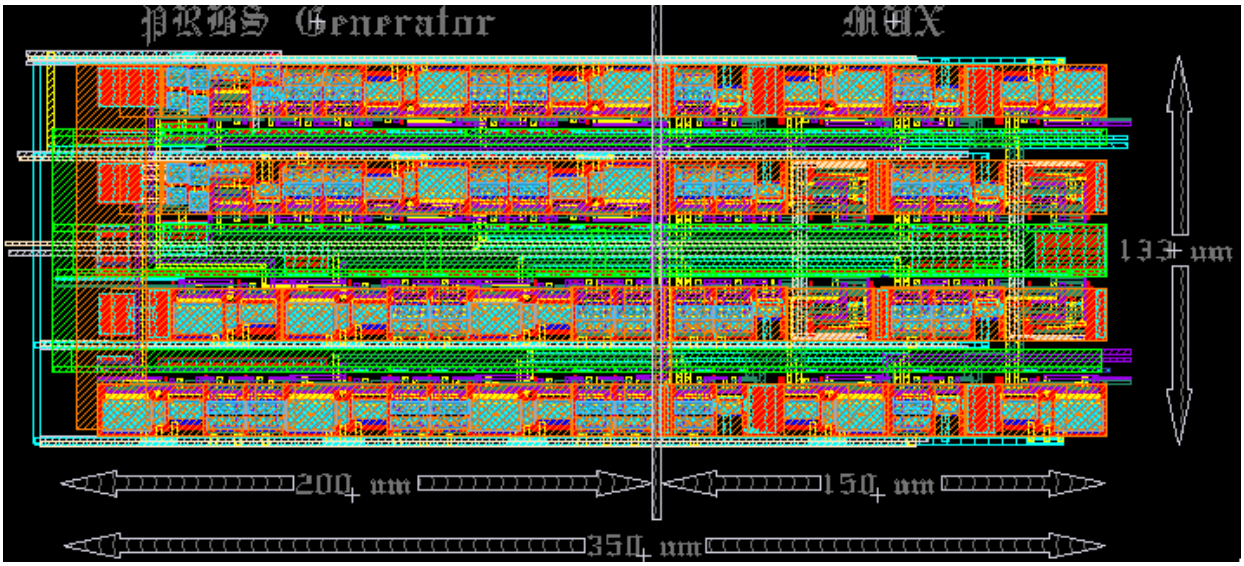


Figure 2.19: Layout of PRBS generator.

(Fig. 2.20c shows 205mV single ended voltage swing at 18Gb/s data rate with 2.3 ps jitter$_{pp}$. Intial condition circuit is not connected yet. Speed reduction is expected by 0.5GHz to 1GHz after connecting intial condition circuit.

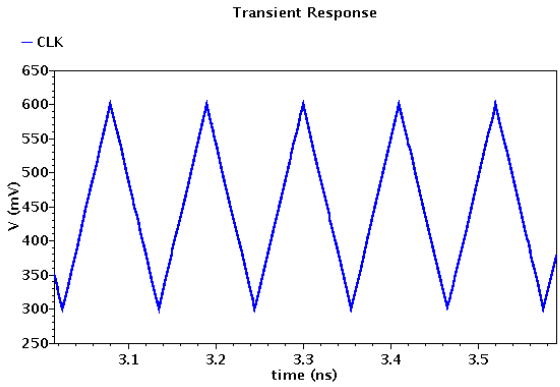
2.4 Comparison with Other Published Work

$$FOM_1{}^* = \frac{log_2(MLS) \times DataRate}{f_T \times Area \times Power}$$
$$FOM_2{}^* = \frac{Power}{(log_2(MLS) \times DataRate)}$$

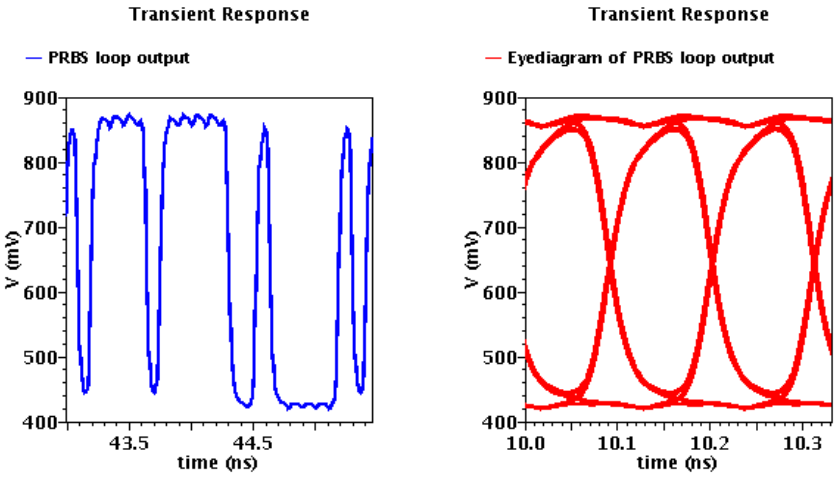
Table 2.3: Comparison with other published work

Ref.	Technology	f_T (GHz)	Data-rate	MLS	Power /lane	Supply Voltage	Area	FOM$_1^*$ ($\frac{pJ}{bit}$)	FOM$_2^{**}$
[13]	0.13 μm SiGe BiCMOS	150	1×72Gb/s	2^{31}-1	9.28W	3.3V	3.5×3mm^2	4.15	0.15
[12]	0.13 μm SiGe BiCMOS	150	1×80Gb/s	2^{31}-1	9.8W	3.3V	3.5×3.5mm^2	3.95	0.14
[8]	0.18 μm SiGe BiCMOS	120	1×45Gb/s	2^7-1	1.32W	3.3V	NA	3.77	–
[11]	InP HBT	300	1×104Gb/s	2^{11}-1	2.8W	3.5V	1.3×1.6mm^2	2.45	0.65
[11]	InP HBT	300	1×110Gb/s	2^9-1	2.2W	3.5V	1.3×1.6mm^2	2.35	0.72
[18]	SiGe BiCMOS	120	1×55Gb/s	2^7-1	550mW	2.5V	1×0.8mm^2	1.43	0.73
[19]	CMOS 0.13 um	NA	1×24Gb/s	2^7-1	274 mW	1.5V	0.63×0.47mm^2	1.63	–
[6]	CMOS 0.18 um	NA	3×12Gb/s	2^{31}-1	262 mW	1.8V	0.5×0.7mm^2	0.7	–
[20]	0.25 um SiGe BiCMOS	75	1×25Gb/s	2^9-1	151 mW	2.85V	1×1mm^2	0.67	2
[10]	0.13μm CMOS	80	1×20Gb/s	2^7-1	0.84W	1.5V	0.7×1.1mm^2	6	2.7
[9]	0.13 um SiGe BiCMOS	150	4×23Gb/s	2^7-1	60 mW	2.5V	0.393×0.178mm^2	0.37	25.57
This work	CMOS 90 nm	135	4×18Gb/s	2^9-1	60 mW	1V	0.35×0.133mm^2	0.37	43

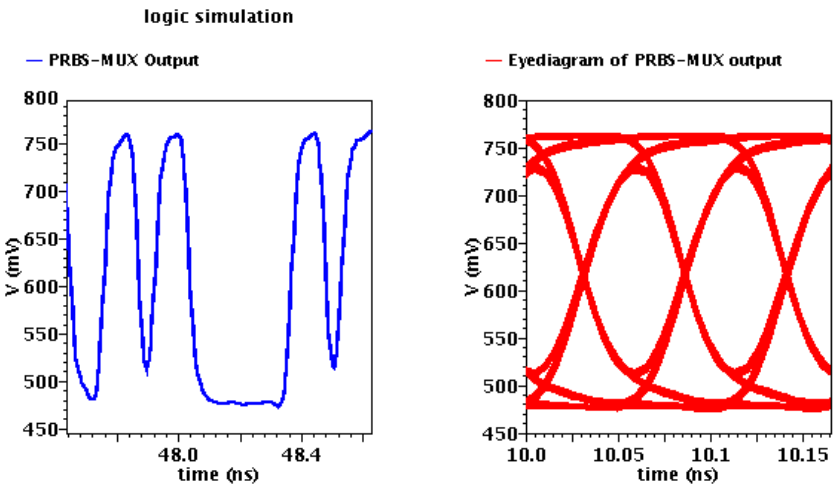
$FOM_1{}^* = \frac{log_2(MLS)\times DataRate}{f_T \times Area \times Power}$ $FOM_2{}^{**} = \frac{Power}{(log_2(MLS)\times DataRate)}$



(a)



(b)



(c)

Figure 2.20: (a) 9GHz clock (b)PRBS Generator output at 9Gb/s and (c) PRBS Generator output after MUX-20Gb/s buffer at 18Gb/s.

Chapter 3

Layout Issues in High Speed circuits

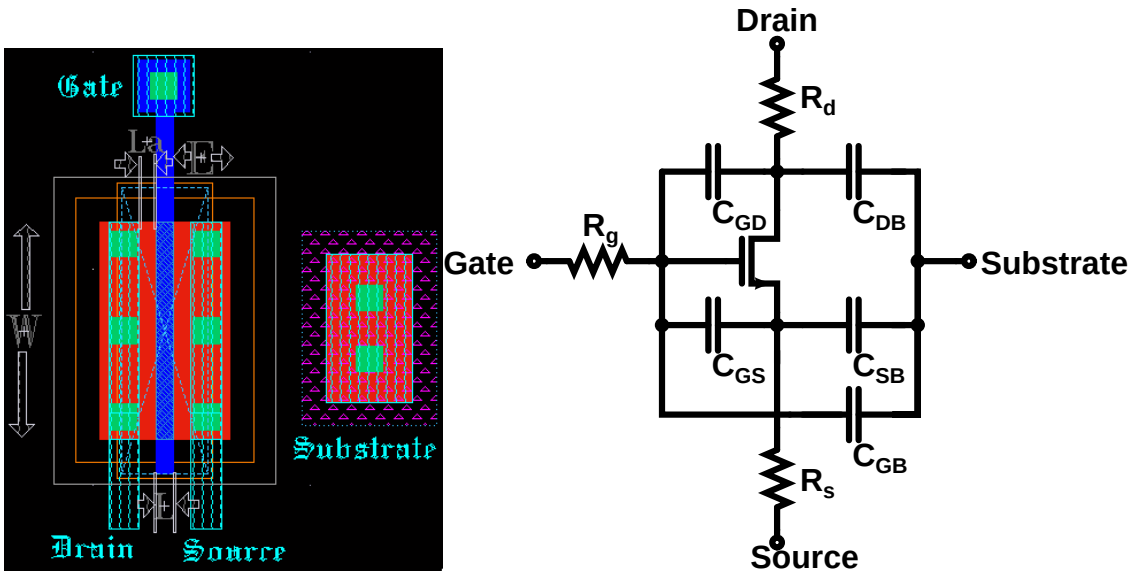
High speed layout requires some extra precautions otherwise it affects speed of integrated circuits. The main key to get high speed layout is reduction of layout area. Selection of number of fingers plays important role in area reduction. Number of finger is selected keeping compromise between parasitic resistance and capacitance in mind. Parasitic resistance and capacitance reduction is also necessary to improve bandwidth in high speed circuit design and layout. In this chapter, method to find correct number of fingers is explained and method to ensure correct common centroid is also mentioned in detail. [21]

3.1 Layout Parasitic

Analog integrated circuits are affected by transistor and interconnect parasitic more as compare to resistors and capacitors. It affects performance of circuits as reduction of gain, bandwidth, phase margin etc.

Parasitics in Transistors

MOSFET device capacitance and resistance are determined by architecture itself as shown in Fig. 3.1. [22]
Here,
W = width of MOSFET,
L = length of MOSFET,
C_{GD} = gate to drain capacitance,
C_{DB} = drain to substrate capacitance,
C_{GS} = gate to source capacitance,
C_{SB} = source to substrate capacitance,
C_{GB} = gate to substrate capacitance,.
R_g = gate resistance mainly caused by poly,



(a) (b)

Figure 3.1: (a)Layout of MOSFET and (b) Circuit diagram of MOSFET.

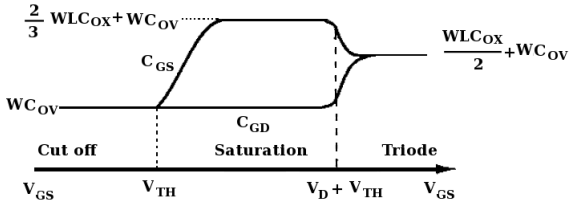


Figure 3.2: Capacitance variation with V_{GS}.

R_d = drain resistance,
R_s = source resistance,

C_{GD} and C_{GS} depend on gate voltage applied on MOSFET as shown in Fig. 3.2. It doesn't depend on layout but it depends on size of MOSFET so during design of circuits, MOSFET should be chosen as low size as possible to reduce area and increase speed.

C_{DB} and C_{SB} depends on layout and given by

$$C_{DB}, C_{SB} = A \times C_j + P \times C_{jsw} \tag{3.1}$$

Here,
C_j = bottom plate depletion capacitance associated with the bottom of the junction,
C_{jsw} = sidewall depletion capacitance due to the perimeter of the junction,
A = total source or drain area
$= T \times E \times \frac{W}{N}$

T = number of drain or source,
N = number of fingers or number of poly gate,
A = $W \times E$ (in Fig. 3.1),
P = total source or drain perimeter
= $2 \times T \times (E + \frac{W}{N})$
= $2(W + E)$ (in Fig. 3.1),

Value of C_j and C_{jsw} can be found in model files of given technology.

$$R_d, R_s = \frac{L}{W} \times R_{sh} \tag{3.2}$$

L_a = length of active,
R_{sh} = sheet resistance of the n+ (for the NMOS model) or p+ (for the PMOS model).

n+ of drain and source is connected to metal with number of contacts so R_d and R_s becomes negligible in MOSFET and can be ignored but R_g has sufficient sheet resistance and it is in series so it can't be ignored.

$$R_g = L \times R_{shg} \tag{3.3}$$

R_{shg} = sheet resistance of poly gate.
C_{GB} is negligible and generally ignored during layout.

Interconnect Parasitic

In High speed design, current mode logic (CML) is used and it is of differential type. Because of differential output, not only wiring capacitance but also coupling capacitance is large. It is given by

$$C_{coup} = C_c(L_{int}/spacing) \tag{3.4}$$

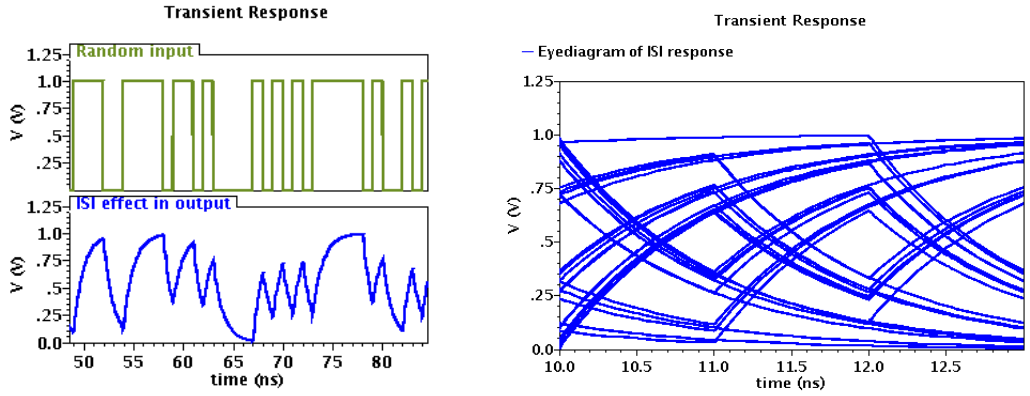
Here, L_{int} is length of interconnect. If circuit is minimally designed then automatically interconnect length reduces. If two interconnect is passing together than use different metal lines to reduce C_{coup}. When two interconnects are crossing try to minimize both interconnects in crossings. If interconnect length is very large in layout then resistance of metal also affects speed of circuit.

$$R_{int} = R_{shint}(L_{int}/W_{int}) \tag{3.5}$$

Here, R_{int} is interconnect resistance, R_{shint} is sheet resistance of metal used and W_{int} is width of interconnect.

3.2 Inter-Symbol Interference in Post Layout Results

Inter-symbol interference (ISI) occurs when a pulse spreads out in such a way that it interferes with adjacent pulses at the sample instant. Basically it occurs as a effect of low



(a) (b)

Figure 3.3: (a) Demonstration of Inter-symbol interference (ISI) effect and (b) eye-diagram showing ISI properly.

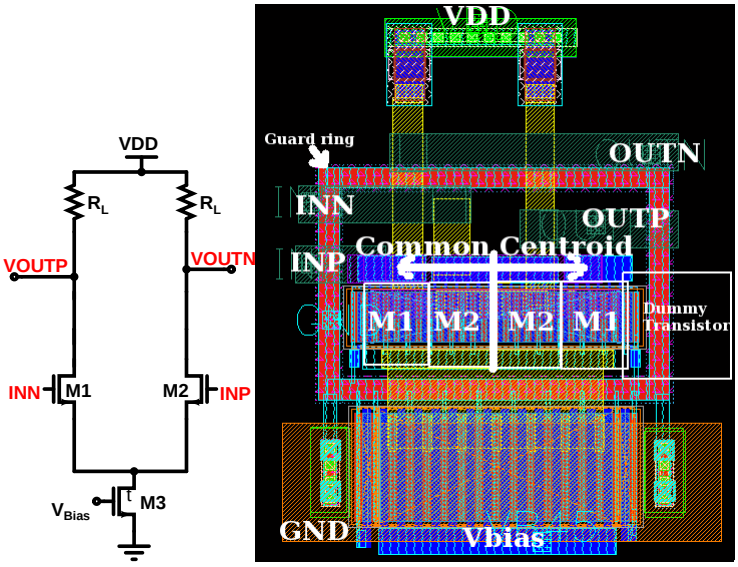
pass filtering action caused by parasitic capacitance and resistance. This low pass filtering action reduces the bandwidth. As shown in Fig. 3.3, in output response, rise time and fall time are not equal and also output response is not reaching upto desired voltage level in given time pulse. This causes jitter in circuits. As frequency increases, the rise and fall time will be longer and ISI will be large. This phenomenon can not be completely removed but it can be reduced by proper layout. Proper layout means circuit should be properly designed such that it has minimum size in given specifications and layout design techniques are properly applied.

3.3 Layout Design Techniques for High Speed Circuits

For high speed circuit layout requires some extra precautions because effect of parasitic resistance and capacitance directly reduces bandwidth of circuit seriously. Area reduction is the main key of layout of high speed circuits and selection of correct number of fingering also helps in reduction of area if it is properly chosen. In this chapter, high speed buffer which works upto 10GHz bandwidth is designed for reference and it's circuit and layout is shown in Fig. 3.4.

Selection of Fingers

Selection of fingers plays important role in optimizing high speed circuits. Wrong selection of fingers not only reduces the speed but also increases area of layout. Fingers should be assumed at the time of schematic simulations itself because this also affects circuit



(a) (b)

Figure 3.4: (a)Circuit of buffer and (b) Layout of buffer.

simulation performance. As fingers increase, circuit performance improves as shown in Fig. 3.6. Effect of interconnect parasitics are difficult to incorporate in circuit simulations so assumption of fingers should be based on compromise between parasitic resistance and parasitic capacitance of interconnect and switching devices. Some of the finger selections

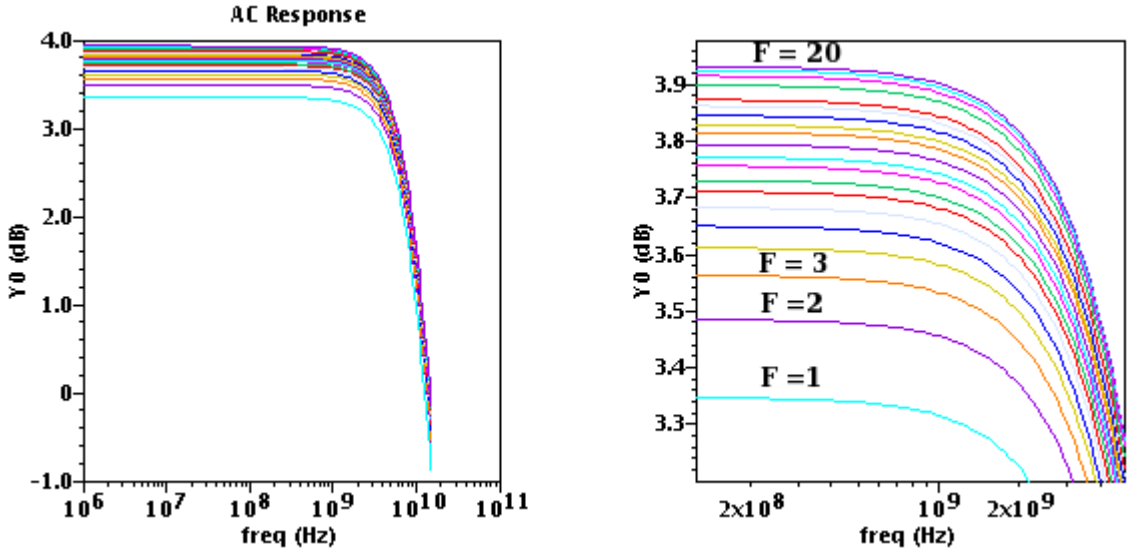


Figure 3.5: Effect of fingering in circuit simulations.

Table 3.1: Specification of Buffer.

Parameter	Value
M1−M2	$20\mu/80n$
R_L	146Ω
M3	$65\mu/250n$
I	$2.7m$A
Technology	$90n$m CMOS process

can be easily ruled out based on placement of dummy transistors and common centroid techniques. In high speed applications, NMOS is used as a switching device because it is faster than PMOS. In rest of the chapter, switching device is considered to be NMOS unless explicitly mentioned.

Dummy Transistors

During the diffusion process, dopant concentrations is different in outer and inner unit cells on the edges. For reducing mismatch in layout of high speed circuits, dummy transistors are compulsory attached in every switching MOSFET pair of circuits. Dummy transistors do nothing electrically but it improves matching. Dummy transistor's one terminal is common to MOSFET' drain/source of switching device and source/drain and gate of dummy transistor is connected to ground. Dummy transistors are shown in Fig. 3.4b. In this case, MOSFET pair's source are at the corner and source is common to dummy transistor. If any dummy is common with drain of switching transistor pair then it is capacitance will be added to the output of the circuit which is undesirable. In CMOS 90nm process in off condition MOSFET adds 0.7fF load to the output and output is in both corners so added capacitance will get doubled which will cause load imbalance. All even fingers fulfill this conditions so we can directly omit odd fingers. Also it is important that dummy should not be connected to drain of switching pair otherwise its capacitance will be added to output and this is not the case, when one source of MOSFET pair are in corners.

Common-centroid Technique

Common centroid is preferable over inter-digitization because of it's more susceptible to mismatch. In CML logic, MOSFET pairs are used and both MOSFET are of same size. Effects of gradient of the variation in local unit area is shown In Fig. 3.7. For 14 fingures, The ratio of unit area of M_1 i.e. $1 + 2 + 3 + 4 + 11 + 12 + 13 + 14 = 60$ and M_2 i.e. $5 + 6 + 7 + 8 + 9 + 10 = 45$ is not equal to ratio of their sizes i.e. $20\mu/20\mu = 1$ so it in not in common centroid configuration. For common centroid, source should be at center as shown in Fig. 3.6. If poly gate or drain comes in center than common centroid

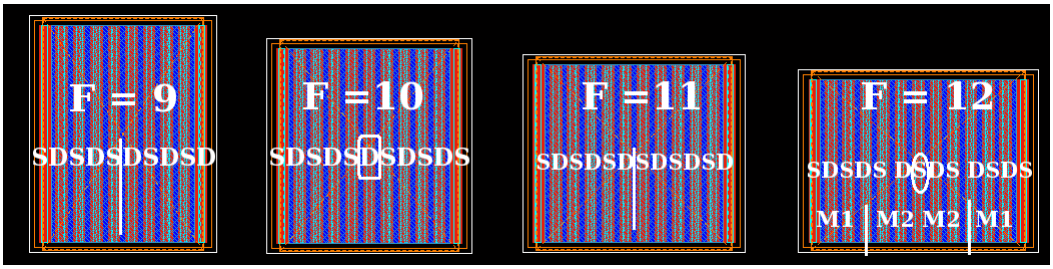


Figure 3.6: Only even finger have source at corners appropriate for dummy transistor connections.

is not possible for equal size of MOSFET pairs. Only multiple of four (4N) fingures can be chosen. 2 layers or more, common centroid configuration can not be selected because of connection complexity. It increases interconnect capacitance. During finguring, all poly belongs to one MOSFET are connected with poly and metal with number of poly-metal contacts. Each contact comes in parallel in case of resistance so resistance of poly reduces. Metal has very less sheet resistance as compare to poly.

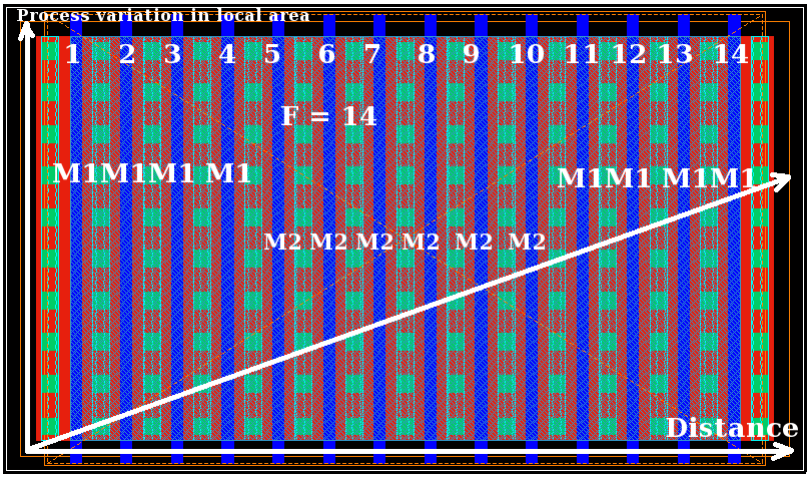


Figure 3.7: Figure showing gradient of variation for 14 fingers in buffer transistor pair.

Guard Ring

Guard ring is also one of the important layout technique to reduce substrate noise in circuits. Substrate noise results from adjacent circuits injection current into one another. The guard ring is connected to gnd or vdd. In Fig. 3.4, it is connected to ground. In high speed layout current requirement of circuit is very large because of this, resistance in gnd or vdd can cause a large drop. Generally vdd and gnd are in top metals and the

connection between metal 1 to top metal is done in layout. For reducing the resistance, number of contacts between bottom metal to top metal should be large. In circuits, guard ring is connected to gnd or vdd thats why this is a good place to put metal1 to top metal contacts. Apart from this where ever there is free space in complete layout put contacts to connect vdd and gnd with bottom metal to top metal.

3.4 Post Layout Simulations

Post layout simulation of buffer for F =4,8,12,16,20 is shown in Fig. 3.8. It is performed in typical-typical process in 100°C temperature after parasitic resistance and capacitance extraction. Post layout simulation clearly shows for F=8,12 and 16 have comparable

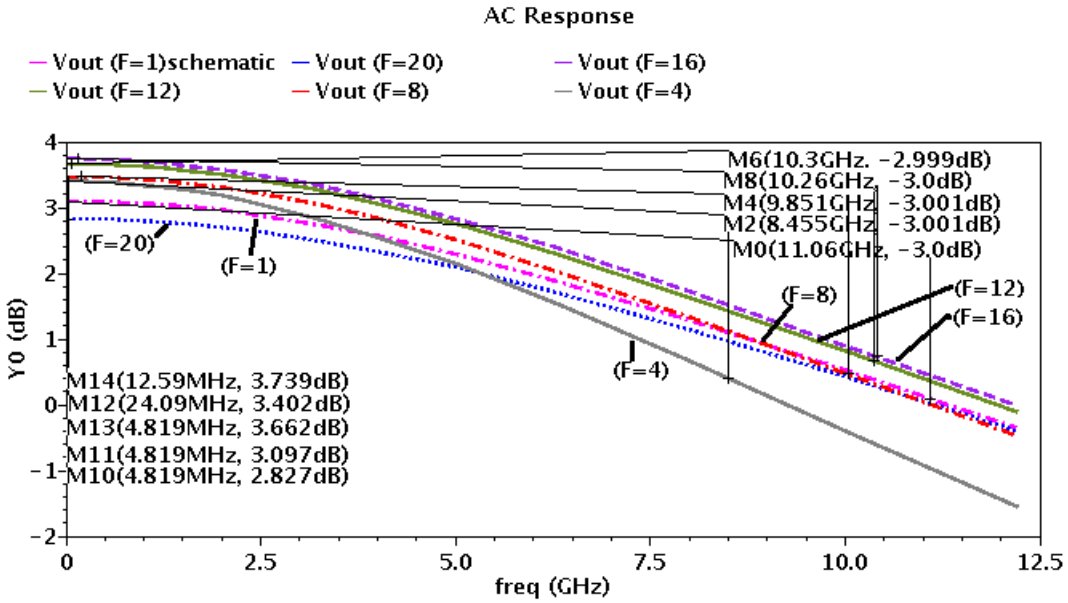


Figure 3.8: Post layout AC response for Fingers =1,4,8,12,16,20 in buffer.

results as desired. But looking into area and bandwidth, one can chose F=12 for final design. In a system, if same buffer is repeating number of times then this area reduction helps to improve speed. The same method is applied on latch, xor also and find that when finger width is approximately 2 μ then it gives better results as compare to other fingure widths.

Table 3.2: Comparison of different fingers buffer design.

Number of fingures	Fingure width	Area	Gain	Bandwidth
1	20μ	schematic	3.097dB	11.06GHz
4	5μ	$6\mu \times 30\mu$	3.402dB	8.37GHz
8	2.5μ	$9\mu \times 26\mu$	3.402dB	9.93GHz
12	1.67μ	$12\mu \times 23\mu$	3.739dB	10.16GHz
16	1.25μ	$14\mu \times 25\mu$	3.665dB	10.26GHz
20	1μ	$17.5\mu \times 25.5\mu$	2.827dB	signal attenuation

Chapter 4

Conclusion and Future Work

4.1 Conclusion

In this report, a 9-bit 20 GS/s pseudo-random sequence generator has been designed in schematic level. CML multiplexer is modified to reduce jitter in output response. A layout methodology, to ensure a optimize layout is developed based on correct finger width selection of switching device in CML logic. Comparable result of PRBS generator is achieved by optimized layout design. After layout, PRBS generator core reduces to 9Gb/s data rate which is designed for 10Gb/s data rate in schematic level. It doubles to 18Gb/s after MUXes. This report also suggests way to reduce parasitic capacitance and resistance in layout.

4.2 Future Work

Future work includes completion of PRBS Generator design and send it for fabrication and testing of it. PRBS generator and MUX is working with ideal clock. Attaching of VCO, initial condition circuit and DAC are yet to be done.

References

[1] Jianjun Yu, Xiang Zhou, Yue-Kai Huang, Shalabh Gupta, Ming-Fang Huang, Ting Wang, and Peter Magill, "112.8-Gb/s PM-RZ-64QAM Optical Signal Generation and Transmission on a 12.5GHz WDM Grid," in *Optical Fiber Communication Conference*. 2010, p. OThM1, Optical Society of America.

[2] Y.M. Greshishchev, D. Pollex, S.C. Wang, M. Besson, P. Flemeke, S. Szilagyi, J. Aguirre, C. Falt, N. Ben-Hamida, R. Gibbins, et al., "A 56gs/s 6b dac in 65nm cmos with 256× 6b memory," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*. IEEE, pp. 194–196.

[3] M. Alioto and G. Palumbo, "Design strategies for source coupled logic gates," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 50, no. 5, pp. 640–654, 2003.

[4] P. Heydari, "Design and analysis of low-voltage current-mode logic buffers," in *Quality Electronic Design, 2003. Proceedings. Fourth International Symposium on*. IEEE, 2003, pp. 293–298.

[5] S. Bommalingaiahnapallya, K.J. Sham, M.R. Ahmadi, and R. Harjani, "High-speed circuits for a multi-lane 12 gbps cmos prbs generator," in *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*. IEEE, 2007, pp. 3896–3899.

[6] K.J. Sham, S. Bommalingaiahnapallya, M.R. Ahmadi, and R. Harjani, "A 3×5-gb/s multilane low-power 0.18-μm cmos pseudorandom bit sequence generator," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 5, pp. 432–436, 2008.

[7] M. Singh, M. Sakare, and S. Gupta, "Testing of high-speed dacs using prbs generation with "alternate-bit-tapping"," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2011*. IEEE, pp. 1–6.

[8] S. Kim, M. Kapur, M. Meghelli, A. Rylyakov, Y. Kwark, and D. Friedman, "45-gb/s sige bicmos prbs generator and prbs checker [pseudorandom bit sequence]," *Proceedings of the IEEE Custom Integrated Circuits Conference,*, pp. 313–316, 2003.

[9] E. Laskin and S.P. Voinigescu, "A 60 mw per lane, 4× 23-gb/s 27 prbs generator," in *Compound Semiconductor Integrated Circuit Symposium, 2005. CSIC'05. IEEE*. IEEE, 2006, pp. 3–pp.

[10] J.K. Kim, J. Kim, and D.K. Jeong, "A 20-gb/s full-rate 2^7-1 prbs generator integrated with 20-ghz pll in 0.13-μm cmos," *IEEE Asian Solid-State Circuits Conference,(A-SSCC'08)*, pp. 221–224, 2008.

[11] T. Kjellberg, J. Hallin, and T. Swahn, "104gb/s 2^{11}-1 and 110gb/s 2^9-1 prbs generator in inp hbt technology," *ISSCC, Digest of Technical Papers*, pp. 2160–2169, 2006.

[12] T.O. Dickson, E. Laskin, I. Khalid, R. Beerkens, Jingqiong Xie, B. Karajica, and S.P. Voinigescu, "An 80-gb/s 2^{31}-1 pseudorandom binary sequence generator in sige bicmos technology," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 12, pp. 2735 – 2745, dec. 2005.

[13] T. Dickson, E. Laskin, L. Khalid, R. Beerkens, J. Xie, B. Karajica, and S. Voinigescu, "A 72 gb/s 2^{31}-1 prbs generator in sige bicmos technology," *Digest of Technical Papers. ISSCC. 2005*, pp. 342–602, 2005.

[14] M. Sakare, M. Singh, and S. Gupta, "A 4× 20 gb/s 2 9-1 prbs generator for testing a high-speed dac in 90nm cmos technology," *Progress in VLSI Design and Test*, pp. 252–257, 2012.

[15] J.J. O Reilly, "Series-parallel generation of m-sequences," *The Radio and Electronic Engineer*, vol. 45, no. 4, pp. 171–176, 1975.

[16] T.O. Dickson, K.H.K. Yau, T. Chalvatzis, A.M. Mangan, E. Laskin, R. Beerkens, P. Westergaard, M. Tazlauanu, Ming-Ta Yang, and S.P. Voinigescu, "The invariance of characteristic current densities in nanoscale mosfets and its impact on algorithmic design methodologies and design porting of si(ge) (bi)cmos high-speed building blocks," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 8, pp. 1830 –1845, aug. 2006.

[17] S. Galal and B. Razavi, "10-gb/s limiting amplifier and laser/modulator driver in 0.18-μm cmos technology," *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 12, pp. 2138–2146, 2003.

[18] D. Kucharski and K. Kornegay, "A 40 gb/s 2.5 v 27-1 prbs generator in sige using a low-voltage logic family," in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, feb. 2005, pp. 340 –602 Vol. 1.

[19] F. Weiss, H.-D. Wohlmuth, D. Kehrer, and A.L. Scholtz, "A 24-gb/s 2^7 - 1 pseudo random bit sequence generator ic in 0.13 -μm bulk cmos," in *Solid-State Circuits Conference, 2006. ESSCIRC 2006. Proc. of the 32nd European*, sept. 2006, pp. 468 –471.

[20] B. Laemmle, B. Sewiolo, and R. Weigel, "A $2^9 - 1$ up to 25gb/s m-sequence generator ic for uwb radar applications in a low-cost sige bicmos technology," in *German Microwave Conference, 2009*, march 2009, pp. 1 –4.

[21] Behazad Razavi, *Principles of Data Conversion System Design*, NJ Press, 1995.

[22] R.J. Baker, *CMOS: Circuit design, layout, and simulation*, vol. 18, Wiley-IEEE Press, 2011.