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Determining the reliable minimum unit capacitance for the DAC capacitor array of SAR ADCs

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ABSTRACT

The layout area of an SAR ADC is mainly occupied by its DAC capacitor array. Since there are 2^N matched unit capacitors employed for a binary-weighted N-bit DAC, selecting a small unit capacitance is the key to reducing the layout area of the capacitor array, and accordingly reduce the total area of an SAR ADC for size-constrained implantable or wearable applications. In this paper the matching error and thermal noise of the capacitor array are considered systematically for the whole SAR ADC to determine the minimum unit capacitance. The statistical analysis shows that the matching error of the capacitor array depends not only on the matching parameter of the given process but also on the confidence level of the design, while thermal noise analysis shows that thermal noise of the capacitor array does not equal that of either the unit capacitor or the total capacitance of the capacitor array. The calculations for the matching error and thermal noise of a 10-bit DAC show that although the matching error is 7 times bigger, thermal noise which consumes 1/8 error budget should not be ignored for determining the reliable minimum unit capacitance. An iterative algorithm is proposed to find the minimum value when both matching error and thermal noise are considered. A 10-bit SAR ADC adopting an 89.44 fF poly–poly unit capacitor in the 0.35 μm CMOS process validated the method.

1. Introduction

The successive approximation register (SAR) ADC has been reported as the lowest power consuming ADC [1], and has proven particularly useful in low-power, low data rate biomedical applications such as implantable neural recording devices [2–5] where both the chip size and the power consumption are restricted. The general block diagram of a SAR ADC is shown in Fig. 1, which illustrates the sample and hold operation, the charge scaling DAC capacitor array, the comparator, and the SAR control logic. The N-bit binary-weighted DAC is composed of N capacitors with values of C, $2C$, $4C$ up to $2^{N-1}C$ in N charging branches plus one extra non-charging branch with unit capacitance C. To convert the analog signal sampled and held by capacitor C_i to digital form, each charging branch is switched to the reference voltage (V_{ref}) or to ground at a given time controlled by the successive approximation register (SAR).

For an N-bit binary-weighted DAC capacitor array with unit capacitance C, the maximum capacitance in the charging branches reaches the value of 2^{N-1}C. Decreasing the unit capacitance value can greatly reduce the layout area of the capacitor array for area constrained applications whilst also reducing the charging power consumption [1] for low-power applications. Different types of capacitor arrays have been demonstrated in the literature, such as the series-split capacitor array [6], in which a fractional value bridge capacitor reduces both the area and the power consumption of the capacitor array. However extra effort is required to match the bridge capacitor to the unit capacitor. Furthermore, even in a split capacitor array, the fundamental issue of determining the minimum unit capacitance value remains. The work presented in this paper is motivated by the need for the implementation of a small area (~1 mm^2) neural recording die incorporating multiple differential input channels, amplifiers, a multiplexer and a 10-bit SAR ADC. The die is intended to be implanted into the brain of a blowfly for the benefit of a high signal to noise ratio (SNR), in order to record visual neural signals from the freely behaving blowfly for the in vivo study on flight control in a Human Frontier Scientific Program (HFSP). The available implantable area of the blowfly is 1.2 mm by 1.0 mm in each side of the brain, therefore the unit capacitor value should be chosen as small as possible to reduce the chip size for easy implantation and to lower the power consumption to prevent heat effects on neural cells.

Typical unit capacitor values employed by other groups include a 24 fF unit capacitor for an 8-bit ADC [1] and a 33 fF unit capacitor for a 10-bit ADC [2]. In those applications, the unit capacitor values of the capacitor array are given without providing a rigorous method for the determination of the unit capacitance.

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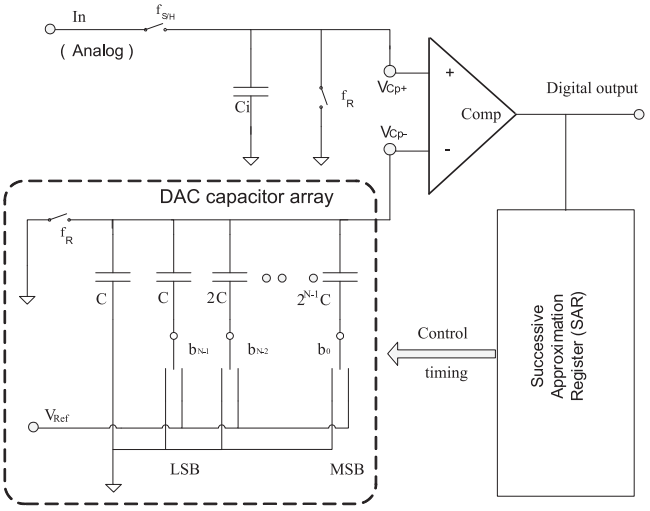

Fig. 1. Generic block diagram of the SAR ADC.

Previously, a rather large unit capacitor value of 657 fF has been calculated for a 12-bit SAR ADC based on the thermal noise restriction and the fabrication error in the 0.35 μm CMOS process [7], and recently, a small unit capacitor value of 13.5 fF has been adopted for a 10-bit SAR ADC [8]. However, in these designs the error budget of the DAC capacitor array has been assigned as the whole ADC error budget. Therefore a systematic method which considers the design restrictions for the entire SAR ADC to determine the minimum unit capacitor of the DAC capacitor array is in need.

Section II of the paper presents the statistical calculations for matching error of the capacitor array with a given confidence level of 99.9% for a high yield rate. Section III describes the thermal noise estimation of an entire capacitor array to show that thermal noise of the DAC capacitor array is slightly different from the commonly considered form of $\sqrt{\frac{KT}{C}}$. Section IV describes the algorithm to search for the minimum unit capacitance when both thermal noise and matching error are considered. Section V presents an application example of choosing unit capacitance for a 10-bit SAR ADC where DAC capacitor array is treated as part of the SAR ADC and consequently the DAC capacitor array has to be assigned a reduced error budget, validating the proposed method. Section VI concludes the paper.

2. Matching-determined minimum unit capacitance

Integrated CMOS capacitors can be implemented by means of conductive layers such as metal, polysilicon or other diffused layers. The absolute accuracy of the capacitor value is relatively poor. Special layout techniques such as the common centroid one [9] which are sensitive only to the matching of the capacitors rather than to their absolute values [9,10] are commonly employed for the implementation of a binary-weighted DAC capacitor array. The following discussion on capacitor matching assumes a common centroid layout.

In the common centroid layout of an N-bit DAC, the capacitor of value $2^M C$ (see Fig. 1) in the Mth charging branch ($0 \leq M < N$) is implemented by 2^M unit capacitors connected in parallel. Therefore the number of the total unit capacitors employed in the whole capacitor array is $1+1+2+4+\ldots+2^{N-1}=2^N$.

The values of the fabricated unit capacitor, which deviate from its nominal value due to imperfections in the fabrication process, can be modeled as the Gaussian distribution. Given that the process variation ratio $\frac{\Delta C}{C}$ of the capacitor C in a CMOS fabrication process holds that $\frac{\Delta C}{C} \sim N(0,\ \sigma^2)$ [11], the capacitor matching error for the DAC capacitor array can be estimated as follows:

The capacitor $C_M=2^M C$ in the Mth charging branch can be expressed as:

$$C_M = (C+\Delta C_1)+(C+\Delta C_2)+\cdots+(C+\Delta C_{2^M}) = 2^M C + \sum_{i=1}^{2^M} \Delta C_i \tag{1}$$

where ΔC_i denotes the deviation from the nominal value of the ith unit capacitor. The variation ratio of the capacitor $2^M C$ is:

$$\frac{\Delta C_M}{2^M C} = \frac{\Delta C_1 + \Delta C_2 + \cdots + \Delta C_{2^M}}{2^M C} = \frac{1}{2^M}\left(\frac{\Delta C_1}{C} + \frac{\Delta C_2}{C} + \cdots + \frac{\Delta C_{2^M}}{C}\right) \tag{2}$$

Given that the distribution of the variation $(\Delta C/C)$ for the single unit capacitor is $N(0,\sigma^2)$and assuming that the fabrication error for each C is independent [12], the probability distribution for $\left(\frac{\Delta C_1}{C} + \frac{\Delta C_2}{C} + \cdots + \frac{\Delta C_{2^M}}{C}\right)$ becomes [13]:

$$\left(\frac{\Delta C_1}{C} + \frac{\Delta C_2}{C} + \cdots + \frac{\Delta C_{2^M}}{C}\right) \sim N(0,\ 2^M\sigma^2) \tag{3}$$

Similarly, the probability distribution of $\left(\frac{\Delta C_1}{C} + \frac{\Delta C_2}{C} + \cdots + \frac{\Delta C_{2^N}}{C}\right)$ holds that:

$$\left(\frac{\Delta C_1}{C} + \frac{\Delta C_2}{C} + \cdots + \frac{\Delta C_{2^N}}{C}\right) \sim N(0,\ 2^N\sigma^2) \tag{4}$$

To calculate the matching error of a capacitor array, the ideal output voltage V_{out_M} of the Mth branch when charged to V_{ref} is calculated as the voltage divided between two capacitors (one of value $2^M C$, and the other which is the parallel combination of the rest of the charging branches) as $\frac{2^M C}{2^N C} V_{ref}$, which is the ratio of the total capacitance corresponding to 2^M and 2^N unit capacitors. The worst case capacitor matching error for the Mth branch can be calculated by taking into account the variations of both $2^M C$ and $2^N C$ as $Err_{m-m} = \frac{\Delta C_M}{2^N C - \Delta C_N} V_{ref}$, which can be calculated under a given confidence level corresponding to the reliability and the expected yield rate of the design.

For a given confidence level of 99.9% (taking $3.5\times\sigma$ as the deviation) for high reliability, Err_{m-m} can be calculated as:

$$Err_{m_m} = \frac{\Delta C_M}{2^N C - \Delta C_N} V_{ref} = \frac{2^M C(1/2^M)(3.5\sigma\sqrt{2^M})}{2^N C - 2^N C(1/2^N)(3.5\sigma\sqrt{2^N})} V_{ref} = \frac{3.5\sigma\sqrt{2^M}}{2^N - 3.5\sigma\sqrt{2^N}} V_{ref} \tag{5}$$

The worst-case mismatch error Err_m for an N-bit DAC becomes:

$$Err_m = \sum_{i=0}^{N-1} Err_{m_i} = \frac{3.5\sigma\sum_{i=0}^{N-1}\sqrt{2^i}}{2^N - 3.5\sigma\sqrt{2^N}} V_{ref} = \frac{3.5\sigma(\sqrt{2^N}-1)}{\left(\sqrt{2}-1\right)(2^N - 3.5\sigma\sqrt{2^N})} V_{ref} \tag{6}$$

Considering that the maximum tolerable error for an N-bit DAC is $\pm(1/2)$ LSB which equals $V_{ref}/2^{N+1}$, the required σ value to constrain the matching error to within $\pm(1/2)$ LSB can be obtained from (6) as:

$$\frac{3.5\sigma(\sqrt{2^N}-1)}{(\sqrt{2}-1)(2^N - 3.5\sigma\sqrt{2^N})} V_{ref} \leq \frac{1}{2^{N+1}} V_{ref} \tag{7}$$

therefore

$$\sigma \leq \frac{(\sqrt{2}-1)2^N}{3.5[2^{N+1}(\sqrt{2^N}-1) + (\sqrt{2}-1)\sqrt{2^N}]} \tag{8}$$

For a given CMOS process, the standard deviation σ is a known function of the capacitor area which corresponds to a specific capacitance value.

In practice the static performance of the DAC is commonly described by the integral nonlinearity (INL) and the differential nonlinearity (DNL). For a given DAC code of $b_{N-1}b_{N-2}\ldots b_0$, the INL of the code can be expressed as:

$$INL = \sum_{i=0}^{N-1} b_i Err_{m_i} \le \sum_{i=0}^{N-1} Err_{m_i} = Err_m \tag{9}$$

where equal is taken when $b_{N-1}b_{N-2}\ldots b_0 = 11\ldots1$.

For two adjacent ADC codes of $b_{N-1}b_{N-2}\ldots b_0$ and $a_{N-1}a_{N-2}\ldots a_0$ ($b_{N-1}b_{N-2}\ldots b_0 = a_{N-1}\,a_{N-2}\ldots a_0 + 1$), the DNL can be expressed as:

$$DNL = \left| \sum_{i=0}^{N-1} b_i Err_{m_i} - \sum_{i=0}^{N-1} a_i Err_{m_i} \right| = \sum_{i=0}^{N-1} |(b_i - a_i)| Err_{m_i} \le \sum_{i=0}^{N-1} Err_{m_i} = Err_m \tag{10}$$

where equal is taken when $b_{N-1}b_{N-2}\ldots b_0 = 10\ldots0$ and $a_{N-1}a_{N-2}\ldots a_0 = 01\ldots1$.

Formulae (9) and (10) show that unit capacitor calculated by matching error Err_m satisfies both INL and DNL requirements.

3. Unit capacitance determined by the capacitor array's thermal noise estimation

When considering the capacitor matching error, charging switches used in the capacitor array are treated as ideal switches which have zero on-resistance and no effect upon the final voltage output of the capacitor array. However, for thermal noise analysis, the on-resistance of the switching transistors should be taken into consideration as sources of thermal noise which affects the output of the capacitor array.

The thermal noise of the capacitor used in the simple switching circuit shown in Fig. 2 can be calculated as $\sqrt{KT/C}$ [14], where K denotes the Boltzmann constant of 1.38×10^{-23} J K^{-1}, T the absolute temperature value and r the on-resistance of the CMOS transistor. $V_R{}^2$ denotes the thermal noise produced by this transistor. The on-resistance of a CMOS switching transistor is related to the transistor size by:

$$r = \frac{L}{\mu C_{ox} W (V_{GS} - V_T - V_{DS})} \tag{11}$$

where W and L denote the width and the length of the transistor, respectively.

In previous works [7], the quantity $\sqrt{KT/C}$ has been adopted as the thermal noise restriction when choosing the value of the unit capacitance. However, when considering the capacitor array as a whole, its noise properties differ from those of a single capacitor. The thermal noise of a capacitor array with N branches (see Figs. 1 and 3) is composed of N independent thermal noise components produced by the on-resistances of N switches in the DAC capacitor array. Assuming that the charging switches used in the capacitor array are identical and that V_{ref} is an ideal voltage source, the thermal noise caused by the individual switching transistor noise sources of an N-bit DAC can be estimated by means of the equivalent circuits shown in Fig. 3, where 2^MC is the capacitance of the Mth charging branch and the remaining

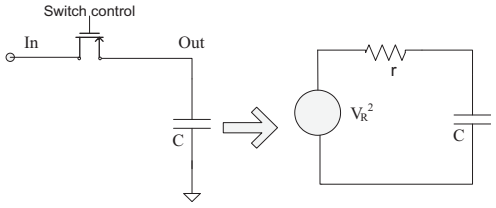

Fig. 2. Basic switched capacitor circuit and its thermal noise model equivalent.

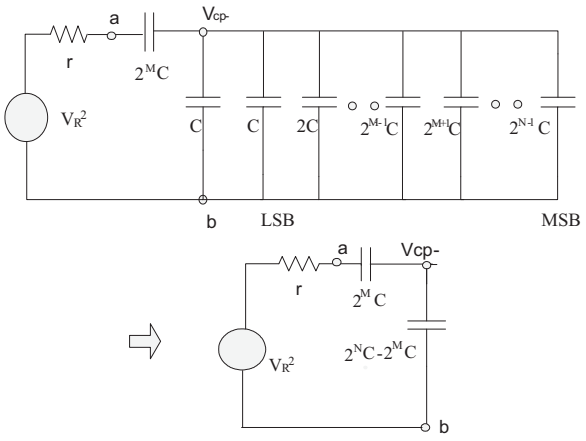

Fig. 3. The equivalent circuit of the capacitor array for thermal noise estimation. Point 'a' corresponds to the capacitor's terminal connected to the charging switch in Fig. 1 while point 'b' corresponds to ground.

Table 1
Calculated noise factors.

Number of bits (N)	8	10	12	14	16
λ factor value	1.266	1.267	1.268	1.268	1.268

charging branches are connected either to the reference voltage (V_{ref}) or to ground via ideal charging switches.

The thermal noise of the Mth charging path at point 'a' in Fig. 3 can be calculated from the equivalent capacitance of 2^MC in series with the rest of the charging capacitors in parallel. The noise contribution of the Mth charging branch to the total output noise of the capacitor array (Err_{n_m}) is therefore determined by the thermal noise voltage at point 'a' divided between capacitor 2^MC and the rest of the capacitors in parallel (2^NC–2^MC):

$$Err_{n_m} = \frac{V_{cp-}}{V_a} \times V_a = \frac{2^M}{2^N}\sqrt{\frac{KT}{(2^M(2^N-2^M)C/2^N)}} = \sqrt{\frac{2^M}{2^N-2^M}} \times \sqrt{\frac{KT}{2^NC}} \tag{12}$$

The total noise from the capacitor array during the period of converting a sampled signal can be estimated as:

$$Err_n = \sqrt{\sum_{M=0}^{N-1} \frac{2^M}{2^N-2^M}} \times \sqrt{\frac{KT}{2^NC}} \tag{13}$$

considering that

$$\sqrt{\sum_{M=0}^{N-1} \frac{2^M}{2^N-2^M}} = \sqrt{\sum_{M=0}^{N-1} \frac{1}{2^{N-M}-1}} = \sqrt{1+\frac{1}{3}+\frac{1}{7}+\frac{1}{15}\cdots+\frac{1}{2^N-1}} > 1 \tag{14}$$

the thermal noise of the capacitor array Err_n shown in (13) is larger than $\sqrt{\frac{KT}{2^NC}}$ (2^NC is the total capacitance of the capacitor array), therefore theoretically $\sqrt{\frac{KT}{2^NC}}$ should not be considered as the thermal noise of the whole capacitor array.

Defining the value of a new factor λ as $\lambda = \sqrt{\sum_{M=0}^{N-1} \frac{2^M}{2^N-2^M}}$, the noise factor of $\sqrt{\frac{KT}{2^NC}}$ is calculated for different numbers of bits (N) and listed in Table 1. The λ values shown in Table 1 are not sensitive to the number of bits, and the thermal noise of the

capacitor array is less than 1.3 times $\sqrt{\frac{KT}{2^N C}}$ for N values up to 16, which is the typical case for SAR ADC applications. Although the calculated noise factor shown in Table 1 is about 30% higher than $\sqrt{\frac{KT}{2^N C}}$, when comparing to the accuracy of the designed ADC (such as 0.1% accuracy for 10-bit one) 30% is a relatively big figure.

Given $\frac{1}{2^{N+1}}V_{ref}$ as the noise budget of $\pm$½ LSB, the magnitude of the unit capacitance C must satisfy the following relationship in order to remain within this budget for an N-bit DAC:

$$\sqrt{\sum_{M=0}^{N-1}\frac{2^M}{2^N-2^M}}\times\sqrt{\frac{KT}{2^N C}}<\frac{1}{2^{N+1}}V_{ref} \tag{15}$$

Taking $\lambda=2$, the relation (15) can be simplified as:

$$Err_n<2\sqrt{\frac{KT}{2^N C}}<\frac{1}{2^{N+1}}V_{ref} \tag{16}$$

The above analysis demonstrates that the commonly adopted value of $\sqrt{KT/C}$ should not be assumed as the thermal noise for a capacitor array. However, using $\sqrt{KT/C}$ to estimate an upper bound limit for the thermal noise of a capacitor array is not inappropriate, since

$$\sqrt{\sum_{M=0}^{N-1}\frac{2^M}{2^N-2^M}}\times\sqrt{\frac{KT}{2^N C}}<2\sqrt{\frac{KT}{2^N C}}=\frac{2}{\sqrt{2^N}}\sqrt{\frac{KT}{C}}<\sqrt{\frac{KT}{C}}\quad \text{when} N>1 \tag{17}$$

On the other hand, it can be seen from (17) that $\sqrt{KT/C}$ cannot be used as the thermal noise restriction for the determination of the minimum unit capacitor.

4. Determining the reliable minimum unit capacitance of the SAR ADC for the 0.35 μm AMS process

As discussed in Sections II and III, the value of the unit capacitor in a capacitor array can be determined by the matching error and the thermal noise error respectively. For an N-bit capacitor array with a reference voltage V_{ref}, the total error should be within $\pm(1/2)$ LSB:

$$Err_m+Err_n\ \le V_{ref}/2^{N+1} \tag{18}$$

Half of the total error budget has been assigned to the matching error and the other half to the thermal noise to calculate the matching restricted unit capacitance and thermal noise restricted one, respectively, which in turn demonstrates whether the process matching or thermal noise is the dominant factor to determine the unit capacitance.

For process matching, (8) can be modified as:

$$\sigma\le\frac{(\sqrt{2}-1)2^N}{3.5\times[2^{N+2}(\sqrt{2^N}-1)+(\sqrt{2}-1)\sqrt{2^N}]} \tag{19}$$

Under the 0.35 μm AMS process poly–poly capacitor with the typical capacitive density of 0.86 fF/μm^2, it holds that [11]:

$$\sigma\left(\frac{\Delta C_{nom}}{C_{nom}}\right)=\frac{0.45\%}{\sqrt{WL}} \tag{20}$$

where W and L denote the width and the length of the capacitor in μm. C_{nom} denotes the nominal value of the capacitor and ΔC_{nom} the deviation due to the imperfect fabrication process. Eq. (20) indicates that the deviation of a capacitor value from nominal is inversely proportional to the square root of the area of the capacitor therefore a large unit capacitor results in a better matching. Combining (19) and (20), the reliable minimum value of the unit capacitor (fF) for process matching can be calculated as:

$$C_{m_min}=0.86\left\{\frac{0.45\%\times 3.5\times\left[2^{N+2}(\sqrt{2^N}-1)+(\sqrt{2}-1)\sqrt{2^N}\right]}{(\sqrt{2}-1)2^N}\right\}^2 \tag{21}$$

For thermal noise, referring back to (16), the minimum unit capacitance constrained by thermal noise is:

$$C_{n_min}=\frac{4KT\times 2^{N+4}}{{V_{ref}}^2} \tag{22}$$

Since both matching induced error and thermal noise induced error correspond to half of the total error budget each and in both cases increasing the unit capacitance decreases both types of errors, the minimum value of the unit capacitor for a capacitor array can be chosen as follows:

$$C_{min}=max\{C_{m_min},\ C_{n_min}\} \tag{23}$$

Table 2 shows the calculated unit capacitance for different numbers of bits under a reference voltage of 1 V for the 0.35 μm AMS process. Both C_{m_min} and C_{n_min} show a tendency of doubling when the number of bits is increased by 1 (error budget reduces by ½). In all cases the capacitance calculated according to thermal noise restriction is much smaller than that calculated from process matching, which means that the dominant error in a capacitor array is the capacitor matching error. Therefore a modern process with better matching performance will result in a smaller unit capacitor value and consequently easing the area restraint of the design.

Table 2
Calculated unit capacitance (fF) for DAC.

Number of bits	C_{m_min} (fF)	C_{n_min} (fF)	Reliable min. unit capacitance (fF)	Area (μm^2)
8	4.5	0.08	4.5	5.2
10	19.1	0.34	19.1	22.2
12	78.9	1.36	78.9	91.7

The capacitance values to account for process matching error are 50 times those for thermal noise considerations shown in Table 2, indicating that the equal error budget assignment for (18) can be further optimized for area restricted applications. Furthermore, this 50-time means that the thermal noise contributed by the capacitor chosen by (23) is about 1/7 the matching error, therefore thermal noise of the capacitor array should not be ignored in the determining of the reliable minimum unit capacitance. A search algorithm is proposed to find the minimum unit capacitance from formula (18) where capacitor matching and thermal noise are considered together,

Step 1. Calculate the matching determined unit capacitance using (21). Assign 50% of the total error budget to the thermal noise.
Step 2. Calculate thermal noise produced by the matching determined unit capacitance using (13).
Step 3. Calculate the available error budget for improvement: subtract the calculated thermal noise from thermal noise budget. If the calculated thermal noise is greater than the error budget left for it, stop searching. Otherwise go to step 4.
Step 4. Add 50% of the available error budget for improvement to the matching error, combining (6) and (20) to calculate the matching determined unit capacitance.
Step 5. Go to step 2.

5. A design case for a 0.35 μM AMS SAR ADC

5.1. Unit capacitance

A DAC capacitor array has been designed for a 10-bit SAR ADC. The unit capacitance for this design was not chosen based on Table 2 since the unit capacitance values shown in Table 2 are calculated for a total error budget of $\pm 1/2$ LSB. When the DAC is used as part of an SAR ADC, $\pm ½$ LSB becomes the error budget for the whole ADC and therefore the error budget of the DAC should be less than that of the whole ADC. To be in the safe side, allocating 50% of the error budget of the entire SAR ADC for the DAC, the figures required for DAC of the SAR ADC should be about 4 times larger than their counterparts in Table 2, resulting in 76.4 fF for a 10-bit ADC. Given the capacitor density of 0.86 fF/μm^2 for the 0.35 μm AMS process, it corresponds to a poly–poly capacitor with an area of 88.8 μm^2 (about 9.43 μm by 9.43 μm). A 10 μm by 10 μm poly–poly unit capacitor corresponding to 89.44 fF, a value safely above this theoretical minimum unit capacitance, was chosen for this design.

5.2. Chip tests

A 10-bit SAR ADC with a unit capacitance of 89.44 fF has been fabricated as part of a die with dimensions of 1.1 mm by 1.0 mm as shown in Fig. 4. The die contains two differential input amplifiers, a multiplexer, and the 10-bit SAR ADC. The DAC capacitor array, occupying about 1/3 of its active area, is illustrated in the middle right of the die. Choosing a small unit capacitance was the key point to reducing the size of this design, making the designed die suitable for the implantable neural recording in the brain of the blowfly.

The static performance of the SAR ADC has been tested, which shows an INL of +0.68/−0.41 LSB and DNL of +0.82/−0.67 LSB. The signal to noise ratio (SNR) calculated from the tested spectrum shown in Fig. 5 is 56.68 dB, which corresponds to 9.1 effective number of bits (ENOB) calculated via ENOB=(SNR−1.76)/6.02. Therefore the chosen 89.44 fF poly–poly unit capacitor is big enough to perform the 10-bit SAR ADC in 0.35 μm AMS process.

For the matching error calculation codified by (6), the 3.5σ process deviation meant there was less than a 0.05% chance that the matching error became larger than the assigned error budget. The unit capacitor value chosen in this design was slightly larger than the calculated minimum acceptable value, which actually resulted in an even smaller matching error, corresponding to less than a 0.05% chance of exceeding the error budget. Similar test results obtained from the 19 other chips from the same batch further validated the proposed method for the determination of the reliable minimum unit capacitance for a size-constrained SAR ADC.

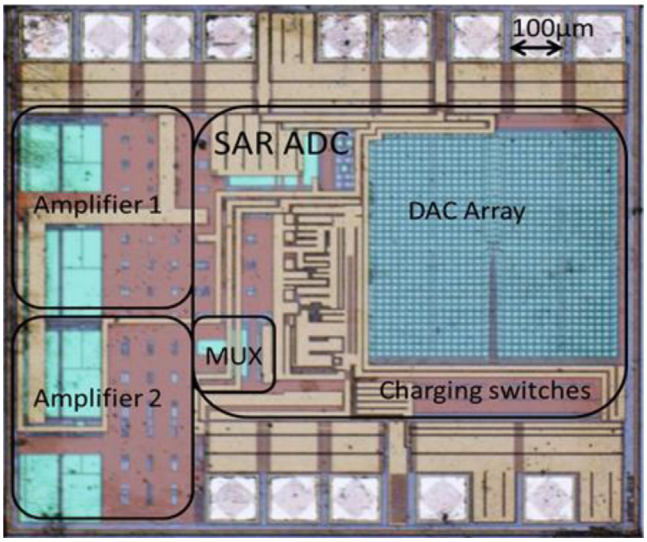

Fig. 4. Layout of the die containing the capacitor array and charging switches for a SAR ADC.

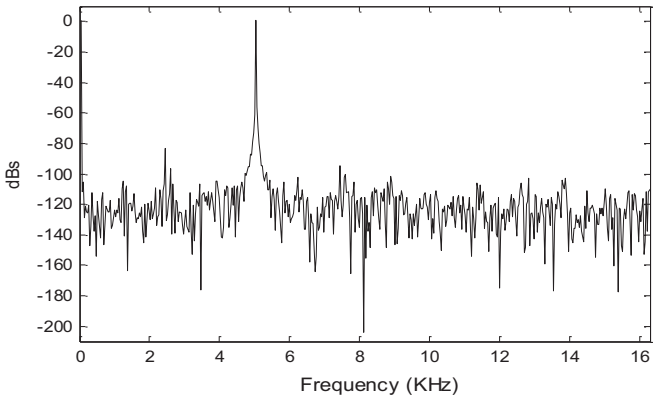

Fig. 5. Noise performance of the designed ADC (5 KHz single tone under the sample frequency of 33 KHz).

Table 3
Comparison matching error calculation of this work against that in Ref. [7] for a 12-bit ADC.

	Ref. [7]	This work
Confidence level	99.7% (3σ)	99.9% (3.5σ)
Error budget assigned	½ LSB	1/8LSB
Unit capacitance (fF)	657	315 (76.4[a])
Improvement (1-this work/[7])	51.9% (88.3%[a])	

[a] Results from the calculation using the error budget assignment of ½ LSB.

5.3. Comparisons

The unit capacitance values reported in [1,2] were given without clear descriptions of how they were determined. Therefore it is not easy to fairly compare the reported figures against the values determined by the proposed method due to the unclear factors such as reference voltage (although it can be normalized), error budget assignment, and the confidence level. The unit capacitance value determined by the matching error calculations for a 12-bit SAR ADC are compared to that reported in [7] in Table 3. The calculations demonstrate a greater than 50% improvement when 1/8LSB is assigned as error budget for this work. If the same error budget of $\pm 1/2$ LSB were assigned to the DAC alone, a more than 80% improvement would be achieved using the proposed method with an even higher confidence level.

It is worth noting that the unit capacitor reported in [8] is 14.5 fF which seems much smaller than 76.4 fF calculated in this work. However, considering that a whole error budget of ½ LSB was assigned in [8], a less than 5 fF poly–poly unit capacitor would be calculated by the proposed method under that error budget.

Smaller unit capacitors lead to lower power consumption since the power consumption of the capacitor array is directly proportional to the total capacitance of the array [1]. The saving in power consumption would in turn result in reduced battery capacity requirements for implantable or wearable applications. A smaller unit capacitance value would also reduce charging time and thus improve the maximum achievable bandwidth or sampling rate of the system.

5.4. Discussions

The reliable minimum unit capacitor calculated for a 10-bit SAR ADC using 0.35 um process is about 90 fF in theory. Test results confirm the yield but DNL results are slightly bigger than the expected value of ½ LSB. Although it is a fact that the performance of the SAR ADC depends on other parts of the SAR ADC as well, a more precise model with the consideration of parasitic effects, process gradients [15], and the modified thermal noise model with the consideration of all on-resistance of each charging switch, might be helpful to explain the results.

Unit capacitors can be chosen smaller than the calculated reliable minimum unit capacitor since the minimum unit capacitor calculated in this paper is based on restricting the worst case matching error within the error budget of ½ LSB with a very high reliability. In practice the reliability of the design can be modified by adjusting the confidence level to ease the process matching restriction which is the dominant one in the design. If taking 68% as the confidence level, formula (5) becomes,

$$Err_{m_m} = \frac{\sigma\sqrt{2^M}}{2^N - \sigma\sqrt{2^N}} V_{ref} \tag{24}$$

Using formula (24) will result in an approximate 3.5-time smaller capacitor value. Therefore there is a trade-off between the value of the unit capacitance and the reliability (yield rate) in SAR ADC design. For the extreme area-restricted applications, taking a smaller unit capacitor with a reduced yield rate could be a choice. Also in this paper the error budget of the DAC has been assigned as 50% of the error budget of entire SAR ADC and therefore it has room to optimize this percentage figure in order to reduce the value of the unit capacitor. Finally, as demonstrated in formulae (8) and (20), a modern CMOS process promising a better matching, therefore a smaller unit capacitor can be expected. The ability of choosing a variable unit capacitance demonstrates that the proposed method is generic enough to meet different application requirements.

6. Conclusions

The minimum unit capacitance value to implement the binary weighted N-bit DAC capacitor arrays in SAR ADCs can be accurately determined by statistical methods and thermal noise calculations. The thermal noise calculation shows that thermal noise of the entire DAC capacitor array does not equal either $\sqrt{KT/C}$ or $\sqrt{\frac{KT}{2^N C}}$. The calculations for a 10-bit SAR ADC demonstrate that the unit capacitance value is primarily dominated by process matching limitations, therefore the algorithm for searching the reliable minimum unit capacitor can start from the point where half of the error budget is assigned to calculate the process matching restricted unit capacitance. Since the matching error is related to the confidence level, an even small unit capacitor can be chosen by trading the yield. It also suggests that a modern process with better matching performance will result in a smaller unit capacitor value easing the area restraint of the design. The ADC test results on a small production-run 10-bit SAR ADC chip validated the method of determining the minimum unit capacitance which is able to reduce chip area, lower power consumption, and improve conversion rate, being particularly desirable for implantable or wearable biomedical applications.

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