$$\text{For the MOSFET:} \quad I_D = \frac{g_m(V_{GS} - V_{TN})}{2} = \frac{40\text{ mS}(0.5\text{ V})}{2} = 10\text{ mA}$$

$$K_n = \frac{g_m^2}{2I_D} = \frac{(40\text{ mS})^2}{2(10\text{ mA})} = 0.08\frac{\text{A}}{\text{V}^2} \quad \text{and}$$

$$\frac{W}{L} = \frac{K_n}{K_n'} = \frac{80\text{ mA/V}^2}{50\ \mu\text{A/V}^2} = \frac{1600}{1}$$

The 25-Ω requirement can be met with either device, but the BJT requires an order of magnitude less current. In addition, the MOSFET requires a large W/L ratio.

Discussion: The options developed here represent our first attempts, and there is no guarantee that we will actually be able to fully achieve the desired specifications. After attempting a full design, we may have to change the circuit choice or use more than one transistor in a more complex amplifier configuration.

EXERCISE: Suppose the BJT amplifier in part (b) of Design Ex. 14.6 will be designed with symmetric 15-V supplies using a circuit similar to the one in Figure P14.1(f). Choose a collector current.

ANSWER: 5 μA, (10 μA does not account for the effect of R_B)

EXERCISE: Estimate the collector current needed for a BJT to achieve the input resistance specification in part (f) of Design Ex. 14.6.

ANSWER: 12.5 μA

14.7 COUPLING AND BYPASS CAPACITOR DESIGN

Up to this point, we have assumed that the impedances of coupling and bypass capacitors are negligible, and have concentrated on understanding the properties of the single transistor building blocks in their "midband" region of operation. However, since the impedance of a capacitor increases with decreasing frequency, the coupling and bypass capacitors generally reduce amplifier gain at low frequencies. In this section, we discover how to pick the values of these capacitors to ensure that our midband assumption is valid. Each of the three classes of amplifiers will be considered in succession. The technique we use is related to the "short-circuit" time constant (SCTC) method that we shall study in greater detail in Chapter 17. In this method, each capacitor is considered separately with all the others replaced by short circuits ($C \to \infty$).

14.7.1 COMMON-EMITTER AND COMMON-SOURCE AMPLIFIERS

Let us start by choosing values for the capacitors for the C-E and C-S amplifiers in Fig. 14.2. For the moment, assume that C_3 is still infinite in value, thus shorting the bottom of R_E and R_S to ground, as drawn in Fig. 14.34(a) and (b).

Coupling Capacitors C_1 and C_2

First, consider C_1. In order to be able to neglect C_1, we require the magnitude of the impedance of the capacitor (its capacitive reactance) to be much smaller than the equivalent resistance that appears at its terminals. Referring to Fig. 14.34, we see that the resistance looking to the left from capacitor

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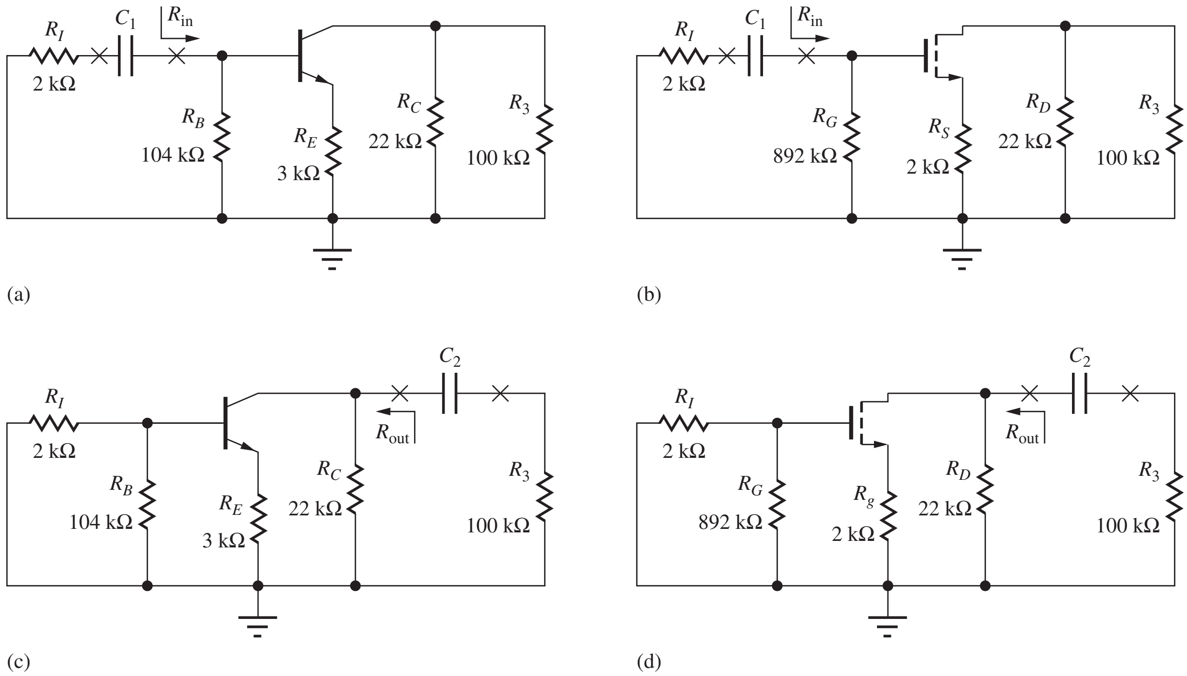

Figure 14.34 Coupling capacitors in the common-emitter and common-source amplifiers.

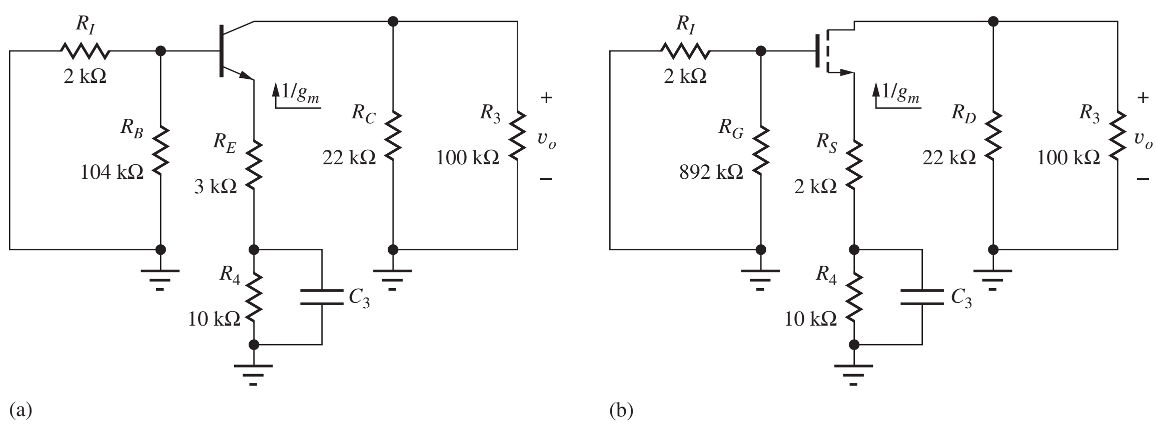

Figure 14.35 Bypass capacitors in the common-emitter and common-source amplifiers.

C_1 (with $v_i = 0$) is R_I, and that looking to the right is R_{in}. Thus, design of C_1 requires

$$\frac{1}{\omega C_1} \ll (R_I + R_{\text{in}}) \qquad \text{or} \qquad C_1 \gg \frac{1}{\omega(R_I + R_{\text{in}})} \tag{14.107}$$

Frequency ω is chosen to be the lowest frequency for which midband operation is required in the given application.

For the common-emitter stage, bias resistor R_B appears in parallel (shunt) with the input resistance of the transistor, so $R_{\text{in}} = R_B \| R_{iB}$. For the common-source stage, bias resistor R_G shunts the input resistance of the transistor, and $R_{\text{in}} = R_G \| R_{iG} = R_G$.

A similar analysis applies to C_2. We require the reactance of the capacitor to be much smaller than the equivalent resistance that appears at its terminals. Referring to Fig. 14.34(b), the resistance

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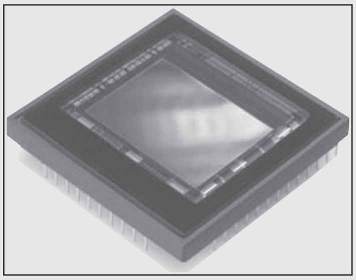
ELECTRONICS IN ACTION

Revisiting the CMOS Imager Circuitry

In the first Electronics in Action feature in Chapter 4, we introduced a CMOS imager circuit. The chip contains 4 million pixels in a 2352×1728 imaging array. A typical photodiode based imaging pixel consists of a photo diode with sensing and access circuitry. Let us revisit this sensor circuit in light of what we have learned about single transistor amplifiers.



DALSA 8 MegaPixel CMOS image sensor.[1]
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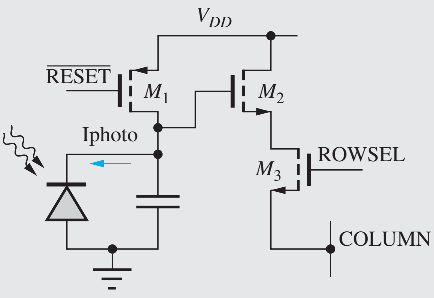

(b)

Typical photo diode pixel architecture.

M_1 is a reset switch, and after the $\overline{\text{RESET}}$ signal is asserted, the storage capacitor is fully charged to V_{DD}. The reset signal is then removed, and light incident on the photodiode generates a photo current that discharges the capacitor. Different light intensities produce different voltages on the capacitor at the end of the light integration time. Transistor M_2 is a source follower that buffers the photo-diode node. The source follower transfers the signal voltage at the photo-diode node to the output with nearly unity gain, and M_2 does not disturb the voltage at the photo diode output since it has an infinite dc input resistance. The voltage at the source of M_2 is then transferred to the output column via switch M_3. The source follower provides a low output resistance to drive the capacitance of the output column. The W/L ratio of switch M_3 must be chosen carefully so it does not significantly degrade the overall output resistance.

[1] The chip pictured above is a DALSA CMOS image sensor and is reprinted here with permission from Dalso Corporation.

looking to the left from capacitor C_2 is R_{out}, and that looking to the right is R_3. Thus, C_2 must satisfy

$$\frac{1}{\omega C_2} \ll (R_{\text{out}} + R_3) \qquad \text{or} \qquad C_2 \gg \frac{1}{\omega(R_{\text{out}} + R_3)} \tag{14.108}$$

For the common-emitter stage, collector resistor R_C appears in parallel with the output resistance of the transistor, and $R_{\text{out}} = R_C \| R_{iC}$. For the common-source stage, drain resistor R_D shunts the output resistance of the transistor, so $R_{\text{out}} = R_D \| R_{iD}$.

Bypass Capacitor C_3

The formula for C_3 is somewhat different. Figure 14.35 depicts the circuit assuming we can neglect the impedance of capacitors C_1 and C_2. At the terminals of C_3 in Fig. 14.35(a), the equivalent resistance is equal to R_4 in parallel with the sum $(R_E + 1/g_m)$,[8] the resistance looking up toward the

[8] For the BJT case, we are neglecting the $R_{th}/(\beta_o + 1)$ term. Since the additional term will increase the equivalent resistance, its neglect makes Eq. (14.109) a conservative estimate.

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emitter of the transistor. Thus, for the C-E and C-S amplifiers, C_3 must satisfy

$$C_3 \gg \frac{1}{\omega\left[R_4 \middle\| \left(R_E + \dfrac{1}{g_m}\right)\right]} \quad \text{or} \quad C_3 \gg \frac{1}{\omega\left[R_4 \middle\| \left(R_S + \dfrac{1}{g_m}\right)\right]} \tag{14.109}$$

In order to satisfy the inequalities in Eqs. (14.107) through (14.109), we will set the capacitor value to be approximately 10 times that calculated in the equations.

DESIGN EXAMPLE 14.7 CAPACITOR DESIGN FOR THE C-E AND C-S AMPLIFIERS

In this example, we select capacitor values for the three capacitors in both inverting amplifiers in Figs. 14.2, 14.34, and 14.35.

PROBLEM Choose values for the coupling and bypass capacitors for the amplifiers in Fig. 14.2 so that the presence of the capacitors can be neglected at a frequency of 1 kHz (1 kHz represents an arbitrary choice in the audio frequency range).

SOLUTION **Known Information and Given Data:** Frequency $f = 1000$ Hz; for the C-E stage described in Fig. 14.2 and Table 14.3, $R_{iB} = 310$ kΩ, $R_{iC} = 4.55$ MΩ, $R_I = 2$ kΩ, $R_B = 104$ kΩ, $R_C = 22$ kΩ, $R_E = 3$ kΩ, $R_4 = 10$ kΩ, and $R_3 = 100$ kΩ; for the C-S stage from Table 14.4, $R_{iG} = \infty$, $R_{iD} = 442$ kΩ, $R_I = 2$ kΩ, $R_G = 892$ kΩ, $R_D = 22$ kΩ, $R_S = 2$ kΩ, $R_4 = 10$ kΩ, and $R_3 = 100$ kΩ

Unknowns: Values of capacitors C_1, C_2, and C_3 for the common-emitter and common-source amplifier stages.

Approach: Substitute known values in Eqs. (14.107) through (14.109). Choose nearest values from the appropriate table in Appendix A.

Assumptions: Small-signal operating conditions are valid, $V_T = 25$ mV.

Analysis: For the common-emitter amplifier,

$$R_{\text{in}} = R_B \| R_{iB} = 104 \text{ k}\Omega \| 310 \text{ k}\Omega = 77.9 \text{ k}\Omega$$

$$R_{\text{out}} = R_C \| R_{iC} = 22 \text{ k}\Omega \| 4.55 \text{ M}\Omega = 21.9 \text{ k}\Omega$$

$$C_1 \gg \frac{1}{\omega(R_I + R_{\text{in}})} = \frac{1}{2000\pi(2 \text{ k}\Omega + 77.9 \text{ k}\Omega)} = 1.99 \text{ nF} \rightarrow C_1 = 0.02\ \mu\text{F (20 nF)}$$[9]

$$C_2 \gg \frac{1}{\omega(R_{\text{out}} + R_3)} = \frac{1}{2000\pi(21.9 \text{ k}\Omega + 100 \text{ k}\Omega)} = 1.31 \text{ nF} \rightarrow C_2 = 0.015\ \mu\text{F} \quad (15 \text{ nF})$$

$$C_3 \gg \frac{1}{\omega\left[R_4 \middle\| \left(R_E + \dfrac{1}{g_m}\right)\right]} = \frac{1}{2000\pi\left[10 \text{ k}\Omega \middle\| \left(3 \text{ k}\Omega + \dfrac{1}{9.80 \text{ mS}}\right)\right]}$$

$$= 67.2 \text{ nF} \rightarrow C_3 = 0.68\ \mu\text{F}$$

For the common-source stage, $R_{\text{in}} = R_G$ since the input resistance at the gate of the transistor is infinite, and $R_{\text{out}} = R_D \| R_{iD}$

$$C_1 \gg \frac{1}{\omega(R_I + R_{\text{in}})} = \frac{1}{2000\pi(2 \text{ k}\Omega + 892 \text{ k}\Omega)} = 178 \text{ pF} \rightarrow C_1 = 1800 \text{ pF}$$

$$C_2 \gg \frac{1}{\omega(R_{\text{out}} + R_3)} = \frac{1}{2000\pi(21.9 \text{ k}\Omega + 100 \text{ k}\Omega)} = 1.31 \text{ nF} \rightarrow C_2 = 0.015\ \mu\text{F} \quad (15 \text{ nF})$$

[9] We are using $C_1 = 10(1.99 \text{ nF})$ to satisfy the inequality.

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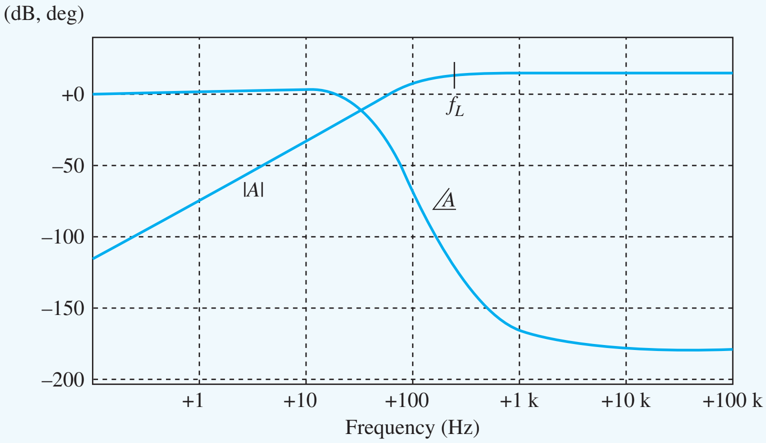
$$C_3 \gg \frac{1}{\omega\left[R_4 \middle\| \left(R_S + \dfrac{1}{g_m}\right)\right]} = \frac{1}{2000\pi\left[10\text{ k}\Omega \middle\| \left(2\text{ k}\Omega + \dfrac{1}{0.491\text{ mS}}\right)\right]}$$

$$= 55.3\text{ nF} \rightarrow C_3 = 0.56\ \mu\text{F}$$

Check of Results: A double check of the calculations indicates they are correct. This would be a good place to check the analysis with simulation.

Discussion: We have chosen each capacitor to have negligible reactance at the frequency of 1 kHz and would expect the lower cutoff frequency of the amplifier to be well below this frequency. The choice of frequency in this example was arbitrary and depends upon the lowest frequency of interest in the application.

WWW **Computer-Aided Analysis:** The graph below gives SPICE simulation results for the common-emitter amplifier with the capacitors as designed here. The midband gain is 15.0 dB and the lower cutoff frequency is 195 Hz. Note the two-pole roll-off at low frequencies indicated by the 40-dB/decade slope in the magnitude characteristic. The slope indicates that there are two zeros at dc, which are associated with capacitors C_1 and C_2. A signal cannot pass through either capacitor at dc, hence the frequency response exhibits a double zero at the origin. We have ended up with an amplifier that has three low frequency poles at approximately 100 Hz (1 kHz/10), and bandwidth shrinkage (Secs. 12.1.3 and 14.7.4) causes the resulting lower cutoff frequency f_L to increase to 195 Hz.



Frequency response for the common-emitter amplifier.

EXERCISE: Reevaluate the capacitor values for the two amplifiers in Ex. 14.7 if the frequency is 250 Hz and the values of R_I and R_3 are changed to 1 kΩ and 82 kΩ, respectively.

ANSWERS: 8.05 nF → 0.082 μF, 0.269 μF → 2.7 μF, 6.13 nF → 0.068 μF; 713 pF → 8200 pF, 6.40 nF → 0.068 μF, 0.221 μF → 2.2 μF

EXERCISE: Use SPICE to simulate the frequency response of the common-source amplifier and find the midband gain and lower cutoff frequency.

ANSWERS: 12.8 dB; 185 Hz

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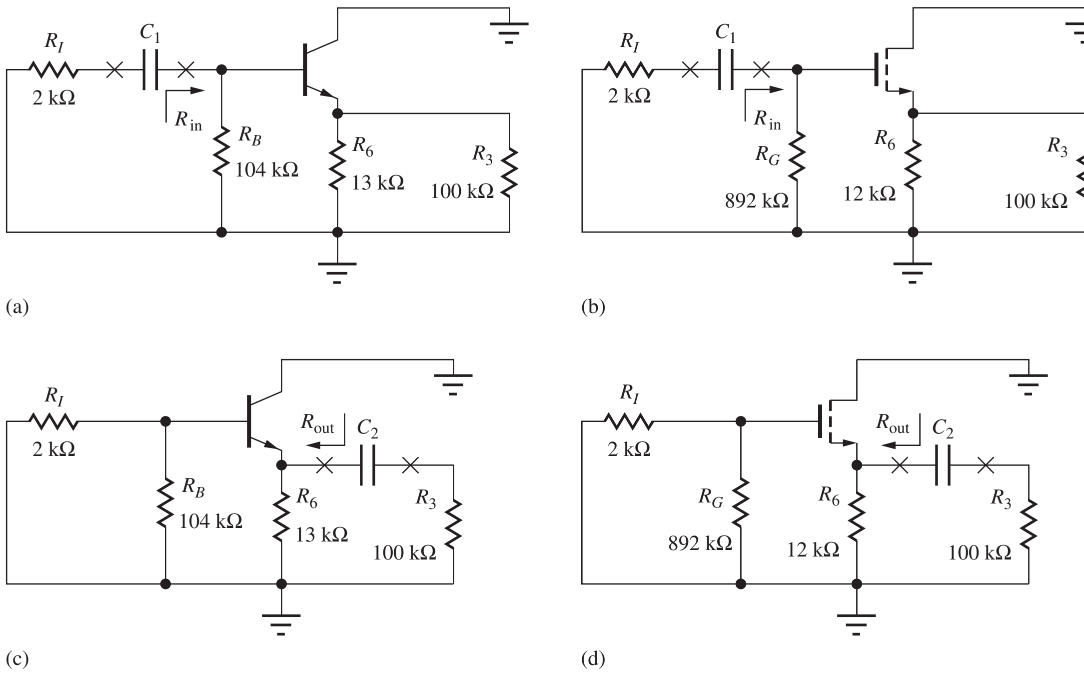

Figure 14.36 Coupling capacitors in the common-collector and common-drain amplifiers.

14.7.2 COMMON-COLLECTOR AND COMMON-DRAIN AMPLIFIERS

The simplified C-C and C-D amplifiers in Fig. 14.4 have only two coupling capacitors. In order to be able to neglect C_1, the reactance of the capacitor must be much smaller than the equivalent resistance that appears at its terminals. Referring to Fig. 14.36, we see that the resistance looking to the left from C_1 is R_I, and that looking to the right is R_{in}. Thus, design of C_1 is the same as Eq. (14.107):

$$\frac{1}{\omega C_1} \ll (R_I + R_{in}) \qquad \text{or} \qquad C_1 \gg \frac{1}{\omega(R_I + R_{in})} \tag{14.110}$$

Be sure to note that the values of the input and output resistances will be different in Eq. (14.110) from those in Eq. (14.107)! For the common-collector stage, bias resistor R_B shunts the input resistance of the transistor, so $R_{in} = R_B \| R_{iB}$. For the common-drain stage, gate bias resistor R_G appears in parallel with the input resistance of the transistor, and $R_{in} = R_G \| R_{iG}$.

For C_2, the resistance looking to the left from capacitor C_2 is R_{out}, and that looking to the right is R_3. Thus, design of C_2 requires

$$\frac{1}{\omega C_2} \ll (R_{out} + R_3) \qquad \text{or} \qquad C_2 \gg \frac{1}{\omega(R_{out} + R_3)} \tag{14.111}$$

where $R_{out} = R_6 \| R_{iE}$ or $R_6 \| R_{iS}$, because resistor R_6 appears in parallel with the output resistance of the transistor. Note again that the value of R_{out} in Eq. (14.111) differs from that in Eq. (14.108).

DESIGN EXAMPLE 14.8 CAPACITOR DESIGN FOR THE C-C AND C-D AMPLIFIERS

This example selects capacitor values for the followers in Figs. 14.4 and 14.36.

PROBLEM Choose values for the coupling and bypass capacitors for the amplifiers in Figs. 14.4 and 14.36 so that the presence of the capacitors can be neglected at a frequency of 2 kHz.

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SOLUTION **Known Information and Given Data:** Frequency $f = 2000$ Hz; for the C-C stage from Fig. 14.4 and Table 14.5, $R_{iB} = 1.17$ MΩ, $R_{iC} = 0.121$ kΩ, $R_6 = 13$ kΩ, $R_I = 2$ kΩ, $R_B = 104$ kΩ, and $R_3 = 100$ kΩ; for the C-S stage, $R_{iG} = \infty$, $R_{iS} = 2.04$ kΩ, $R_6 = 12$ kΩ, $R_I = 2$ kΩ, $R_G = 892$ kΩ, and $R_3 = 100$ kΩ

Unknowns: Values of capacitors C_1 and C_3 for the common-collector and common-drain amplifiers.

Approach: Substitute known values in Eqs. (14.110) and (14.111). Choose the nearest values from the capacitor table in Appendix A.

Assumptions: Small-signal operating conditions are valid.

Analysis: For the common-collector amplifier,

$$R_{\text{in}} = R_B \| R_{iB} = 104\text{ k}\Omega \| 1.17\text{ M}\Omega = 95.5\text{ k}\Omega$$

$$C_1 \gg \frac{1}{\omega(R_I + R_{\text{in}})} = \frac{1}{4000\pi(2\text{ k}\Omega + 95.5\text{ k}\Omega)} = 816\text{ pF} \to C_1 = 8200\text{ pF}^{10}$$

$$R_{\text{out}} = R_6 \| R_{iC} = 13\text{ k}\Omega \| 121\ \Omega = 120\ \Omega$$

$$C_2 \gg \frac{1}{\omega(R_{\text{out}} + R_3)} = \frac{1}{4000\pi(120\ \Omega + 100\text{ k}\Omega)} = 795\text{ pF} \to C_2 = 8200\text{ pF}$$

and for the common-drain stage,

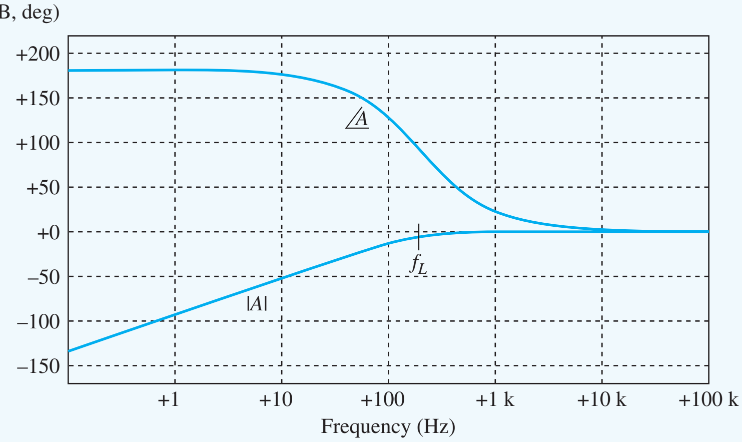
$$R_{\text{in}} = R_G \| R_{iG} = 892\text{ k}\Omega \| \infty = 892\text{ k}\Omega$$

$$C_1 \gg \frac{1}{\omega(R_I + R_{\text{in}})} = \frac{1}{4000\pi(2\text{ k}\Omega + 892\text{ k}\Omega)} = 89.0\text{ pF} \to C_1 = 1000\text{ pF}$$

$$R_{\text{out}} = R_6 \| R_{iS} = 12\text{ k}\Omega \| 2.04\text{ k}\Omega = 1.74\text{ k}\Omega$$

$$C_2 \gg \frac{1}{\omega(R_{\text{out}} + R_3)} = \frac{1}{4000\pi(1.74\text{ k}\Omega + 100\text{ k}\Omega)} = 782\text{ pF} \to C_2 = 8200\text{ pF}$$

Check of Results: A double check of the calculations indicates they are correct. This represents a good place to check the analysis with simulation.



Emitter follower frequency response.

[10] $C_1 = 10(816\text{ pF})$ is used to satisfy the inequality.

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Discussion: We have chosen each capacitor to have negligible reactance at the frequency of 2 kHz and would expect the lower cutoff frequency of the amplifier to be well below this frequency. The choice of frequency in this example was arbitrary and depends upon the lowest frequency of interest in the application.

WWW **Computer-Aided Analysis:** The graph on the previous page shows SPICE simulation results for the common-emitter amplifier with the capacitors as designed above. The midband gain is −0.262 dB (0.970) and the lower cutoff frequency is 310 Hz. Note the two-pole roll off at low frequencies indicated by the 40-dB/decade slope in the magnitude characteristic. As in Design Ex. 14.7, a dc signal cannot pass through capacitor C_1 or C_3, and the amplifier transfer function is characterized by a double zero at the origin.

EXERCISE: Reevaluate the capacitor values for the two amplifiers in Ex. 14.8 if the frequency is 250 Hz and the values of R_I and R_3 are changed to 1 kΩ and 82 kΩ, respectively?

ANSWERS: 6.79 nF → 0.068 μF, 8.16 nF → 0.082 μF; 713 pF → 8200 pF, 7.98 nF → 0.082 μF

EXERCISE: Use SPICE to simulate the frequency response of the common-drain amplifier and find the midband gain and lower cutoff frequency.

ANSWERS: −1.54 dB; 293 Hz

14.7.3 COMMON-BASE AND COMMON-GATE AMPLIFIERS

For the C-B and C-G amplifiers, C_3 is first assumed to be infinite in value, thus shorting the base and gate of the transistors in Fig. 14.5 to ground as redrawn in Fig. 14.37. In order to neglect C_1 the magnitude of the impedance of the capacitor must be much smaller than the equivalent resistance that appears at its terminals. Referring to Fig. 14.37, the resistance looking to the left from the capacitor

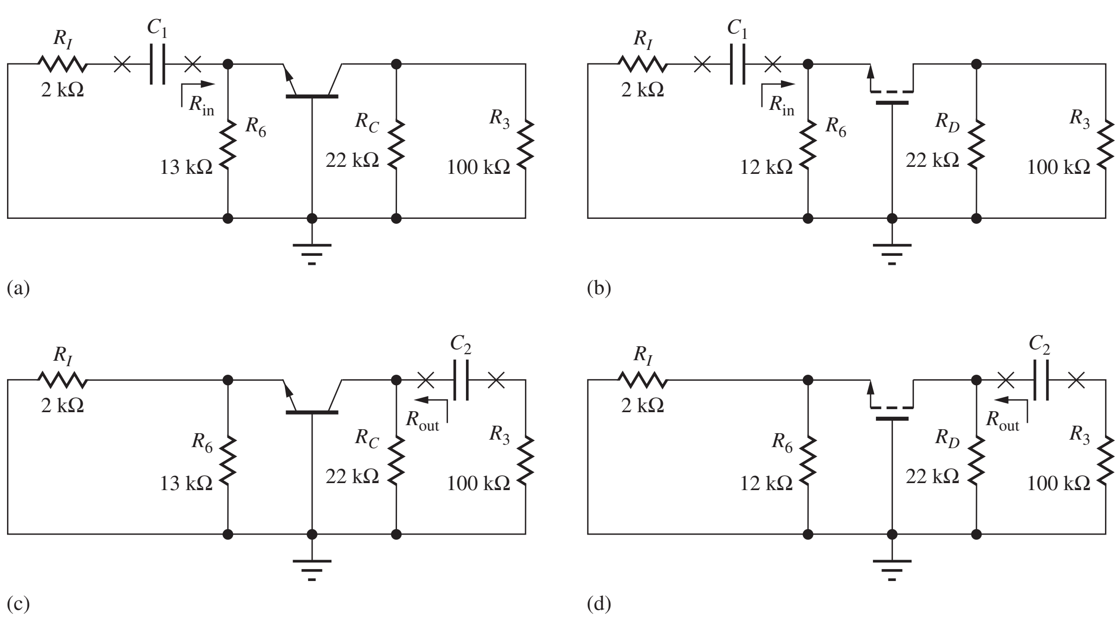

Figure 14.37 Coupling capacitors in the common-base and common-gate amplifiers.

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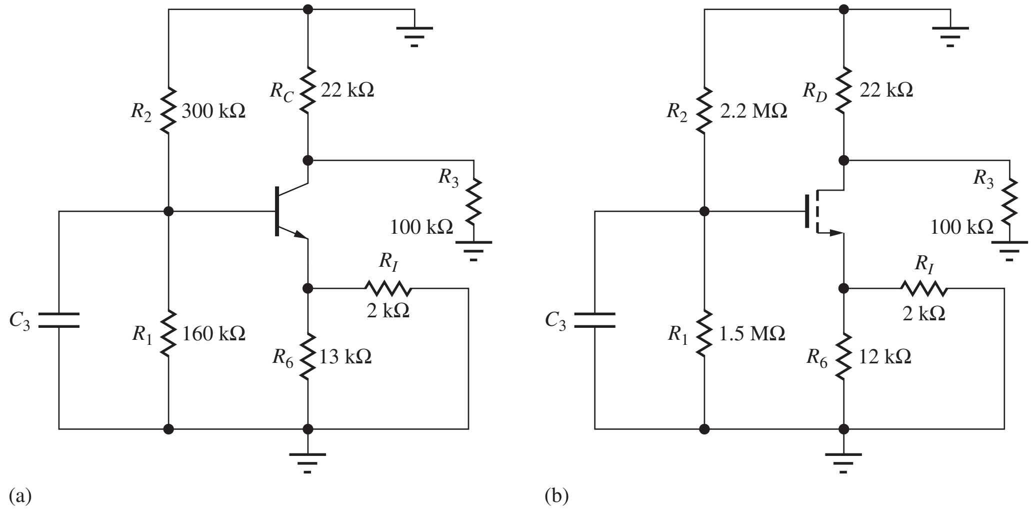

Figure 14.38 Bypass capacitors in the (a) common-collector and (b) common-drain amplifiers.

is R_I, and that looking to the right is R_{in}. Thus, design of C_1 is the same as Eq. (14.107):

$$\frac{1}{\omega C_1} \ll (R_I + R_{in}) \quad \text{or} \quad C_1 \gg \frac{1}{\omega(R_I + R_{in})} \tag{14.112}$$

For the two amplifier stages, resistor R_6 appears in shunt with the input resistance of the transistor, so $R_{in} = R_6 \| R_{iE}$ or $R_{in} = R_6 \| R_{iS}$.

For C_2, we see that the resistance looking to the left from capacitor C_2 is R_{out}, and that looking to the right is R_3. Thus, design of C_2 requires

$$\frac{1}{\omega C_2} \ll (R_{out} + R_3) \quad \text{or} \quad C_2 \gg \frac{1}{\omega(R_{out} + R_3)} \tag{14.113}$$

For the amplifiers, resistor R_C or R_D appears in parallel with the output resistance of the transistor, so $R_{out} = R_C \| R_{iC}$ or $R_{out} = R_D \| R_{iD}$.

To be an effective bypass capacitor, the reactance of C_3 must be much smaller than the equivalent resistance at the base or gate terminal of the transistors in Fig. 14.5 with the other capacitors assumed to be infinite, as depicted in Fig. 14.38. The resistances at the base and gate nodes are

$$R_{eq}^{CB} = R_1 \| R_2 \| [r_\pi + (\beta_o + 1)(R_6 \| R_I)] \quad \text{and} \quad R_{eq}^{CG} = R_1 \| R_2 \tag{14.114}$$

respectively. The corresponding value of C_3 must satisfy

$$C_3 \gg \frac{1}{\omega R_{eq}^{CB,CG}}$$

DESIGN EXAMPLE 14.9 — CAPACITOR DESIGN FOR THE C-B AND C-G AMPLIFIERS

This example selects capacitor values for the noninverting amplifiers in Fig. 14.5.

PROBLEM Choose values for the coupling and bypass capacitors for the amplifiers in Fig. 14.5 so that the presence of the capacitors can be neglected at a frequency of 1 kHz.

SOLUTION **Known Information and Given Data:** Frequency $f = 1000$ Hz; for the C-B stage from Fig. 14.5 and Table 14.6, $R_{iE} = 102\ \Omega$, $R_{iC} = 3.40\ \text{M}\Omega$, $R_I = 2\ \text{k}\Omega$, $R_1 = 160\ \text{k}\Omega$, $R_2 = 300\ \text{k}\Omega$, $R_C = 22\ \text{k}\Omega$, and $R_6 = 13\ \text{k}\Omega$; for the C-G amplifier, $R_{iS} = 2.04\ \text{k}\Omega$, $R_{iD} = 411\ \text{k}\Omega$, $R_I = 2\ \text{k}\Omega$, Ω, $R_1 = 1.5\ \text{M}\Omega$, $R_2 = 2.2\ \text{M}\Omega$, $R_6 = 12\ \text{k}\Omega$, and $R_D = 22\ \text{k}\Omega$

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Unknowns: Values of capacitors C_1, C_2, and C_3

Approach: Substitute known values in Eqs. (14.112) through (14.114). Choose the nearest values from the capacitor table in Appendix A.

Assumptions: Small-signal operating conditions are valid. Use a factor of 10 to satisfy the inequalities.

Analysis: For the common-base amplifier,

$$R_{\text{in}} = R_6 \| R_{iE} = 13\ \text{k}\Omega \| 102\ \Omega = 100\ \Omega$$

$$C_1 \gg \frac{1}{\omega(R_I + R_{\text{in}})} = \frac{1}{2000\pi(2\ \text{k}\Omega + 100\ \Omega)} = 75.8\ \text{nF} \rightarrow C_1 = 0.82\ \mu\text{F}^{11}$$

$$R_{\text{out}} = R_C \| R_{iC} = 22\ \text{k}\Omega \| 3.40\ \text{M}\Omega = 21.9\ \text{k}\Omega$$

$$C_2 \gg \frac{1}{\omega(R_{\text{out}} + R_3)} = \frac{1}{2000\pi(21.9\ \text{k}\Omega + 100\ \text{k}\Omega)} = 1.31\ \text{nF} \rightarrow C_2 = 0.015\ \mu\text{F} \quad (15\ \text{nF})$$

$$C_3 \gg \frac{1}{\omega(R_1 \| R_2 \| [r_\pi + (\beta_o + 1)(R_6 \| R_I)])}$$

$$= \frac{1}{2000\pi(160\ \text{k}\Omega \| 300\ \text{k}\Omega \| [10.2\ \text{k}\Omega + (101)(13\ \text{k}\Omega \| 2\ \text{k}\Omega)])}$$

$$= 2.38\ \text{nF} \rightarrow C_3 = 0.027\ \mu\text{F}$$

and for the common-gate stage,

$$R_{\text{in}} = R_6 \| R_{iS} = 12\ \text{k}\Omega \| 2.04\ \Omega = 1.74\ \text{k}\Omega$$

$$C_1 \gg \frac{1}{\omega(R_I + R_{\text{in}})} = \frac{1}{2000\pi(2\ \text{k}\Omega + 1.74\ \text{k}\Omega)} = 42.6\ \text{nF} \rightarrow C_1 = 0.42\ \mu\text{F}$$

$$R_{\text{out}} = R_6 \| R_{iD} = 22\ \text{k}\Omega \| 411\ \text{k}\Omega = 20.9\ \text{k}\Omega$$

$$C_2 \gg \frac{1}{\omega(R_{\text{out}} + R_3)} = \frac{1}{2000\pi(20.9\ \text{k}\Omega + 100\ \text{k}\Omega)} = 1.31\ \text{nF} \rightarrow C_2 = 0.015\ \mu\text{F} \quad (15\ \text{nF})$$

$$C_3 \gg \frac{1}{\omega(R_1 \| R_2)} = \frac{1}{2000\pi(1.5\ \text{M}\Omega \| 2.2\ \text{M}\Omega)} = 178\ \text{pF} \rightarrow C_3 = 1800\ \text{pF}$$

Check of Results: A double check of the calculations indicates they are correct. This is a good place to check the analysis with simulation.

Discussion: We have chosen each capacitor to have negligible reactance at the frequency of 1 kHz and expect the lower cutoff frequency of the amplifier to be well below this frequency. The choice of frequency in this example was arbitrary and depends upon the lowest frequency of interest in the application.

WWW **Computer-Aided Analysis:** The graph below shows SPICE simulation results for the common-base amplifier with the capacitors as just designed. The midband gain is 18.5 dB (8.41) and the lower cutoff frequency is 174 Hz. Note the two-pole roll-off at low frequencies indicated by the 40-dB/decade slope in the magnitude characteristic. Here again, since a dc signal cannot pass through capacitor C_1 or C_2, the amplifier transfer function exhibits a double zero at the origin.

[11] $C_1 = 10(75.8\ \text{nF})$ is used to satisfy the inequality.

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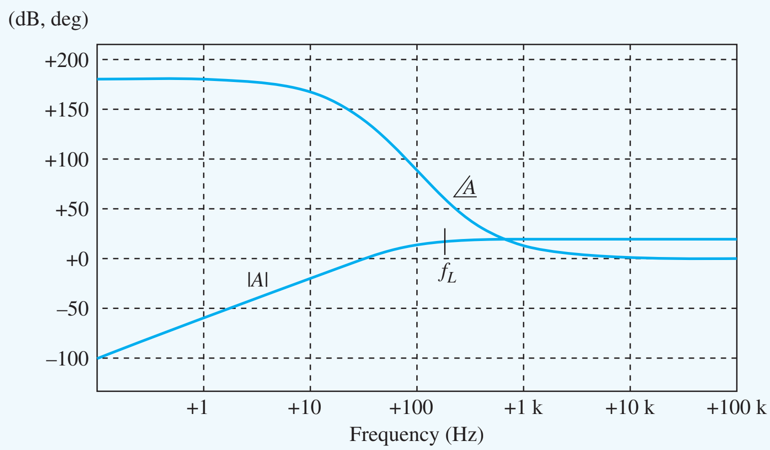

Common-base amplifier frequency response.

EXERCISE: Recalculate the capacitor values for the two amplifiers in Design Ex. 14.9 if the frequency is 250 Hz and the values of R_I and R_3 are changed to 1 kΩ and 82 kΩ, respectively.

ANSWERS: 0.579 μF → 6.8 μF, 6.13 nF → 0.068 μF, 12.2 nF → 0.12 μF; 0.232 μF → 2.2 μF, 6.19 nF → 0.068 μF, 714 pF → 8200 pF

EXERCISE: Use SPICE to simulate the frequency response of the common-gate amplifier and find the midband gain and lower cutoff frequency.

ANSWERS: 12.2 dB, 156 Hz

14.7.4 SETTING LOWER CUTOFF FREQUENCY f_L

In the previous sections, we have designed the coupling and bypass capacitors to have a negligible effect on the circuit at some particular frequency in the midband range of the amplifier. An alternative is to choose the capacitor values to set the lower cutoff frequency of the amplifier where we want it to be. Referring back to the high-pass filter analysis in Sec. 10.10.3, we see that the pole associated with the capacitor occurs at the frequency for which the capacitive reactance is equal to the resistance that appears at the capacitor terminals.

Multiple Poles and Bandwidth Shrinkage

In the circuits we have considered, there are several poles, and bandwidth shrinkage occurs at low frequencies in a manner similar to that which was presented in Table 12.2 for high frequencies. A transfer function which exhibits n identical poles at a low frequency ω_o can be written as

$$T(s) = A_{\text{mid}}\frac{s^n}{(s+\omega_o)^n} \tag{14.115}$$

$$|T(j\omega)| = A_{\text{mid}}\frac{\omega^n}{\left(\sqrt{\omega^2+\omega_o^2}\right)^n} \tag{14.116}$$

$$|T(j\omega_L)| = \frac{A_{\text{mid}}}{\sqrt{2}} \rightarrow \omega_L = \frac{\omega_o}{\sqrt{2^{1/n}-1}} \qquad \text{or} \qquad f_L = \frac{f_o}{\sqrt{2^{1/n}-1}} \tag{14.117}$$

The factor in the denominator of Eq. (14.117) is less than 1, so that the lower cutoff frequency is higher than the frequency corresponding to the individual poles. Table 14.13 gives the relationship between ω_o and ω_L for various values of n.

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