TABLE 14.12
Simplified Characteristics of Single FET Amplifiers

	COMMON-SOURCE ($R_S = 0$)	COMMON-SOURCE WITH SOURCE RESISTOR R_S	COMMON-DRAIN	COMMON-GATE
Terminal voltage gain $A_{vt} = \frac{v_o}{v_1}$	$-g_m R_L \cong -V_{DD}$ (moderate)	$-\frac{R_L}{R_S}$ (moderate)	1 (low)	$+g_m R_L \cong +V_{DD}$ (moderate)
Input terminal resistance	∞ (high)	∞ (high)	∞ (high)	$1/g_m$ (low)
Output terminal resistance	r_o (moderate)	$\mu_f R_S$ (high)	$1/g_m$ (low)	$\mu_f (R_I \| R_6)$ (high)
Current gain	∞ (high)	∞ (high)	∞ (high)	1 (low)

In a manner similar to the BJT amplifiers, the magnitude of the terminal gain of all three FET stages can be expressed as the ratio of total resistance R_L at the drain terminal to the total resistance R_{SQ} in the source loop. R_{SQ} represents the sum of the external resistance R_X [i.e., R_S, R_L, or $(R_I \| R_6)$, as appropriate] plus the resistance $(1/g_m)$ found looking back into the source of the transistor itself. Thus, when properly interpreted, the gain expressions for the single stage BJT and FET amplifier stages can all be considered as identical!

Table 14.12 is a relative comparison of the FET amplifiers. The common-source amplifier provides moderate voltage gain and output resistance but high values of input resistance and current gain. The common-drain amplifier provides low voltage gain and output resistance, and high input resistance and current gain. Finally, the common-gate amplifier provides moderate voltage gain, high output resistance, and low input resistance and current gain. Tables 14.9 to 14.12 are very useful in the initial phase of amplifier design, when the engineer must make a basic choice of amplifier configuration to meet the design specifications.

DESIGN NOTE

The magnitude of the overall gain of the single-stage amplifiers can all be expressed approximately by

$$|A_v| \cong \frac{g_m R_L}{1 + g_m R} = \frac{R_L}{\frac{1}{g_m} + R}$$

in which R is the external resistance in the emitter or source loop of the transistor.

Now we have a toolbox full of amplifier configurations that we can use to solve circuit design problems. Design Ex. 14.6 on page 896 demonstrates how to use our understanding to make design choices between the various configurations.

14.6 COMMON-SOURCE AMPLIFIERS USING MOS INVERTERS

As originally discussed in Chapter 6, resistor loads are problematic in integrated circuits because they tend to take up a large amount of area relative to the size MOS transistors. However, we can use a transistor in place of the load resistor in a common-source amplifier as depicted in Fig. 14.29

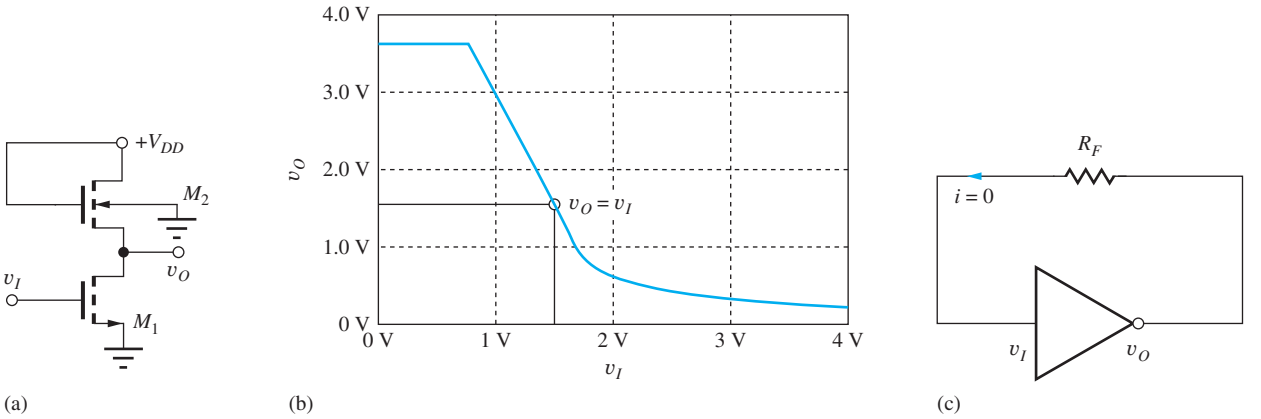

Figure 14.29 (a) Common-source amplifier with the load resistor replaced with a saturated transistor; (b) voltage transfer characteristic; (c) simple bias circuit for high gain operation.

where R_L is replaced as a transistor operating in the saturation region.[6] This is the same circuit that we encountered in Chapter 6 where it was called the "Saturated Load Inverter."

Remember from Chapter 10 that the gain is equal to the slope of the amplifier's voltage transfer characteristic evaluated at the Q-point, $A_v = dv_O/dv_I\big|_{Q-pt}$, and the VTC in Fig. 14.29(b) has a region of high gain. In particular, if the circuit can be biased at a Q-point having $v_O = v_I$, then the inverter operates as a high-gain amplifier.

It is actually easy to bias the MOS inverter into the high-gain region using negative feedback as in Fig. 14.29(c).[7] Since there is no dc current into the amplifier input, v_I and v_O must be equal, and the circuit operates in its high-gain region.

14.6.1 VOLTAGE GAIN ESTIMATE

Let us estimate the gain of the circuit in Fig. 14.29(a) based upon the characteristics of the single-transistor amplifiers studied thus far. M_1 is connected as a common-source transistor, so the gain will be $A_v = -g_{m1}R_L$ where R_L is the overall load resistance connected to the drain of M_1. The load resistance consists of the parallel combination of the output resistance r_{o1} of M_1 and the resistance R_{iS2} looking into the source of M_2, which we now know is given by $R_{iS2} = 1/g_{m2}$:

$$R_L = r_{o1} \parallel R_{iS2} = r_{o1} \parallel \frac{1}{g_{m2}} \cong \frac{1}{g_{m2}} \tag{14.95}$$

Since the transistors must operate at the same drain current, we expect $r_{o1} \gg 1/g_{m2}$, and the voltage gain becomes

$$A_v^{CS} \cong -\frac{g_{m1}}{g_{m2}} = -\frac{\sqrt{2K_{n1}I_D}}{\sqrt{2K_{n2}I_D}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \tag{14.96}$$

The gain of the amplifier with a saturated-load device is equal to the square root of the ratio of the (W/L) ratios of the input and load transistors. The gain is controlled by the designer's choice of the size of the transistors and is independent of the other transistor parameters. Unfortunately, even moderate gain requires large differences in the W/L ratios. For example, a 20 dB gain requires $(W/L)_1 = 100(W/L)_2$.

[6] Saturated by connection (see Sec. 6.6).

[7] In Chapter 15, we will see how to eliminate R_F.

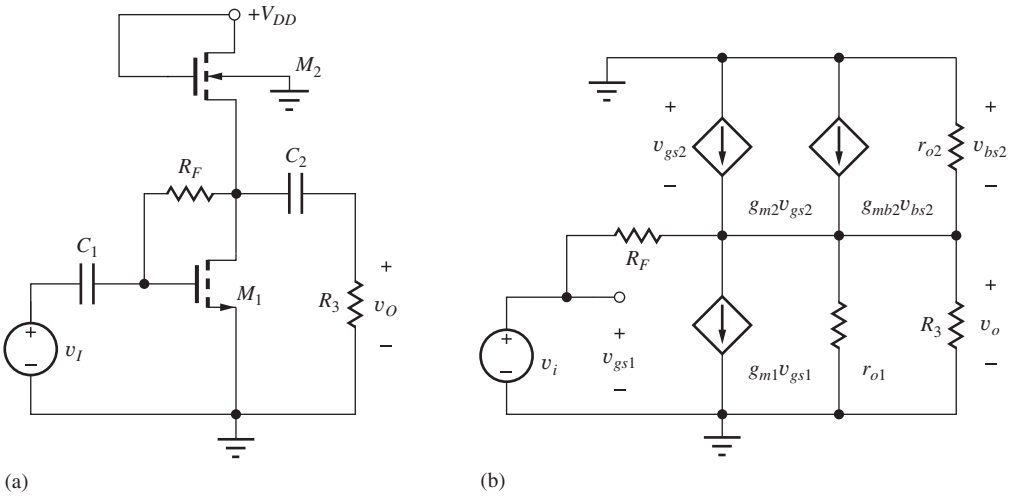

Figure 14.30 (a) Complete common-source amplifier; (b) small-signal model.

14.6.2 DETAILED ANALYSIS

Now let us explore the C-S amplifier in more detail in order to account for effects that have been neglected in our simplified analysis. The circuit in Fig. 14.30 includes bias resistor R_F, coupling capacitors C_1 and C_2, and external load resistor R_3, and the small-signal model includes the back-gate transconductance of transistor M_2 (see Sec. 13.8.4). An expression for the gain of the amplifier in Fig. 14.30 is found by writing a nodal equation at the output node:

$$G_F(\mathbf{v_o} - \mathbf{v_i}) + g_{m1}\mathbf{v_i} + \mathbf{v_o}(g_{o1} + g_{o2} + G_F + G_3) - g_{m2}\mathbf{v_{gs2}} - g_{mb2}\mathbf{v_{bs2}} = 0 \qquad (14.97)$$

Collecting terms, realizing that both v_{gs2} and v_{bs2} are equal to $-v_o$, and solving for the voltage gain yields

$$A_v^{CS} = \frac{\mathbf{v_o}}{\mathbf{v_i}} = -\frac{(g_{m1} - G_F)}{g_{m2}(1+\eta) + g_{o1} + g_{o2} + G_F + G_3} \qquad (14.98)$$

where $g_{mb2} = \eta g_{m2}$. This expression can be written in a more recognizable form as

$$A_v^{CS} \cong -g_{m1}R_L \qquad \text{where} \qquad R_L = R_3 \parallel R_F \parallel r_{o1} \parallel r_{o2} \parallel \frac{1}{g_{m2}(1+\eta)} \qquad (14.99)$$

is the total equivalent resistance on the output node. We already know that r_{o1} and r_{o2} will be much larger than $1/g_{m2}$, and R_F is normally designed to be much larger than R_3. In most cases, R_3 will also be much greater than $1/g_{m2}$, so the gain reduces to

$$A_v^{CS} \cong -\frac{g_{m1}}{g_{m2}(1+\eta)} = -\frac{1}{1+\eta}\sqrt{\frac{(W/L)_1}{(W/L)_2}} \qquad (14.100)$$

Equation (14.100) is the same as Eq. (14.96) except for the gain degradation caused by the back-gate transconductance. The effective load resistance is still limited by the relatively large conductance of the load transistor.

EXERCISE: What is the W/L ratio of M_1 required to achieve a gain of 26 dB if $\eta = 0.2$ and $(W/L)_2 = 4/1$?

ANSWER: 2290/1

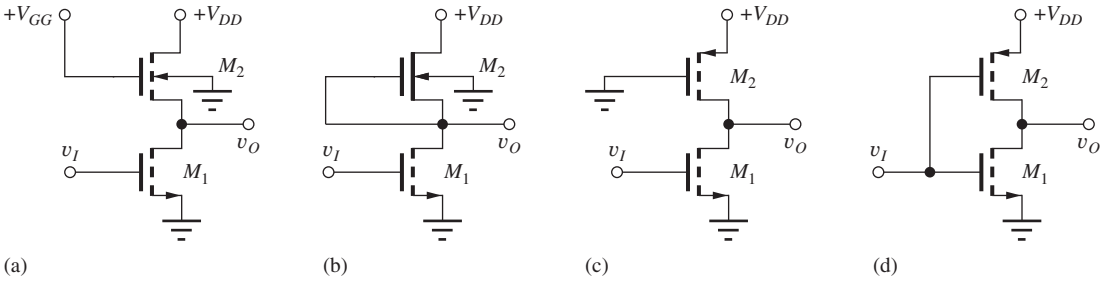

Figure 14.31 MOS inverting amplifiers: (a) linear load; (b) depletion-mode load; (c) pseudo NMOS; (d) CMOS.

14.6.3 ALTERNATIVE LOADS

To improve the gain of the circuit, g_{m2} needs to be eliminated from the expression for the load resistance, Eq. (14.99). We know from our study of logic gates that there are a number of alternative transistor configurations for the load device as depicted in Fig. 14.31. NMOS transistors can be used as linear loads and depletion-mode loads, whereas PMOS transistors can be employed in psuedo NMOS and CMOS inverters. Any one of these circuits can be substituted for the saturated load inverter in Fig. 14.30.

However, the linear load configuration achieves nothing, since the gate of M_2 is still at ac ground and R_{iS2} is still determined by $1/g_{m2}$. On the other hand, the depletion-mode load yields an improvement. Voltage v_{GS} is forced to be zero by connection, so the forward transconductance is eliminated and the gain is approximately

$$A_v^{CS} \cong -\frac{g_{m1}}{\eta g_{m2}} \tag{14.101}$$

which improves the gain by a factor of $(1+\eta)/\eta$. For $\eta = 0.2$, the gain is improved by a factor of 6. In discrete circuits, v_{BS} can also be set to zero, and the back-gate transconductance is also eliminated. For this case the gain becomes

$$A_v^{CS} \cong -g_{m1}R_L = -g_{m1}\left(R_3 \parallel R_F \parallel r_{o1} \parallel r_{o2}\right) \cong -g_{m1}R_3 \tag{14.102}$$

since we expect r_{o1} and r_{o2} to be much larger than R_3, and R_F can also be designed to be much larger than R_3. This configuration has more gain than our original C-S circuit because external load resistor R_3 is normally much larger than drain resistor R_D.

Circuits in Fig. 14.31(c) and (d) employ PMOS transistors and require CMOS technology. For the pseudo NMOS inverter, the load resistance on transistor M_1 is the same as that given in Eq. (14.102), and the gain is also the same. In the CMOS inverter case as depicted in Fig. 14.32, the transistors are connected in parallel: the gates are connected together, the drains are connected together, and the sources are both at ac ground potential. The input is applied to both gates so the gain expression becomes

$$A_v^{CS} \cong -(g_{m1}+g_{m2})R_L = -g_{m1}\left(R_3 \parallel R_F \parallel r_{o1} \parallel r_{o2}\right) \cong -(g_{m1}+g_{m2})R_3 \tag{14.103}$$

which can be a factor of two improvement for a symmetrical inverter design ($K_p = K_n$).

Note that if we use a symmetrical CMOS inverter, eliminate R_3, and make R_F very large, the gain becomes approximately

$$A_v^{CS} \cong -(g_{m1}+g_{m2})\left(r_{o1} \parallel r_{o2}\right) = -2g_{m1}\frac{r_{o1}}{2} \cong -\mu_f \tag{14.104}$$

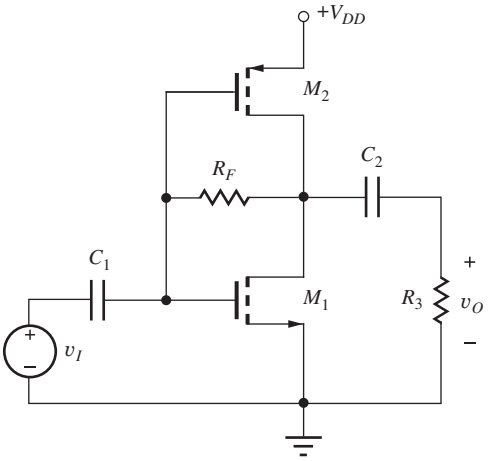

Figure 14.32 Common-source amplifier employing CMOS inverter.

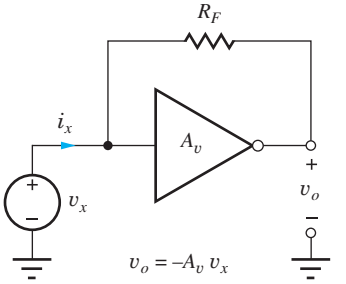

Figure 14.33 Circuit for determining input resistance.

We have discovered a circuit that achieves a gain equal to the amplification factor of the transistor, and we can't do better than that! Similar techniques will be used to design high-performance amplifiers in the next several chapters.

14.6.4 INPUT AND OUTPUT RESISTANCES

The input resistance of the amplifiers can be found with the assistance of the circuit in Fig. 14.33. R_{in} is calculated by finding an expression for i_x in terms of v_x:

$$\mathbf{i_x} = \frac{\mathbf{v_x} - \mathbf{v_o}}{R_F} = \frac{\mathbf{v_x} - (-A_v \mathbf{v_x})}{R_F} = \mathbf{v_x}\left(\frac{1 + A_v}{R_F}\right) \quad \text{and} \quad R_{\text{in}} = \frac{\mathbf{v_x}}{\mathbf{i_x}} = \frac{R_F}{1 + A_v} \tag{14.105}$$

For high gain, the input resistance is approximately equal to the feedback resistance divided by the amplifier's gain.

If input source v_i is set to zero for the circuit in Fig. 14.30(b), we immediately see that the output resistance there is given by

$$R_{\text{out}} = R_F \parallel r_{o1} \parallel r_{o2} \parallel \frac{1}{g_{m2}(1 + \eta)} \quad \text{or} \quad R_{\text{out}} = R_F \parallel r_{o1} \parallel r_{o2} \tag{14.106}$$

depending upon the inverter configuration.

EXERCISE: Find the Q-point for the amplifier in Fig. 14.30 if $R_F = 1$ MΩ, $K_n' = 100$ μA/V², $V_{TN} = 1$ V, $\lambda = 0.02$, $\eta = 0$, $(W/L)_1 = 8/1$, $(W/L)_2 = 2/1$ and $V_{DD} = 5$ V.

ANSWER: $V_o = 2.01$ V, $I_o = 421$ μA

EXERCISE: Find the Q-point for the amplifier in Fig. P14.32 if $R_F = 560$ kΩ, $K_n' = 100$ μA/V², $K_p' = 40$ μA/V², $V_{TN} = 0.7$ V, $V_{TP} = -0.7$ V, $\lambda = 0.02$, $(W/L)_1 = 20/1$, $(W/L)_2 = 50/1$ and $V_{DD} = 3.3$ V.

ANSWER: $V_o = 1.65$ V, $I_o = 932$ μA

DESIGN EXAMPLE 14.6 SELECTING AN AMPLIFIER CONFIGURATION

One of the first things we must do to solve a circuit design problem is to decide on the circuit topology to be used. A number of examples are given here.

PROBLEMS What is the preferred choice of amplifier configuration for each of these applications?

(a) A single-transistor amplifier is needed that has a gain of approximately 80 dB and an input resistance of 100 kΩ.
(b) A single-transistor amplifier is needed that has a gain of 52 dB and an input resistance of 250 kΩ.
(c) A single-transistor amplifier is needed that has a gain of 30 dB and an input resistance of at least 5 MΩ.
(d) A single-transistor amplifier is needed that has a gain of approximately 0 dB and an input resistance of 20 MΩ with a load resistor of 10 kΩ.
(e) A follower is needed that has a gain of at least 0.98 and an input resistance of at least 250 kΩ with a load resistance of 5 kΩ.
(f) A single-transistor amplifier is needed that has a gain of +10 and an input resistance of 2 kΩ.
(g) An amplifier is needed with an output resistance of 25 Ω.

SOLUTION **Known Information and Given Data:** In each case, we see that a minimum amount of information is provided, typically only a voltage gain and resistance specification.

Unknowns: Circuit topologies

Approach: Use our estimates of voltage gain, input resistance, and output resistance for the various configurations to make a selection.

Assumptions: Typical values of current gain, Early voltage, power supply voltage, and so on will be assumed as necessary: $\beta_o = 100$, $0.25\text{ V} \leq V_{GS} - V_{TN} \leq 1\text{ V}$, $V_T = 0.025\text{ V}$, $V_A \leq 80\text{ V}$, $1/\lambda \leq 80\text{ V}$.

Analyses:

(a) The required voltage gain is $A_v = 10^{80/20} = 10{,}000$. This value of voltage gain exceeds the intrinsic voltage gain of even the best BJTs:

$$A_v \leq \mu_f = 40V_A = 40(80) = 3200$$

An FET typically has a much lower value of intrinsic gain and is at an even worse disadvantage. Thus, such a large gain requirement cannot be met with a single-transistor amplifier.

(b) For the second set of specifications, we have $R_{\text{in}} = 250\text{ k}\Omega$ and $A_v = 10^{52/20} \cong 400$. We require both large gain and relatively large input resistance, which point us toward the common-emitter amplifier. For the C-E stage, $A_v = 10\ V_{CC} \rightarrow V_{CC} = 40\text{ V}$, which is somewhat large. However, we know that the $10\ V_{CC}$ estimate for the voltage gain is conservative and can easily be off by a factor of 2 or 3, so we can probably get by with a smaller power supply, say 20 V. Achieving the input of resistance requirement requires r_π to exceed 250 kΩ:

$$r_\pi = \frac{\beta_o V_T}{I_C} \geq 250\text{ k}\Omega \rightarrow I_C \leq \frac{100(0.025\text{ V})}{2.5 \times 10^5\ \Omega} = 10\ \mu\text{A}$$

which is small but acceptable. Achieving the gain specification with an FET would be much more difficult. For example, even with a small gate overdrive,

$$A_v = \frac{V_{DD}}{V_{GS} - V_{TN}} \cong \frac{V_{DD}}{0.25\ \text{V}} \rightarrow V_{DD} = 100\ \text{V}$$

which is unreasonably large for most solid-state designs. Note that the sign of the gain was not specified, so either positive or negative gain would be satisfactory, based on our limited specifications. However, the input resistance of the noninverting (C-B or C-G) amplifiers is low, not high.

(c) In this case, we require $R_{\text{in}} \geq 5\,\text{M}\Omega$ and $A_v = 10^{30/20} \cong 31.6$—large input resistance and moderate gain. These requirements can easily be met by a common-source amplifier:

$$A_v = \frac{V_{DD}}{V_{GS} - V_{TN}} = \frac{15\ \text{V}}{0.5\ \text{V}} = 30$$

The input resistance is set by our choice of gate bias resistors (R_1 and R_2 in Fig. 14.2), and 5 MΩ can be achieved with standard resistor values.

Since the gain is moderate, a C-E stage with emitter resistor could probably achieve the required high input resistance, although the values of the base bias resistor could become a limiting factor. For example, the input resistance and voltage gain could be met approximately with

$$R_{\text{in}} \cong \beta_o R_E \geq 5\,\text{M}\Omega \rightarrow R_E \geq \frac{5\,\text{M}\Omega}{100} = 50\,\text{k}\Omega \quad \text{and} \quad |A_v| = \frac{R_L}{R_E} \rightarrow R_L = 1.5\,\text{M}\Omega$$

(d) Zero-dB gain corresponds to a follower. For an emitter follower, $R_{\text{in}} \cong \beta_o R_L \cong 100(10\ \text{k}\Omega) = 1\ \text{M}\Omega$, so the BJT will not meet the input resistance requirement. On the other hand, a source follower provides a gain of approximately one and can easily achieve the required input resistance.

(e) A gain of 0.98 and an input resistance of 250 kΩ should be achievable with either a source follower or an emitter follower. For the MOSFET,

$$A_v = \frac{g_m R_L}{1 + g_m R_L} = 0.98 \qquad \text{requires} \qquad g_m R_L = \frac{2 I_D R_L}{V_{GS} - V_{TN}} = 49$$

which can be satisfied with $I_D R_L = 12.3$ V for $V_{GS} - V_{TN} = 0.5$ V.

The BJT can achieve the required gain with a much lower supply voltage and still meet the input resistance requirement: $R_{\text{in}} \cong \beta_o R_L \cong 100(5\ \text{k}\Omega) = 500\ \text{k}\Omega$.

$$g_m R_L = \frac{I_C R_L}{V_T} = 49 \rightarrow I_C R_L = 49(0.025\ \text{V}) = 1.23\ \text{V}$$

(f) A noninverting amplifier with a gain of 10 and an input resistance of 2 kΩ should be achievable with either a common-base or common-gate amplifier with proper choice of operating point. The gain of 10 is easily achieved with either the MOSFET or BJT design estimate: $A_v = V_{DD}/(V_{GS} - V_{TN})$ or $A_v = 10V_{CC}$. $R_{\text{in}} \cong 1/g_m = 2\ \text{k}\Omega$ is within easy reach of either device.

(g) Twenty-five ohms represents a small value of output resistance. The follower stages are the only choices that provide low output resistances. For the followers, $R_{\text{out}} = 1/g_m$, and so we need $g_m = 40$ mS.

$$\text{For the BJT:} \quad I_C = g_m V_T = 40\ \text{mS}(25\ \text{mV}) = 1\ \text{mA}$$