ECE428 Class Project

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In the project, your design team is responsible for developing a back ground subtraction circuit block that is used in motion detection application. The overall system setup is shown in Figure 1. Other circuit blocks used in the system will be provided to you as IP blocks during the final system integration. There are several milestones. **At least, your team is requested to accomplish the first milestone and show reasonable efforts toward hardware demonstration (the second milestone)**. The more milestones that you can accomplish the more bonus points will be earned by your design team.

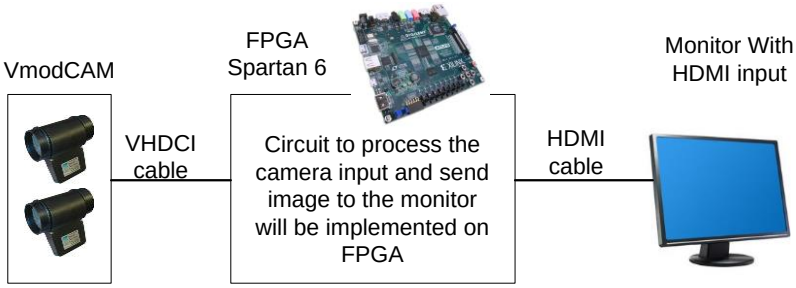

Figure 1 System demonstration setup

As shown in Figure 1, the camera module sends the video stream to the FPGA circuit. Several signal processing functions will be performed by the circuits on the FPGA boards. The processed video will be displayed on the computer monitor. The circuit that your team is responsible for is the image back ground subtraction circuit used for motion detection.

The purpose of background subtraction is to extract foreground objects, by using two frames and performing subtraction of these frames. This method helps identify moving objects from the portion of a video frame that differs significantly from a background model. The two frames are subtracted from each other pixel by pixel and the result is accumulated. If the accumulated result is bigger than threshold then the moving object is detected. The following pictures show an example of background subtraction.

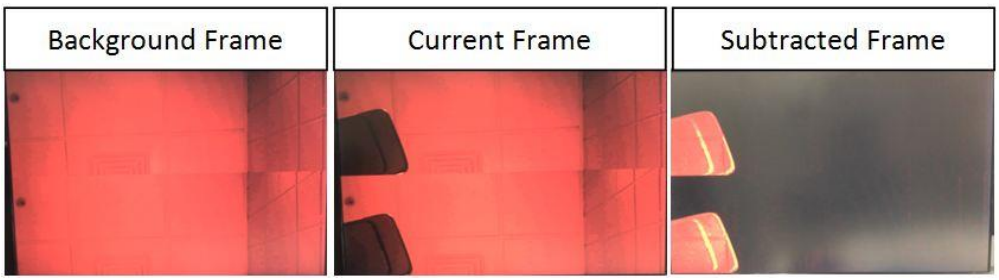

Figure 2 Background subtraction

Milestone 1: Design and Evaluation of Background Subtraction Circuit (100%)

To simplify your design in this phase, we can assume that the back ground subtraction circuit has a simple interface with the rest of the circuit. Its block diagram and interface circuits are shown in Figure 3. The background subtraction circuit calculates the difference between two picture frames: reference frame and current frame. Each frame has a size of 640X240 pixels and the data size for each pixel is 5-bit. Your design takes the pixel data of the two frames from two SRAM like buffers and hence your design should include the proper memory address generation circuit. The difference (absolute value) between two pixel data is computed by the first subtractor and subsequently accumulated by the added and register. The final output, which is the accumulated difference between the two frames, should be loaded to the output register once the entire computation is complete. Note that your circuit operation should be synchronized by input clock **PClk**. Also, **VtcVde** is a high-active enable for the address generation circuit.

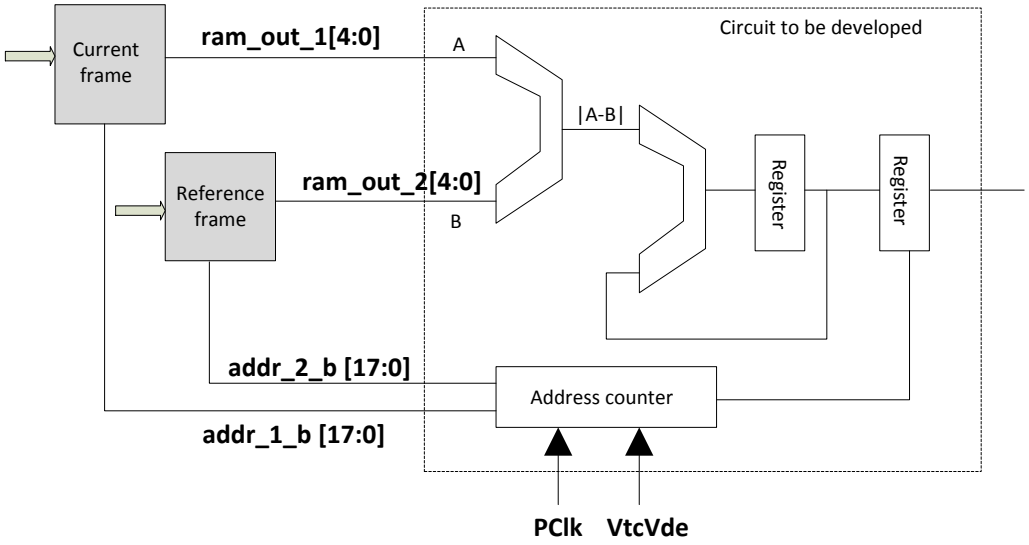

Figure 3 Background subtraction circuit

The VHDL code (**file name: milestone1.zip**) for the two memory components will be provided for you to run circuit simulation. The symbol of the memory IP is shown in below:

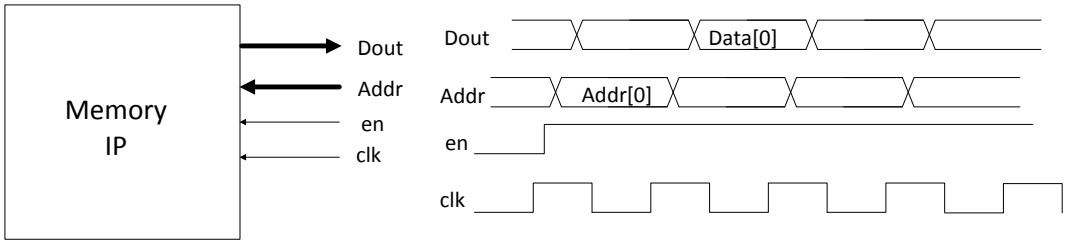

Figure 4 Memory IP operation

The complete design should include the following information

- Complete HDL code
- The maximum clock frequency determined from the static time analysis report for the final design (the design after placement and routing). **Please highlight any efforts that you have done to improve the clock frequency (This will greatly affect the final score of your report)**
- The resources used in your design
- Estimated power consumption
- A snapshot of the final layout (you can see it from the FPGA editor and you need show only the potion that occupied by the design)
- A snapshot of the simulated waveform which indicates the final output value of your design.

Based on the clock frequency, answer the following question:

- For the give frame size (640X240), can your design meet the speed requirement of the system with a frame rate of 24 frames per second (fps)? **Justify your answer**.
- Will your design work with the frame size of 1920X1080 (high definition) and the frame rate of 24 fps? If not, could you propose a design to meet the new speed requirement? Show the schematic

Milestone 2: Hardware Demonstration (25%)

In this phase, you will integrate your design with other functional blocks which are provided as IP blocks (**file name: milestone2.zip**) and design a simple threshold comparator circuit, which compares the output of the background subtraction circuit with three threshold values and light three LED accordingly. The block diagram of the system in this phase is shown in Figure 5. ***When you instantiate your design into the design project (provided in milestone2.zip), make sure you connect the I/O ports of your design to signals with the names highlighted in the block diagram.*** The goal of this phase is to practice your skills to handle relatively large designs. The threshold values used in the comparison are: 2×10^6, 1×10^6, 1×10^5.

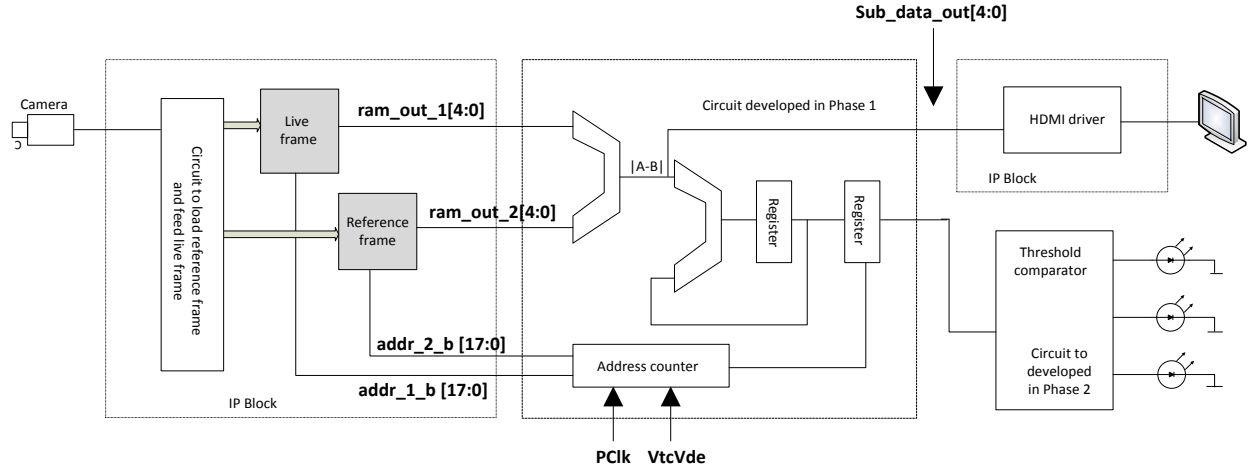

Figure 5 FPGA Circuit for hardware demonstration

In the demo, you need capture the reference frame first. To start the capture process, pull switch SW2 to the upper position (logic 1). The first frame from the camera after SW2 switching to 1 will be captured as the reference frame. After the reference frame is captured, the frames from the camera will be fed to live frame buffer and your circuit should continuously compute the difference between the reference frame and current frame (in the live buffer). If you want to re-capture the reference frame, pull switch SW2 to logic 0 (the bottom position) and switch it back to logic 1.

Milestone 3: Sending the computation results to computer via UART serial communication (25%)

In this phase, you will develop circuit that enables the system to send the computation results to a computer via serial communication port (USART) as shown in Figure 6. The UART is emulated by a USB connection and HyperTerminal is used to display the received data. The circuit sends the result for one frame and skips the results for the next 23 frames. Then, repeat the same pattern. In this way, the results sent to the computer fill the display in a slow pace. The UART design will be provided as an IP block (**file name: milestone3_uart.zip**). Note that you still need the IP blocks used in milestone 2 design. You need design a circuit to convert the computation result into ASCII format and control which computation result to be sent. The interface of the UART module is very simple and is described in the header (comments) of the HDL code file.

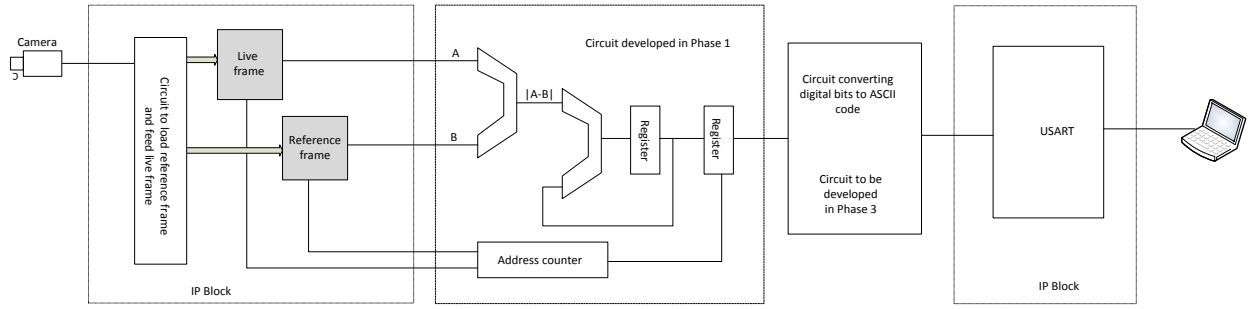

Figure 6 FPGA Circuit for sending computation result to computer

Milestone 4: Implementing the frame buffers using on-board DDR memory (50%)

In the previous phase, the frame buffers are implemented using FPGA embedded RAMs, which provide simple interface but has limited storage capacity. In this phase, you will modify the existing design to implement the frame buffers into the on-board DDR memory. Meanwhile, you will modify your circuit to handle video with frame size of 640X480 (VGA). The block diagram of the system to be developed in this phase is shown in Figure 6. The HDL code for the circuit to interface DDR memory already exists in the design files provided to you. However, you need understand it and modify it to fit your design requirement.

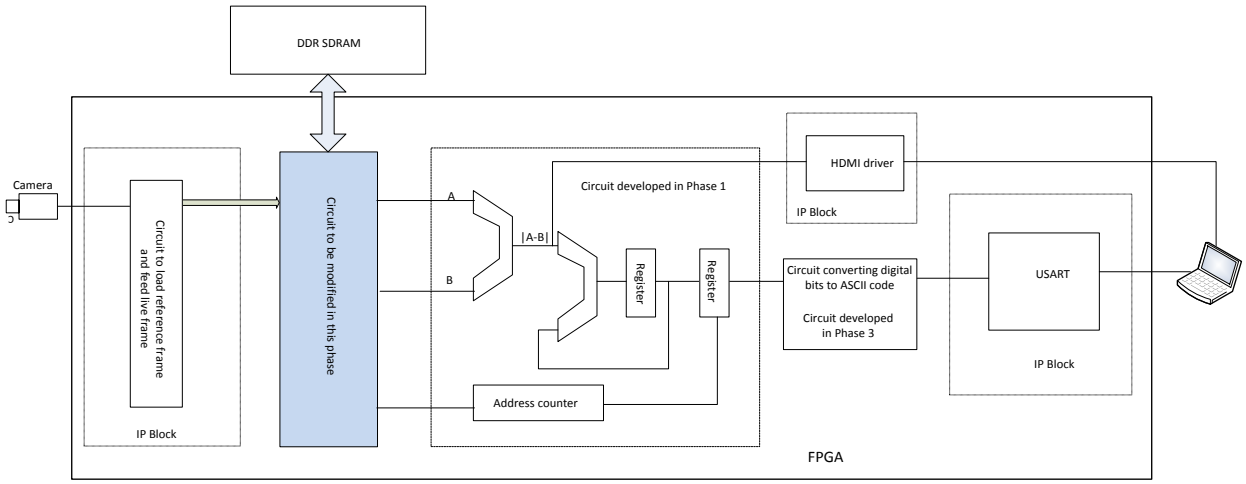

Figure 7 System with using DDR memory as frame buffer