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Advanced Light Intensity Indicator

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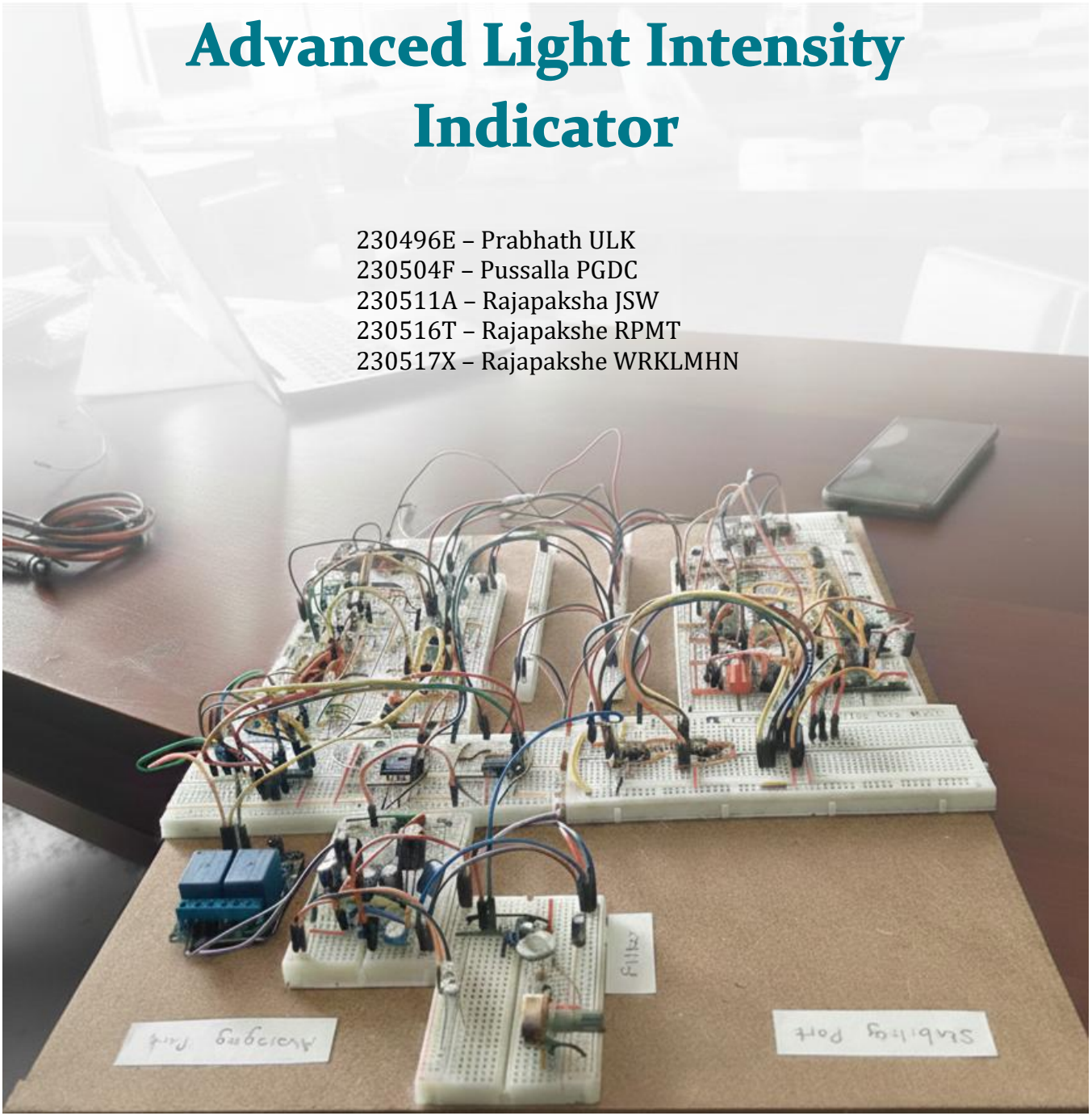

Group 12 | Digital Signal Processing | December 12, 2025

1. Introduction

The Advanced Light Intensity Indicator (ALII) module is designed to measure, process, and display ambient light intensity in a reliable and energy-efficient manner. By combining analog signal conditioning with digital logic-based processing, the system provides both instantaneous and averaged light intensity indications without using programmable devices. The module addresses common real-world issues such as power-line noise, temporary light fluctuations, and unstable readings, ensuring accurate and meaningful light level information. With applications in energy conservation, public safety, and renewable energy powered systems, the ALII module demonstrates a practical, hardware-oriented approach to intelligent light monitoring using fundamental electronic building blocks.

For convenience, this model can be divided into 4 subsections.

1. Filter
2. LDR and Real-time Monitoring
3. Stability
4. Average

2. Simulation

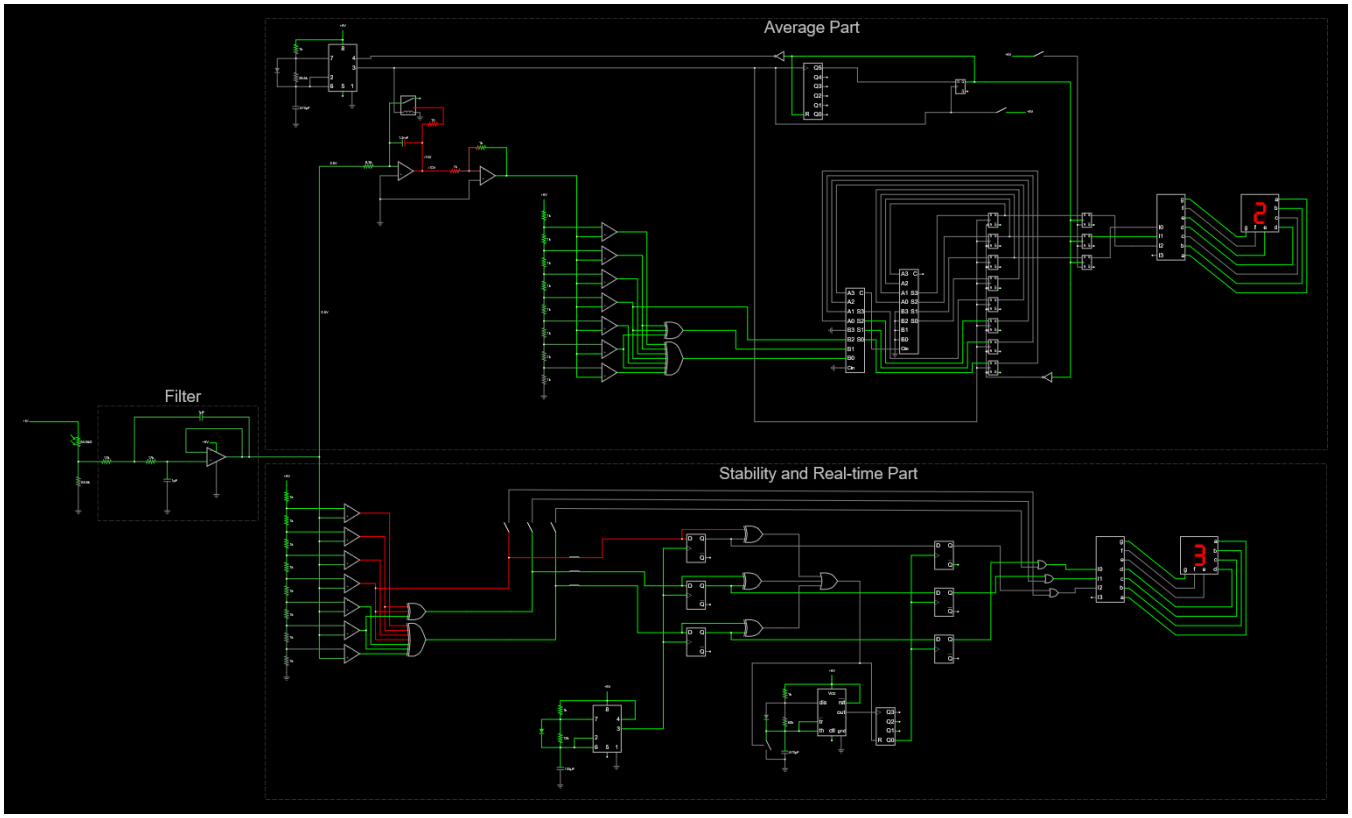

Figure 2.1

Simulation link

3. Filter

3.1 Purpose

The purpose of this stage is to remove unwanted noise and fluctuations from the light sensor output. This ensures that only genuine changes in ambient light intensity are passed to the subsequent processing stages, improving the accuracy and stability of the system.

3.2 Design Requirements

- Must suppress noise components in the 50–100 Hz range
- Must allow slow changes in ambient light to pass
- Must provide a clean and reliable signal for subsequent processing and display

3.3 Principle of Operation

The circuit operates based on the Butterworth low-pass filtering principle with unity gain Sallen-key topology. High-frequency components are attenuated, while low-frequency components pass with minimal attenuation.

3.4 Circuit Description

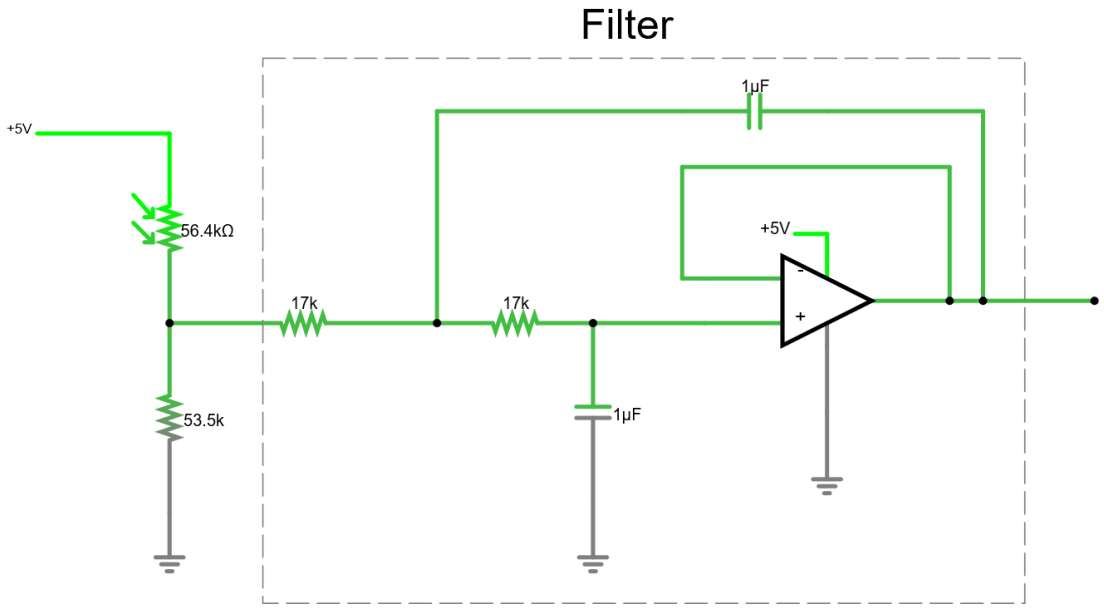

Figure 3.1

As shown in Figure 3.1, the LDR is connected in a voltage divider configuration with a variable resistor. The output voltage is fed into the filtering circuit, where the capacitor smooths rapid voltage variations before the signal is passed to the next stage.

3.5 Design Calculations

$Cut-off\ frequence = 5\ Hz$

$Pass\ band\ tolerance = 3\ dB$

$$10\log_{10}(1+\epsilon^2) = 3 \implies \epsilon \approx 1$$

$High\ frequency\ attenuation\ at\ 50\ Hz = 20\ dB$

$$10\log_{10}\left[1+\epsilon^2\left(\frac{\omega}{\omega_c}\right)^{2n}\right] = 20 \implies n = 1.99 \approx 2^{nd}\ \text{order}$$

2^{nd} order Butterworth normalized filter transfer function

$$H(s) = \frac{1}{s^2+\sqrt{2}s+1}$$

For 5 Hz

$$H(s) = \frac{1}{\left(\frac{s}{10\pi}\right)^2+\sqrt{2}\left(\frac{s}{10\pi}\right)+1} = \frac{100\pi^2}{s^2+10\sqrt{2}\pi s+100\pi^2} \leftrightarrow \frac{K{\omega_0}^2}{s^2+\frac{\omega_0}{Q}s+{\omega_0}^2}$$

$$\frac{\omega_0}{Q} = 10\sqrt{2}\pi \implies Q = \frac{1}{\sqrt{2}} = \frac{1}{3-A} \implies A = 3-\sqrt{2}$$

So, this gave a gain around 1.586. To avoid this gain, we reversely calculated cut-off frequency and attenuation choosing $A = 1$.

$$Q = \frac{1}{3-A} = \frac{1}{2}$$

$$\frac{\omega_0}{Q} = 10\sqrt{2}\pi \implies \frac{\omega_0}{1/2} = 10\sqrt{2}\pi \implies \omega_0 = 5\sqrt{2}\pi \implies f_0 = 3.5355\ Hz$$

$$Attenuation\ at\ 50\ Hz\ in\ these\ conditions\ = 10\log_{10}\left[1+\epsilon^2\left(\frac{50}{3.5355}\right)^{2\times2}\right] = 46.02\ \text{dB}$$

$$\omega_0 = \frac{1}{RC} = 5\sqrt{2}\pi$$

$$Choosing\ C\ = 1\times10^{-6}$$

$$\text{Then R} = 14.14\ \text{k}\Omega$$

3.6 Component Selection

Standard resistor and capacitor values were selected to ensure ease of availability and reduce cost. Op-amp ICs were chosen to comply with the design constraint of avoiding programmable and task-specific ICs. Here choose UA741[1] IC and gave it to +7V and -7V supply voltages, because this IC saturated the output below the supply.

$$\omega_0 = \frac{1}{RC} = 5\sqrt{2}\pi$$

$$Choosing\ C\ =\ 1\ \mu F$$

$$\text{Then R}\ =\ 14.14\ k\Omega$$

For availability of the resistor, we choose R = 17 kΩ

3.7 Features

- Effectively suppresses electrical noise
- Provides a stable signal for digital processing
- Simple and low-cost implementation

3.8 Test Results

The circuit was implemented in real world. It was shown on the Oscilloscope that rapid fluctuations given by wave generator in the input signal (Yellow color) are significantly reduced (Blue color), while slow changes in light intensity are preserved. Figure 3.2 and 3.3 illustrates the input waveform and filtered output waveform.

When f = 5 Hz

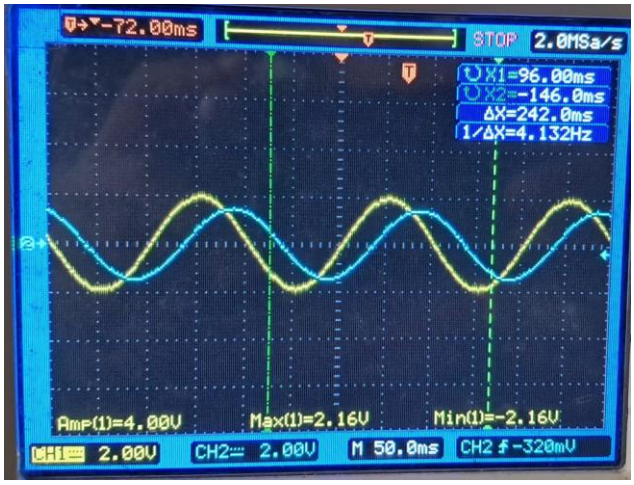

Figure 3.2

When f = 50 Hz

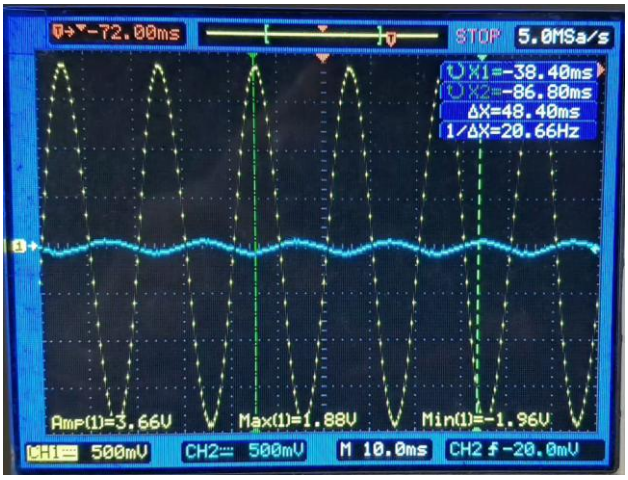

Figure 3.3

4. LDR and Real-Time Monitoring

4.1 Purpose

The purpose of this stage is to sense ambient light intensity and convert it into a discrete digital representation that can be displayed on a seven-segment display. This stage forms the core sensing unit of the system and provides real-time information about the surrounding light conditions.

4.2 LDR Characteristics

A Light Dependent Resistor (LDR) is a passive photo-resistive sensor whose resistance decreases with increasing light intensity. In low-light or dark conditions, the resistance of the LDR is high (in the order of megaohms), while in bright light conditions it drops to a few kilo-ohms. Due to this wide resistance variation, the LDR is well suited for ambient light sensing applications. However, its response is relatively slow, which makes it more appropriate for measuring gradual changes in light rather than rapid variations.

4.3 Principle of Operation

The LDR operates based on the principle of photoconductivity. When light photons fall on the surface of the LDR, they generate charge carriers within the semiconductor material, reducing its resistance. This change in resistance is converted into a corresponding voltage change using a voltage divider circuit. The resulting analog voltage is proportional to the incident light intensity and is used for further processing.

4.4 Circuit Description

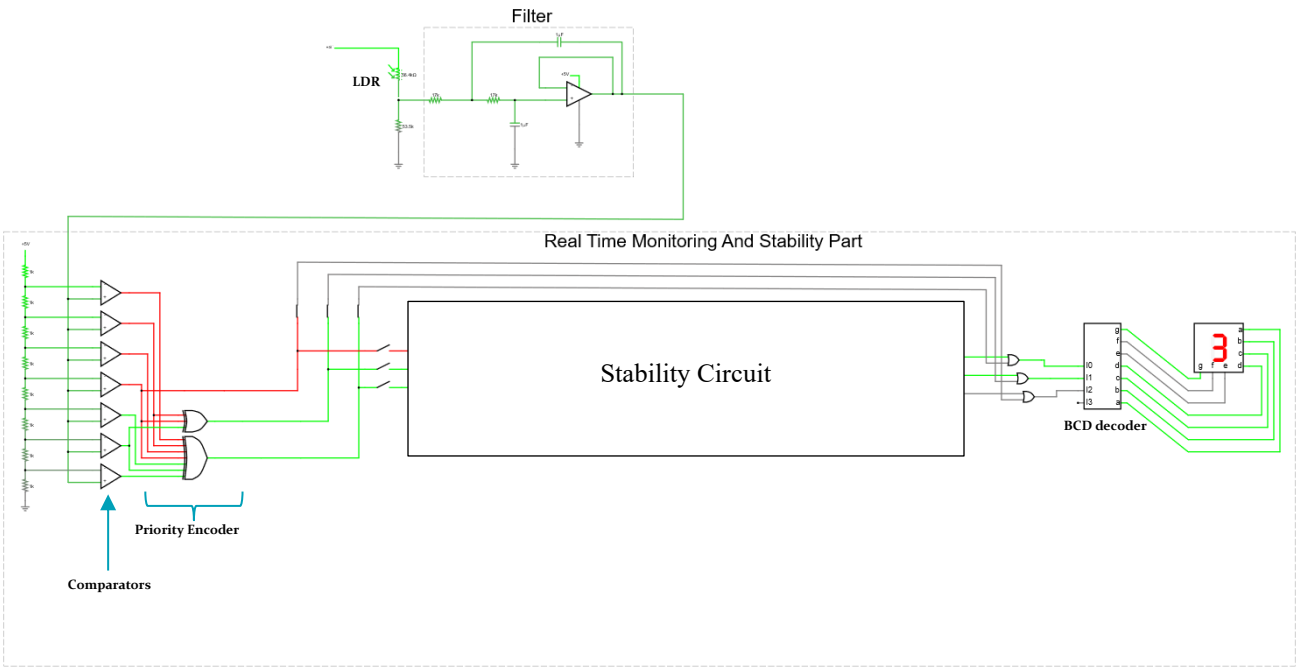

Figure 4.1

As shown in Figure 4.1, the LDR is connected in series with a fixed resistor to form a voltage divider. The output voltage is taken from the junction between the LDR and the resistor. As the light intensity increases, the resistance of the LDR decreases, causing the output voltage to change accordingly. This voltage is then fed into a comparator network that compares the sensed voltage against predefined reference levels (0.625 V) to generate a digital output representing the light intensity level.

The analog voltage obtained from the LDR divider is divided into eight distinct levels corresponding to light intensity values from 0 to 7. This is achieved using a set of comparators with reference voltages generated by a resistor ladder network. Each comparator switches its output when the LDR voltage exceeds the corresponding threshold. The comparator outputs are then encoded into a 3-bit binary value, which represents the detected light level. This is then displayed on a 7-segment display via going through OR gates and decoder.

4.5 Component Selection

The LDR was selected due to its low cost, ease of use, and suitability for ambient light sensing.

Standard 1kΩ resistors were used to create resistor ladder.

LM339B Quad Differential Comparators [2] were used to compare reference voltages with the LDR output voltage.

An SN74HC148 8-Line to 3-Line Priority Encoder [3] was used for encoding and display control in accordance with the design constraint of avoiding programmable or task-specific integrated circuits.

An CD4511B CMOS BCD-to-7-Segment Latch Decoder Drive [4] was used for decode the encoded signal and 7 Segment Display [5] was used for display output.

4.6 Features

- Detects ambient light intensity using a simple and reliable sensor.
- Converts analog light information into discrete digital levels (0–7).
- Provides clear visual indication through a seven-segment display.
- Low-cost and easy-to-implement sensing circuit.
- Suitable for real-time monitoring of lighting conditions.

5. Stability

5.1 Purpose

The purpose of the stability detection stage is to prevent false or sudden changes in the displayed light intensity caused by temporary disturbances such as shadows, passing objects, or short-term variations in lighting. This stage ensures that the system updates its output only when the detected light level remains stable for a predefined duration (30 seconds to 300 seconds).

5.2 Stability Criteria

A light level is considered stable when the digital output of the light sensing stage remains unchanged continuously for a specified time interval. Any change in the detected light level during this interval resets the stability timer. Only after the light level remains constant for the entire stability period is the output considered valid and forwarded to the display.

5.3 Timing Principle

The stability timing is achieved using an RC-based timing circuit combined with digital logic. When the light level remains unchanged, the timing capacitor charges gradually. If a change in light level is detected, the capacitor is discharged and the timing process restarts. Once the capacitor voltage reaches a predefined threshold, the system generates a “stable” signal indicating that the light has remained constant for the required duration.

5.4 Circuit Description

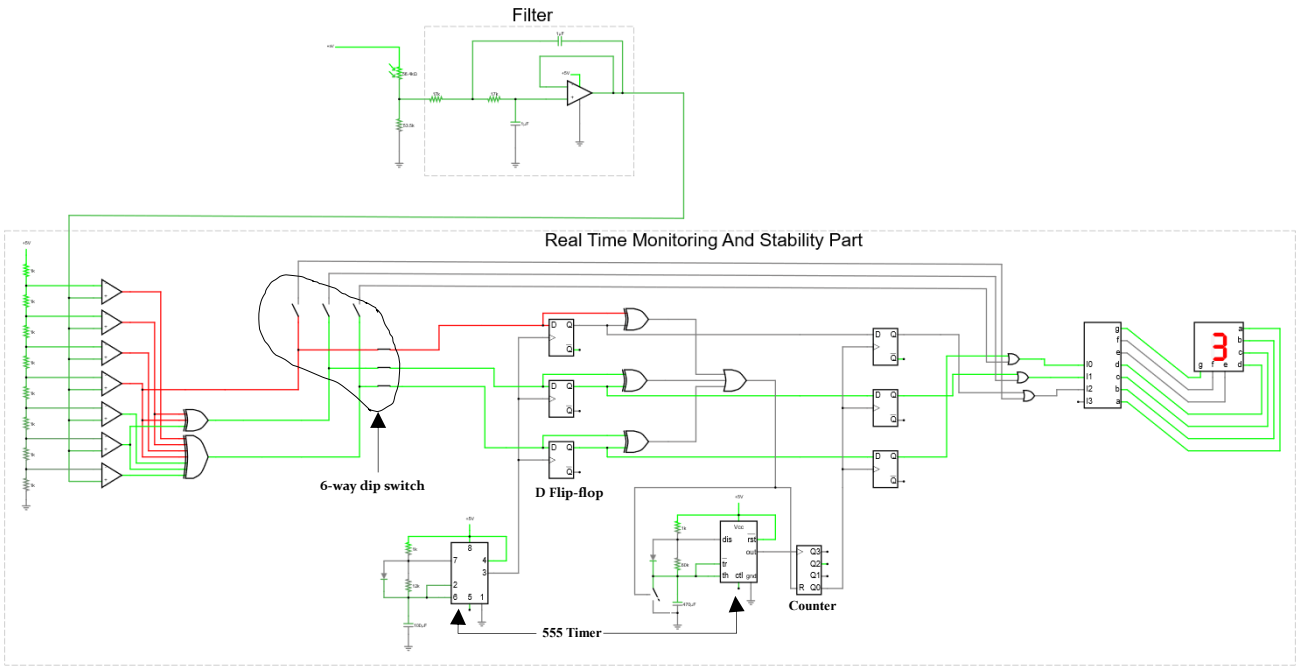

Figure 5.1

As shown in Figure 5.1, the digital output from the light sensing stage is continuously monitored for changes using XOR gates and flip-flops using pulses from the timer on the left-hand side each and every 1 second period. Any change in the light level triggers a reset signal that discharges the timing capacitor on right-hand side timer and reset the counter. When there is no change, the RC network of the timer starts charging, and after reaching the threshold voltage, a steady signal is generated and goes to the counter. From the counter, the first counter signal is obtained. But due to the timing mismatch of the circuit in the actual implemented circuit, the signal cannot be obtained from the first counter signal. Further, when the XOR gates detect a change and it resets the counter and the timer. Theoretically, at that moment a pulse comes from the timer, but in the real world it does not come at the same time. For that, we need to obtain the counter signal from the second counter output. It updates flip-flop values and display stability light intensity using decoder and 7 segment display. A manual 6-way dip switch is included to enable or disable the stability detection feature as required.

5.5 Time Adjustment Method

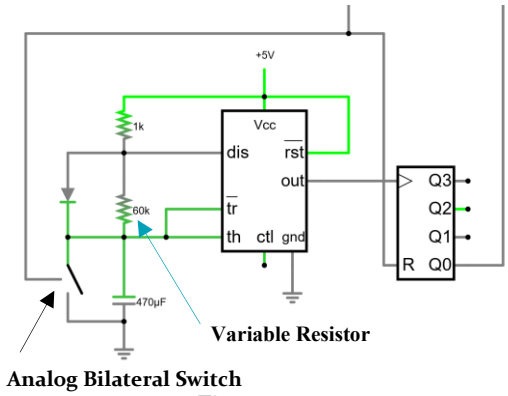

Figure 5.2

The stability time is adjustable between 30 seconds and 300 seconds using a variable resistor connected in the RC timing network. By varying the resistance, the RC time constant is modified, allowing the user to control the delay before the output is updated. This provides flexibility to adapt the system to different environmental conditions and application requirements.

5.6 Component Selection

A manual 6-way dip switch is included to enable or disable the stability detection feature with real-time monitoring as required.

CD4013B CMOS Dual D-Type Flip-Flops [6] are selected to store data to check the stability and update the display.

SN74HC86 Quadruple 2-Input XOR Gates [7] are used to check the stability of the light intensity.

SN74HC32 Quadruple 2-Input OR Gates [8] are used to combine XOR outputs and integrate real-time monitoring and stability checking.

NE555 Precision Timers [9] are used to check the stability of each and every seconds. Another timer is also used to calculate the stability time.

CD4066B CMOS Quad Bilateral Switch [10] is used to discharge the capacitor of the timer automatically when a control pulse comes.

500 kΩ range variable resistor is used for the adjust the integrator time constant.

One 470 µF capacitor and 100 µF capacitor are used for timers.

Two 1kΩ resistors, one 12 kΩ resistor and two diodes are used for timers.

CD4040B CMOS Ripple-Carry Binary Counter [11] is used to count the time pulses come from the timer.

5.7 Features

- Suppresses false indications caused by temporary light fluctuations
- Updates the display only after sustained light stability
- Adjustable stability period from 30 s to 300 s
- User-selectable enable/disable switch
- Improves reliability in real-world lighting environments

6. Average

6.1 Purpose

The purpose of the averaging circuit is to determine the average ambient light intensity over an extended period of time. This provides a more reliable representation of lighting conditions by reducing the effect of short-term fluctuations and momentary changes in light intensity.

6.2 Averaging Method

The averaging is performed in both analog and digital domains by averaging over a predetermined time interval using an integrator, where the samples (we obtain 32 samples) from the integrator is quantized and digitally added to the accumulated value. At the end of the averaging period, the accumulated result represents the average light intensity, which is then displayed on a dedicated seven-segment display.

6.3 Timing Control

The averaging time is controlled using a 555-timing circuit with a variable time periods and a digital counter. Since 32 samples are typically taken in the digital domain, the duration should be adjustable from around 9.375 seconds to 28.125 seconds using a variable resistor. Then the duration can be varied between 300 seconds and 900 seconds.

6.4 Circuit Description

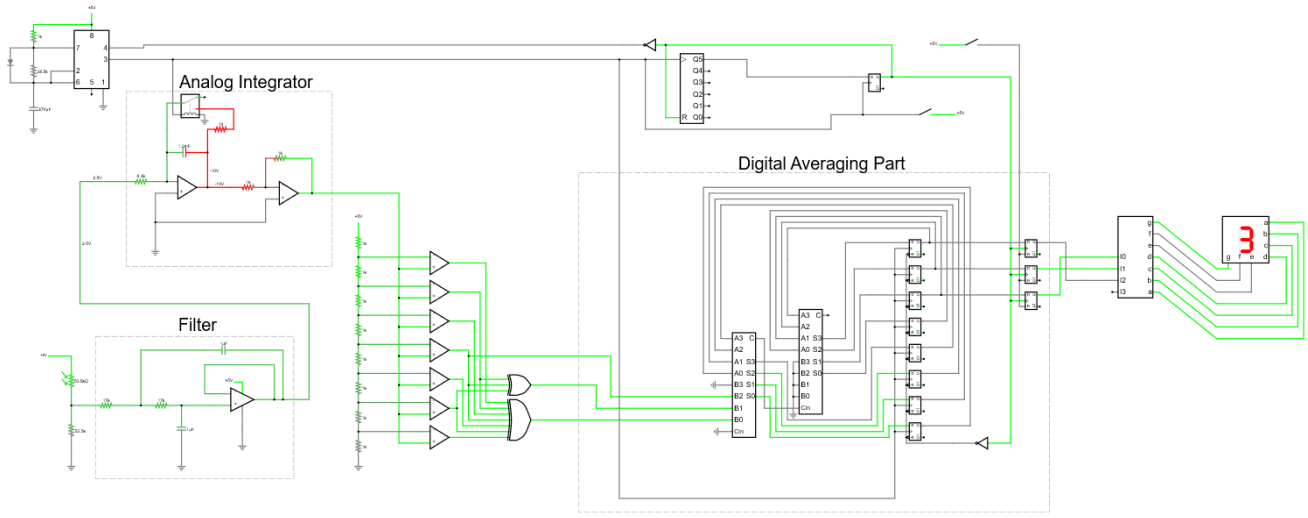

Figure 6.1

As illustrated in Figure 6.1, the filtered light level output is fed into the averaging circuit. A 555-timer generates periodic sampling pulses that enable registers or counters to capture and accumulate the light level data came from the integrator. In that sampling period about 9.375 seconds to 28.125 seconds was averaged analog domain using integrator. After each sample pulse the integrated voltage through capacitor must be discharged. A relay switch is used for this. Then the output of the integrator must be inverted and quantized using inverter and flash ADC respectively. Conter and Flip-flops control the data flow and ensure that only valid stable samples are included. After the average time has elapsed, the timer stops, the accumulated value is averaged and sent to the seven-segment display driver, which displays the average light intensity on a dedicated display. 2 push buttons have also been added to reset the 7-segment display and start the timer.

6.5 Reset Operation

A manual push-button reset is provided to clear the averaging circuit. When the reset button is pressed, all counters and storage registers are reset to zero, and the averaging process restarts. This allows the user to initiate a new averaging cycle at any desired moment.

6.6 Component Selection

Two µA741 General-Purpose Operational Amplifiers [1] are used for integrator and inverter.

500 kΩ range variable resistor is used for the adjust the integrator time constant.

2 Channel 5V Relay Module [12] and one 10 Ω resistor are used to discharge the capacitor bank in the integrator.

Five 220 µF capacitors, one 470 µF capacitor and 100 µF capacitor are used for integrator and timer.

NE555 Precision Timer [9] is used for generate the pulses within fixed time period between 9.375 s to 28.125 s.

50 kΩ range variable resistor is used for the adjust the difference between pulses of timer.

Three 1kΩ resistors and one diode are used for inverter and timer.

Eight 1kΩ resistors are used to create resistor ladder.

LM339B Quad Differential Comparators [2] were used to compare reference voltages with the integrator output voltage.

An SN74HC148 8-Line to 3-Line Priority Encoder [3] was used for encoding and display control in accordance with the design constraint of avoiding programmable or task-specific integrated circuits.

An CD4511B CMOS BCD-to-7-Segment Latch Decoder Drive [4] was used for decode the encoded signal and 7 Segment Display [5] was used for display output.

Two SN74LS83A 4-bit Binary Full Adders [13] are used to create 7-bit adder.

SN74HC273 Octal D-Type Flip-Flop [14] is used to store each accumulated value in the adder by clock pulse.

Two CD4013B CMOS Dual D-Type Flip-Flops [6] are used to store final averaged intensity value.

One CD4020B CMOS Ripple-Carry Binary Counter [11] is used to count 32 pulses from the timer.

One CD4069UB CMOS hex inverter [15] is used as NOT gate.

Two push buttons.

6.7 Features

- Computes average light intensity over an extended period.
- Adjustable averaging duration from **300 s to 900 s.**
- Minimizes the effect of short-term light fluctuations.
- Separate seven-segment display for averaged output.
- Manual reset for user control.
- Fully hardware-based implementation using gates and flip-flops.

7. References

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