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**DE 1**

**Intro to VLSI**

**9/7/2022**

**Professor James Moulic**

**Part A**

8 micron meters by 5.4 micron meters

Background pattern

Description automatically generated

**2.4K ohm using P+ diffusion  
1. First, I created a 8 micron meters by 1 micron meters using the P+ diffusion for the resistance which gave me a 2.4k ohm resistor.**

Timeline

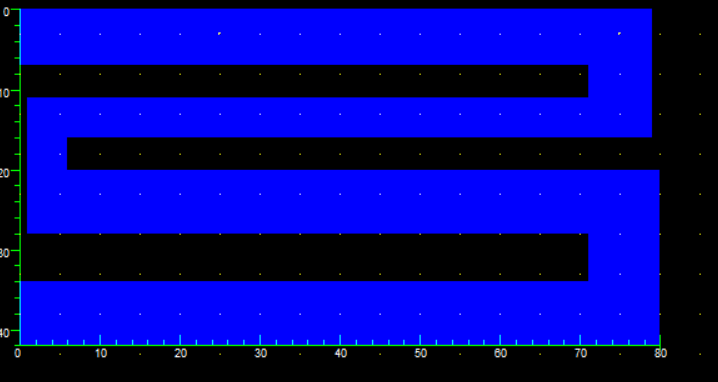
Description automatically generated with low confidence

A screenshot of a computer

Description automatically generated with medium confidence

**4.99 fF using Metal 1**

**2.** **I created a 4.99 fF using Metal 1 and meandered the capacitor. The size was 8 microns meter by 4.2 microns meter.**



Graphical user interface

Description automatically generated

**Part B**

**1.** **Graphical user interface, application

Description automatically generated**

**2.**

A screenshot of a computer

Description automatically generated with medium confidence

**NMOS’s Effective Resistance = 2351 Ohms**

**3.**

**Graphical user interface

Description automatically generated**

**4. Effective Gate Capacitance = 5.01 fF**

Graphical user interface

Description automatically generated

**5. The gate capacitance has almost the same capacitance as my capacitor which is approximately around 5 fF. The active components take less space but has more different types of materials and has different layers while the passive components take up a lot of space but is made of one material and is one layer.**