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**DE 2**

**Intro to VLSI**

**9/18/2022**

**Professor James Moulic**

**Part A**

**PMOS & NMOS = 17 lambda by 2 lambda**

**A screenshot of a computer

Description automatically generated**

**Voltage Vs. time**

**Diagram

Description automatically generated**

**Current Vs. Time**

**Diagram

Description automatically generated**

**6. The rise and time delays are different because the rise depends on the PMOS which depends on holes which moves slower than electrons. On the other hand, the fall depends on electrons which moves faster than holes, hence why the fall is faster.**

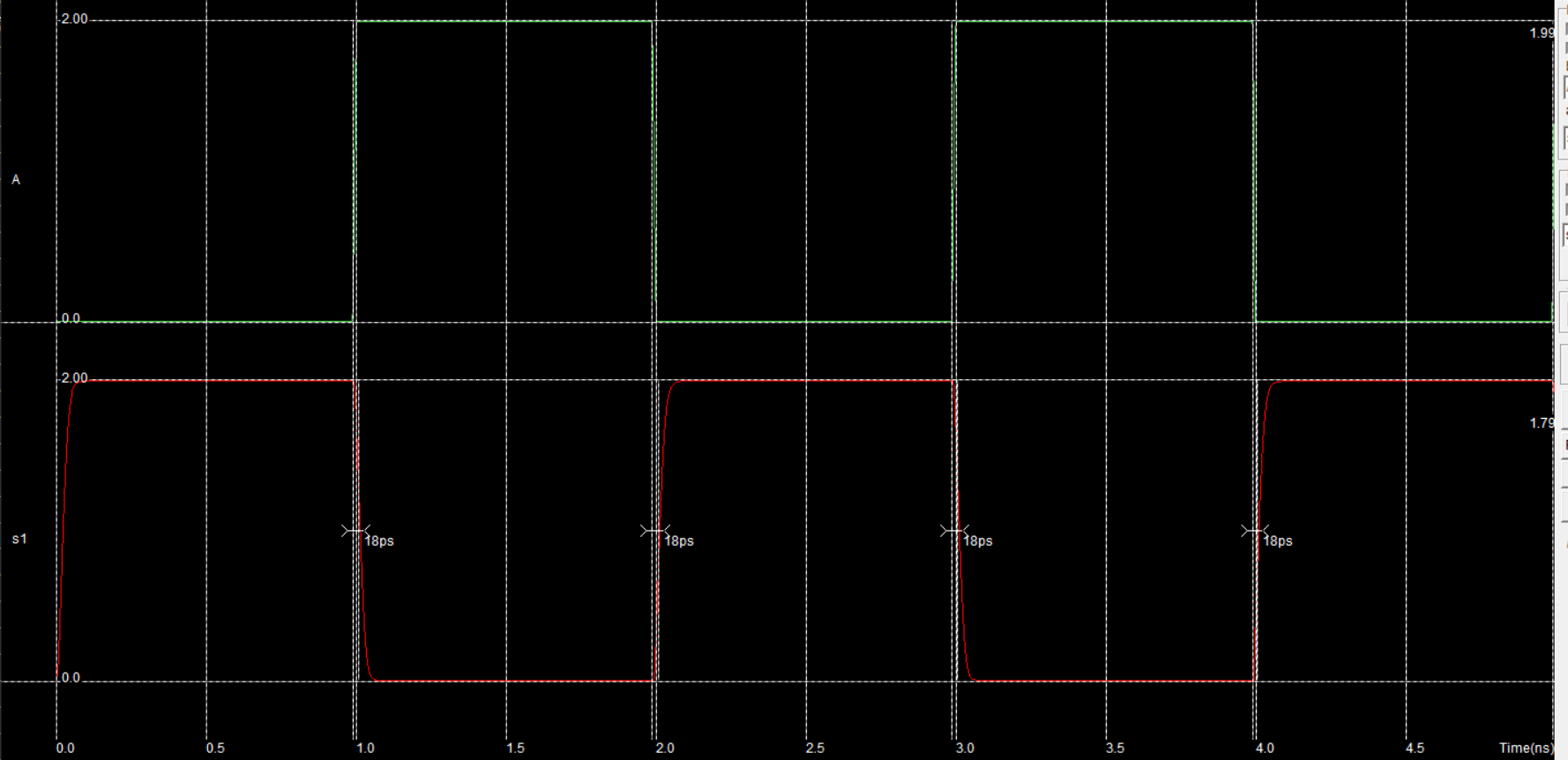
**PART B**

**PMOS(42 Lambda by 2 Lambda), NMOS (20 Lambda by 2 Lambda)**

**A screenshot of a computer

Description automatically generated**

**Voltage Vs. Time( Output Rise = 18 ps, Output Fall 28ps)**

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**Current Vs. Time**

**Chart, line chart

Description automatically generated**

**7. The rise and fall times approximately the same because the PMOS width is twice that of the NMOS width. The mobility of electrons is twice that of holes and so to make the fall and rise equal, we would need to double the PMOS.**

**PART C (BONUS)**

**A screenshot of a computer

Description automatically generated with medium confidence**

**Voltage Vs. Time  
Chart

Description automatically generated with medium confidence**

**Current Vs. Time**

**Chart, line chart

Description automatically generated**

**3. The rise and fall time delays are the same because the inverters are connected in series and each inverters have the same PMOS and NMOS widths and lengths.**