**Jan Karl Galia**

**DE 3**

**Intro to VLSI**

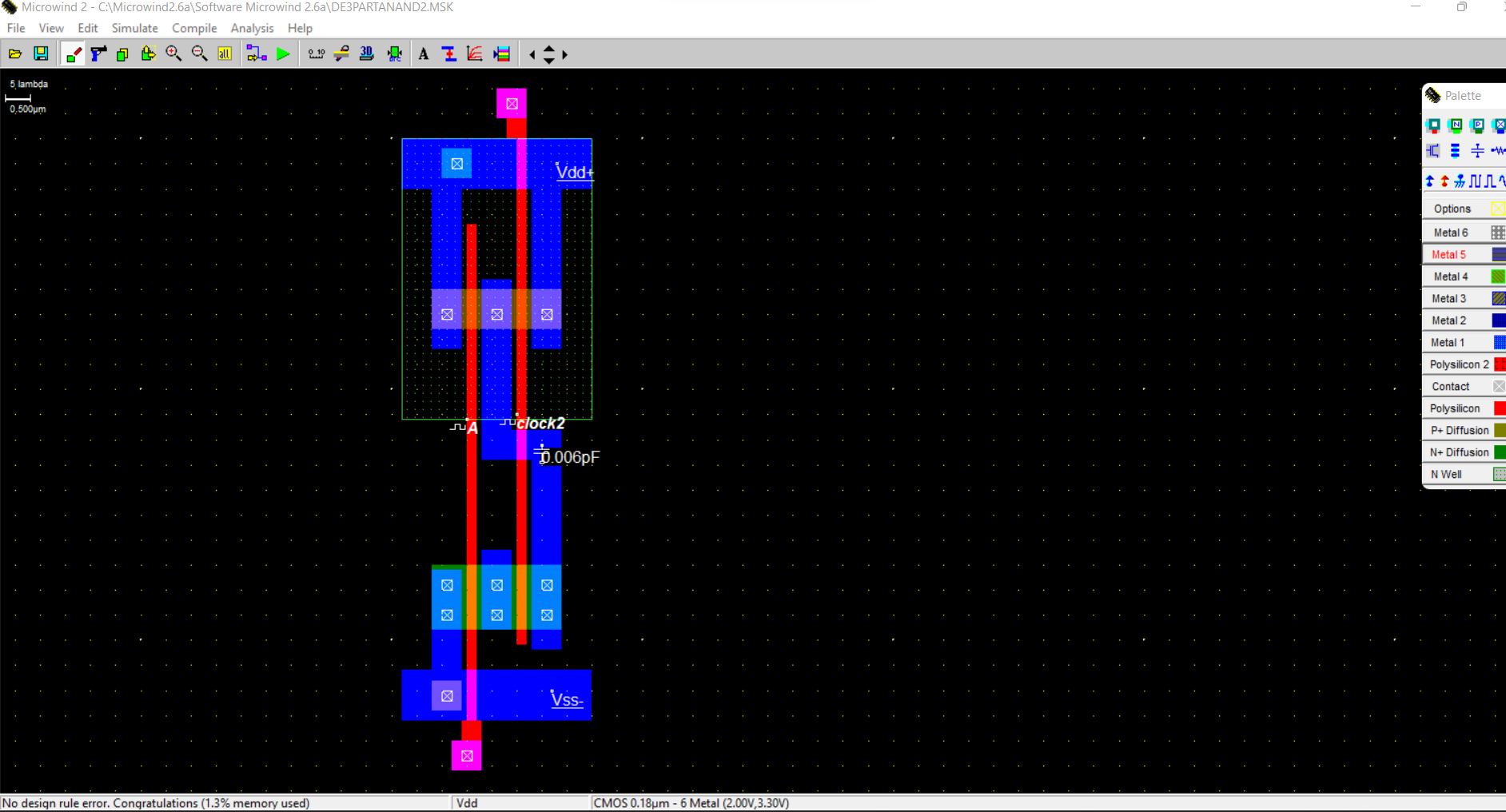
**9/21/2022**

**Professor James Moulic**

**Part A**

**2- Input NAND Gate**

**PMOS (2 fingers, 8 lambda by 2 Lambda), NMOS (2 fingers, 13 lambda by 2 lambda)**

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**A screenshot of a computer

Description automatically generated with medium confidence**

**Voltage Vs. Time (Rise = 19 ps, Fall = 19 ps, 0 ps Difference)**

**Diagram

Description automatically generated**

**Current Vs. Time (Between .4 mA - .8 mA)**

**Diagram

Description automatically generated**

**3-Input NAND GATE**

**PMOS (3 fingers, 6 lambda by 2 Lambda), NMOS (3 fingers, 21 lambda by 2 lambda)**

**A screenshot of a computer

Description automatically generated with medium confidence**

**Graphical user interface

Description automatically generated**

**Voltage Vs. Time(Fall = 19ps, Rise = 19ps, Difference = 0 ps)**

**Graphical user interface, diagram

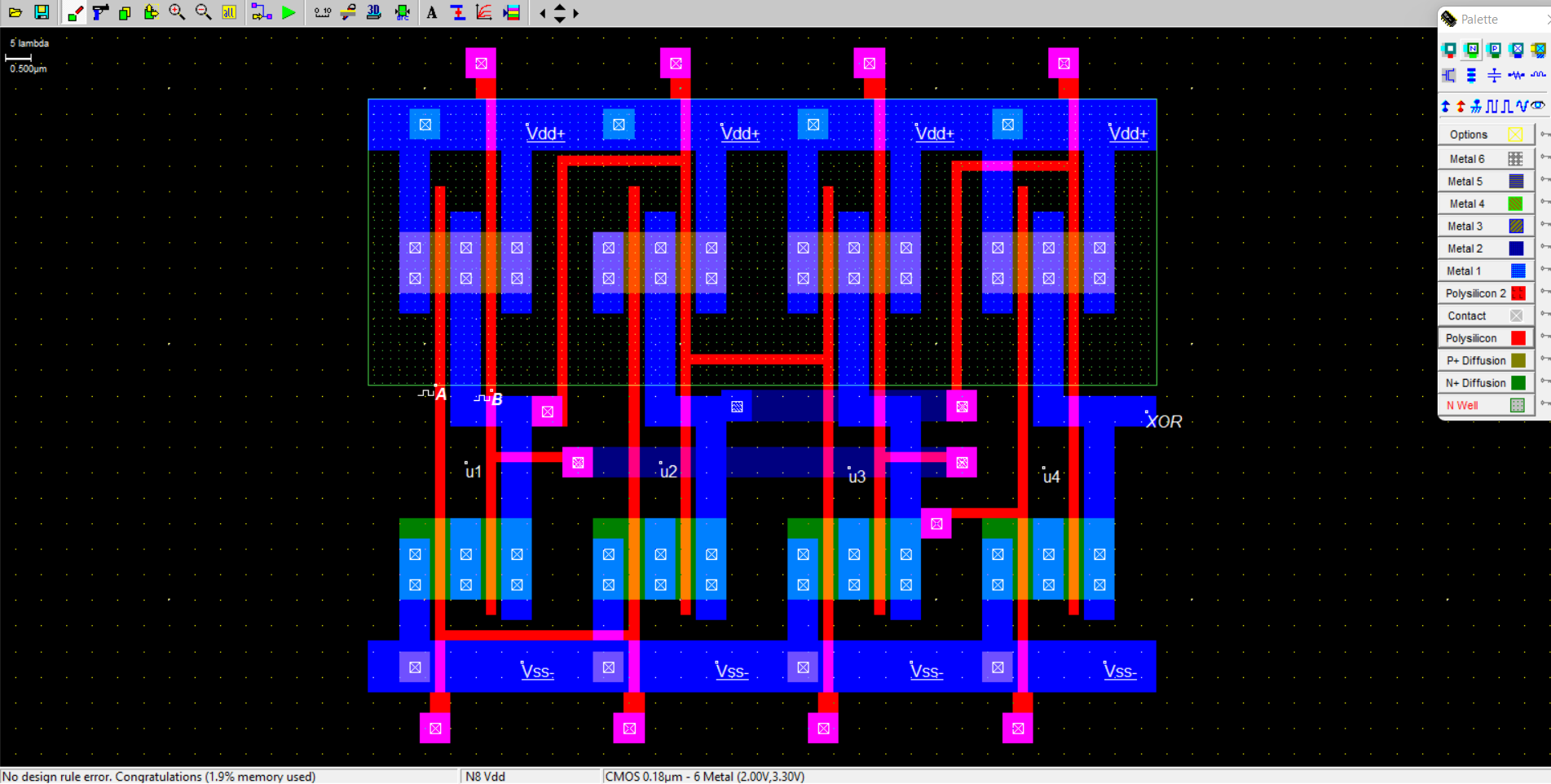
Description automatically generated**

**Current Vs. Time**

**Diagram, schematic

Description automatically generated**

**PART B (XOR using NAND Gates)**

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**A screenshot of a computer

Description automatically generated with medium confidence**

**Voltage vs Time(Fall = 49 ps, Rise 21ps)**

**Diagram

Description automatically generated with medium confidence**

**PART CBONUS**

**The fall time is much slower than the rise time because the fall time primarily depends on the NMOS and the rise time primarily depends on the PMOS. Since there are more PMOS in parallel, then the on time is much greater because the currents add in parallel. On the other hand, the NMOS are in series so the on time of the NMOS is almost the same since the currents of transistors in series are equivalent and don’t add. So the more NAND gates, the faster the on time for the PMOS which causes the rise time to be faster.**

**Using current formula I = C\*(dv/dt) => dt = C\*(dv)/I**

**Once we reorganize the current formula, if current is big then the delay time is smaller and if current is small then the delay time is larger.**

**Substituting numbers,**

**A NMOS has 0.00095 A while the PMOS in this circuit has a combined 0.0014 A. All in all, the PMOS in this circuit has a larger current causing the delay time of the rise to be smaller or faster.**