Heaven's Light is Our Guide

Rajshahi University of Engineering and Technology

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ECE 4128

Course Title
VLSI Design

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Lab Report 1:
Implementation of CMOS Inverter.

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Implementation of CMOS Inverter.

Theory

A CMOS inverter is a fundamental building block in digital logic, consisting of a PMOS and an NMOS transistor connected in a complementary arrangement [1]. The PMOS transistor is linked to the supply voltage (VDD), while the NMOS is connected to ground. Both transistors share the same input signal (Vin), and the output is taken from the junction between them. When the input is low (logic 0), the PMOS conducts and the NMOS is off, resulting in a high output (logic 1). Conversely, when the input is high (logic 1), the NMOS turns on, the PMOS switches off, and the output drops to logic 0. This complementary switching greatly reduces static power consumption, making CMOS technology highly energy efficient [2].

An important dynamic property of CMOS inverters is the transition time, which includes rise time (tr) and fall time (tf). These times indicate how quickly the output voltage responds to changes in the input. Rise time refers to the interval during which the output increases from about 10% to 90% of VDD, while fall time measures the decrease from 90% to 10% of VDD. The speed of these transitions is crucial for high-speed digital circuits [3].

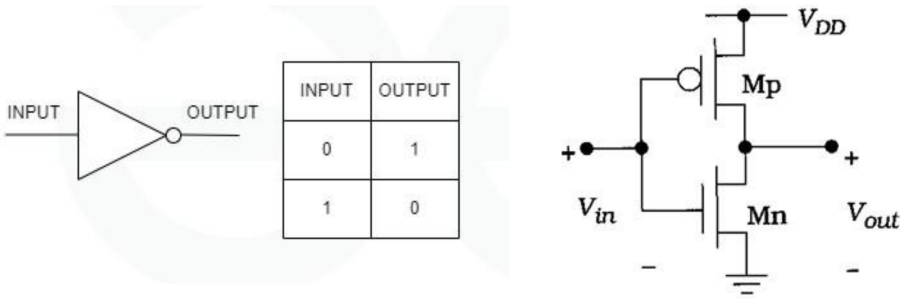

Figure 1: Block diagram of a CMOS inverter circuit.[4]

The rise and fall times of a CMOS inverter depend on the output load capacitance (C_{out}) and the aspect ratios (W/L) of the transistors. Because PMOS transistors have lower carrier mobility (μ_p) than NMOS transistors (μ_n), the PMOS is usually

made wider—often about twice the width of the NMOS—to equalize the speeds of the rising and falling edges [1]. This matching is achieved when:

$$\frac{W_1}{L_1}\mu_n = \frac{W_2}{L_2}\mu_p$$

where T_1 is the NMOS and T_2 is the PMOS. This relationship helps ensure that the inverter switches symmetrically.

The propagation delay due to the output capacitance can be approximated by:

$$t_r \approx 35 \cdot \frac{C_{out}}{W_1/L_1} \text{ ns}$$

where C_{out} is in picofarads and W_1/L_1 is the NMOS aspect ratio. This means that larger output capacitance or smaller transistor sizes result in slower signal transitions [2].

Required Tools

- Microwind
- MS Word
- LaTeX

Circuit Schematic

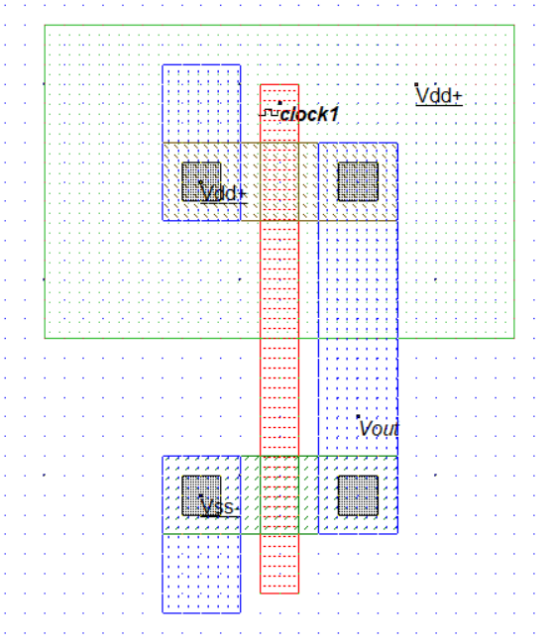

Figure 2: CMOS Inverter Schematic without Load Capacitor

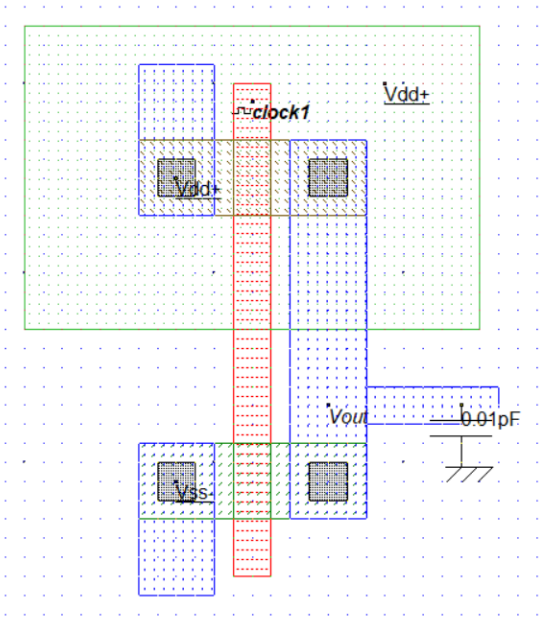

Figure 3: CMOS Inverter Schematic with Load Capacitor

Output

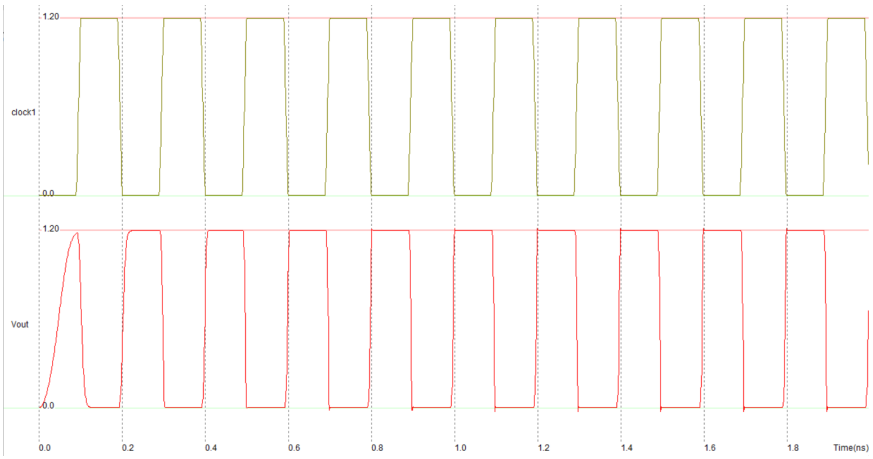

Figure 4: Plot of voltage over time without a capacitor.

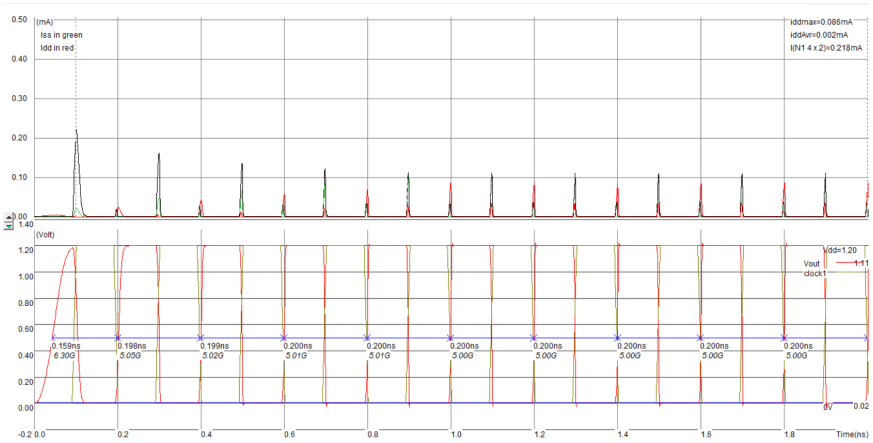

Figure 5: Plot of voltage versus current without a capacitor.

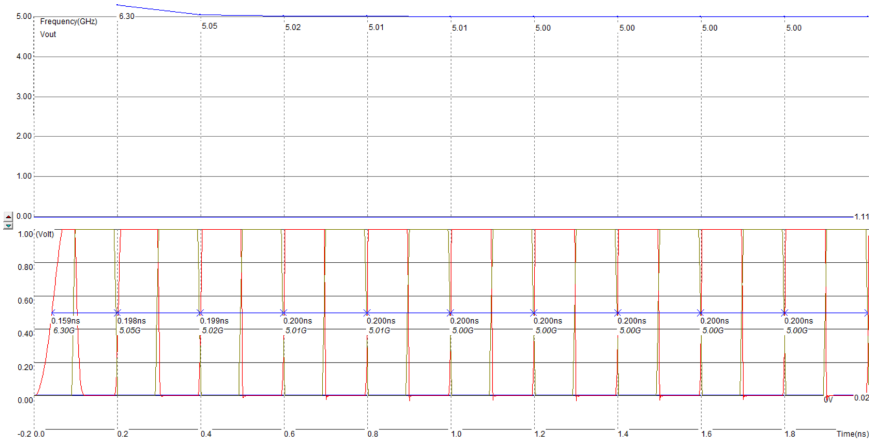

Figure 6: Plot of frequency over time without a capacitor.

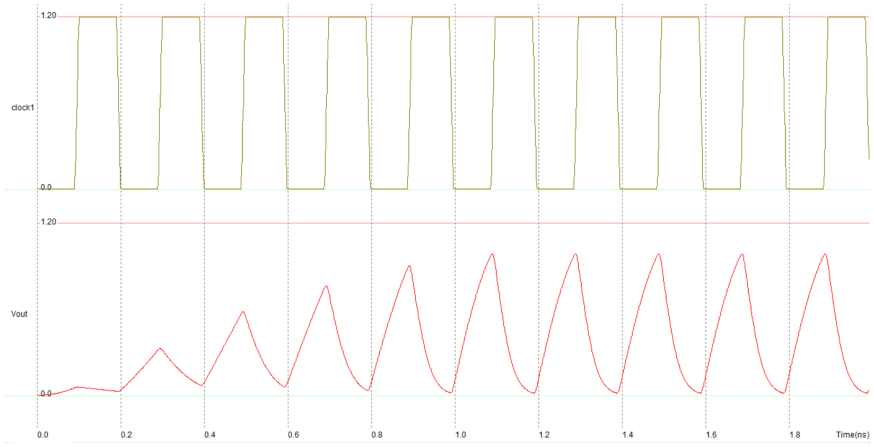

Figure 7: Plot of voltage over time with a capacitor.

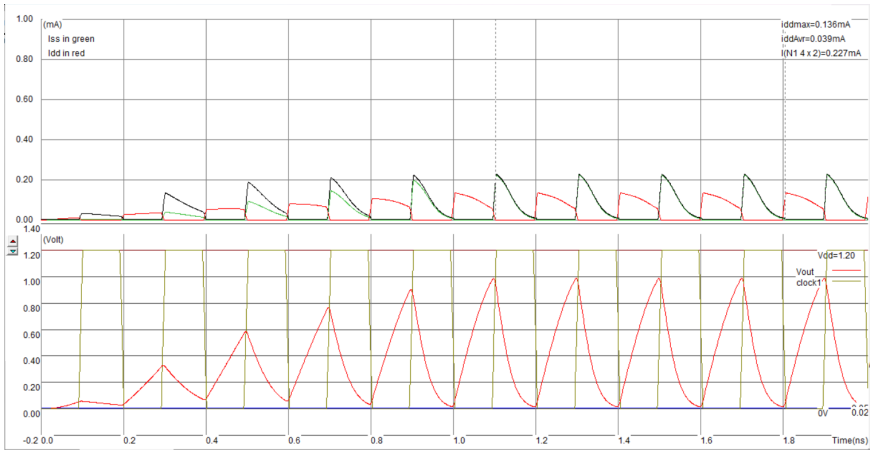

Figure 8: Plot of voltage versus current with a capacitor.

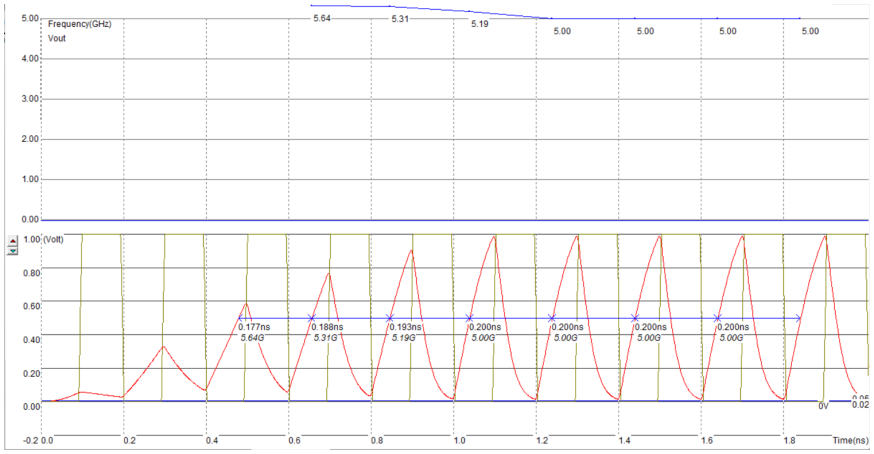

Figure 9: Plot of frequency over time with a capacitor.

Discussion and Conclusion

This experiment involved designing and simulating a CMOS inverter in Microwind to analyze its switching behavior with a clocked input cycling between 0 V and 1.2 V. The simulation results verified the inverter's basic function: the output reliably inverted the input signal. Various waveforms—including voltage versus time, current versus voltage, and frequency versus time—were examined for both unloaded and loaded output conditions.

Adding a load capacitor highlighted the rise and fall times, which stem from the charging and discharging of the output node, consistent with the relation $t_r = 35 \cdot C_{out}$ ns. In the absence of the capacitor, transitions appeared sharp and nearly ideal; with the capacitor, minor delays and current peaks were observed. These effects reflect fundamental CMOS principles, notably the impact of load capacitance and the necessity of balancing transistor dimensions to offset PMOS and NMOS mobility differences. Adjusting the aspect ratios achieved more symmetrical signal edges, enhancing timing characteristics.

In summary, the study confirmed theoretical expectations and practical behavior of CMOS inverters. It demonstrated that dynamic factors—such as output capacitance, transistor sizing, and carrier mobility—significantly influence propagation delay, switching speed, and power consumption. The findings reinforced the importance of careful design choices for efficient and robust VLSI circuits.

References

[1] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Prentice Hall, 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. McGraw-Hill, 2003.

[3] N. H. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed. Pearson, 2015.

[4] GeeksforGeeks, "CMOS Inverter," *GeeksforGeeks*, Jul. 2025. [Online]. Available: https://www.geeksforgeeks.org/electronics-engineering/cmos-inverter