Heaven's Light is Our Guide

Rajshahi University of Engineering and Technology

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Lab Report 3:
Implementation NAND Gate and NOR Gate Using CMOS

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Implementation NAND Gate and NOR Gate Using CMOS

Theory

Logic gates are fundamental components in digital electronics, enabling the implementation of arithmetic, memory, and control operations within integrated circuits [1]. NAND and NOR gates are particularly important because they are universal gates—meaning any logic function (such as AND, OR, NOT, XOR) can be constructed using only NAND or NOR gates [2]. As a result, understanding the design and operation of CMOS NAND and NOR gates is essential for grasping the foundations of digital VLSI (Very Large Scale Integration) systems [3].

CMOS Technology Overview

CMOS (Complementary Metal-Oxide-Semiconductor) is the predominant technology for digital circuit design, valued for its low power consumption and scalability [1]. CMOS circuits utilize both PMOS and NMOS transistors in a complementary configuration. The structure consists of a pull-up network (PUN) made of PMOS transistors connected to the supply voltage (VDD) and a pull-down network (PDN) of NMOS transistors connected to ground [3]. Inputs are applied to both networks, and the output is taken from their shared node. This arrangement ensures that, ideally, only one network conducts at a time, minimizing static power usage and producing sharp logic transitions.

CMOS NAND Gate

A CMOS NAND gate features two PMOS transistors in parallel for the pull-up network and two NMOS transistors in series for the pull-down network [1]. Its operation is as follows:

- When both inputs are high (logic 1), both NMOS transistors conduct, creating a low-resistance path to ground and pulling the output to logic 0.
- For any other input combination (00, 01, or 10), at least one PMOS transistor conducts in the parallel pull-up network, pulling the output to logic 1.

This configuration matches the NAND gate truth table, with the parallel PMOS arrangement ensuring a strong pull-up except when both inputs are high.

CMOS NOR Gate

The CMOS NOR gate is the logical counterpart to the NAND gate. It uses two PMOS transistors in series for the pull-up network and two NMOS transistors in parallel for the pull-down network [3]. Its operation is:

- When both inputs are low (logic 0), both PMOS transistors conduct, providing a path from VDD to the output and driving it to logic 1.
- For all other input combinations (01, 10, or 11), at least one NMOS transistor conducts in the parallel pull-down network, pulling the output to logic 0.

This setup produces the NOR gate truth table, where the output is high only when both inputs are low.

Advantages of CMOS NAND and NOR Gates

CMOS implementations of NAND and NOR gates offer several benefits. The complementary design results in minimal static power dissipation, as there is no direct path from VDD to ground except during switching [2]. CMOS gates also provide high noise immunity, sharp switching thresholds, and are easily scalable with modern fabrication techniques [1]. Their universality makes NAND and NOR gates essential building blocks for more complex logic circuits, underscoring their importance in VLSI and digital system design [3].

Required Tools

- Microwind
- MS Word
- LaTeX

Circuit Schematic

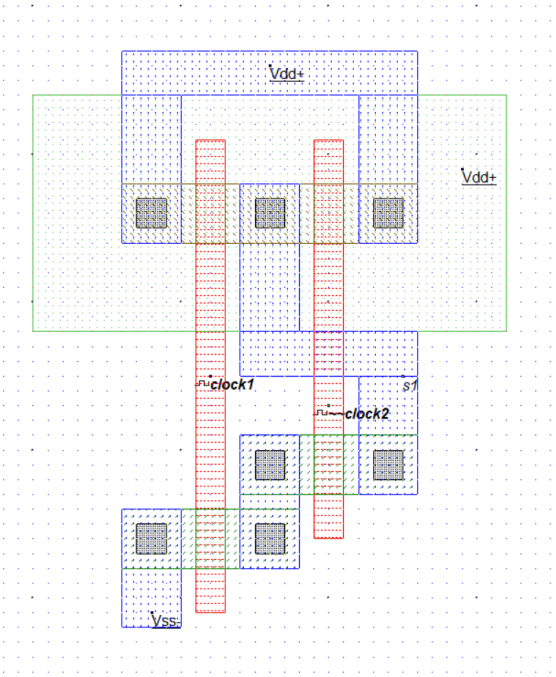

Figure 1: CMOS NAND Gate Schematic

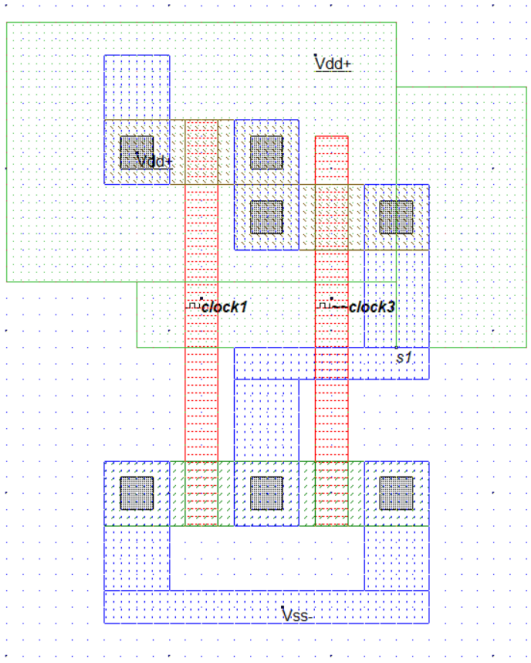

Figure 2: CMOS NOR Gate Schematic

Output

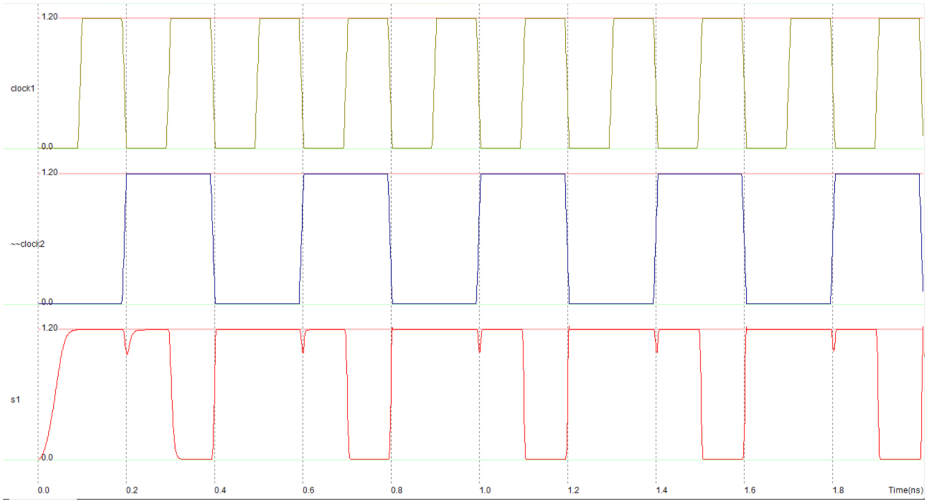

Figure 3: Output Waveform of CMOS NAND Gate

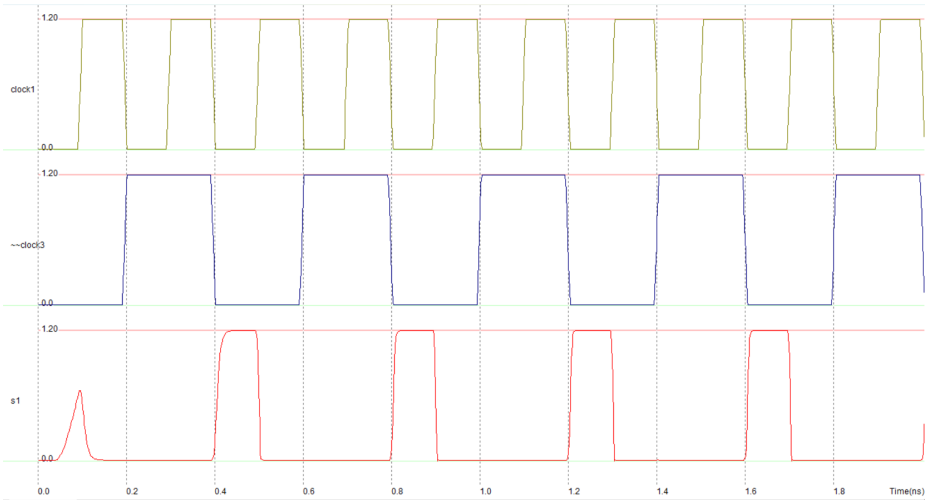

Figure 4: Output Waveform of CMOS NOR Gate

Output Analysis

NOR Gate:
The output signal `s1` is high only when both `clock1` and `clock3` are at logic 0. If either input is at logic 1, `s1` transitions low, which is consistent with the NOR gate truth table. The waveform segments correspond to the following input combinations:

- (0,0): `s1` = 1
- (1,0), (0,1), (1,1): `s1` = 0

NAND Gate:
The output `s1` is low only when both `clock1` and `clock2` are at logic 1. For all other input combinations, `s1` remains high, matching the NAND gate truth table. The waveform mapping is as follows:

- (1,1): `s1` = 0
- (0,0), (0,1), (1,0): `s1` = 1

Discussion and Conclusion

In this experiment, CMOS NAND and NOR gates were implemented and simulated to observe their logical behavior. The simulation results aligned with the theoretical truth tables: the NAND gate produced a low output only when both inputs were high, and the NOR gate generated a high output only when both inputs were low. These outcomes verified the correct functioning of the complementary pull-up and pull-down networks in CMOS logic circuits.

The simulation further demonstrated the efficiency of CMOS technology. Static power dissipation was minimal, as only one network (either pull-up or pull-down) was active

at any given time, with transient power consumption occurring during input transitions. The configuration of PMOS and NMOS transistors—whether in series or parallel—determined both the logic operation and the robustness of output transitions.

In summary, the experiment confirmed the theoretical foundations of CMOS logic design, highlighting its advantages in low power consumption, noise immunity, and scalability. It also underscored the significance of NAND and NOR gates as universal elements for constructing complex digital systems.

References

[1] N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed. Pearson, 2015.

[2] R. K. Manohar, *Digital Logic Design.* Oxford University Press, 2017.

[3] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 4th ed. McGraw-Hill Education, 2019.