Heaven's Light is Our Guide

Rajshahi University of Engineering and Technology

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VLSI Design Sessional

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Lab Report 4:
Design and Observe the Characteristics Curve of CMOS Circuit

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Design and Observe the Characteristics Curve of CMOS Circuit

Task

Design and observe the characteristics curve of CMOS circuits using the following equations:

1. **Equation I:** $Y = \overline{(A + B) \cdot C}$
2. **Equation II:** $Y = A\overline{B} + ABC$

For each equation:

- Design the corresponding CMOS logic gate schematic.
- Simulate the circuit to obtain the output characteristics curve.
- Analyze the output waveform and discuss the behavior of the circuit.

Theory

Complex CMOS logic gates implement Boolean functions in a single stage, offering greater efficiency compared to constructing the same function from multiple NAND or NOR gates [1]. These gates are composed of a pull-up network (PUN) using PMOS transistors and a pull-down network (PDN) using NMOS transistors. The PDN provides a path to ground (V_{SS}) when the output should be logic '0', while the PUN connects the output to the supply voltage (V_{DD}) when the output should be logic '1'. The PUN is the logical dual of the PDN, meaning series connections in one correspond to parallel connections in the other [2].

Equation I: $Y = \overline{(A + B) \cdot C}$ This equation describes a 2-1 AND-OR-Invert (AOI21) gate [1].

- The pull-down network implements the logic $(A + B) \cdot C$, which consists of two parallel NMOS transistors (for A and B) in series with a third NMOS transistor (for C) [2].

- The complementary pull-up network implements $(\overline{A} \cdot \overline{B}) + \overline{C}$, realized by two series PMOS transistors (for A and B) in parallel with a third PMOS transistor (for C) [1].

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Table 1: Truth Table for $Y = \overline{(A + B) \cdot C}$

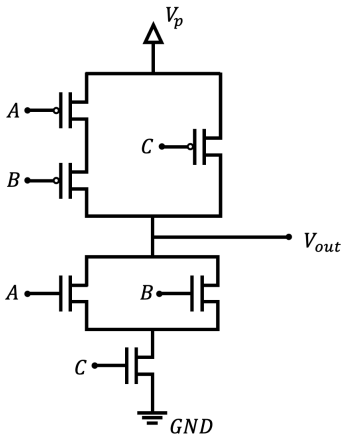

Figure 1: Connection diagram of the CMOS circuit for $Y = \overline{(A + B) \cdot C}$

Equation II: $Y = A\overline{B} + ABC$

- The pull-down network (PDN) implements the logic for (after simplification) $\overline{A} + B\overline{C}$. This requires one NMOS transistor for $\overline{A}$ (A input inverted), and a branch with NMOS transistors for $B\overline{C}$ (B in series with C inverted), both branches connected in parallel [1, 2].
- The pull-up network (PUN) implements the dual logic, which for $Y = A\overline{B} + ABC$ is $A(\overline{B} + C)$. This is realized by two PMOS transistors for B and C in parallel, both in series with a PMOS transistor for A [1].
- The circuit implements the function $Y = \overline{A} + B\overline{C}$, which can be realized efficiently using CMOS logic [2].

Table 2: Truth Table for $Y = A\overline{B} + ABC$

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

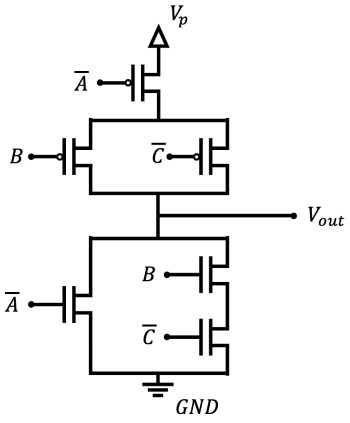

Figure 2: Connection diagram of the CMOS circuit for $Y = A\overline{B} + ABC$

Used Tools

- Microwind
- MS Word
- MS PowerPoint
- LaTeX

Circuit Schematic in Microwind

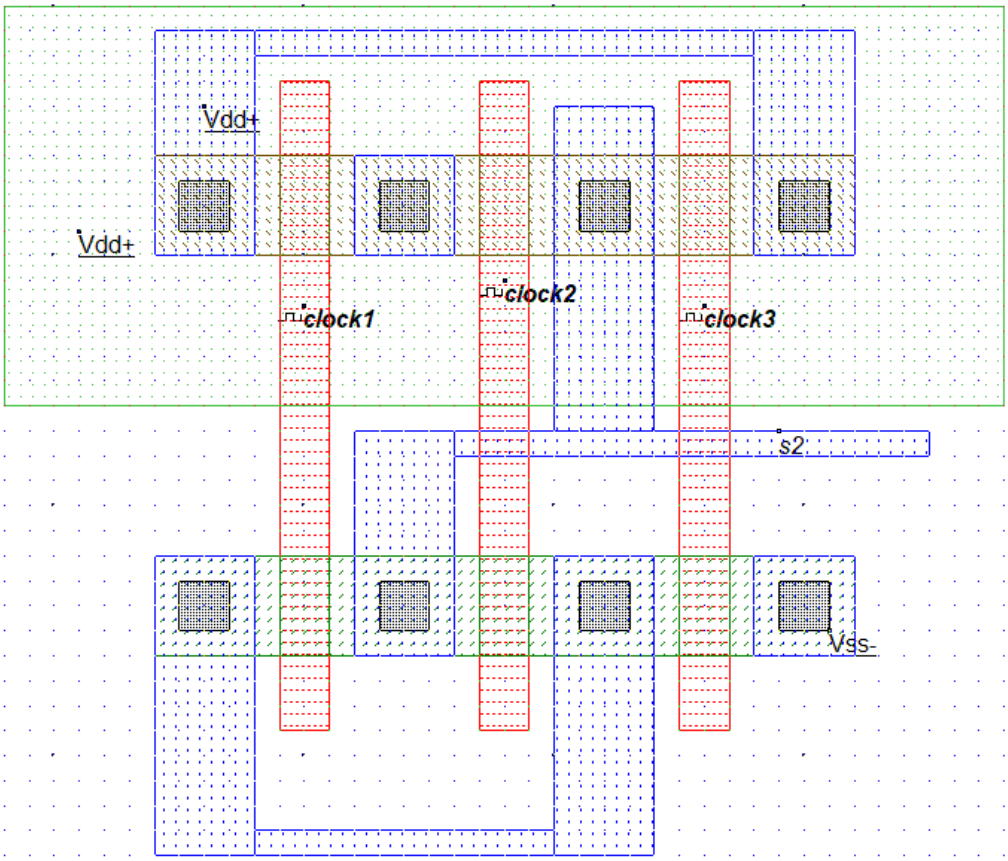

Figure 3: Connection diagram of the CMOS circuit for $Y = \overline{(A + B) \cdot C}$

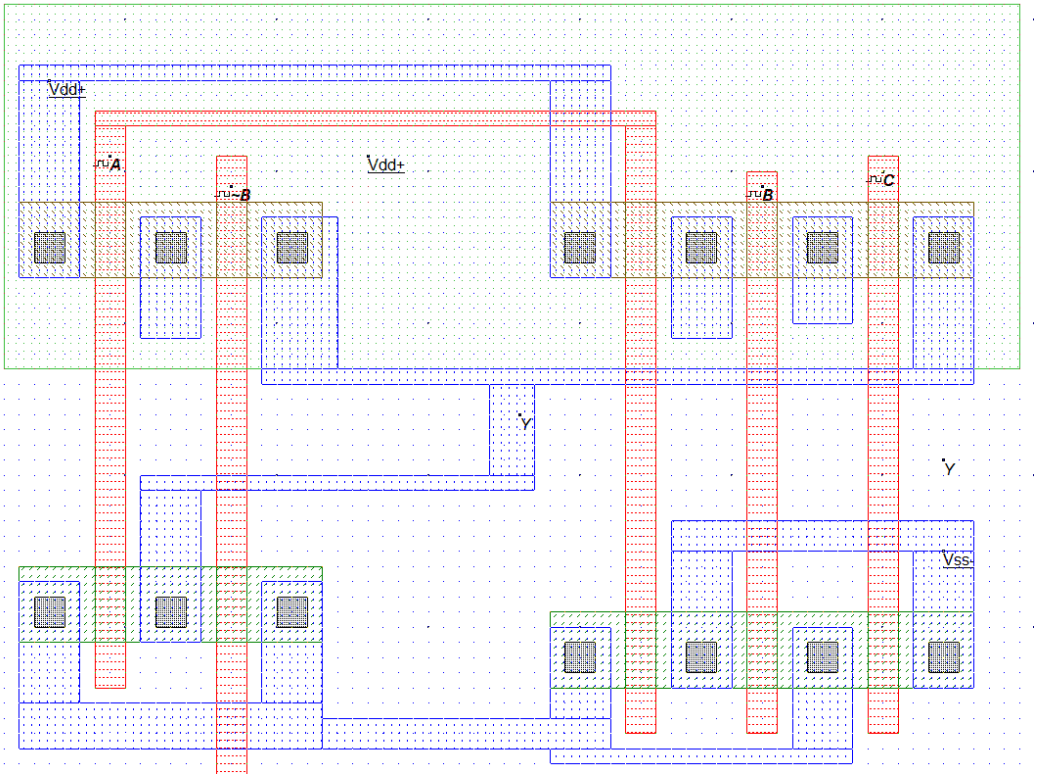

Figure 4: Connection diagram of the CMOS circuit for $Y = A\overline{B} + ABC$

Output

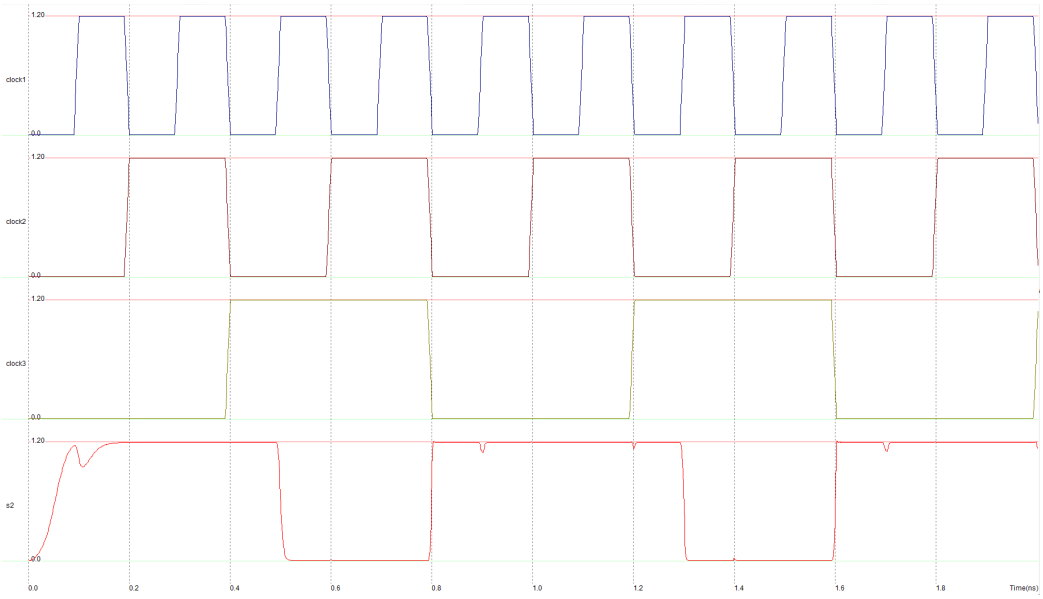

Figure 5: Output Waveform of $Y = \overline{(A + B) \cdot C}$

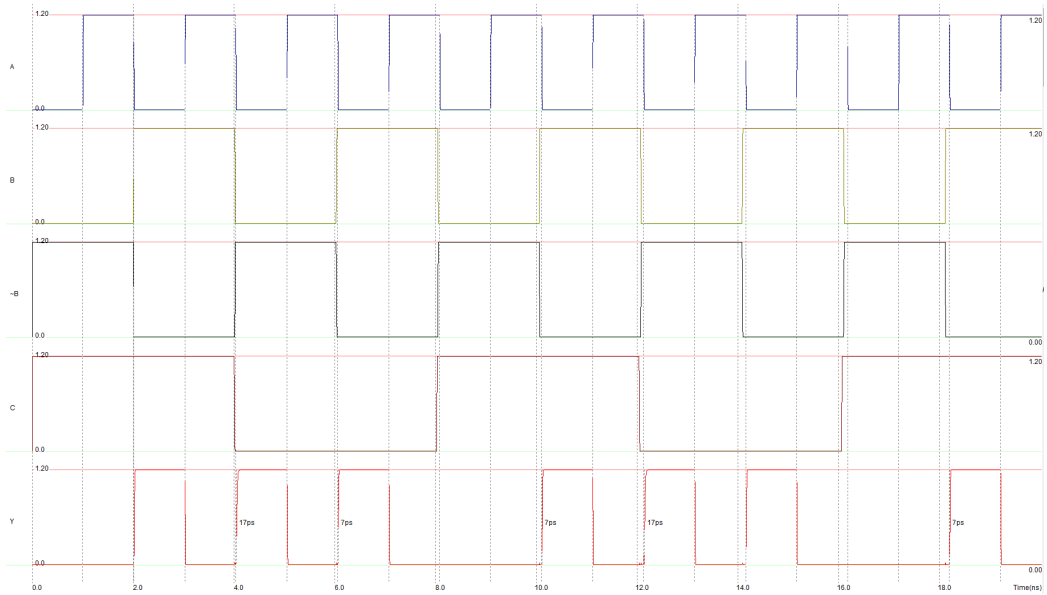

Figure 6: Output Waveform of $Y = A\overline{B} + ABC$

Output Analysis

The complex CMOS circuits were implemented and simulated using Microwind. The resulting output waveforms align with the expected logical behavior as defined by the truth tables for each equation.

Case I: $Y = \overline{(A + B) \cdot C}$

- When $C = 0$, the output remains HIGH (1) for all values of A and B.
- When $C = 1$ and either $A = 1$ or $B = 1$, the output switches to LOW (0).
- When $C = 1$ and both $A = 0$ and $B = 0$, the output is HIGH (1).
- Simulation results confirm that the output is LOW only for input combinations (A,B,C) of (0,1,1), (1,0,1), and (1,1,1), consistent with the truth table.

Case II: $Y = A\overline{B} + ABC$

- When $A = 1$ and $B = 0$, the output is HIGH (1), regardless of C.
- When $A = 1$, $B = 1$, and $C = 1$, the output is HIGH (1).
- For all other input combinations, the output remains LOW (0).
- The simulation confirms that the output is HIGH only for (A,B,C) values of (1,0,0), (1,0,1), and (1,1,1), matching the truth table.

Discussion

This experiment explored the design and simulation of complex CMOS logic gates at the transistor level. By creating complementary pull-up (PMOS) and pull-down (NMOS) networks, complex Boolean functions such as AOI and OAI can be implemented in a single logic stage. This method is typically more efficient and faster than building the same function from multiple universal gates like NAND or NOR. The simulated output waveforms in Microwind closely matched the expected results from the truth tables, confirming both the dynamic and static behavior of the circuits.

Conclusion

To summarize, the experiment confirmed the correct operation of complex CMOS circuits for the specified Boolean equations using Microwind. The observed results validated the design approach of using complementary pull-up and pull-down networks. This reinforces that complex logic functions can be directly and efficiently realized in CMOS technology, which is essential for integrated circuit design.

References

[1] N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed. Pearson, 2010.

[2] J. M. Rabaey, A. Chandrakasan, and B. Nikolić, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Prentice Hall, 2003.