Heaven's Light is Our Guide

Rajshahi University of Engineering and Technology

Course Code
ECE 4128

Course Title
VLSI Design

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Lab Report 2:
Implementation of NMOS Ratio-less Inverter.

Submitted to	**Submitted by**
Moloy Kumar Ghosh Lecturer Dept of ECE, RUET & Md. Faysal Ahamed Lecturer Dept of ECE, RUET	Md. Tajim An Noor Roll: 2010025

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Implementation of NMOS Ratio-less Inverter

Theory

An inverter is a fundamental digital logic gate that outputs the logical opposite of its input [1]. In transistor-based designs, inverters can be constructed using CMOS technology, which combines PMOS and NMOS transistors, or using NMOS-only approaches [2]. In NMOS logic, both the pull-up and pull-down networks utilize NMOS transistors. Traditionally, a load resistor connects the supply voltage (VDD) to the output node, while an NMOS transistor pulls the output to ground. However, physical resistors are inefficient in terms of area and speed for integrated circuits, especially as circuit complexity increases [3].

To address these limitations, active load NMOS transistors can replace the resistor, resulting in a ratio-less inverter design [4]. This configuration, known as the 3-NMOS ratio-less inverter, uses three NMOS transistors: one as the main driver and two as active loads. The driver transistor receives the input signal at its gate and connects its source to ground. The active load transistors are placed between VDD and the output node, with their gates biased to remain partially on, acting as constant current sources. This approach simplifies fabrication in NMOS technology and eliminates the need for precise transistor sizing ratios, making it suitable for large-scale integration [2].

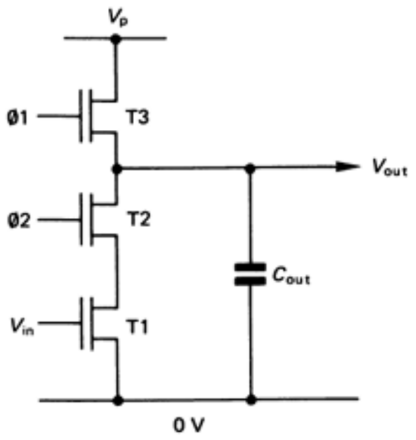

Figure 1: Schematic diagram of the NMOS ratio-less inverter

Operation

1. **Input Low (Logic 0):** When the input is at logic 0, transistor T1 remains OFF. The active load transistors (T2 and T3) conduct sufficient current to raise the output voltage to logic 1.
2. **Input High (Logic 1):** When the input switches to logic 1, T1 turns ON, creating a low-resistance path from the output node to ground. This pulls the output down to logic 0. The active load transistors continue to conduct a small amount of current, resulting in static power consumption.

Required Tools

- Microwind
- MS Word
- LaTeX

Circuit Schematic

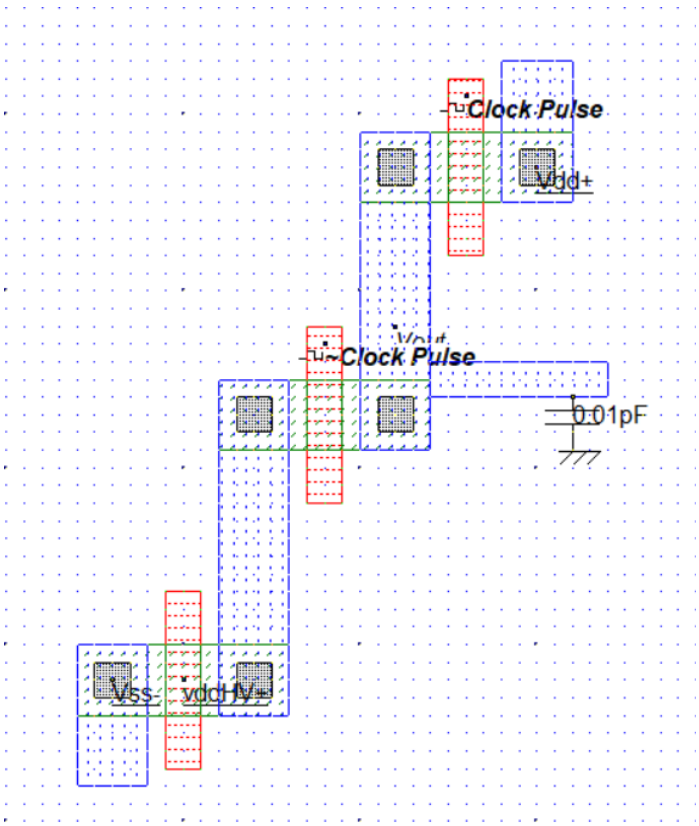

Figure 2: Schematic of the NMOS ratio-less inverter circuit

Output

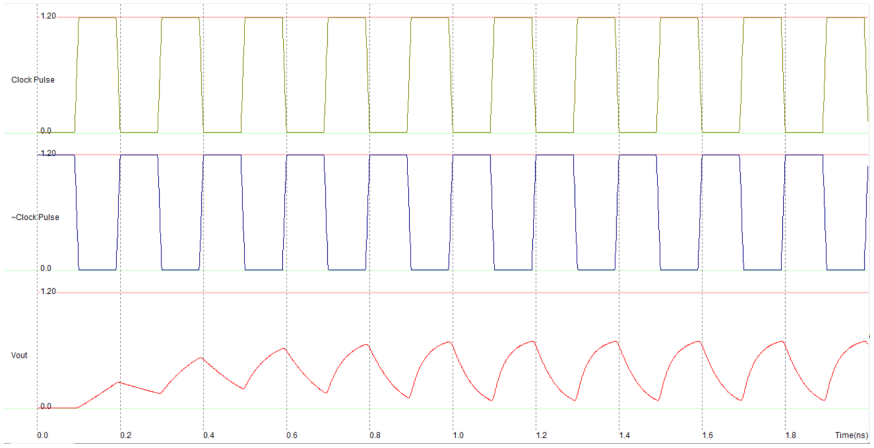

Figure 3: Time-domain voltage response for $V_in = 1$V.

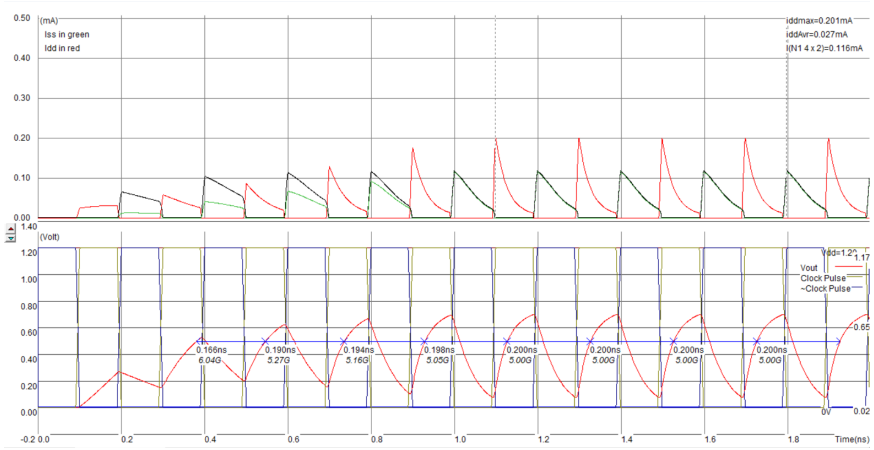

Figure 4: Current-voltage characteristics for $V_in = 1$V.

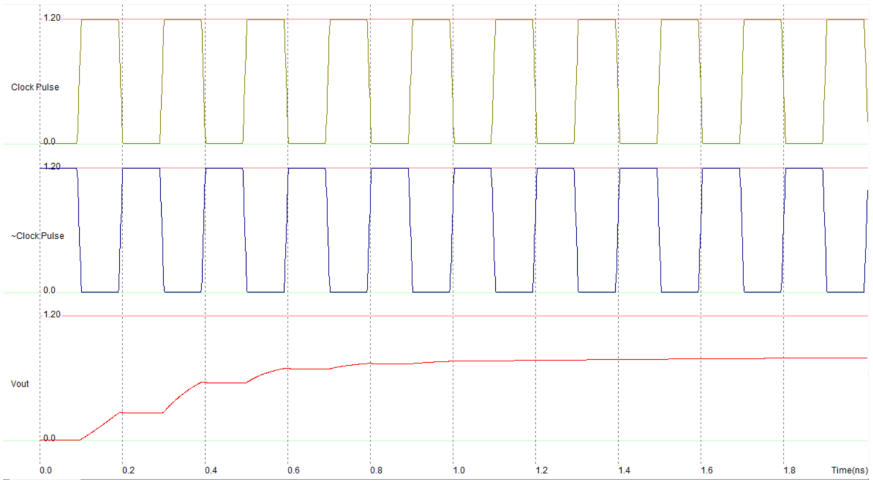

Figure 5: Time-domain voltage response for $V_in = 0$V.

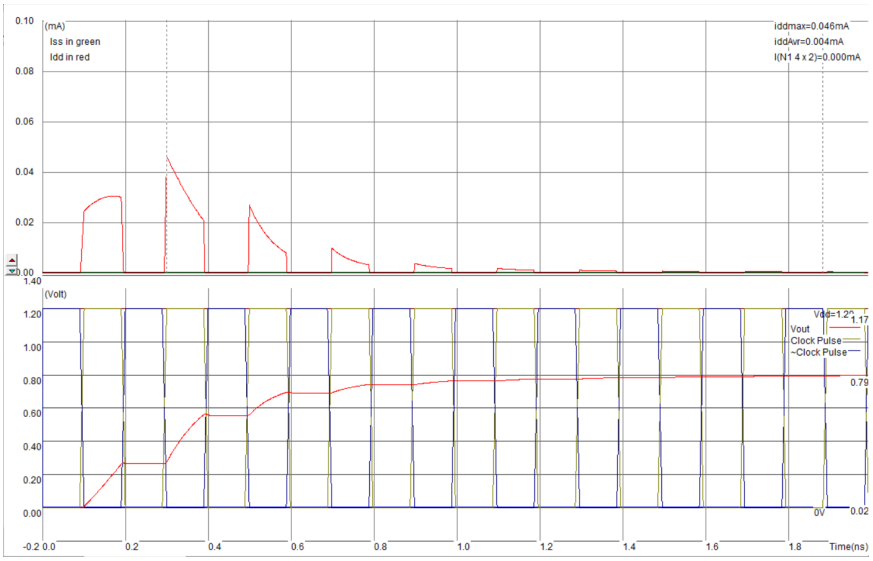

Figure 6: Current-voltage characteristics for $V_in = 0$V.

Discussion and Conclusion

In this experiment, a 3-NMOS ratio-less inverter was designed and simulated to analyze its switching characteristics and overall performance. The circuit consisted of one NMOS driver transistor and two NMOS active load transistors, removing the need for resistors. Simulations verified that the output was the logical inverse of the input: when the input was low, the active loads pulled the output high; when the input was high, the driver transistor pulled the output low.

The results indicated that the rise time was slower than the fall time, attributed to the weaker pull-up capability of the active loads. Additionally, static power dissipation was observed during the low output state due to continuous current flow. These

outcomes are consistent with theoretical expectations, demonstrating how transistor biasing and active load design influence switching speed, delay, and power consumption.

A key observation was that the inverter's switching threshold did not depend on transistor sizing ratios, which is a defining feature of ratio-less designs. Eliminating resistors makes the design more compatible with NMOS IC fabrication. Overall, this study reinforced important concepts in transistor operation, active loading, and the trade-offs between speed, power, and simplicity, providing valuable insights for VLSI design.

References

[1] N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed. Pearson, 2015.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. McGraw-Hill, 2003.

[3] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Wiley, 2008.

[4] J. M. Rabaey, A. Chandrakasan, and B. Nikolić, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Prentice Hall, 2003.