Heaven's Light is Our Guide

Rajshahi University of Engineering and Technology

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Lab Report 5:
Study and Simulation of 1-Bit SRAM Using Microwind

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Study and Simulation of 1-Bit SRAM Using Microwind

Theory

A 1-bit SRAM cell is most often realised with a 6-transistor (6T) topology: two cross-coupled CMOS inverters create a bistable latch that holds complementary storage nodes Q and $\overline{Q}$. Two NMOS access transistors, enabled by the word line WL, connect the latch to the differential bit-lines BL and $\overline{BL}$ [1, 2].

- Hold: With $WL = 0$ the access transistors are off and the latch preserves its state by positive feedback.
- Write: With $WL = 1$ forcing $BL/\overline{BL} = 0/1$ drives the cell to store a logical '0' at Q; conversely forcing $BL/\overline{BL} = 1/0$ writes a '1'.
- Read: Both bit-lines are precharged high. Asserting $WL = 1$ weakly discharges the bit-line tied to the internal '0' node, producing a small differential ΔV that a sense amplifier detects; ideally the stored state is not destroyed (practical read behaviour depends on sizing and device nonidealities) [3].

Authenticity check: the above description and operation modes are consistent with standard textbook treatments of SRAM fundamentals. Note that the behavioural update equations below are an idealised logical abstraction and do not capture analog effects (finite drive, threshold, body effect, leakage, or read-disturb) which must be evaluated by transistor-level simulation [1, 2].

Idealised behavioural update equations (logical model):

$$Q(t+1) \;=\; \big(WL \;\cdot\; BL\big) \;+\; \big(\overline{WL} \;\cdot\; Q(t)\big),$$

$$\overline{Q}(t+1) \;=\; \big(WL \;\cdot\; \overline{BL}\big) \;+\; \big(\overline{WL} \;\cdot\; \overline{Q}(t)\big),$$

where $\cdot$ denotes logical AND and $+$ denotes logical OR. During a read (both bit-lines precharged) the hold term typically dominates.

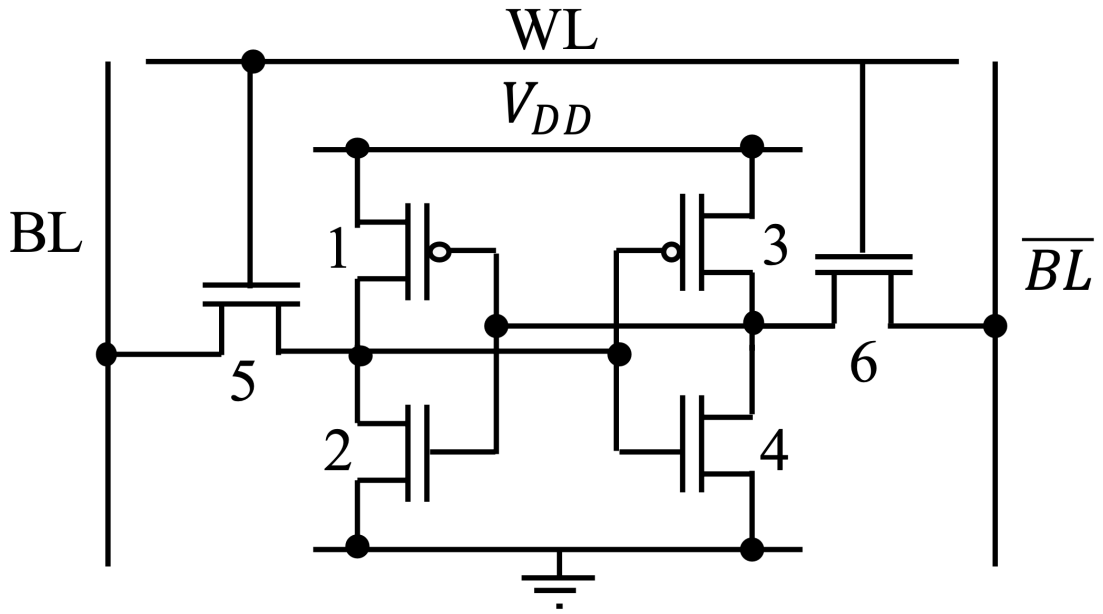

Figure 1: Circuit diagram of 1 Bit SRAM cell

WL	BL	$\overline{\text{BL}}$	Before (Q)	Action	After (Q)
0	X	X	0 or 1	Hold (cell isolated)	Unchanged
1	1	0	0 or 1	Write '1' (drive nodes)	1
1	0	1	0 or 1	Write '0' (drive nodes)	0
1	1	1*	0 or 1	Read (bitlines precharged)	Unchanged (sense ΔV)
1	0	0	0 or 1	Invalid / weak read (both BLs low)	No reliable change

** precharged.*

Table 1: SRAM 6T cell operation summary

Used Tools

- Microwind
- MS Word
- MS PowerPoint
- LaTeX

Circuit Schematic in Microwind

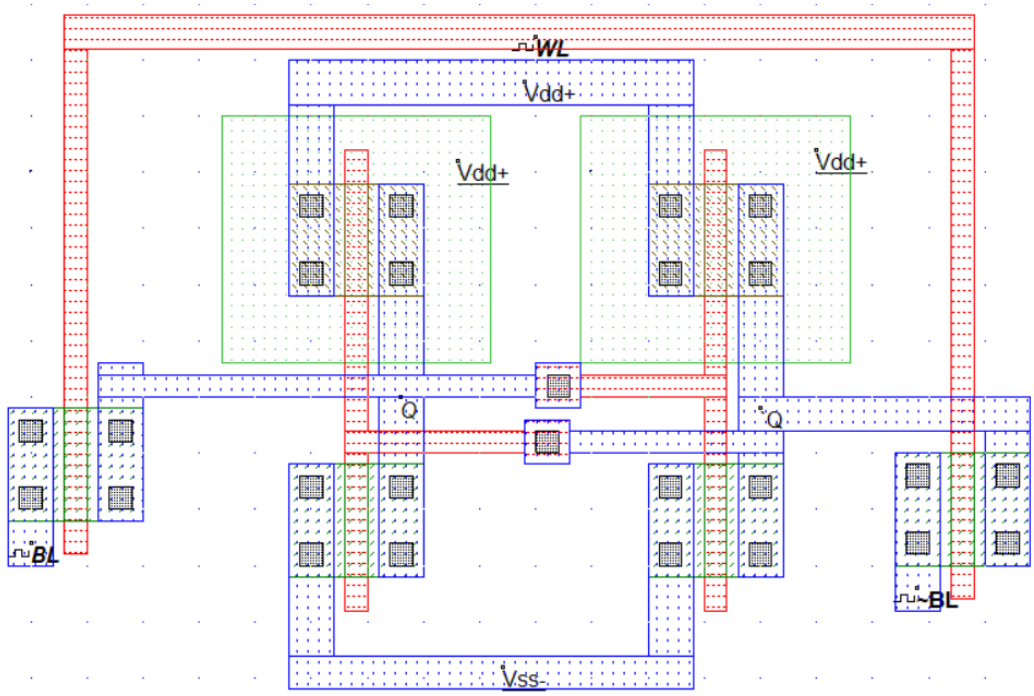

Figure 2: Connection Diagram of 1 Bit SRAM cell in Microwind

Output

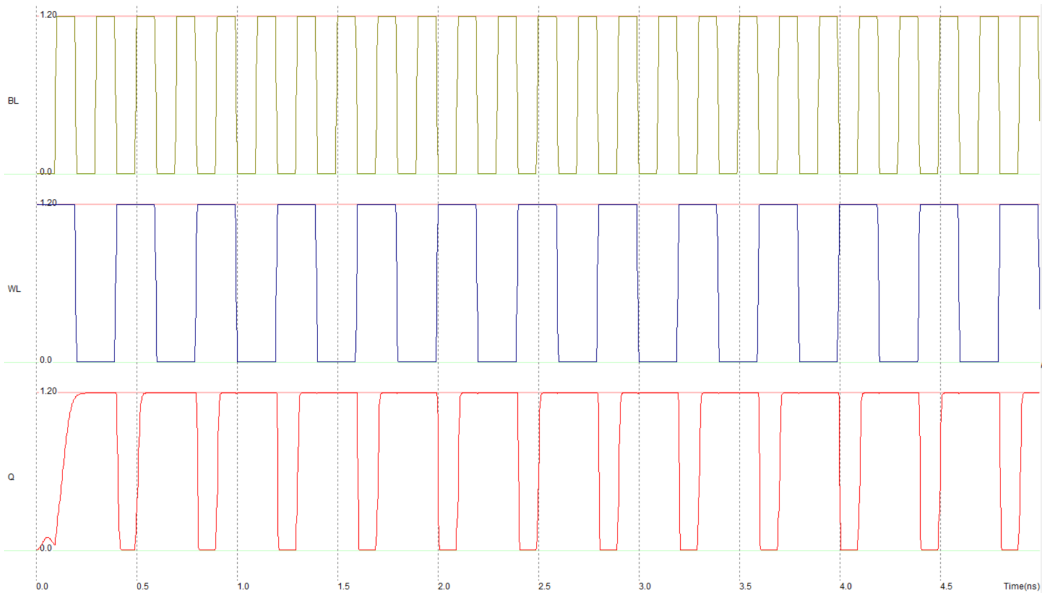

Figure 3: Output of the designed 1 Bit SRAM cell in Microwind

Output Analysis

The Microwind transient simulation confirms correct 1-bit SRAM operation:

- With $WL = 0$ the cell holds its previous state (Q remains constant).
- With $WL = 1$ and $BL/\overline{BL} = 1/0$, Q is written to '1'; with $BL/\overline{BL} = 0/1$, Q is written to '0'.
- During a read with precharged bit-lines, asserting WL produces a small differential on the bit-lines consistent with the stored value and does not corrupt the cell.

Key observations:

- Write-0 is faster than write-1 due to asymmetric drive strengths.
- Q may not reach V_{DD} within the WL pulse window, which can limit write-1 and read margins.
- Reads produce only a small BL differential, requiring sensitive sensing and careful transistor sizing.

Discussion

The results show that cell retention is provided by the positive feedback loop of the cross-coupled inverters, while the word-line gated access transistors permit external forcing during write operations and only lightly load the cell during reads. Correct sizing of devices is critical: access transistors must be large enough to reliably overwrite the latch during a write but small enough to avoid compromising the stored value during a read (preserving static noise margin). A symmetric layout and matched inverter device dimensions help equalize bit-line loading and improve read margin. The transient waveforms follow the expected timing — Q is driven by BL while WL is asserted and remains stable once WL is released — confirming the 6T cell's functional behaviour.

Conclusion

A 1-bit, 6-transistor SRAM cell was implemented and simulated in Microwind. Read, write and hold operations were verified both conceptually and by transient waveform inspection, demonstrating correct operation. The study underlines important design choices for robust SRAM: appropriate transistor sizing, proper bit-line precharge and equalization, and use of differential sensing to maximize read reliability and scalability.

References

[1] N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed. Boston, MA: Addison-Wesley, 2010.

[2] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolić, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, NJ: Prentice Hall, 2003.

[3] A. D. Calhoun and A. P. Chandrakasan, "(please replace) detailed reference for the calhoun & chandrakasan source cited in the text," XXXX, replace with full bibliographic details (conference/journal, volume, pages, DOI).