Heaven's Light is Our Guide

Rajshahi University of Engineering and Technology

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Lab Report 6:
Implementation of Half Adder Circuit Using CMOS in Microwind

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Implementation of Half Adder Circuit Using CMOS in Microwind

Theory

A half adder is a combinational logic circuit that adds two single-bit binary numbers A and B and produces two outputs: Sum (S) and Carry (C). It performs the least-significant-bit addition without an incoming carry. The signals have the following meanings:

- A, B: single-bit binary inputs to be added.
- Sum (S): the least-significant bit of the addition result.
- Carry (C): the carry-out bit (1 if the sum exceeds 1 and must be carried to the next higher bit).

The half-adder logic and practical CMOS realizations are discussed in standard texts on digital and VLSI design[1, 2, 3].

Boolean expressions

$$S = A \oplus B = A\overline{B} + \overline{A}B$$

$$C = A \cdot B$$

These expressions and their transistor-level mappings (XOR implemented via complementary networks or transmission gates, AND via NAND+inverter or static AND) are treated in detail in the cited books[2, 1].

A	B	Sum (S)	Carry (C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth table of Half Adder (definition after [3])

Logic (gate-level) circuit:

- Sum: XOR gate taking inputs A and B.
- Carry: AND gate taking inputs A and B.

Both inputs A and B feed the XOR (for S) and the AND (for C) so the block diagram is the two inputs branching to these two gates.

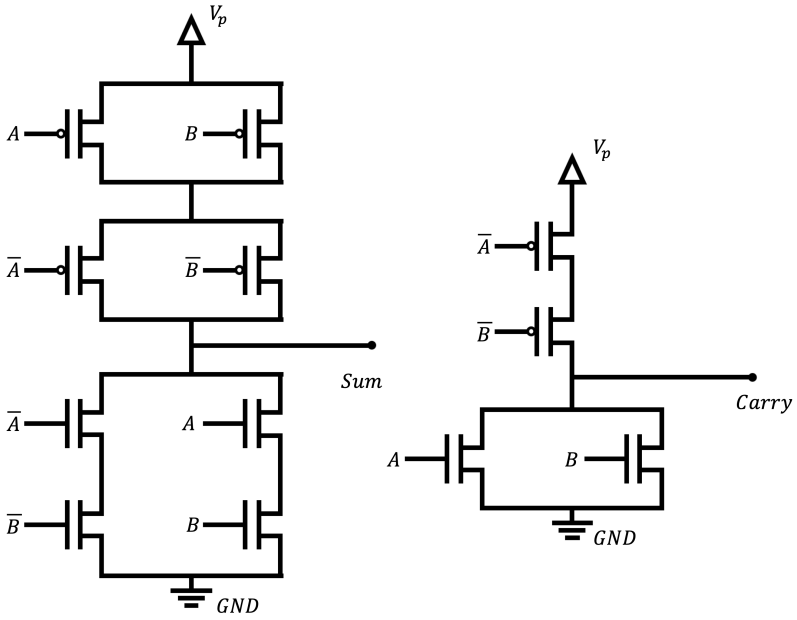

Figure 1: CMOS Circuit Diagram of Half Adder

CMOS implementation[4]:

CMOS implementation

Sum (XOR)

$$S = A \oplus B = \overline{A}B + A\overline{B}$$

Complement (output low condition), obtained by De Morgan:

$$\overline{S} = \overline{\overline{A}B + A\overline{B}} = (A + \overline{B})(\overline{A} + B) = AB + \overline{A}\,\overline{B} \quad \text{(XNOR)}$$

Implementation mapping:

- nMOS pull-down network (implements $\overline{S}$): two parallel branches — one branch is nMOS(A) in series with nMOS(B); the other branch is nMOS($\overline{A}$) in series with nMOS($\overline{B}$). (If complementary signals $\overline{A}$, $\overline{B}$ are not available, provide inverters or realize XOR with transmission gates.)
- pMOS pull-up network (dual of $\overline{S}$): series combination of two parallel pairs, i.e. (pA $\parallel$ p$\overline{B}$) in series with (p$\overline{A}$ $\parallel$ pB). This network pulls the output high when $\overline{S} = 0$.

Carry (AND)
Equation for Carry (Pull-up network):

$$C = A \cdot B$$

Complement (for the nMOS pull-down network), by De Morgan:

$$\overline{C} = \overline{A \cdot B} = \overline{A} + \overline{B}$$

Used Tools

- Microwind
- MS Word
- MS PowerPoint
- LaTeX

Circuit Schematic in Microwind

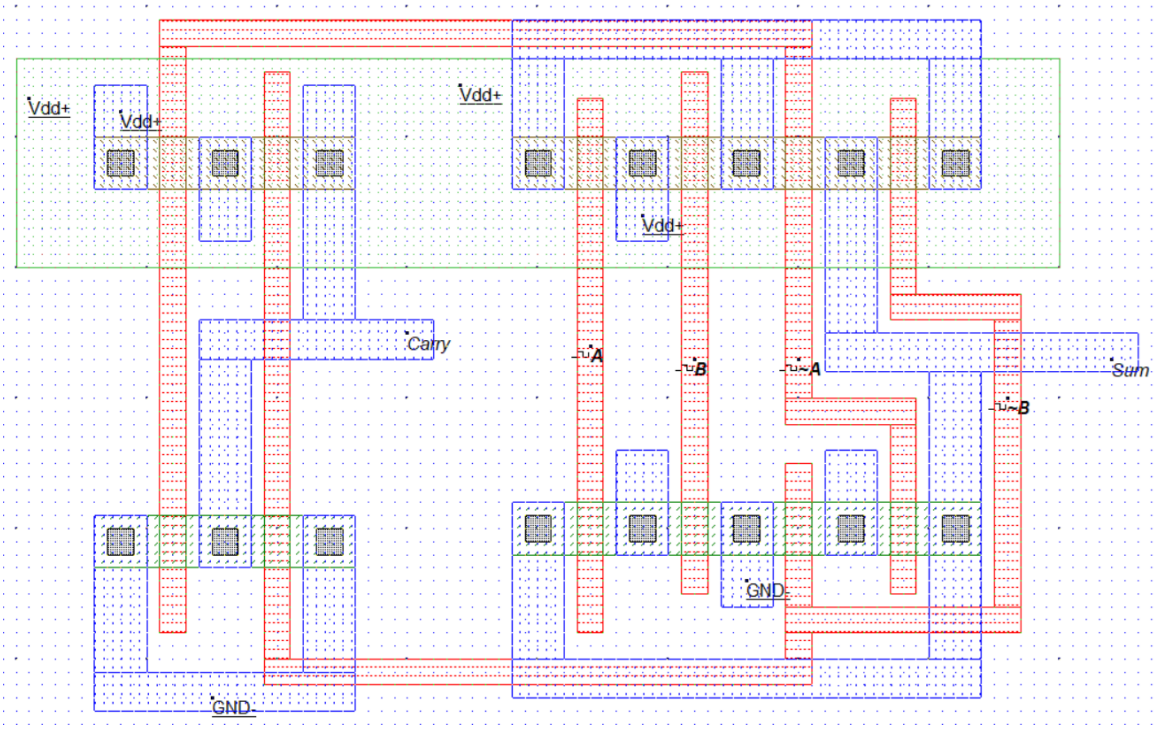

Figure 2: Half Adder Circuit Schematic in Microwind

Output

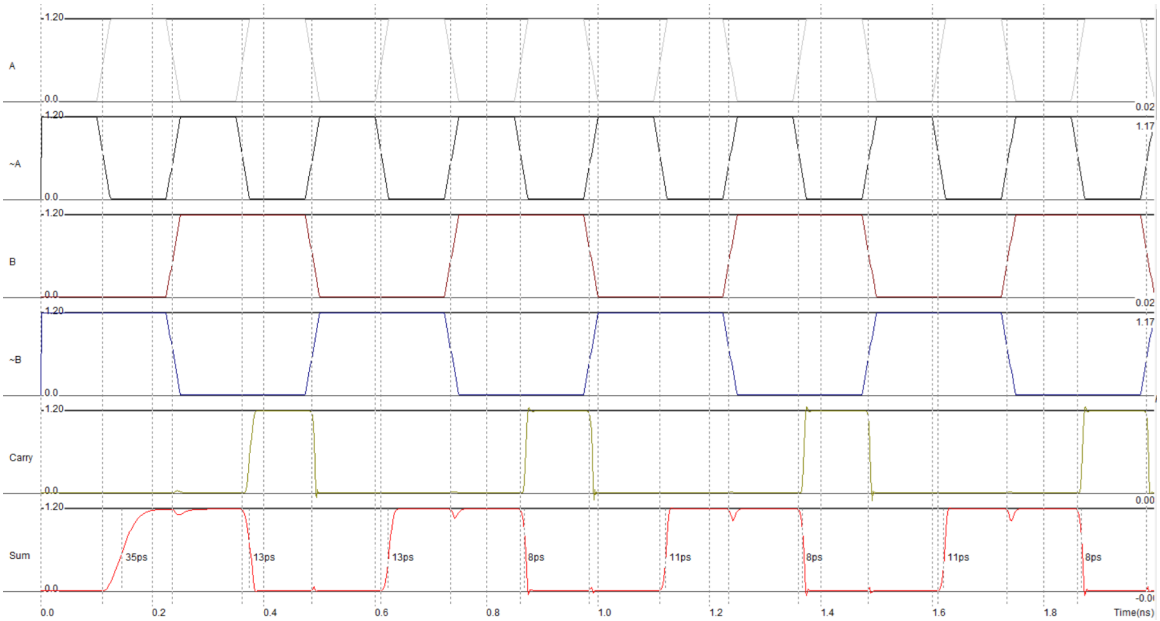

Figure 3: Sum & Carry Output Waveform of Half Adder Circuit

Output Analysis

1. Testbench and signal summary
   - Supply: VDD $\approx 1.20\,\text{V}$ (top trace marker).
   - Inputs: A and B driven with periodic pulses (top traces).
   - Outputs: Carry (green) and Sum (red). Time base in the plot is nanoseconds; zoomed markers show pulses spaced 0–2 ns.
2. Logic-level correctness
   - Carry ($C = A \cdot B$): goes high (1.20 V) only when both A and B are high; remains near 0 V otherwise. Example: cycle near 0.3–0.45 ns both inputs high and Carry rises to VDD.
   - Sum ($S = A \oplus B$): high when exactly one input is high, low when inputs are equal (both 0 or both 1). Sum falls to 0 when both inputs are high while Carry goes high, matching expected half-adder outputs.

Discussion

The implemented half adder ($S = A \oplus B$, $C = A \cdot B$) was simulated in Microwind and matches the truth table: Carry rises only when A and B are high and Sum follows XOR behavior. Waveforms show finite propagation delays and non-ideal rise/fall

times — the XOR (Sum) path is slower due to a larger transistor network, and PMOS devices were widened to better balance rise/fall. Dynamic switching dominates power; buffering the outputs with inverters and using a carefully sized static complementary or transmission-gate XOR reduces delay and voltage degradation.

Overall the simulation confirms a correct CMOS half adder implementation while highlighting the usual tradeoffs between speed, area (transistor count), and power.

Conclusion

A CMOS half adder was implemented and simulated in Microwind. The circuit produced the expected Sum and Carry waveforms for all input combinations, demonstrating correct logical operation. The exercise illustrates important design considerations for CMOS combinational circuits: choose transistor sizes to balance speed and noise margin, use buffering for improved drive and signal swing, and evaluate power/delay tradeoffs. Future work could measure propagation delay and energy per operation quantitatively, optimize the XOR topology for speed or area, and extend the design to a full adder and multi-bit adder chains.

References

[1] N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed. Boston, MA: Addison-Wesley, 2011.

[2] J. M. Rabaey, A. Chandrakasan, and B. Nikolić, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, NJ: Prentice Hall, 2003.

[3] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th ed. New York, NY: Oxford University Press, 2015.

[4] "Implement half adder circuit using static CMOS." Oct. 2025, [Online; accessed 23. Oct. 2025]. [Online]. Available: https://www.ques10.com/p/36440/implement-half-adder-circuit-using-static-cmos