Letters

Accurate Calorimetric Switching Loss Measurement for 900 V 10 mΩ SiC MOSFETs

Jon Azurza Anderson, *Student Member, IEEE*, Christoph Gammeter, *Student Member, IEEE*, Lukas Schrittwieser, *Student Member, IEEE*, and Johann W. Kolar, *Fellow, IEEE*

***Abstract*—This letter presents and evaluates three accurate (±20 %) calorimetric switching loss measurement methods, which are capable of measuring hard- and soft-switching losses at high speed (20–25 min/point) compared to other calorimetric methods. A comprehensive switching loss measurement data accuracy analysis is done, setting the benchmark for the accuracy analysis of switching loss data. The high accuracy in the switching loss data is obtained by a high ratio of switching losses to total measured losses in the Device Under Test. This is achieved by using a full-bridge configuration, where the conduction losses are reduced up to 80% in the Device Under Test by utilizing the duty cycle as an additional degree of freedom compared to a half-bridge configuration. Furthermore, the proposed calorimetric methods yield more reliable switching loss data than electrical methods, particularly than the double pulse test. Switching loss data are presented for the 900 V, 75 A, 10 mΩ SiC MOSFETs from CREE, that are one of the first discrete SiC MOSFETs to come with a TO-247-4 package.**

***Index Terms*—Calorimetric, SiC, switching losses.**

I. Introduction

With the eruption of wide band-gap semiconductors, SiC MOSFETs offer improved performance compared to their Si counterparts. One of the main advantages is that the reduced switching losses of SiC MOSFETs allow higher frequency operation, enabling a reduction of the volume of passive components, and thus achieve higher power densities at the same efficiencies, which is advantageous in data centers [1], More Electric Aircraft (MEA) [2], and electric vehicle applications [3]. For optimization purposes reliable switching loss data is required, but the data provided in the datasheets are typically insufficient for converters that employ soft-switching modulation schemes. Furthermore, the reliability of the switching energy data is questionable, since they are usually acquired through a Double Pulse Test (DPT). Moreover, the DPT results are commonly presented without an accuracy estimation of the switching losses, adding uncertainty to the switching loss data.

The DPT consists of the integration of the drain–source voltage and the drain current of the Device Under Test (DUT). However, this method has several drawbacks. Firstly, the turn-on ($E_{\mathrm{sw,on}}$) and turn-off ($E_{\mathrm{sw,off}}$) switching loss values acquired through the DPT do usually not reflect the actual losses that occur in the on- and off-transitions, respectively

Manuscript received March 9, 2017; revised April 11, 2017; accepted May 2, 2017. Date of publication May 5, 2017; date of current version August 2, 2017. *(Corresponding author: Jon Azurza Anderson.)*

The authors are with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, Physikstrasse 3, 8092 Zurich, Switzerland (e-mail: azurza@lem.ee.ethz.ch; gammeter@lem.ee.ethz.ch; schrittwieser@lem.ee.ethz.ch; kolar@lem.ee.ethz.ch).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2701558

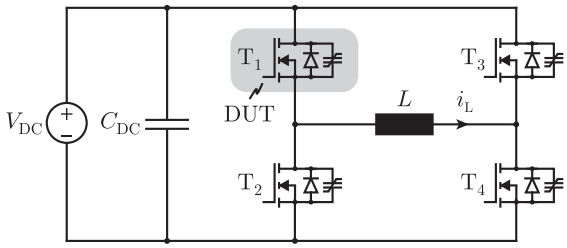

Fig. 1. Full-bridge topology used for the calorimetric switching loss measurement setup, where the losses produced by the DUT are measured independently from the losses occurring in the rest of the circuit. The full-bridge configuration allows to improve the ratio of switching losses to total losses in the DUT by adjusting the duty cycle to reduce its conduction losses and by increasing the switching frequency.

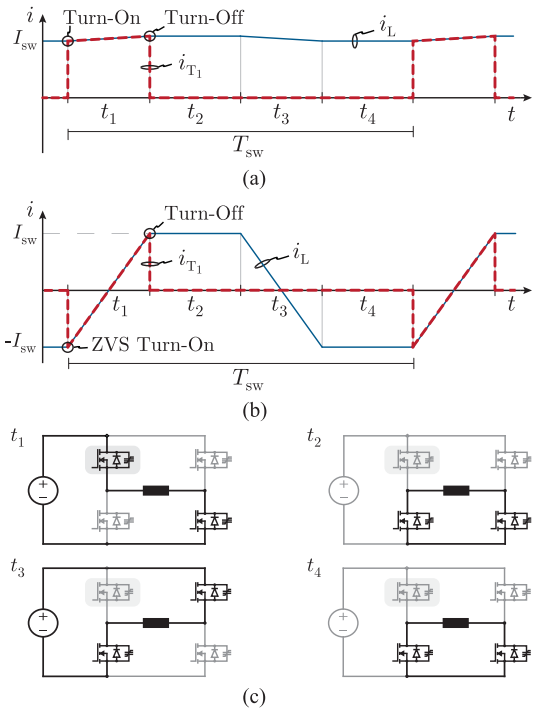

Fig. 2. Proposed modulation technique for the full-bridge shown in Fig. 1 used to reduce the conduction losses in the DUT: (a) hard-switching and (b) soft-switching inductor and DUT (T_1) current waveforms (shown dashed), and (c) the conduction path during a switching period, which is the same for both soft- and hard-switching modulation schemes, where the DUT conduction time t_1 is minimized.

TABLE I
COMPARISON OF THE DIFFERENT SWITCHING LOSS MEASUREMENT METHODS PRESENTED IN LITERATURE

	Electrical		Hybrid		Calorimetric			
					Transient		Steady State	
	DPT	Energy Conserv.	Opposition Method	Inductor Loss Meas.	Block Capacitance (Series Switch)	Block Capacitance (Output Switch)	Half-Bridge Loss Meas.	Air Flow Method
Accuracy	Low	Low	Medium	Medium	High	High	Medium	High
Speed	Fast	Fast	Medium	Slow	Medium	Medium	Slow	Medium
T_j controlled	Yes	No	No	No	No	No	No	Yes
Ref.	[12]	[8]	[9]	[10]	[7]	[13]	[11]	(This)

[4]. On the one hand, while measuring $E_{\text{sw,off}}$ with a DPT, the energy stored in the output capacitance C_{oss} is electrically measured as a loss, and accounted for as part of $E_{\text{sw,off}}$. On the other hand, while measuring $E_{\text{sw,on}}$ with the DPT, the energy that was stored in the C_{oss} previous to turn-on is consumed within the channel, but this cannot be measured electrically, since it occurs internally, thus leading to lower measured $E_{\text{sw,on}}$ values. For hard-switching cases, and provided that both semiconductors in the half-bridge are the same, $E_{\text{sw,on}}$ + $E_{\text{sw,off}}$ yields the correct sum of the switching loss values, since these energy differences cancel out. For soft-switching applications, however, the stored energy in the MOSFET, E_{oss}, needs to be subtracted from the $E_{\text{sw,off}}$ data, since the $E_{\text{sw,off}}$ data provided in the datasheets typically does not coincide with the losses occurring during soft-switching [5], [6]. Second, the DPT requires high-bandwidth measurements of the DUT current and voltage waveforms, which typically entails the insertion of a shunt in the commutation path to measure the current. This inserts an additional parasitic inductance that may corrupt the loss values, especially for fast switching devices. Third, the DPT measurement data are significantly influenced by the skew of the probes, DC offsets, choice of integration limits, and common mode noise [7]. Finally, as presented in [7], a ± 5 % measurement error of a soft-switching transitions could result in a relative error in the soft-switching loss data of ± 105 %, leading to unacceptable accuracies. The problem with the skew can be solved through the energy conservation method presented in [8], where the switching losses are calculated out of the stored energy difference between the dc link capacitors and inductor. But a significant step towards solving the measurement issues is presented in the opposition method [9], where power is circulated in the system, and the total system losses, that are supplied by a dc input, can be measured with precision. Nonetheless, a new challenge arises, as it is not trivial to accurately separate the switching losses from the measured total losses. In [9], an elaborate loss calculation of the inductor is performed, in [10] the inductor losses are measured calorimetrically, and in [11] a half-bridge is inserted into a calorimeter to measure its losses independent from the inductor. However, these approaches assume the other system losses to be negligible, e.g., the losses in capacitors, PCB tracks, connectors, etc. The semiconductor loss separation issue is completely solved in [7] directly measuring the switch-generated losses in a transient calorimetric measurement, by attaching the switch to a metal block and measuring the temperature rise time. Furthermore, the conduction and switching losses are separated, but an additional switch in series to the half-bridge is needed. This has proven to be very accurate; however, the measurements are relatively time consuming. In Table I, the different switching loss measurement methods presented in literature are summarized.

In this letter, three alternative accurate and fast (20–25 min/point) steady-state calorimetric switching measurement loss methods are presented, where by using a full-bridge configuration, as seen in Fig. 1, the conduction losses in the DUT are minimized by adjusting its duty cycle. The proposed full-bridge configuration, with the capability of reducing the conduction losses in the DUT, is a new principle for continuous calorimetric switching loss measurements that measure the losses of a single device. Although the presented continuous calorimetric methods are slower than the existing DPT method, where each data point can be obtained in a matter of minutes, the large advantage is that the worst case error is defined (± 20 % for Methods 1 and 2). Furthermore, the proposed methods are faster than alternative calorimetric methods, that for the case of continuous measurement methods which use a calorimeter have large thermal time constants (in the order of magnitude up to ~ 60 min), or transient calorimetric methods that need to be thermally cycled (heated up and cooled down) one or several times to obtain each data point. In Section II, the three methods are proposed, followed by Section III where the experimental hardware setup is described and an accuracy analysis is performed. In Section IV, the switching losses of 900 V 10 mΩ SiC MOSFETs from CREE are presented, and finally, in Section V several conclusions are drawn.

II. PROPOSED CALORIMETRIC MEASUREMENT METHODS

In this section, three calorimetric switching loss measurement methods are presented, where the data points are taken in the thermal steady state, without the need of thermally cycling the system to obtain the different data points. Furthermore, the power losses occurring in form of heat in the DUT are directly measured, since the measured power losses $P_{\text{loss,m}}$ consist of the switching losses P_{sw} and conduction losses P_{cond} of the DUT, independently of the losses occurring in the rest of the system, e.g., other switches, inductor, capacitors, PCB tracks, etc. Knowing the RMS value of the MOSFET current $I_{\text{d,rms}}$, and its on-state resistance $R_{\text{ds,on}}(T_{\text{j}}, v_{\text{gs}})$, the conduction losses are known, and hence, the switching loss energy is calculated as

$$E_{\text{sw,m}} = \frac{P_{\text{loss,m}} - R_{\text{ds,on}}(T_{\text{j}}, v_{\text{gs}}) \cdot I_{\text{d,rms}}^2}{f_{\text{sw}}} \tag{1}$$

with f_{sw} being the switching frequency, T_{j} the junction temperature, and v_{gs} the applied on-state gate–source voltage to the MOSFET. However, one of the remaining challenges is to separate the conduction losses from the switching losses. A simple and effective way of minimizing the conduction losses is by implementing a full-bridge topology, where the losses are measured for the high-side MOSFET of the first half-bridge. By introducing this additional degree of freedom, the current can be free-wheeled on the lower side of the full-bridge (T_2, T_4), substantially reducing the DUT conduction time (cf. Fig. 2), and thus optimizing its measured switching power ratio

$$SW_{\text{ratio}} = \frac{P_{\text{sw}}}{P_{\text{tot}}} = \frac{P_{\text{sw}}}{P_{\text{sw}} + P_{\text{cond}}} \tag{2}$$

and improving the measured switching loss data accuracy. Moreover, the full-bridge topology enables the energy to constantly shift between the capacitors and the inductor, and hence, the use of a load resistor for hard-switching operation is avoided.

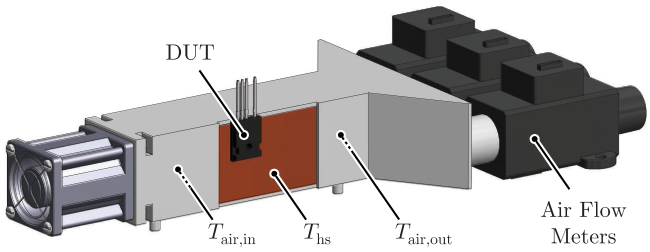

Fig. 3. Illustration of the DUT duct, with three air flow meters (AFMs) connected in parallel at the output to measure the volumetric air flow. Additionally, the different measured temperature magnitudes in the switching loss measurement setup are shown.

With the DUT setup and the measurements shown in Fig. 3, three steady-state calorimetric switching loss measurement methods are proposed in the following.

A. Method 1: Heat Sink Thermal Resistance

This method requires the heat sink's thermal resistance $R_{\text{th,hs}}$, which can be obtained through a calibration measurement for different volumetric flows. Once the $R_{\text{th,hs}}$ is characterized, the power losses can be obtained by measuring the heat sink temperature T_{hs} and heat sink input air temperature $T_{\text{air,in}}$ as

$$P_{\text{loss,m}} = \frac{T_{\text{hs}} - T_{\text{air,in}}}{R_{\text{th,hs}}} \,. \tag{3}$$

B. Method 2: Heat Sink Air Flow Temperature Difference

Alternatively, instead of measuring the heat sink temperature, the heat sink output air temperature can be measured, and the power losses result in

$$P_{\text{loss,m}} = \beta \cdot (T_{\text{air,out}} - T_{\text{air,in}}) \tag{4}$$

where β is obtained through calibration for different volumetric flows.

C. Method 3: Air Enthalpy Increase

However, the power losses can be measured directly, theoretically without the need of a calibration, should the air mass flow be determined. If air flow meters (AFM) are used to measure the air volumetric flow $\dot{V}$, the enthalpy difference of the air is measured, which is essentially the power loss that occurs in the DUT once the system has reached thermal equilibrium. Hence

$$P_{\text{loss,m}} = \rho \cdot C_{\text{p}} \cdot (T_{\text{air,out}} - T_{\text{air,in}}) \cdot \dot{V} \cdot \psi \tag{5}$$

where ρ is the air density, C_{p} the specific heat of air, and ψ a correction factor that can be obtained through calibration.

III. Experimental Setup

The converter used for the switching loss measurements is presented in Fig. 4. When operating it in hard-switching mode, both hard turn-on and turn-off losses are measured, for which the current ripple is minimized with a 767 µH magnetic core inductor so that $i_{\text{L}} \cong I_{\text{sw}} \geq 0$, where I_{sw} is the switching current.

For the soft-switching operation, an air core inductor, whose value is adapted between 3 and 7 µH by changing the amount of turns, is used to create a trapezoidal current waveform with maximum and minimum values of $\pm I_{\text{sw}}$. Here, only turn-off losses are measured, assuming that the ZVS turn-on losses are negligible compared to the turn-off transition, since the dead-time intervals are adjusted to minimize the body diode conduction time. Hence, the (hard) turn-on losses are obtained by subtracting the soft-switching losses from the measured hard-switching losses.

TABLE II
Comparison of the Theoretical Minimum Switching Energy Losses at Zero-Current and the Measured Values, Corrected for the Parasitic PCB Capacitance C_{PAR}

E_{sw}	200 V	400 V	600 V
Theoretical	57 µJ	149 µJ	266 µJ
Method 1	57 µJ (0.39 %)	151 µJ (0.70 %)	276 µJ (3.18 %)
Method 2	56 µJ (−1.30 %)	147 µJ (−1.34 %)	270 µJ (1.49 %)
Method 3	53 µJ (−6.80 %)	141 µJ (−5.82 %)	255 µJ (−3.97 %)

The thermal resistance path from the MOSFETs to the air is minimized by soldering each MOSFET (TO-247–4 package) onto separate custom-made high-performance copper heat sinks, as it is not desirable to lose any power in the form of heat through existing heat leakage paths (e.g., conduction to the PCB through the leads or convection from the MOSFET case). To avoid air leakage, the heat sinks are tightly placed and sealed inside individual ducts (cf. Fig. 3). PWM controlled 12.6 W 40 × 40 mm fans are used, whose speeds are also monitored. For full fan speed, the thermal resistance of the DUT heat sink, whose air output is connected to the AFMs, is of $R_{\text{th,hs}} = 0.42$ K/W, which yields a cooling system performance index (CSPI) of 13.78 W/(K·dm^3), whereas for the remaining MOSFETs, $R_{\text{th,hs}} = 0.12$ K/W, which yields a CSPI of 48.22 W/(K·dm^3). The increase in $R_{\text{th,hs}}$ of the DUT heat sink is due to the additional pressure drop inserted in the air flow path by the selected precision AFMs, for which three AFMs are used in parallel. Low $R_{\text{th,hs}}$, together with a reduced size and weight of the heat sinks (40 × 40 × 60 mm, 372 g), reduces the thermal time constant, which speeds up the measurement process. The temperatures are read with 100 kΩ NTC resistors which offer an accuracy of ±0.1 °C, that were not affected by the switching transients. For the output air temperature reading, in order to create turbulence and homogenize the temperature distribution of the laminar air flow coming out of the heat sink [14], inserting a mixer in form of blades in the air duct is recommended. The junction temperature of the DUT is determined by measuring the heat sink temperature (T_{hs}), which is assumed to be homogeneous on the 5-mm-thick copper heat sink baseplate that the DUT is soldered on to, and adding the product of the junction-to-case thermal resistance of the MOSFET ($R_{\text{th,j-c}}$) and the measured power losses ($P_{\text{loss,m}}$).

Accuracy Analysis

To validate the measurement data and assess its accuracy, the zero-current loss measurements, performed without any inductor attached, can be compared to the theoretical minimum zero-current hard-switching losses, by doing an energy balance between before and after the switching period [15]. Assuming that the same switches are used in the half-bridge, the zero-current switching losses are $E_{\text{sw,zc}} = Q_{\text{oss}} \cdot V_{\text{DC}}$, where Q_{oss} is the output capacitance charge, obtained from the supplier datasheet. These results are shown in Table II, where the accuracy of the switching loss measurement setup can be evaluated. The data in Table II are corrected for the additional parasitic capacitance ($C_{\text{par}} = 103$ pF in this setup) that exists, e.g., in the PCB tracks, and is parallel to the output capacitance C_{oss} of the MOSFETs, thus contributing to the losses measured in the setup. These losses are quadratically dependent on the voltage ($E_{\text{sw,par}} = 1/2 \cdot C_{\text{par}} \cdot V_{\text{DC}}^2$).

The results for all the performed measurements with Methods 1 and 2 are very similar, being the average difference between them for all measurement points of 1.5 %. However, for the air enthalpy increase equation [cf. (5)] used for Method 3, it has been determined that due to the unavoidable heat and air leakage in the system, a calibration has to be done to introduce the correction factor ψ, which has a value of $\psi = 1.15$–1.20.

For completeness, an absolute worst case for the switching loss error has to be defined. By starting from (1) and normalizing the values

$$\frac{f_{\text{sw}} \cdot E_{\text{sw,m}}}{P_{\text{sw}}} = \frac{P_{\text{loss,m}} - P_{\text{cond,m}}}{P_{\text{sw}}} \tag{6}$$

is obtained. Subsequently, the measured switching losses $E_{\text{sw,m}}$, the measured total power loss $P_{\text{loss,m}}$, and conduction losses $P_{\text{cond,m}}$ can be written as

$$E_{\text{sw,m}} = (1 \pm \varepsilon_{\text{sw}}) \cdot E_{\text{sw}} \,, \tag{7}$$

$$P_{\text{loss,m}} = (1 \pm \varepsilon_{\text{calib}}) \cdot (1 \pm \varepsilon_{\text{temp}}) \cdot (1 \pm \varepsilon_{\dot{\text{V}}}) \cdot P_{\text{loss}} \,, \tag{8}$$

$$P_{\text{cond,m}} = (1 \pm \varepsilon_{\text{cond}}) \cdot P_{\text{cond}} \tag{9}$$

where ε_{sw} is the error of the switching loss energy, $\varepsilon_{\text{calib}}$ is the calibration error, done when measuring the known input power to the loss measurement setup during calibration, which was measured by a four-wire power measurement with a high-precision shunt resistor (Burster 10 mΩ 0.02 %) and two high-precision voltage meters (Agilent 34410A), $\varepsilon_{\text{temp}}$ is the temperature measurement error, that depends predominantly on the NTC accuracy and its analog voltage reference, $\varepsilon_{\dot{\text{V}}}$ is the air flow measurement error of the AFMs (or fan speed repeatability for Methods 1 and 2, where the air flow is not measured) and $\varepsilon_{\text{cond}}$ is the conduction power loss calculation error. By substituting (2) and (6) into (9), the worst case or maximum switching loss energy error $\varepsilon_{\text{sw,max}}$ is introduced

$$\max |1 \pm \varepsilon_{\text{sw,max}}| = \max \left| \frac{(1 \pm \varepsilon_{\text{calib}}) \cdot (1 \pm \varepsilon_{\text{temp}}) \cdot (1 \pm \varepsilon_{\dot{\text{V}}})}{SW_{\text{ratio}}} - \frac{(1 \pm \varepsilon_{\text{cond}}) \cdot (1 - SW_{\text{ratio}})}{SW_{\text{ratio}}} \right| . \tag{10}$$

If the second- and third-order error terms in (10) are neglected, the worst case error can then be calculated as

$$\varepsilon_{\text{sw,max}} \cong \frac{(\varepsilon_{\text{calib}} + \varepsilon_{\text{temp}} + \varepsilon_{\dot{\text{V}}})}{SW_{\text{ratio}}} + \varepsilon_{\text{cond}} \cdot \frac{(1 - SW_{\text{ratio}})}{SW_{\text{ratio}}} \,. \tag{11}$$

The importance of having a high switching ratio (SW_{ratio}) can be noticed in (11), which is further highlighted in Figs. 5 and 6, where the error done while measuring the total power losses $P_{\text{loss,m}}$ is summarized as $\varepsilon_{\gamma} = (\varepsilon_{\text{calib}} + \varepsilon_{\text{temp}} + \varepsilon_{\dot{\text{V}}})$. On the one hand, in Fig. 5 the influence of ε_{γ} on the maximum switching loss error $\varepsilon_{\text{sw,max}}$ is shown in (a), together with the influence of $\varepsilon_{\text{cond}}$ in (b). In the case of the setup at hand, for Methods 1 and 2, the maximum measurement error for the total power losses for all operating points is $\varepsilon_{\gamma,\text{max}} = 8.8\,\%$, and for Method 3, $\varepsilon_{\gamma,\text{max}} = 22.8\,\%$, where the larger error for Method 3 is explained by the accuracy of the AFMs. On the other hand, in Fig. 6 the obtained measurement data accuracy improvement for the full-bridge topology (b) against the half-bridge topology (a) is shown. It is assumed that total power losses in the DUT are the same, in order to take the switching loss measurements for the same junction temperature. Since with the half-bridge the duty cycle is limited to 0.5 for soft-switching measurements, contrary to the duty cycle of 0.15 used in the full-bridge, the switching ratio SW_{ratio} decreases from 81.0 % to 38.7 %, increasing the worst-case error $\varepsilon_{\text{sw,max}}$ from 13.3 % to 38.5 %, in the case of the $V_{\text{DC}} = 600$ V and $I_{\text{sw}} = 70$ A measurements.

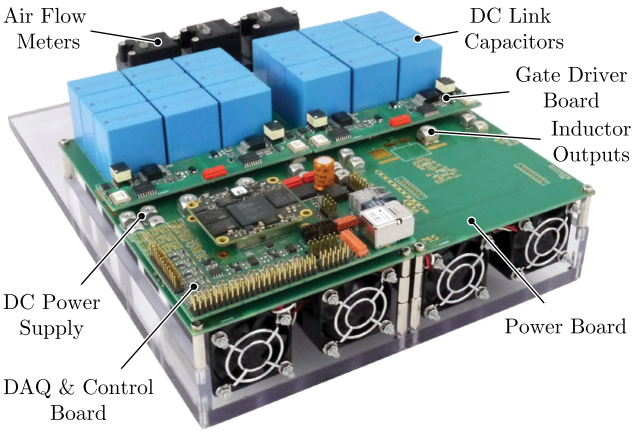

Fig. 4. Switching loss measurement converter, composed of two separate half-bridges, each one with its respective gate driver board. All the measurements are taken in the data acquisition (DAQ) and control board.

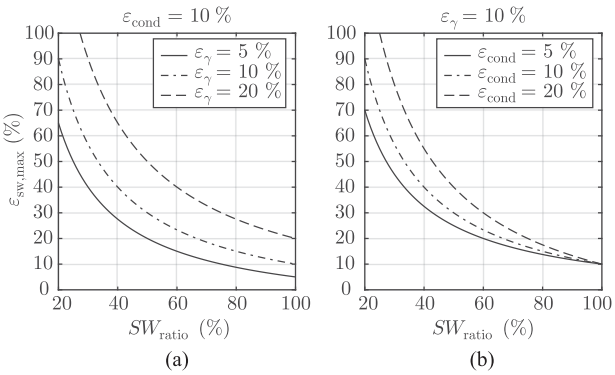

Fig. 5. Example of the influencing factors on the worst-case error $\varepsilon_{\text{sw,max}}$, in function of the switching ratio SW_{ratio}. The influence of $\varepsilon_{\gamma} = \left(\varepsilon_{\text{calib}} + \varepsilon_{\text{temp}} + \varepsilon_{\dot{\text{V}}}\right)$ (a), and the influence of $\varepsilon_{\text{cond}}$ (b).

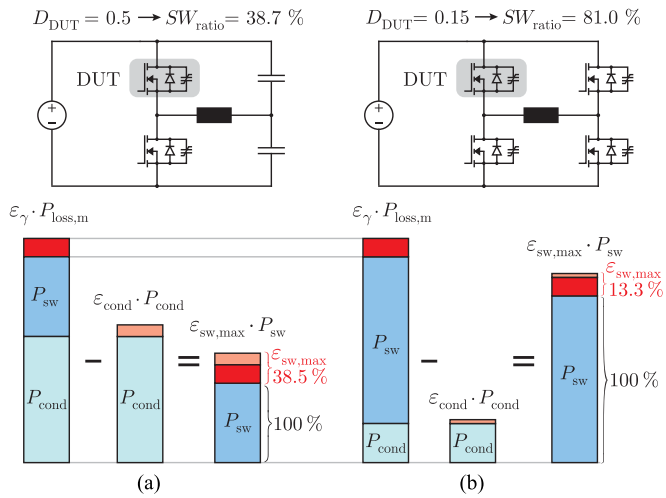

Fig. 6. Improvement on the switching loss data quality compared to a half-bridge topology (a) where the duty cycle has to be 0.5 for soft-switching, by introducing the presented full-bridge topology (b), that allows us to reduce the conduction losses on the DUT by varying the duty cycle. For the comparison, the same total losses in the same semiconductor DUT device are assumed, in order to take the measurements at the same junction temperature. The results are presented for the soft-switching case of $V_{\text{DC}} = 600$ V and $I_{\text{sw}} = 70$ A, and the errors assumed are $\varepsilon_{\gamma} = 8.8$ % and $\varepsilon_{\text{cond}} = 10$ %.

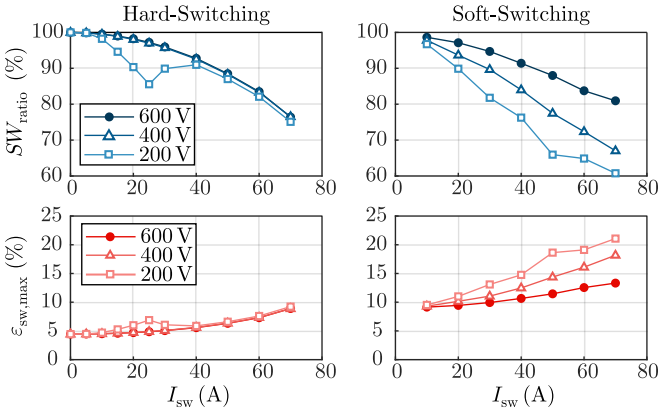

Fig. 7. Switching ratio SW_{ratio} (switching losses to total measured losses) and worst-case switching energy error $\varepsilon_{sw,max}$ ($\varepsilon_{cond} = 10$ % is conservatively assumed) for the presented 0 Ω external gate driver resistor switching losses in Fig. 8. It has to be noted that for hard-switching, since the losses occurring in the DUT are larger, higher fans speeds are used, that lead to more accurate results.

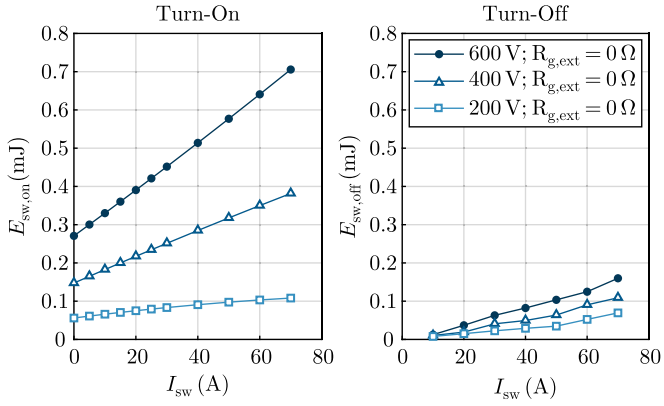

Fig. 8. Measured turn-on ($E_{sw,on}$) and turn-off ($E_{sw,off}$) switching losses for 0 Ω external gate driver resistor at 70 °C junction temperature for different voltages, corrected for C_{par}.

The switching ratios of the obtained measurements (SW_{ratio}) and worst case error ($\varepsilon_{sw,max}$) that correspond to the switching loss data presented in Fig. 8 are shown in Fig. 7. The drop in Fig. 7 of the SW_{ratio} for the hard-switching case of 200 V is due to the controller instability at high switching frequencies used for low currents. However, due to the results for zero-current switching and the observed repeatability of the measurements, the authors are confident that the error is substantially lower than the maximum error $\varepsilon_{sw,max}$ presented.

IV. Results

In this section, the switching loss measurement results for the 900 V, 75 A, 10 mΩ SiC MOSFETs (X3M0010090X-ES) from CREE are presented, where only the results from Method 2 are shown, since they are very similar to those of Method 1, and are more accurate than those of Method 3.

The switching loss data for 0 Ω external turn-on and turn-off gate driver resistors is shown in Fig. 8. By optimizing the power commutation loop in the PCB, and without the use of any additional damping circuit, these SiC MOSFETs can be driven with 0 Ω external gate resistor, 144 V being the maximum overshoot observed for 600 V hard-switching. However, it has to be noted that the gate driver IC (IXIS IXDD630MYI) has an output resistance of 0.2 Ω, and that the internal resistance of the MOSFET is 1.8 Ω. For hard-switching bridge legs, the total switching loss energy in the DUT is the addition of both the turn-on and turn-off switching energy ($E_{sw,on}$ + $E_{sw,off}$), whereas, for soft-switching bridge legs, only the turn-off energy ($E_{sw,off}$) is dissipated. For low I_{sw} values, in order to have the junction temperature at 70 °C, high switching frequencies are used (up to 530 kHz for hard-switching, and 950 kHz for soft-switching), leading to high SW_{ratio} values (cf. Fig. 7), and thus, higher switching loss data accuracy (cf. (11) and Fig. 5). However, with increasing I_{sw}, as both the conduction and switching losses increase, the switching frequency is reduced to keep the junction temperature constant at 70 °C (down to 29 kHz for hard-switching, and 110 kHz for soft-switching), also leading to lower SW_{ratio} values, and hence, lower accuracy.

To further validate the presented switching loss measurement methods and the data, the obtained hard-switching results are compared with those of [12] in Fig. 9, where the switching loss measurements of the same switches are performed with a DPT. In [12], the results

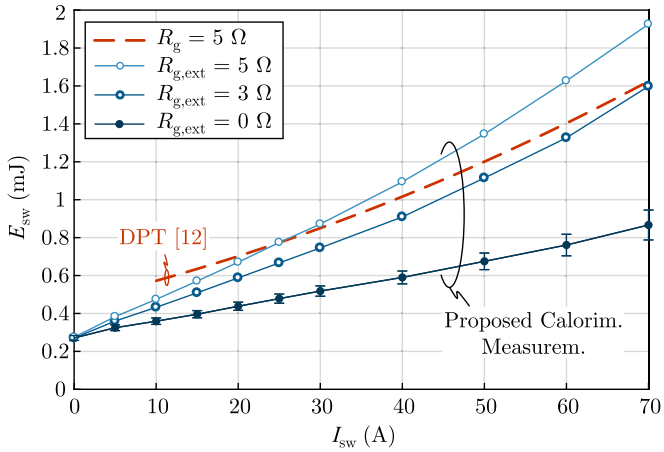

Fig. 9. Comparison of measured 600 V hard-switching losses ($E_{sw,on}$ + $E_{sw,off}$) between the Double Pulse Test (DPT), performed for a half-bridge in [12] (in red, for $T_j = 25$ °C), and the proposed calorimetric method (in blue, for $T_j = 70$ °C, and corrected for C_{par}). Note that for clarity of the representation, only the error bars for the case of $R_{g,ext} = 0\,\Omega$ are shown, but the $\varepsilon_{sw,max}$ is the same for all cases (cf. Fig. 7).

are presented for $R_g = 5\,\Omega$, and since it is not specified if this value includes the internal gate resistance of the DUT ($R_{g,int} = 1.8\,\Omega$) and the gate driver output resistance (0.2 Ω in the case of the presented setup), the results are compared for $R_{g,ext} = 3\,\Omega$ and $R_{g,ext} = 5\,\Omega$. Regardless of the gate driver resistance, the zero-current switching losses should converge to $E_{sw,zc} = Q_{oss} \cdot V_{DC}$ (cf. Table II), as seen for the results obtained with the proposed calorimetric methods in Fig. 9. The difference compared to the electrical DPT switching loss measurement, particularly at low currents, can be explained by potential inaccuracies as discussed in Section I.

V. Conclusion

In this letter, three fast and accurate steady-state calorimetric switching loss measurement methods were presented, where a full-bridge configuration is utilized. By adjusting the duty cycle of the DUT, its conduction losses are considerably decreased (up to 80 % compared to a half-bridge configuration), yielding a high ratio of switching losses to total losses, which leads to a high switching loss data accuracy. Due to the unavoidable heat and air leakage in the system, the direct

power loss measurement of Method 3 underestimates the real power losses by 15–20 %, which means that this method has to also undergo a calibration process to determine a correction factor. This, together with its larger theoretical inaccuracy due to the air volumetric flow measurement and the added system complexity, leads to the conclusion that Methods 1 and 2 are the most recommendable of the proposed methods. Furthermore, a comprehensive analysis of the switching loss measurement data accuracy is done, setting the benchmark for accuracy analysis of switching loss data for fast-switching power semiconductor devices. Finally, accurate switching loss data were presented for 900 V, 75 A, 10 mΩ SiC MOSFETs.

REFERENCES

[1] L. Schrittwieser, J. W. Kolar, and T. B. Soeiro, "99 % Efficient three-phase buck-type SiC MOSFET PFC rectifier minimizing life cycle cost in DC data centers," in *Proc. IEEE Int. Commun. Energy Conf.*, Austin, TX, USA, Oct. 2016, pp. 1–8.

[2] C. Gammeter, F. Krismer, and J. W. Kolar, "Weight and efficiency analysis of switched circuit topologies for modular power electronics in MEA," in *Proc. IEEE Ind. Electron. Soc. Conf.*, Florence, Italy, Oct. 2016, pp. 3640–3647.

[3] R. Bosshard and J. W. Kolar, "All-SiC 9.5 kW/dm3 on-board power electronics for 50 kW/85 kHz automotive IPT system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 419–431, Mar. 2017.

[4] X. Li, L. Zhang, S. Guo, Y. Lei, A. Huang, and B. Zhang, "Understanding switching losses in SiC MOSFET: Toward lossless switching," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, Blacksburg, VA, USA, Nov. 2015, pp. 257–262.

[5] J. Fedison, M. Fornage, and M. Harrison, "C_{oss} related energy loss in power MOSFETs used in zero-voltage-switched applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Fort Worth, TX, USA, Mar. 2014, pp. 150–156.

[6] J. Fedison and M. Harrison, "C_{oss} hysteresis in advanced superjunction MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.,*Long Beach, CA, USA, Mar. 2016, pp. 247–252.

[7] D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate transient calorimetric measurement of soft-switching losses of 10 kV SiC MOSFETs," in *Proc. IEEE Power Electron. Distrib. Generat. Syst. Symp.*, Vancouver, Canada, Jun. 2016, pp. 1–10.

[8] Z. Zhang *et al.*, "Methodology for switching characterization evaluation of wide band-gap devices in a phase-leg conguration," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Fort Worth, TX, USA, Mar. 2014, pp. 2534–2541.

[9] J. Brandelero, B. Cougo, T. Meynard, and N. Videau, "A non-intrusive method for measuring switching losses of GaN power transistors," in *Proc. IEEE Ind. Electron. Soc. Conf.*, Vienna, Austria, Nov. 2013, pp. 246–251.

[10] D. Bortis, O. Knecht, D. Neumayr, and J. W. Kolar, "Comprehensive evaluation of GaN GIT in low-and high-frequency bridge leg applications," in *Proc. IEEE Int. Power Electron. Conf.*, Hefei, China, May 2016, pp. 21–30.

[11] A. Tüysüz, R. Bosshard, and J. W. Kolar, "Performance comparison of a GaN GIT and a Si IGBT for high-speed drive applications," in *Proc. IEEE Int. Power Electron. Conf.*, Hiroshima, Japan, May 2014, pp. 1904–1911.

[12] V. Pala, G. Wang, B. Hull, S. Allen, J. Casady, and J. Palmour, "Record-low 10 mΩ SiC MOSFETs in TO-247, rated at 900 V," in *Proc. IEEE Appl. Symp. Power Electron. Conf. Expo.*, Long Beach, CA, USA, Mar. 2016, pp. 979–982.

[13] D. Neumayr, M. Guacci, D. Bortis, and J. W. Kolar, "Novel temperature-gradient based calorimetric measurement principle to obtain soft-switching benchmark of GaN and SiC power devices," Accepted for publication in *Proc. IEEE Int. Symp. Power Semicond. Dev. and ICs*, Sapporo, Japan, May/Jun. 2017, pp. 979–982.

[14] C. Gammeter, F. Krismer, and J. W. Kolar, "Weight optimization of a cooling system composed of fan and extruded fin heat sink," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 509–520, Jan./Feb. 2015.

[15] M. Kasper, R. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.