Automatic compiler customization for novel hardware

Automatische Anpassung von Compilern für neuartige Hardwarearchitekturen
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Erklärung zur Abschlussarbeit gemäß §22 Abs. 7 und §23 Abs. 7 APB der TU Darmstadt

Hiermit versichere ich, Janne Wulf, die vorliegende Masterarbeit ohne Hilfe Dritter und nur mit den angegebenen Quellen und Hilfsmitteln angefertigt zu haben. Alle Stellen, die Quellen entnommen wurden, sind als solche kenntlich gemacht worden. Diese Arbeit hat in gleicher oder ähnlicher Form noch keiner Prüfungsbehörde vorgelegen.

Mir ist bekannt, dass im Fall eines Plagiats (§38 Abs. 2 APB) ein Täuschungsversuch vorliegt, der dazu führt, dass die Arbeit mit 5,0 bewertet und damit ein Prüfungsversuch verbraucht wird. Abschlussarbeiten dürfen nur einmal wiederholt werden.

Bei der abgegebenen Thesis stimmen die schriftliche und die zur Archivierung eingereichte elektronische Fassung gemäß §23 Abs. 7 APB überein.

Bei einer Thesis des Fachbereichs Architektur entspricht die eingereichte elektronische Fassung dem vorgestellten Modell und den vorgelegten Plänen.

Darmstadt, August 9, 2021

J. Wulf

Contents

Todo list

1 Background

In this chapter we are introducing knowledge which is required to understand the content of this thesis. In section 1.1 we give an overview about how a compiler is typically implemented and which problems it has to solve that we want to tackle.

explain also the other sections

Motivation?

[10] state the important interdependence between instruction scheduling and register allocation.

1.1 Compilers

Making computer programs, written in high-level programming languages, executable on a specific machine is not a trivial task. Compilers are only one piece in the tool-chain required to make a program executable. The compiler translates the high-level language into assembly language, which is translated into object code by the assembler. Basic functionality like allocating memory or outputting strings on the screen is implemented in a standard library. The object code of the standard library and potentially other libraries are linked together with the translated program by the linker.

The pure translation of the program is only one of the tasks a compiler has to fulfill.

What are the different tasks a compiler has?
How are compilers usually implemented? (Front-End, ...)
Front End
Optimization
Back End

Instruction Scheduling
Register Allocation

1.1.1 Instruction Scheduling

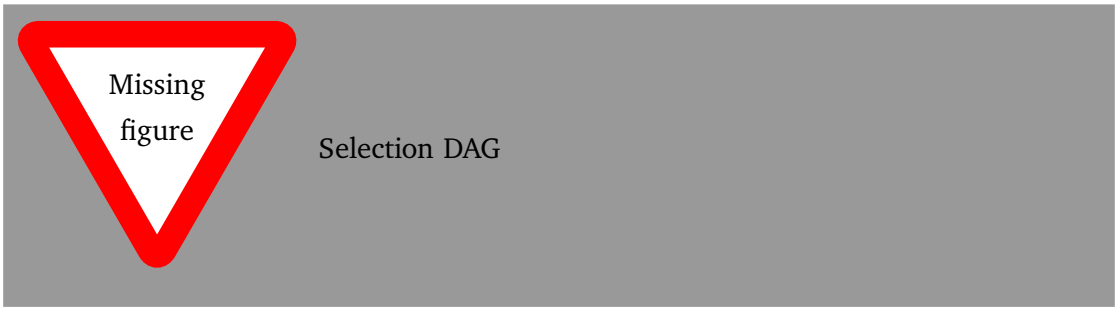
Add Example: e.g. see `https://youtu.be/brpomKUynEA?t=271`

1.1.2 Register Allocation

1.2 LLVM Compiler Infrastructure

1.2.1 Intermediate Representation

1.2.2 Instruction Selection DAG



Selection DAG

1.2.3 Pre-RA-Scheduling

Welche gibt es?
Wie funktionieren sie?
Welche Infos nutzen sie?

1.2.4 Post-RA-Scheduling

1.3 Reinforcement Learning

2 Related Work

2.1 Instruction Scheduling

Code scheduling and register allocation in large basic blocks

[10]

Learning Instruction Scheduling Heuristics from Optimal Data

[23]

Learning to schedule straight-line code

[19]

Using Genetic Algorithms to Fine-Tune Instruction-Scheduling Heuristics

[3]

2.2 Register Allocation

Deep Learning-based Hybrid Graph-Coloring Algorithm for Register Allocation

[9]

Graph colouring meets deep learning: Effective graph neural network models for combinatorial problems

[15]

Register Allocation for Intel Processor Graphics

[6]

2.3 Compiler Phase-Ordering

Autophase: Compiler phase-ordering for hls with deep reinforcement learning

[12]

2.4 Code Representation

For making use of data driven techniques in the area of compiler optimization, it is required to somehow extract features from the code to make it accessible for data driven algorithms. Older works usually made use of approaches that used hand-tuned features.

Maybe add references used in https://chriscu thesis.pdf (3.3.2.1)

Recent works are inspired by the advances in the the field of Natural Language Processing (NLP), which are caused by neural networks and continuous distributed vectors (referred to as embeddings) e.g., word2vec [18]. Although, human language is different from codes of programming languages in many aspects, embeddings prove to be useful in code related tasks, too.

Code inputs may be used directly in a high-level programming language or in an Intermediate Representation (IR) (e.g., LLVM-IR [14]). The advantage of using an IR is that it is independent of the source programming language and the target architecture.

Most approaches for representing high-level language code use some sort of the Abstract Syntax Tree (AST) in combination with various learning mechanisms. Alon et al. [2] used paths of the AST in combination with a Attention Neural Network model. Others have used

the AST in combination with Gated Graph Neural Networks [24, 1], with Support Vector Machines [21] or with Long short-term memory (LSTM) Networks for tree structures [8].

With Neural Code Comprehension (inst2vec) [4], Ben-Nun et al. defined an embedding space for the LLVM-IR. Relevant information to discover code semantics are data and control flow. To emphasize the semantics, the data and control flow are represented in a novel graph structure, called Contextual Flow Graphs (XFGs). The context of an individual statement, with size N, is defined as the statement and its graph neighbors that are connected by a path of length N. This statement is then mapped to its embedding by using the skip-gram model [17], which are known to work good in NLP tasks. The XFG captures features like data and control dependence's, instructions and data types, which are important for our task.

ProGraML: Graph-based Deep Learning for Program Optimization and Analysis

[7]

Write RW text for ProGraML

Compiler-based graph representations for deep learning models of code

[5]

Find Paper PDF and write text

IR2Vec [13] is another approach that maps an IR to a embedding space. [...] However, the datatype size, which is important for code optimizations, is abstracted away during the embedding process.

Write roughly how IR2Vec works

2.5 Applied Machine Learning on Code

Ithemal Accurate, portable and fast basic block throughput estimation using deep neural networks

[16]

NeuroVectorizer: End-to-End Vectorization with DeepReinforcement Learning

[11]

From Loop Fusion to Kernel Fusion: A Domain-Specific Approach to Locality Optimization

[22]

A Machine Learning Approach for Performance Prediction and Scheduling on Heterogeneous CPUs

[20]

Potential exploration -> random scheduling

Compare speedup with complexity of the problem (number of possible schedulings) vs speedup

Compare CPU Architectures, In-Order vs Out-Of-Order (`https://en.wikipedia.org/wiki/Out-of-order_execution`)

Acronyms

AST Abstract Syntax Tree

NLP Natural Language Processing

IR Intermediate Representation

XFG Contextual Flow Graph

LSTM Long short-term memory

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